22V Digital Input, High-Efficiency, Stereo Class-D Amplifier with Ultra-Low I_Q and IV Feedback

MAX98415A/MAX98425A

General Description

The MAX98415A/MAX98425A is a high-efficiency, stereo Class-D speaker amplifier with industry-leading quiescent power featuring Envelope Tracking control, Brownout Prevention Engine (BPE), Dynamic Headroom Tracking (DHT), and RMS Limiter. MAX98415A includes precision output current monitoring (I_{SENSE}) and speaker feedback voltage ($V_{FEEDBACK}$) to enable speaker protection algorithms that can be run by a host device. Both devices support sample rates up to 192kHz and a higher passband (for f_S > 50kHz) to enable high-resolution audio and ultrasound use cases. A separate bypass path is available for inputs, such as an ultrasound signal, so that it is not attenuated by audio processing. SSM and edge rate control minimize EMI and eliminate the need for output filtering found in traditional Class-D devices.

The Envelope Tracking algorithm on the device monitors the incoming audio signal and generates a PWM signal to control an external DC-DC converter to keep the amplifier supply close to the peak output audio signal, thereby improving system efficiency, idle quiescent power consumption, and thermal efficiency.

For battery-powered applications, the BPE helps avoid a system brownout by reducing the device's current consumption. This is achieved by either attenuating or limiting the amplifier output when the device supply drops below a set of programmable thresholds. In addition, as the amplifier supply varies due to sudden transients and declining battery life, DHT automatically optimizes the headroom available to the amplifier to maintain a consistent distortion level.

The device provides a PCM interface for audio data and a standard I^2C interface for control data communication.

Thermal foldback, when enabled, automatically reduces the output power when the temperature exceeds a user-specified threshold. This allows for uninterrupted music playback even at high ambient temperatures. Traditional thermal protection is also available in addition to robust overcurrent protection.

Benefits and Features

- Wide Input Supply Range (3V to 22V)
- Ultra-Low Quiescent Power
  - 155mW at V_{PVDD} = 20V, MAX98415A
  - 89mW at V_{PVDD} = 14V, MAX98425A
- Ultra-Low 28.5µV_{RMS} Output Noise
- Low Distortion
  - -81.1dB THD+N at 2W into 8Ω, f = 1kHz
- MAX98415A Output Power at 1% THD+N:
  - 27W Stereo into 8Ω, V_{PVDD} = 22V
  - 19W into 4Ω, V_{PVDD} = 14V
- MAX98425A Output Power at 1% THD+N:
  - 28W Stereo into 8Ω, V_{PVDD} = 22V
  - 20.5W into 4Ω, V_{PVDD} = 14V
- MAX98415A Speaker Amplifier Efficiency:
  - 87.0% at 1W per ch. into 8Ω, V_{PVDD} = 22V
  - 87.0% at 1W per ch. into 4Ω, V_{PVDD} = 14V
- MAX98425A Speaker Amplifier Efficiency:
  - 87.5% at 1W per ch. into 8Ω, V_{PVDD} = 22V
  - 88% at 1W per ch. into 4Ω, V_{PVDD} = 14V
- Class-D EMI Reduction Enables Filterless Operation
- SSM and Switching Edge Rate Control
- Integrated Speaker Current and Voltage Feedback, Do Not Require External Components (MAX98415A only)
- Flexible Brownout Prevention Engine
- I^2S/16-Channel TDM and I^2C Digital Interfaces
- Playback and IV Paths Support Sample Rates up to 192kHz
- No MCLK Required
- Dynamic Headroom Tracking (DHT)
- Envelope Tracking Output to Maximize System Efficiency
- Extensive Click-and-Pop Suppression
- 40-Bump WLP (0.4mm Pitch)

Applications

- Soundbars
- Mobile Speakers and Smart Speakers
- Tablets, Laptops, and Desktop Computers
- Smart IoT Devices

***Ordering Information* appears at end of data sheet**

19-101979; Rev 0; 3/25

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Simplified Application Diagram

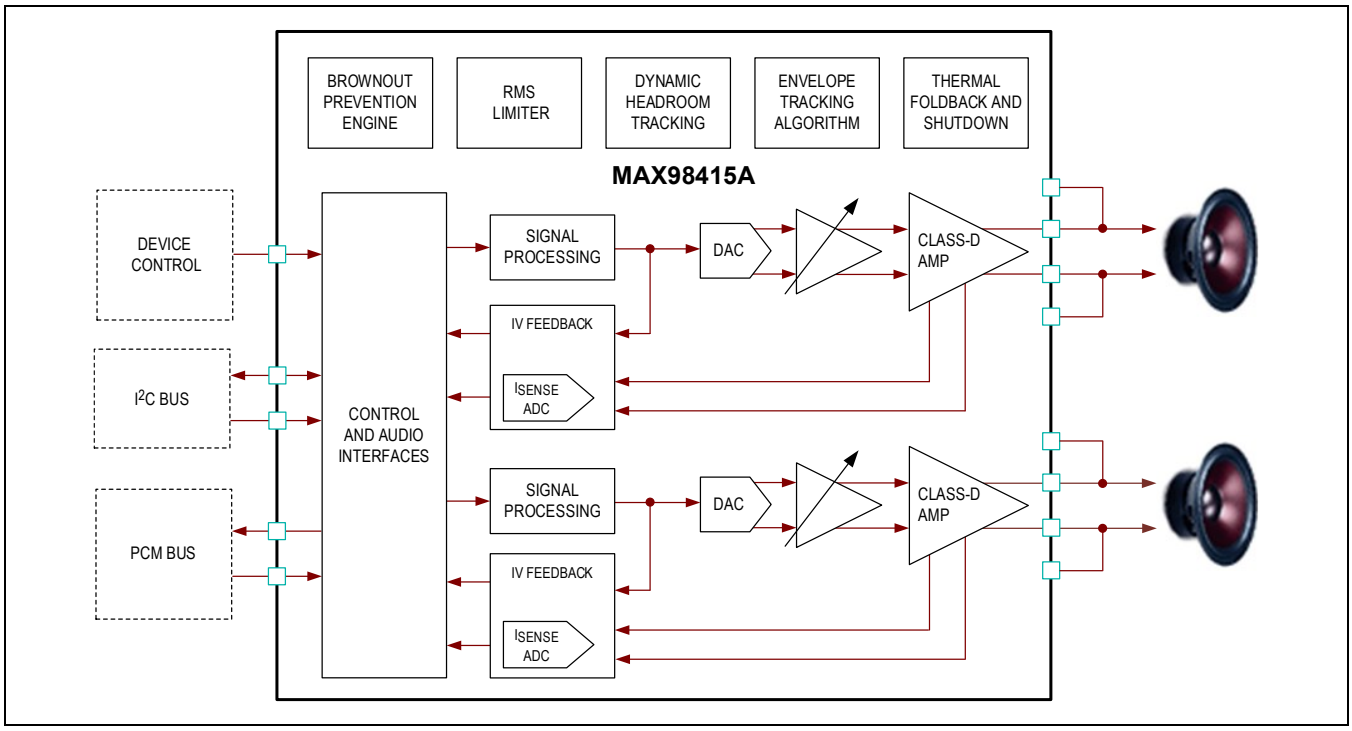


Figure 1. MAX98415A Simplified Block Diagram

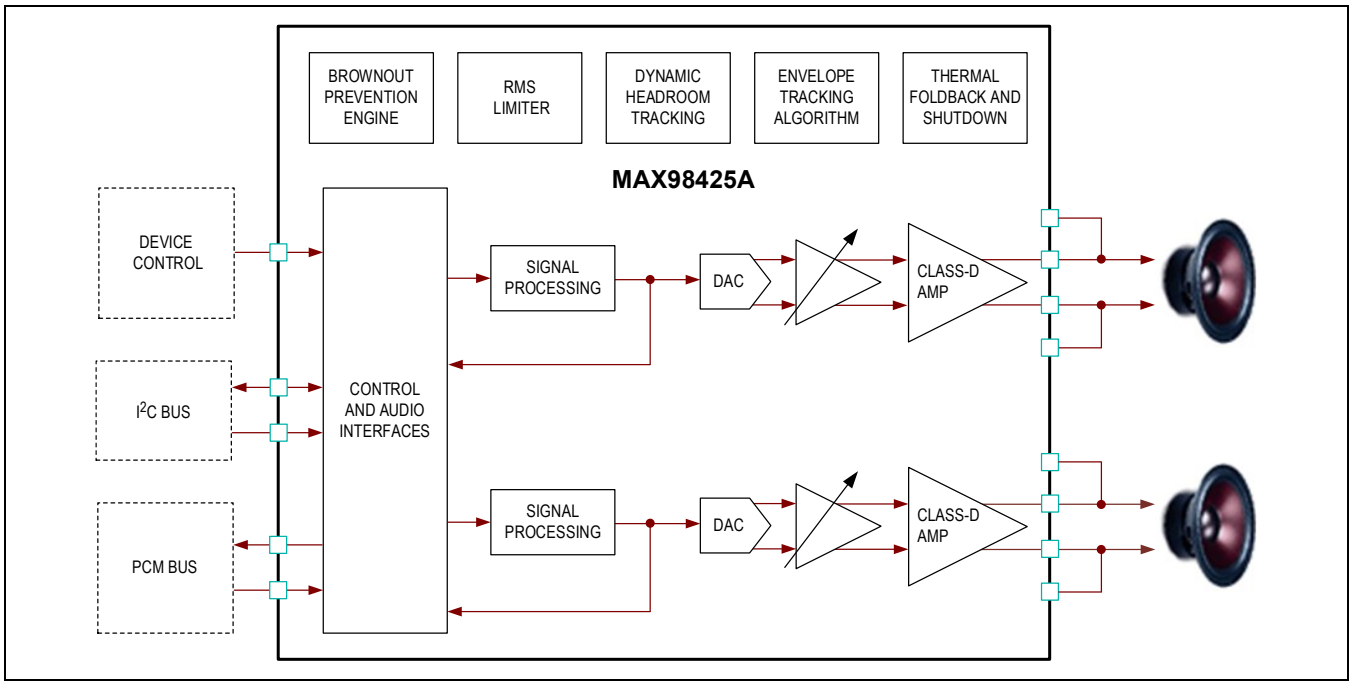


Figure 2. MAX98425A Simplified Block Diagram

Absolute Maximum Ratings

VBAT to DGND ..... -0.3V to +6.0V

PVDD to PGND ..... -0.3V to +24V

AGND, DGND to PGND ..... -0.3V to +0.3V

AVDD to AGND ..... -0.3V to +2.2V

DVDD to DGND ..... -0.3V to +2.2V

OUTP_A, OUTN_A, OUTP_B, OUTN_B to PGND -0.3V to V_{PVDD} + 0.3V

OUTPSNS_A, OUTNSNS_A, OUTPSNS_B, OUTNSNS_B to PGND ..... -0.3V to +24V

V_{BOOTP_A} to OUTP_A, V_{BOOTN_A} to OUTN_A -0.3V to +2.2V

V_{BOOTP_B} to OUTP_B, V_{BOOTN_B} to OUTN_B -0.3V to +2.2V

I2C1, I2C2, ADDR to DGND ..... -0.3V to +6.0V

BCLK, LRCLK, DIN, $\overline{RESET}$, $\overline{MUTE}$ to DGND ..-0.3V to +6.0V

GPIO1, GPIO2, GPIO3 to DGND ..... -0.3V to V_{DVDD} + 0.3V

Short-Circuit Duration Between OUTP_X, OUTN_X, and PGND or PVDD or VBAT .....Continuous

Short-Circuit Duration Between OUTP_X and OUTN_X .....Continuous

Continuous Power Dissipation for Multilayer Board (T_A = +70°C, derate 22.4 mW/°C above +70°C.) 1792mW

Junction Temperature.....+150°C

Operating Temperature Range..... -40°C to +85°C

Storage Temperature Range..... -65°C to +150°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

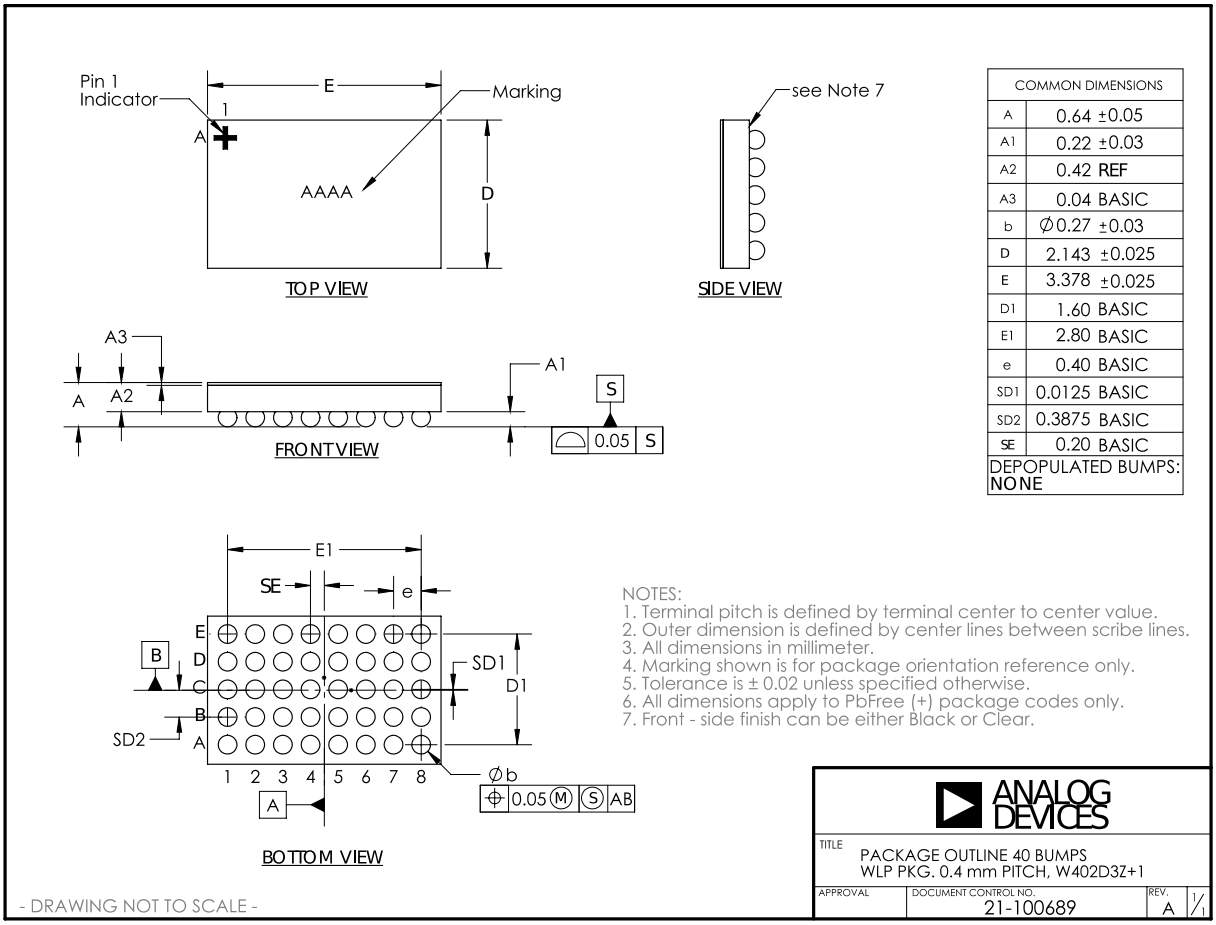
Package Information

40 WLP

Package Code	MAX98415A: W402D3Z+1
	MAX98425A: W402D3Z+2
Outline Number	MAX98415A: *21-100689*
	MAX98425A: *21-100702*
Land Pattern Number	Refer to *www.analog.com/en/resources/technical-articles/waferlevel-packaging-wlp-and-its-applications*
Thermal Resistance, Six-Layer EV Kit Board:	
Junction-to-Ambient (θ_{JA})	28°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A
[1]Thermal Resistance, Four-Layer JEDEC Board:	
Junction-to-Ambient (θ_{JA})	44.64°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

[1] Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages*.



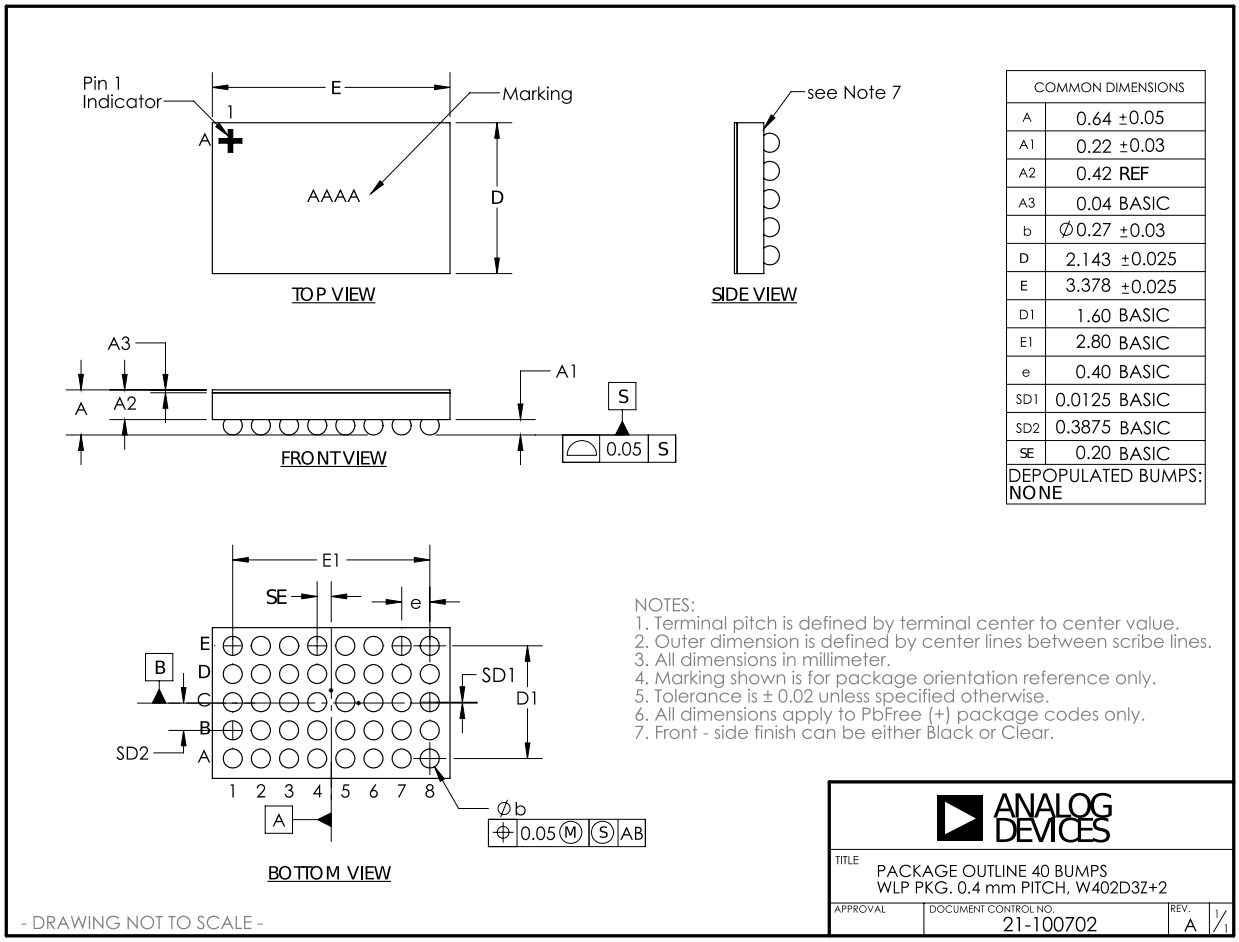
COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.22 ±0.03
A2	0.42 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	2.143 ±0.025
E	3.378 ±0.025
D1	1.60 BASIC
E1	2.80 BASIC
e	0.40 BASIC
SD1	0.0125 BASIC
SD2	0.3875 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 40 BUMPS
WLP PKG. 0.4 mm PITCH, W402D3Z+1

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100689	A	1/1



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A	0.64 ±0.05
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A2	0.42 REF
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E	3.378 ±0.025
D1	1.60 BASIC
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SD1	0.0125 BASIC
SD2	0.3875 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 40 BUMPS
WLP PKG. 0.4 mm PITCH, W402D3Z+2

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-100702	A	1/1

Electrical Characteristics

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
PVDD Power Supply Operating Voltage Range	V_{PVDD}			3.0		22	V
PVDD Voltage	V_{PVDD}	The device is functional but parametric performance is not guaranteed		2.8			V
VBAT Power Supply Operating Voltage Range	V_{VBAT}			2.4		5.5	V
AVDD Power Supply Voltage Range	V_{AVDD}			1.71	1.8	1.89	V
DVDD Power Supply Voltage Range	V_{DVDD}			1.71	1.8	1.89	V
VBAT Undervoltage Lockout	V_{VBAT_UVLO}	V_{VBAT} falling		2.18		2.28	V
PVDD Undervoltage Lockout	V_{PVDD_UVLO}	V_{PVDD} falling		2.54		2.65	V
AVDD Undervoltage Lockout	V_{AVDD_UVLO}	V_{AVDD} falling		1.61		1.68	V
AVDD POK Threshold	V_{AVDD_POK}	V_{AVDD} falling		1.28		1.61	V
DVDD Undervoltage Lockout	V_{DVDD_UVLO}	V_{DVDD} falling		1.61		1.68	V
DVDD POK Threshold	V_{DVDD_POK}	V_{DVDD} falling		1.28		1.61	V
VBAT UVLO Hysteresis		*Note 3*		90	100		mV
PVDD UVLO Hysteresis		*Note 3*		90	100		mV
AVDD UVLO Hysteresis		*Note 3*		10	25		mV
DVDD UVLO Hysteresis		*Note 3*		10	25		mV
Supply Ramp Rate PVDD		*Note 3*		0.1		100	V/ms
POWER CONSUMPTION/QUIESCENT POWER CONSUMPTION							
Total Power Consumption	P_Q	All supplies, IV feedback enabled	V_{PVDD} = 20V, Stereo mode, MAX98415A		155	163	mW
			V_{PVDD} = 14V, Stereo mode, MAX98415A		97	103	
		All supplies, IV feedback disabled	V_{PVDD} = 20V, Stereo mode, MAX98415A		146.5		
		All supplies	V_{PVDD} = 20V, Stereo mode, MAX98425A		146.5	152	
		All supplies, IV feedback disabled	V_{PVDD} = 14V, Stereo mode, MAX98415A		89		

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (Note 2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		All supplies	V_{PVDD} = 14V, Stereo mode, MAX98425A		89	93	
Total Power Consumption	P_Q	All supplies, IV feedback disabled	V_{PVDD} = 20V, Stereo mode, Noise gate enabled		6		mW
		All supplies	V_{PVDD} = 20V, V_{VBAT} = 3.3V, 1 Ch enabled, Noise gate enabled		6		
PVDD Quiescent Current	I_{Q_PVDD}	MAX98415A, MAX98425A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		4.5	5	mA
VBAT Quiescent Current	I_{Q_VBAT}	MAX98425A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		2.92	4.5	mA
		MAX98415A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		2.94	4.5	
AVDD Quiescent Current	I_{Q_AVDD}	MAX98425A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		2	2.5	mA
		IV sense enabled, MAX98415A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		3.1	4	
DVDD Quiescent Current	I_{Q_DVDD}	MAX98425A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		7.5	8.25	mA
		IV sense enabled, MAX98415A	V_{PVDD} = 14V, V_{VBAT} = 3.3V, Stereo mode		11.2	12	
POWER CONSUMPTION/HARDWARE SHUTDOWN							
VBAT Hardware Shutdown Supply Current	$I_{SHDN\_HW\_VBAT}$	V_{VBAT} = 3.3V, T_A = +25°C			0.1	1	µA
		V_{VBAT} = 3.3V, T_A = +85°C, (Note 3)				1	
		V_{VBAT} = 5V, T_A = +25°C			0.2	1.5	
		V_{VBAT} = 5V, T_A = +85°C, (Note 3)				1.5	
PVDD Hardware Shutdown Supply Current	$I_{SHDN\_HW\_PVDD}$	V_{PVDD} = 5.0V, T_A = +25°C			0.15	1	µA
		V_{PVDD} = 5.0V, T_A = +85°C, (Note 3)				1	
		V_{PVDD} = 14V, T_A = +25°C			0.65	3	
		V_{PVDD} = 14V, T_A = +85°C, (Note 3)				5	
		V_{PVDD} = 22V, T_A = +25°C			1	5	
		V_{PVDD} = 22V, T_A = +85°C, (Note 3)				8	
AVDD Hardware Shutdown Supply Current	$I_{SHDN\_HW\_AVDD}$	T_A = +25°C			0.5	2	µA
		T_A = +85°C, (Note 3)				7	
		T_A = +25°C			2	9	µA

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (Note 2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DVDD Hardware Shutdown Supply Current	$I_{SHDN\_HW\_DVDD}$	T_A = +85°C, (Note 3)			38	
POWER CONSUMPTION/SOFTWARE SHUTDOWN						
VBAT Software Shutdown Supply Current	$I_{SHDN\_SW\_VBAT}$	V_{VBAT} = 3.3V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		0.15	1	µA
		V_{VBAT} = 3.3V, no BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			1	
		V_{VBAT} = 5V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		0.6	3	
		V_{VBAT} = 5V, no BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			3	
PVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_PVDD}$	V_{PVDD} = 5.0V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		0.15	1	µA
		V_{PVDD} = 5.0V, no BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			3	
		V_{PVDD} = 14V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		0.65	4	
		V_{PVDD} = 14V, no BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			8	
		V_{PVDD} = 22V, no BCLK/LRCLK/DIN transactions, T_A = +25°C		1	5.5	
		V_{PVDD} = 22V, no BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			9	
AVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_AVDD}$	No BCLK/LRCLK/DIN transactions, T_A = +25°C		1.3	5	µA
		No BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			10	
DVDD Software Shutdown Supply Current	$I_{SHDN\_SW\_DVDD}$	No BCLK/LRCLK/DIN transactions, T_A = +25°C		3.3	11	µA
		No BCLK/LRCLK/DIN transactions, T_A = +85°C, (Note 3)			42	
TURN-ON/OFF TIME						
Turn-On Time	t_{ON}	From EN bit set to 1 to full operation, startup ramp disabled (Note 4)		1.4	3.6	ms
		From EN bit set to 1 to full operation, startup ramp enabled (Note 4)		2.9	6.6	
		Playback path re-enable: From SPK_EN bit set to 1 to full operation, EN = 1, startup ramp disabled		1.2		
Turn-Off Time	t_{OFF}	From full operation, EN bit set to 0 to software shutdown, shutdown ramp disabled		20	100	µs
		From full operation, EN bit set to 0 to software shutdown, shutdown ramp enabled		2.3	6	ms

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		From SPK_EN bit set to 0 to amplifier disabled, shutdown ramp disabled, EN = 1			20		µs
DIGITAL AUDIO PATH							
DIGITAL AUDIO PATH/GAIN CONTROLS/DIGITAL VOLUME CONTROL							
Digital Volume Control (max)	A_{SPK_VOL}	AMPX_SPK_VOL[7:0] = 0x00			0		dB
Digital Volume Control Step Size					0.5		dB
Digital Volume Control (min)	A_{SPK_VOL}	AMPX_SPK_VOL [7:0] = 0xB4			-90		dB
Digital Volume Ramp Co-efficient	t_{VOL_COEFF}				1.8		ms
DIGITAL AUDIO PATH/FILTERING/DIGITAL HIGHPASS FILTER CHARACTERISTICS (*Note 5*)							
DC Attenuation				80			dB
DC Blocking Cutoff Frequency		All sample rates	AMPX_SPK_IVF_DCBLK_CFG = 0x0		1.872		Hz
			AMPX_SPK_IVF_DCBLK_CFG = 0x1		0.936		
			AMPX_SPK_IVF_DCBLK_CFG = 0x2		0.468		
			AMPX_SPK_IVF_DCBLK_CFG = 0x3		0.234		
DIGITAL AUDIO PATH/FILTERING/DIGITAL FILTER CHARACTERISTICS (LRCLK < 50kHz) (*Note 5*)							
Valid Sample Rates				8		48	kHz
Passband Ripple	δ_P	f < f_{PLP}, referenced to the signal level at 1kHz		-0.15		+0.15	dB
Passband Cutoff	f_{PLP}	Ripple < δP		0.452 x f_S			Hz
		Droop < -3dB		0.457 x f_S			
Stopband Attenuation	δ_S	f > f_{SLP}		80			dB
Stopband Cutoff	f_{SLP}	Attenuation > δ_S				0.49 x f_S	Hz
Group Delay		f = 1kHz			6.8		samples
DIGITAL AUDIO PATH/FILTERING/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Valid Sample Rates				88.2		192	kHz
Passband Ripple	δ_P	SPK_WBAND_FILT_EN = 0	f < f_{PLP}, referenced to the signal level at 1kHz	-0.35		+0.35	dB
Passband Cutoff	f_{PLP}	SPK_WBAND_FILT_EN = 0	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.227 x f_S			Hz
		SPK_WBAND_FILT_EN = 0	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.31 x f_S			

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
	f_{PLP}	SPK_WBAND_FILT_EN = 0	Ripple < δP, 176.4kHz ≤ f_S ≤ 192kHz	0.1135 x f_S			
		SPK_WBAND_FILT_EN = 0	Droop < -3dB cutoff, 176.4kHz ≤ f_S ≤ 192kHz	0.227 x f_S			
Stopband Attenuation	δ_S	SPK_WBAND_FILT_EN = 0	f > f_{SLP}	80			dB
Stopband Cutoff	f_{SLP}	SPK_WBAND_FILT_EN = 0	Attenuation < δ_S			0.495 x f_S	Hz
Group Delay		SPK_WBAND_FILT_EN = 0	f = 1kHz, 88.2kHz ≤ f_S ≤ 96kHz		8.3		samples
			f = 1kHz, 176.4kHz ≤ f_S ≤ 192kHz		9.2		
DIGITAL AUDIO PATH/FILTERING/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Valid Sample Rates				88.2		192	kHz
Passband Cutoff	f_{PLP}	SPK_WBAND_FILT_EN = 1	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.44 x f_S			Hz
		SPK_WBAND_FILT_EN = 1	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.45 x f_S			
	f_{PLP}	SPK_WBAND_FILT_EN = 1	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.23 x f_S			
		SPK_WBAND_FILT_EN = 1	Droop < -3dB cutoff, 176.4kHz ≤ f_S ≤ 192kHz	0.3 x f_S			
Passband Ripple	δ_P	SPK_WBAND_FILT_EN = 1	f < f_{PLP}, referenced to the signal level at 1kHz	-0.35		+0.35	dB
Stopband Cutoff	f_{SLP}	SPK_WBAND_FILT_EN = 1	Attenuation < δ_S			0.5 x f_S	Hz
Stopband Attenuation	δ_S	SPK_WBAND_FILT_EN = 1	f > f_{SLP}	80			dB
Group Delay		SPK_WBAND_FILT_EN = 1	f = 1kHz, 88.2kHz ≤ f_S ≤ 96kHz		7.8		samples
			f = 1kHz, 176.4kHz ≤ f_S ≤ 192kHz		9.2		
Max Device to Device Group Delay Variability		f_{IN} = 1kHz			1		µs
TONE GENERATOR							
THD+N		f_S ≤ 96kHz			-60		dB
		f_S > 96kHz			-40		
CLASS-D AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C, Z_{SPK} = 8Ω + 33µH, DRE_EN = 0, AMPX_SPK_GAIN_MAX = 0x12		-5.5	±0.5	+5.5	mV

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click-and-Pop Level	K_{CP}	Peak voltage, Audio playback silent, A-weighted, 32 samples per second, T_A = +25°C (*Note 6*)			-66		dBV
Efficiency	η_{SPK}	MAX98415A	V_{PVDD} = 14V, P_{OUT} = 1W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		87.0		%
			V_{PVDD} = 14V, P_{OUT} = 5W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		90.0		
			V_{PVDD} = 14V, P_{OUT} = 10W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		89.8		
		MAX98425A	V_{PVDD} = 14V, P_{OUT} = 1W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		88.0		
			V_{PVDD} = 14V, P_{OUT} = 5W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		91.0		
			V_{PVDD} = 14V, P_{OUT} = 10W per channel, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode		91.5		
		MAX98415A	V_{PVDD} = 22V, P_{OUT} = 1W per channel, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode		87		
			V_{PVDD} = 22V, P_{OUT} = 5W per channel, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode		90		
			V_{PVDD} = 22V, P_{OUT} = 16W per channel, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode		93		

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		MAX98425A	V_{PVDD} = 22V, P_{OUT} = 1W per channel, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode		87.5		
			V_{PVDD} = 22V, P_{OUT} = 5W per channel, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode		90.5		
Output Power	P_{OUT}	V_{PVDD} = 22V, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode	THD+N ≤ 1%, MAX98415A		27		W
			THD+N ≤ 1%, MAX98425A		28		
		V_{PVDD} = 22V, Z_{SPK} = 8Ω + 33µH, f_{IN} = 1kHz, Stereo mode, AMPX_SPL_CLIP = 0x6 (+3dB)	THD+N ≤ 10%, MAX98415A		33		
			THD+N ≤ 10%, MAX98425A		34.5		
		V_{PVDD} = 14V, Z_{SPK} = 4Ω + 33µH, f_{IN} = 1kHz, Stereo mode	THD+N ≤ 1%, MAX98415A		19		
			THD+N ≤ 1%, MAX98425A		20.5		
			THD+N ≤ 10%, MAX98415A		23		
			THD+N ≤ 10%, MAX98425A		23.5		
Peak Output Power	P_{OUT}	MAX98415A; 50Hz (2 period, peak signal)/1kHz (460 periods, low amplitude signal) alternating signal; crest factor = 12dB; test duration = 1min with T_J < +100°C and THD+N < 1%	Z_{SPK} = 4Ω + 33µH; Stereo mode, V_{PVDD} = 22V		70		W
			Z_{SPK} = 2Ω + 33µH; Stereo mode, V_{PVDD} = 16V		42		
		MAX98425A; 50Hz (2 period, peak signal)/1kHz (460 periods, low amplitude signal) alternating signal; crest factor = 12dB; test duration = 1min with T_J < +100°C and THD+N < 1%	Z_{SPK} = 4Ω + 33µH; Stereo mode, V_{PVDD} = 22V		82		
			Z_{SPK} = 2Ω + 33µH; Stereo mode, V_{PVDD} = 16V		66		

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, P_{OUT} = 2W, Z_{SPK} = 8Ω + 33µH, (*Note 3*)		-72	-81.1		dB
		f_{IN} = 1kHz, V_{PVDD} = 14V, P_{OUT} = 4W, Z_{SPK} = 4Ω + 33µH			-82.9		
		SPK_TRI_FSW2X_MODE = 1	f_{IN} = 6kHz, P_{OUT} = 2W, Z_{SPK} = 8Ω + 33µH		-75		
			f_{IN} = 6kHz, V_{PVDD} = 14V, P_{OUT} = 4W, Z_{SPK} = 4Ω + 33µH		-73		
Intermodulation Distortion		ITU-R standard, f_{IN} = 19kHz/20kHz, V_{IN} = -3dBFS			-63		dB
			SPK_TRI_FSW2X_MODE = 1		-80		
Output Noise	e_N	A-weighted			28.5		$µV_{RMS}$
		$3V_{RMS}$, 40kHz continuous sinewave	Inband (20Hz to 20kHz), A-weighted		104		
Dynamic Range	DR	Measured using EIAJ method, -60dBFS output signal at 1kHz referenced to output power at 1% THD+N, A-weighted			114		dB
DAC Full-Scale					1.4		V_{PK}
CLASS-D AMPLIFIER/POWER-SUPPLY RIPPLE REJECTION							
VBAT Supply DC Rejection	PSRR	V_{VBAT} = 2.4V to 5.5V		80	95		dB
VBAT Supply Rejection AC	PSRR	V_{RIPPLE} = $100mV_{P-P}$	f_{RIPPLE} = 217Hz		80		dB
			f_{RIPPLE} = 1kHz		75		
			f_{RIPPLE} = 20kHz		60		
PVDD Supply DC Rejection	PSRR	V_{PVDD} = 3V to 22V		74	90		dB
PVDD Supply Rejection AC	PSRR	V_{RIPPLE} = $100mV_{P-P}$	f_{RIPPLE} = 217Hz		80		dB
			f_{RIPPLE} = 1kHz		75		
			f_{RIPPLE} = 20kHz		65		
AVDD Supply DC Rejection	PSRR	V_{AVDD} = 1.71V to 1.89V			80		dB
AVDD Supply Rejection AC	PSRR	V_{RIPPLE} = $100mV_{P-P}$	f_{RIPPLE} = 217Hz		80		dB
			f_{RIPPLE} = 1kHz		80		
			f_{RIPPLE} = 20kHz		60		
DVDD Supply DC Rejection	PSRR	V_{DVDD} = 1.71V to 1.89V			80		dB
DVDD Supply Rejection AC	PSRR	V_{RIPPLE} = $100mV_{P-P}$	f_{RIPPLE} = 217Hz		80		dB
			f_{RIPPLE} = 1kHz		75		
			f_{RIPPLE} = 20kHz		63		
CLASS-D AMPLIFIER/POWER-SUPPLY INTERMODULATION							

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Intermodulation		f_{IN} = 1kHz, P_{OUT} = 400mW	V_{PVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-100		dB
			V_{AVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-80		
			V_{DVDD}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-90		
			V_{VBAT}, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{P-P}		-104		
Output Switching Frequency		SPK_TRI_FSW2X_MODE = 0, constant across all sample rates			330		kHz
		SPK_TRI_FSW2X_MODE = 1, constant across all sample rates			650		
Frequency Response Deviation		Across the bandwidth 20Hz to 20kHz referenced to f_{IN} = 1kHz			±0.25		dB
Gain Error	AV_{ERROR}			-0.5		+0.5	dB
Channel-to-Channel Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz, f_S > 32kHz, all DAI operating modes			2		°
		Output phase shift between multiple devices from 20Hz to 0.425 x f_S, f_S ≤ 32kHz, all DAI operating modes			5		
Minimum Load Resistance		Stereo mode, V_{PVDD} = 22V			3.2		Ω
Minimum Load Inductance		In series with a 3.2Ω load			0		µH
Maximum Load Inductance		In series with a 3.2Ω load			1000		µH
Current Limit	I_{LIM}	Per Channel, Stereo Mode		6.0	7.0		A
SPEAKER VOLTAGE FEEDBACK							
Resolution					16		Bits
Sample Rate	f_{S_VFB}			8		192	kHz
Voltage Range	V_{VFB_FS}				±24		V
Power Supply Feedthrough (AVDD, DVDD, VBAT, PVDD to $V_{FEEDBACK}$)	PSF	No Input Signal, f_{RIPPLE} = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AC			-100		dB
Max Device to Device Voltage Feedback Channel Phase Mismatch		f_{IN} = 1kHz, f_S ≤ 32kHz			0.3		Sample
		f_{IN} = 1kHz, f_S > 32kHz			0.05		
SPEAKER VOLTAGE FEEDBACK/DIGITAL FILTER CHARACTERISTICS (LRCLK < 50kHz) (*Note 5*)							
Passband Ripple	δ_P	f_{IN} < f_{PLP}, referenced to the signal level at 1kHz		-0.225		+0.225	dB

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Lowpass Filter Cutoff Frequency	f_{PLP}	Ripple < δ_P		0.445 x f_S			Hz
		Droop < -3dB		0.451 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	Attenuation ≤ -40dB				0.48 x f_S	Hz
Lowpass Filter Stopband Attenuation	δ_S			40			dB
Group Delay		f_{IN} = 1kHz			6		Samples
SPEAKER VOLTAGE FEEDBACK/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Passband Ripple	δ_P	IVFB_WBAND_FILT_EN = 0	f_{IN} < f_{PLP}, referenced to the signal level at 1kHz	-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	IVFB_WBAND_FILT_EN = 0	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.23 x f_S			Hz
		IVFB_WBAND_FILT_EN = 0	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.29 x f_S			
	f_{PLP}	IVFB_WBAND_FILT_EN = 0	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.128 x f_S			
		IVFB_WBAND_FILT_EN = 0	Droop < -3dB, 176.4kHz ≤ f_S ≤ 192kHz	0.178 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	IVFB_WBAND_FILT_EN = 0	Attenuation ≤ -40dB, 88.2kHz ≤ f_S ≤ 96kHz			0.4 x f_S	Hz
			Attenuation ≤ -40dB, 176.4kHz ≤ f_S ≤ 192kHz			0.32 x f_S	
Lowpass Filter Stopband Attenuation	δ_S	IVFB_WBAND_FILT_EN = 0		40			dB
Group Delay		IVFB_WBAND_FILT_EN = 0	f_{IN} = 1kHz, 88.2kHz ≤ f_S ≤ 96kHz		6		Samples
			f_{IN} = 1kHz, 176.4kHz ≤ f_S ≤ 192kHz		7		
SPEAKER VOLTAGE FEEDBACK/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Passband Ripple		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	f_{IN} < f_{PLP}, referenced to the signal level at 1kHz	-0.5		+0.5	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.459 x f_S			Hz

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.46 x f_S			
	f_{PLP}	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.25 x f_S			
		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	Droop < -3dB, 176.4kHz ≤ f_S ≤ 192kHz	0.29 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	-40dB limit, 88.2kHz ≤ f_S ≤ 96kHz			0.49 x f_S	Hz
		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	-40dB limit, 176.4kHz ≤ f_S ≤ 192kHz			0.41 x f_S	
Lowpass Filter Stopband Attenuation	δ_S	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1		40			dB
Group Delay		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	f_{IN} = 1kHz, 88.2kHz ≤ f_S ≤ 96kHz		5.5		Samples
			f_{IN} = 1kHz, 176.4kHz ≤ f_S ≤ 192kHz		7.5		
Max Device-to-Device Voltage Feedback Channel Phase Mismatch		f_{IN} = 1kHz			0.1		Sample
SPEAKER CURRENT ADC							
Resolution					16		Bits
Sample Rate	$f_{S\_ISNS\_ADC}$			8		96	kHz
Current Range	I_{SPK}				±6		A
Dynamic Range	DNR	f_{IN} = 1kHz, AC measurement bandwidth = 20Hz to 20kHz, unweighted			76		dB
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, I_{SPK} = 1A_{RMS}			-58		dB
Differential Mode Gain		T_A = +25ºC		0.98		1.02	
Differential Mode gain Variability		Across Supplies, T_A = -40°C to +85°C		-2.5		+2.5	%
Common Mode Gain		T_A = +25ºC			-60		dB
Highpass Cutoff Frequency		-3dB limit, across all sample rates				2	Hz
DC Offset Current		DC blocking filter enabled, T_A = +25°C		-0.2		+0.2	mA

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		DC blocking filter disabled, V_{PVDD} = 12V, T_A = +25°C			±6		
Voltage and Current Accuracy Drift Tracking		T_A = 0°C to +85°C, relative to +25°C			0.4		%
Speaker Amplifier Voltage to Current Sense Crosstalk		f_{IN} = 1kHz			-60		dB
Power Supply Feedthrough	PSF	No input signal, f_{RIPPLE} = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AC	PVDD, VBAT, DVDD to IMON		-90		dB
			AVDD to IMON		-80		
SPEAKER CURRENT ADC/DIGITAL FILTER CHARACTERISTICS (LRCLK < 50kHz) (*Note 5*)							
Passband Ripple	δ_P	f_{IN} < f_{PLP}		-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	Ripple < δ_P		0.44 x f_S			Hz
		Droop < -3dB		0.45 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit				0.49 x f_S	Hz
Lowpass Filter Stopband Attenuation	δ_S			40			dB
Group Delay		f_{IN} = 1kHz			8		Samples
SPEAKER CURRENT/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Passband Ripple	δ_P	IVFB_WBAND_FILT_EN = 0	f_{IN} < f_{PLP}	-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	IVFB_WBAND_FILT_EN = 0	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.227 x f_S			Hz
		IVFB_WBAND_FILT_EN = 0	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.31 x f_S			
	f_{PLP}	IVFB_WBAND_FILT_EN = 0	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.127 x f_S			
		IVFB_WBAND_FILT_EN = 0	Droop < -3dB, 176.4kHz ≤ f_S ≤ 192kHz	0.178 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	IVFB_WBAND_FILT_EN = 0	-40dB limit			0.48 x f_S	Hz
Lowpass Filter Stopband Attenuation	δ_S	IVFB_WBAND_FILT_EN = 0		40			dB
Group Delay		IVFB_WBAND_FILT_EN = 0	f_{IN} = 1kHz		10		Samples
SPEAKER CURRENT/DIGITAL FILTER CHARACTERISTICS (LRCLK > 50kHz) (*Note 5*)							
Passband Ripple	δ_P	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	f_{IN} < f_{PLP}	-0.5		+0.5	dB

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (Note 2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Lowpass Filter Cutoff Frequency	f_{PLP}	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	-3dB limit, 88.2kHz ≤ f_S ≤ 96kHz		0.45 x f_S		Hz
			-3dB limit, 176.4 kHz ≤ f_S ≤ 192kHz		0.25 x f_S		
		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	-3dB limit, 88.2kHz ≤ f_S ≤ 96kHz		0.46 x f_S		
			-3dB limit, 176.4 kHz ≤ f_S ≤ 192kHz		0.28 x f_S		
Lowpass Filter Stopband Frequency	f_{SLP}	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	-40dB limit			0.49 x f_S	Hz
Lowpass Filter Stopband Attenuation	δ_S	IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1		-40			dB
Group Delay		IVFB_WBAND_FILT_EN = 1, AMPX_SPK_WBAND_FILT_EN = 1	f_{IN} = 1kHz		10		Samples
Max Device-to-Device Current Sense Channel Phase Mismatch		f_{IN} = 1kHz, f_S ≤ 32kHz			0.3		Sample
		f_{IN} = 1kHz, f_S > 32kHz			0.05		
$V_{FEEDBACK}$ / I_{SENSE} RATIO							
$V_{FEEDBACK}/I_{SENSE}$ Tracking		P_{OUT} = 1mW to 0.1% THD+N, 40 Hz, -50dBFS pilot tone			±0.4		%
$V_{FEEDBACK}/I_{SENSE}$ Tracking Error Over Temperature		0°C to +70°C, relative to T_A = +25°C, P_{OUT} = 10W			±0.4		%
MEASUREMENT ADC							
Resolution					9		bits
PVDD Channel Input Voltage Range		T_A = +25°C		2.5		22.25	V
PVDD Channel Voltage Resolution					44		mV
PVDD Channel Measurement Accuracy		T_A = +25°C, (Note 3)		-400		+400	mV
Thermal Channel Input Range				-29		+150	°C
Thermal Channel Resolution					1		°C
BROWNOUT PROTECTION ENGINE (BPE)							
BPE Attack Delay Time to Gain Change		MEAS_ADC_OPT_MODE = 0x2, MEAS_ADC_OPT_AVG = 0x0			12		µs
BPE Attack Delay Time to Interrupt					3		µs
THERMAL PROTECTION							
Thermal Foldback Attenuation Attack Time	$t_{THR\_FB\_ATK}$				1		Sample
Thermal Foldback Max Attenuation					12		dB

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Trigger Point		THERMSHDN_THRESH = 0x64	140	150	160	°C
DIGITAL I/O / INPUT—DIN, BCLK, LRCLK, GPIO1, GPIO2, GPIO3						
Input Voltage High	V_{IH}		0.84			V
Input Voltage Low	V_{IL}				0.54	V
Input Leakage Current		GPIO1, GPIO2, GPIO3	-1		+1	µA
		V_{IN} = 5.5V, BCLK, LRCLK, DIN			+4	
Input Hysteresis	V_{HYS}	*Note 3*	48			mV
Maximum Input Capacitance	C_{IN}			5		pF
Internal Pull-Down Resistance	R_{PD}	BCLK, LRCLK, DIN, GPIO1, GPIO2, GPIO3		3		MΩ
DIGITAL I/O / INPUT—I2C1, I2C2						
Input Voltage High	V_{IH}		0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDD}	V
Input Leakage Current		T_A = +25°C, input high	-1		+1	µA
Input Hysteresis	V_{HYS}	*Note 3*	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / INPUT—RESET, MUTE, ADDR						
Input Voltage High	V_{IH}		0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{DVDD}	V
Input Leakage Current		V_{IN} = 5.5V, ADDR	-1		+1	µA
		V_{IN} = 5.5V, $\overline{RESET}$, $\overline{MUTE}$			+4	
Input Hysteresis	V_{HYS}	*Note 3*	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
Internal Pull-Down Resistance	R_{PD}	$\overline{RESET}$, $\overline{MUTE}$		3		MΩ
DIGITAL I/O / OPEN DRAIN OUTPUT—I2C1, I2C2, GPIO1, GPIO2, GPIO3						
Output Voltage Low	V_{OL}	I_{SINK} = 4mA			0.4	V
Output High Leakage Current	I_{OH}	V_{IN} = V_{DVDD}, GPIO1, GPIO2, GPIO3, T_A = +25°C	-1		+1	µA
		V_{IN} = 5.5V, I2C1, I2C2, T_A = +25°C	-1		+1	
DIGITAL I/O / PUSH-PULL OUTPUT—GPIO1, GPIO2, GPIO3						
Output Voltage High	V_{OH}	I_{OH} = 4mA	V_{DVDD} - 0.3			V
Output Voltage Low	V_{OL}	I_{OL} = 4mA			0.3	V
Output Current	I_{OH}	Maximum-drive mode		8		mA
		High-drive mode		6		

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (*Note 2*).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Normal-drive mode		4		
		Reduced-drive mode		2		
PCM AUDIO INTERFACE TIMING						
LRCLK Frequency Range	f_{LRCLK}	All DAI operating modes	16		192	kHz
PCM AUDIO INTERFACE TIMING						
Data Width				16		Bits
				24		
				32		
BCLK Frequency Range	f_{BCLK}	I^2S/left-justified modes	1.024		12.288	MHz
		TDM mode	1.024		24.576	
BCLK Duty Cycle	DC		45		55	%
BCLK Period	t_{BCLK}	I^2S/left-justified only	160			ns
		TDM mode	40			
Maximum BCLK Input Low-Frequency Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz		0.2		ns
Maximum BCLK Input High-Frequency Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		1		ns
NUMBER OF CHANNELS						
Number of Channels		I^2S, left-justified, or TDM mode		2		
		TDM mode only		4		
				8		
				10		
				16		
INTERFACE TIMING						
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		4			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		4			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
DIN Frame Delay After LRCLK Edge		Measured in number of BCLK cycles, set by selected TDM mode	0		2	cycles
PCM AUDIO INTERFACE TIMING/INTERFACE TIMING/PCM DATA OUTPUT (DOUT on GPIO1/2/3)						
BCLK Inactive Edge to DOUT Delay	t_{CLKTX}				14	ns
BCLK Active Edge to DOUT Hi-Z Delay	t_{HIZ}		4		18	ns
BCLK Inactive Edge to DOUT Active Delay	t_{ACTV}		0		14	ns

(V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, f_S = 48kHz, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C, Limits are 100% tested at T_A = +25°C (Note 2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PCM AUDIO INTERFACE TIMING/INTERFACE TIMING/INTERCHIP COMMUNICATION (ICC on GPIO1/2/3)						
ICC to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
ICC to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
BCLK Inactive Edge to ICC Delay	t_{CLKTX}				14	ns
BCLK Active Edge to ICC Hi-Z Delay	t_{HIZ}		4		18	ns
BCLK Inactive Edge to ICC Active Delay	t_{ACTV}		0		14	ns
I^2C INTERFACE TIMING						
Serial Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$		0		450	ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R		20		120	ns
SDA and SCL Receiving Fall Time	t_F		20 x V_{DVDD} /5.5V		120	ns
SDA Transmitting Fall Time	t_F		20 x V_{DVDD} /5.5V		120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Capacitance	C_{BUS}				550	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
RESET TIMING						
$\overline{RESET}$ Low	t_{RESET_LOW}	Minimum low time for RESET to ensure the device enters hardware shutdown		1		µs
Release from $\overline{RESET}$	t_{I2C_READY}	Time from RESET = 1 to I^2C communication available (software shutdown)			1.5	ms

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages*.

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design. Typical values are based on 1 sigma characterization data unless otherwise noted.

Note 3: Minimum and/or maximum limit is guaranteed by design or by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Note 4: Assumes device is fully programmed (AMPX_SPK_EN = 1) and EN = 1 is the last I^2C write in the sequence

Note 5: Digital filter performance is invariant over temperature and is production tested at T_A = +25ºC.

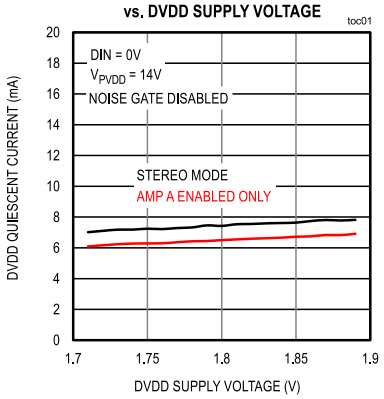
Note 6: This applies to all transitions in/out of full operation with the Noise gate enabled/disabled. Does not include state transitions due to fault conditions

Typical Operating Characteristics

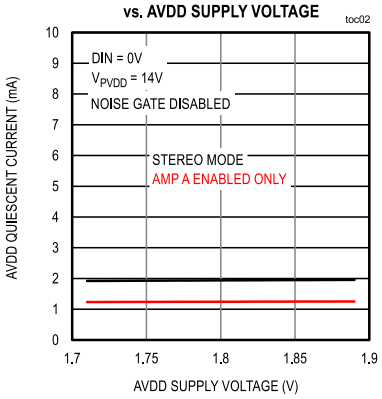
V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

MAX98425A

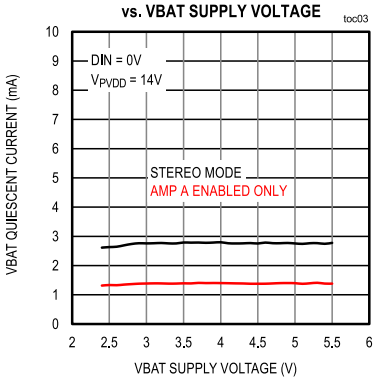
DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



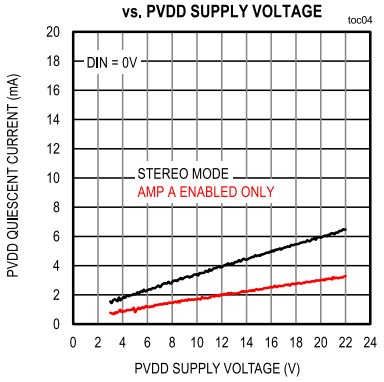
AVDD QUIESCENT CURRENT vs. AVDD SUPPLY VOLTAGE



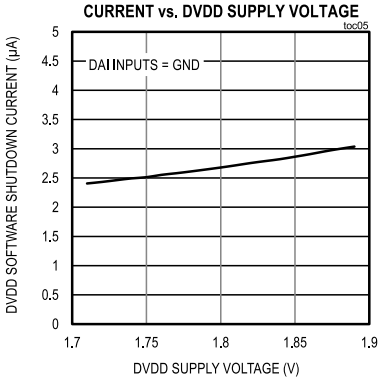
VBAT QUIESCENT CURRENT vs. VBAT SUPPLY VOLTAGE



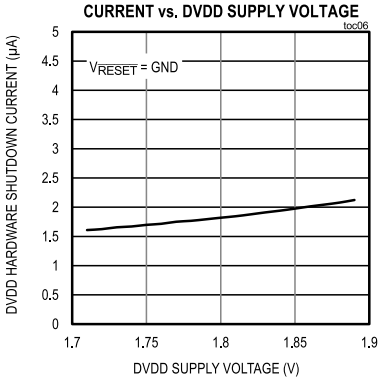
PVDD QUIESCENT CURRENT vs. PVDD SUPPLY VOLTAGE



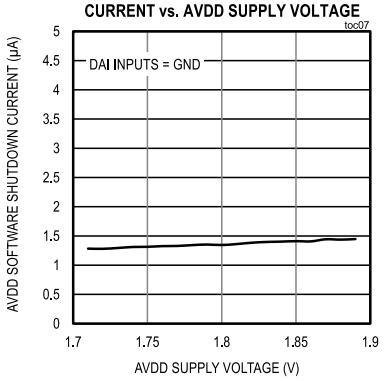
DVDD SOFTWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



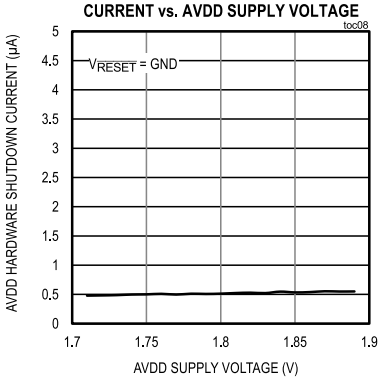
DVDD HARDWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



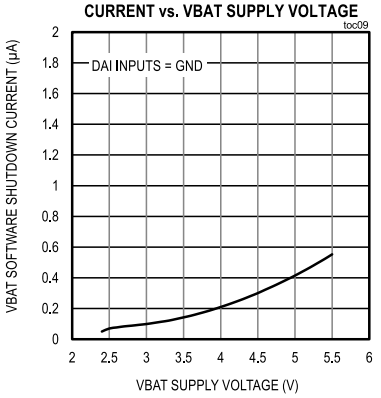
AVDD SOFTWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



AVDD HARDWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



VBAT SOFTWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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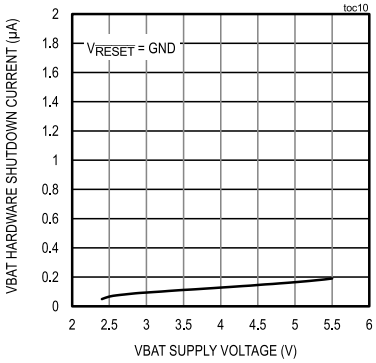
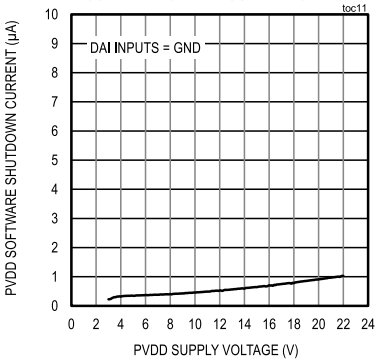
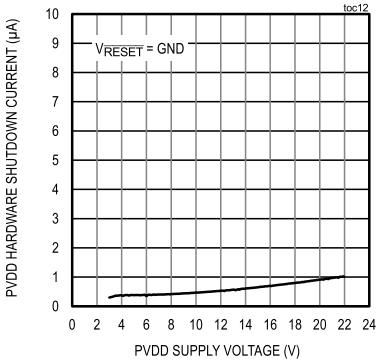
VBAT HARDWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



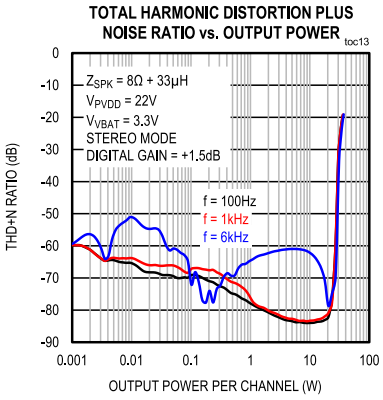
PVDD SOFTWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



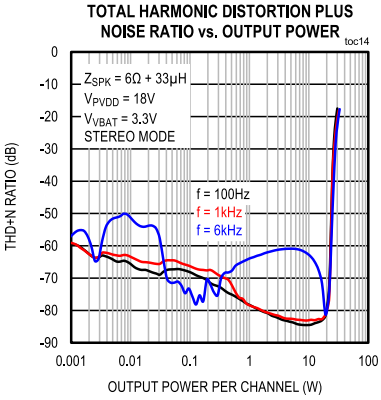
PVDD HARDWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



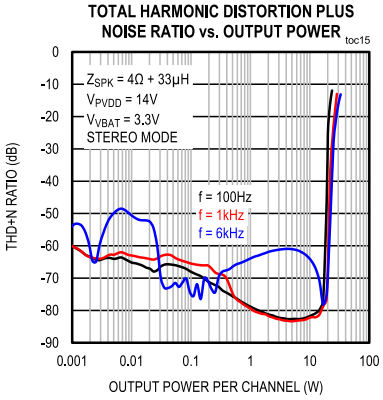
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



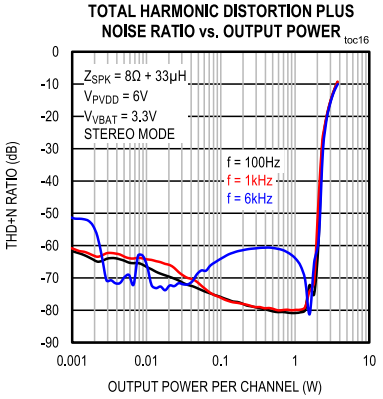
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



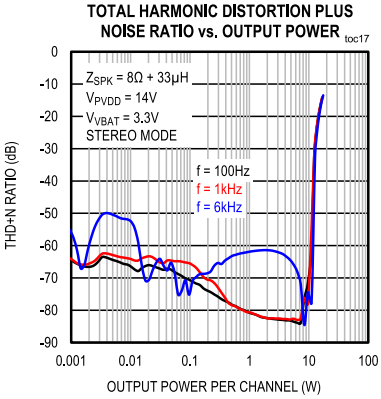
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



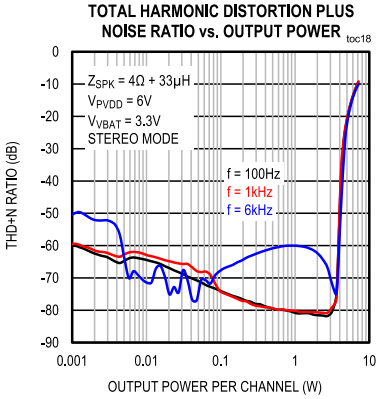
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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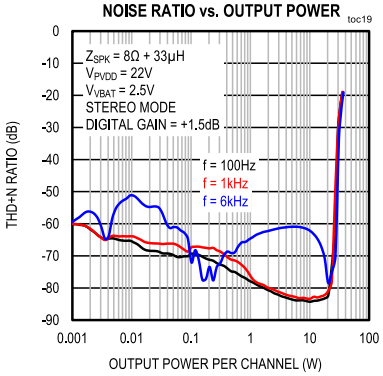
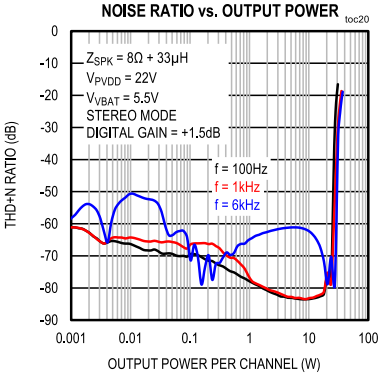
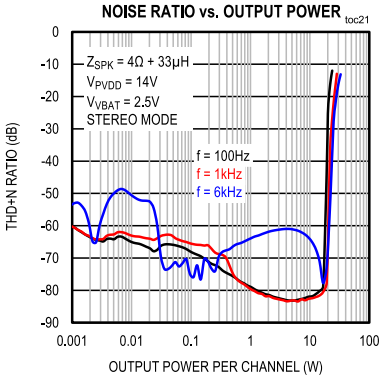
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



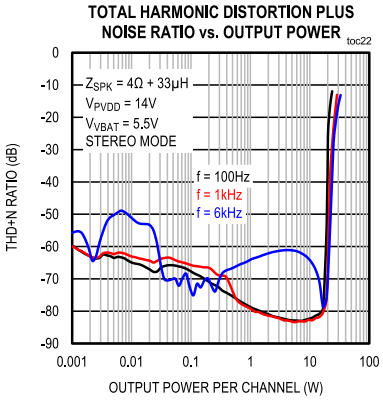
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



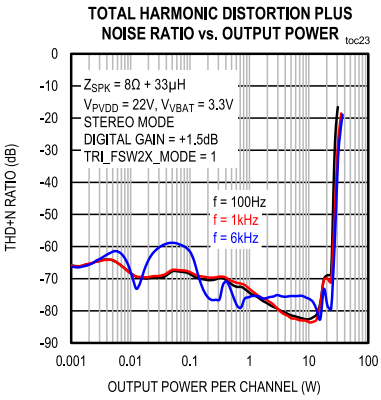
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



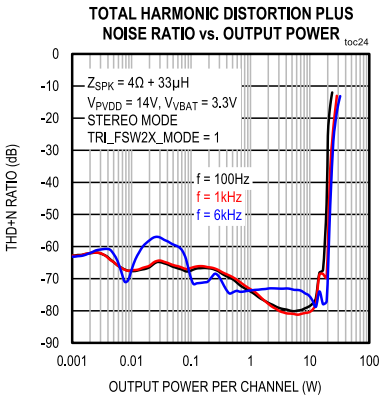
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



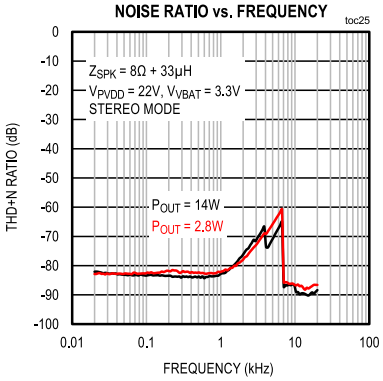
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



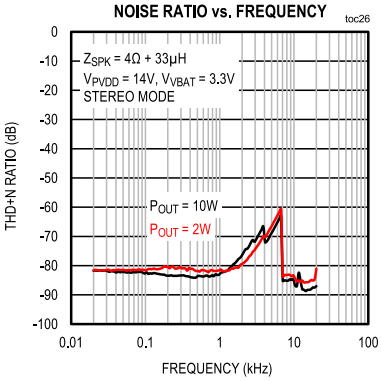
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



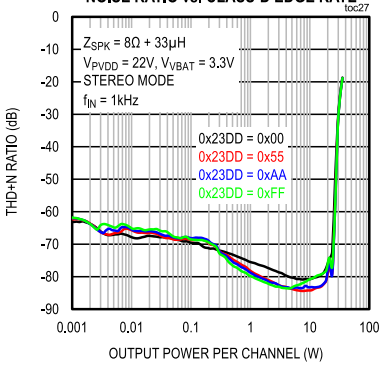
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. CLASS-D EDGE RATE



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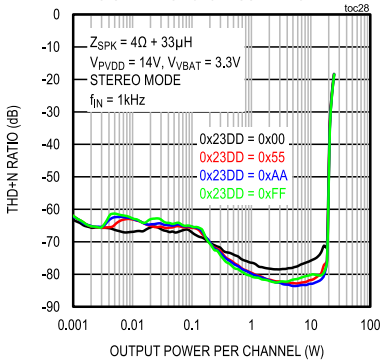
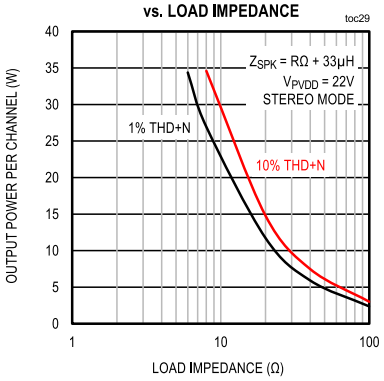
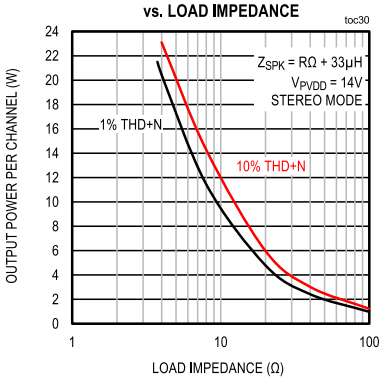
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. CLASS-D EDGE RATE



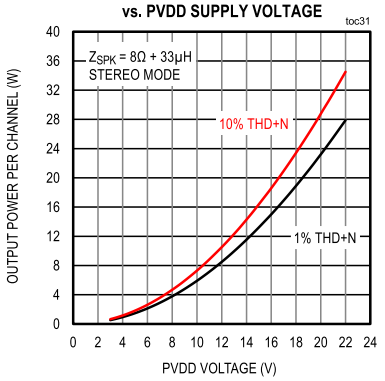
OUTPUT POWER vs. LOAD IMPEDANCE



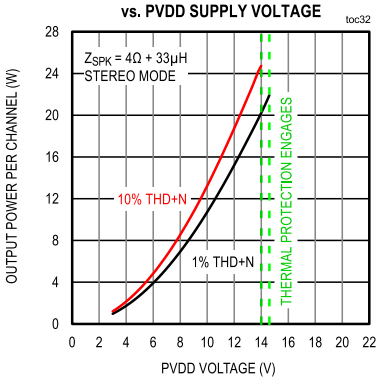
OUTPUT POWER vs. LOAD IMPEDANCE



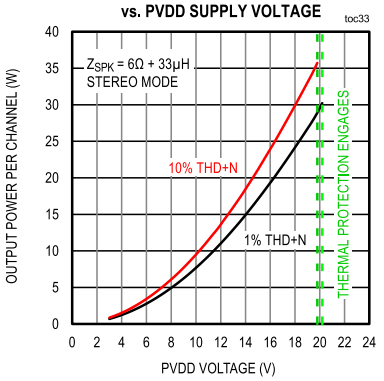
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



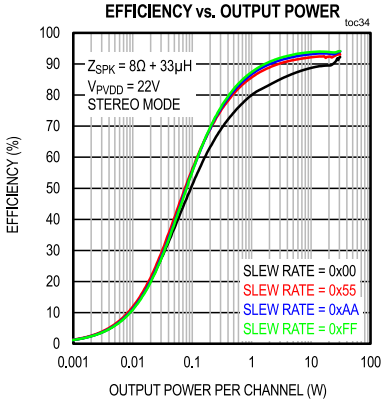
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



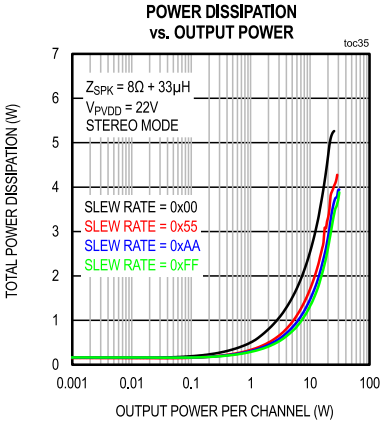
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



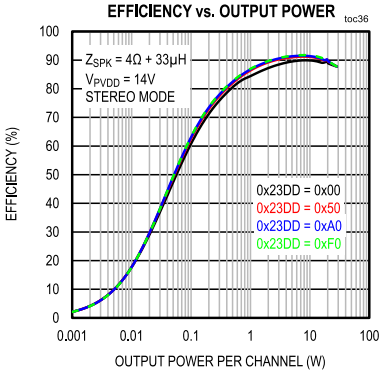
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



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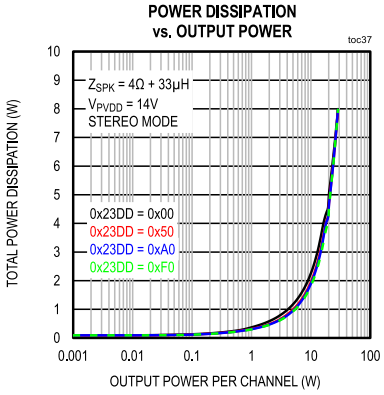

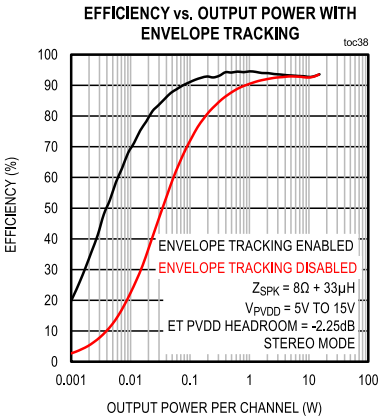

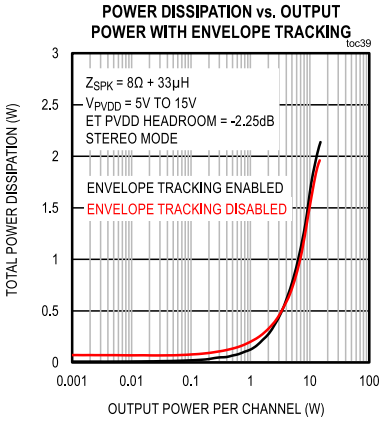

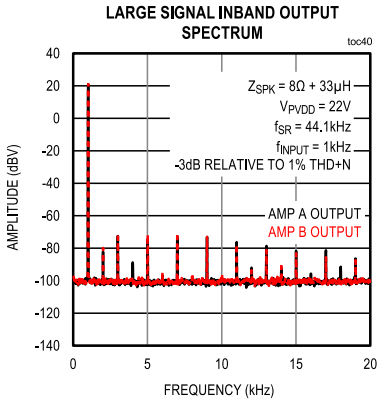

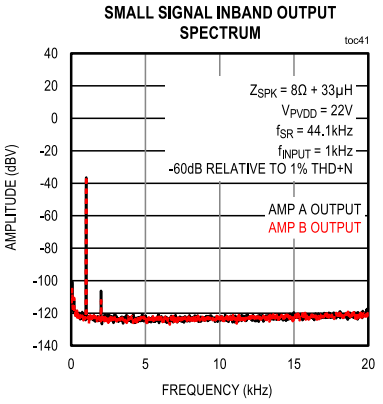

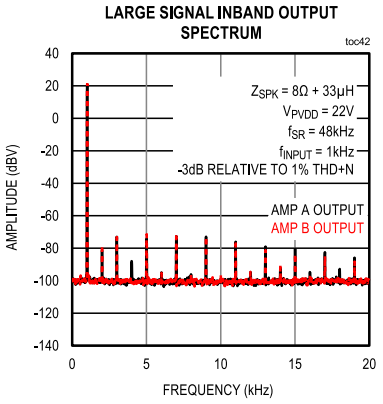

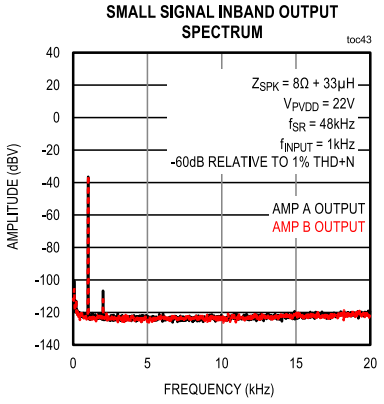

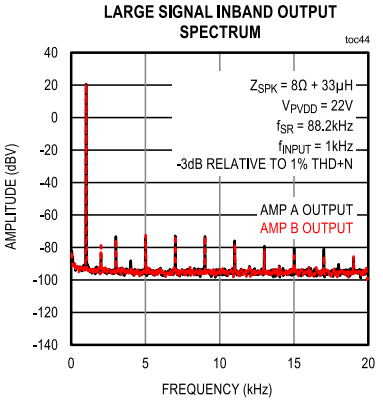

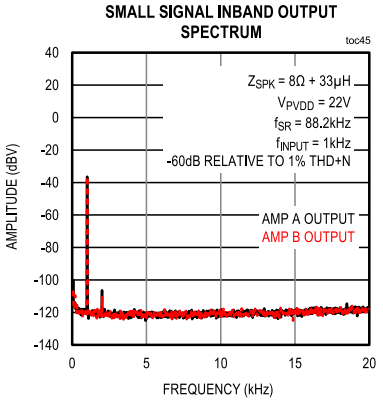

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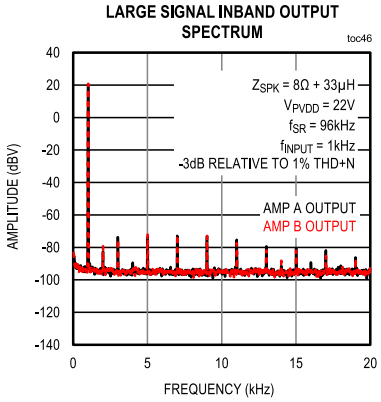
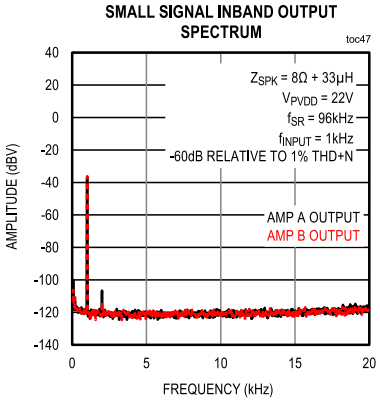
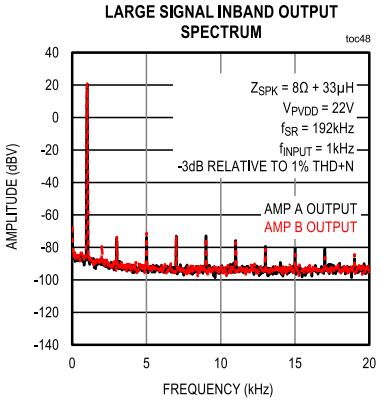
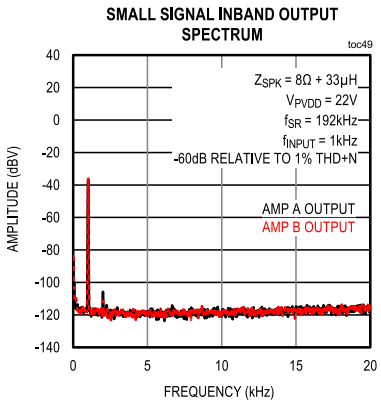
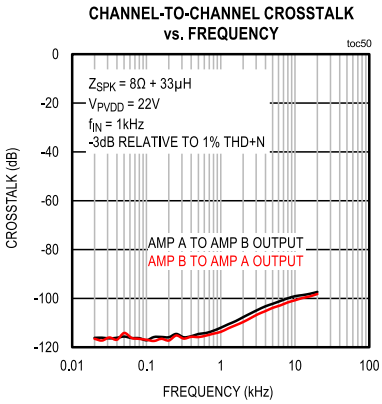
MAX98425A

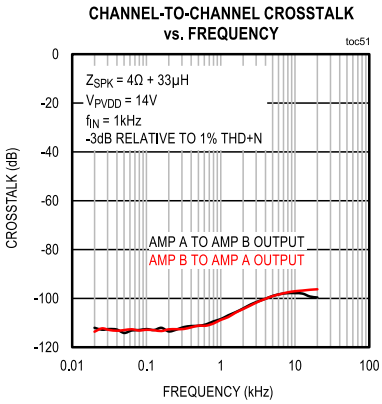












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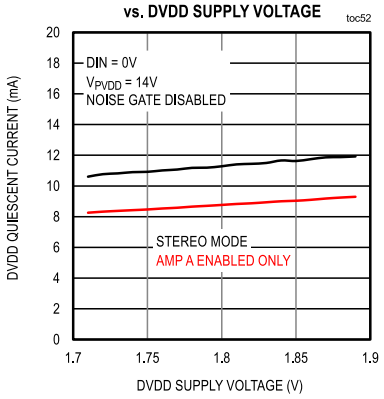
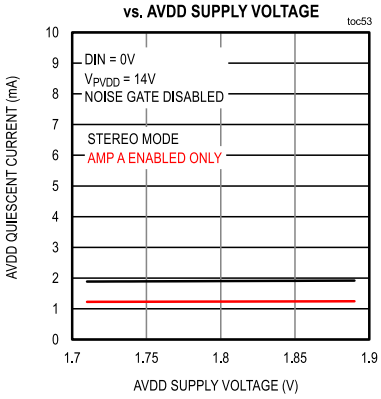
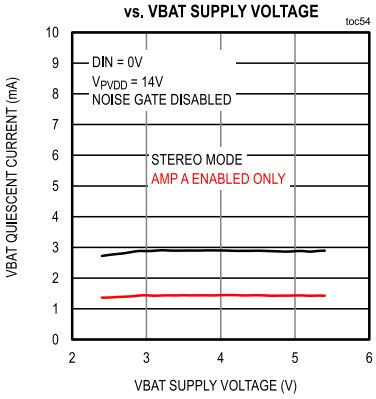
DVDD QUIESCENT CURRENT vs. DVDD SUPPLY VOLTAGE



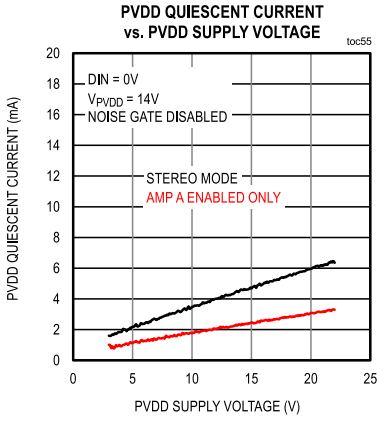
AVDD QUIESCENT CURRENT vs. AVDD SUPPLY VOLTAGE



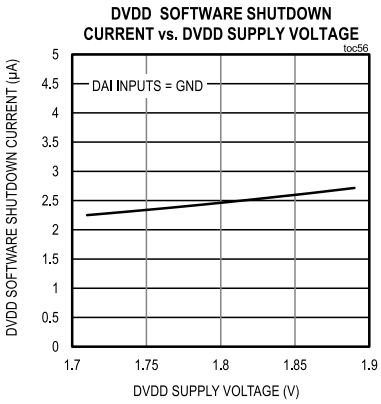
VBAT QUIESCENT CURRENT vs. VBAT SUPPLY VOLTAGE



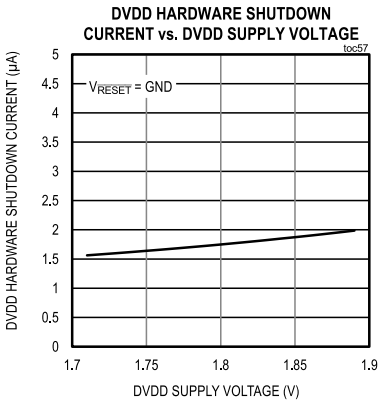
PVDD QUIESCENT CURRENT vs. PVDD SUPPLY VOLTAGE



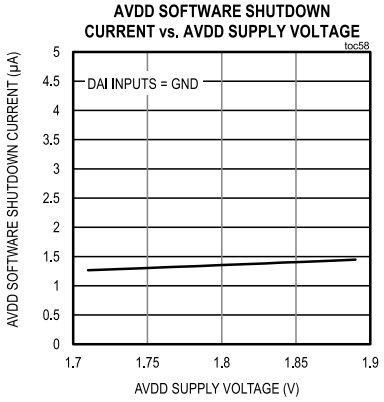
DVDD SOFTWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



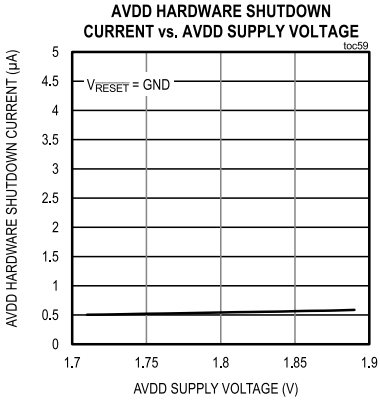
DVDD HARDWARE SHUTDOWN CURRENT vs. DVDD SUPPLY VOLTAGE



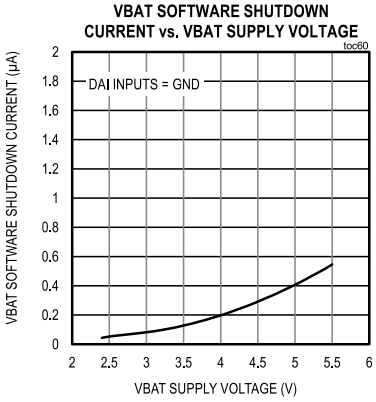
AVDD SOFTWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



AVDD HARDWARE SHUTDOWN CURRENT vs. AVDD SUPPLY VOLTAGE



VBAT SOFTWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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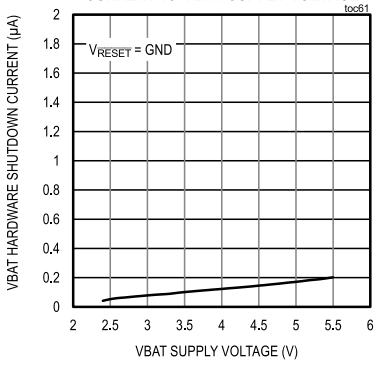
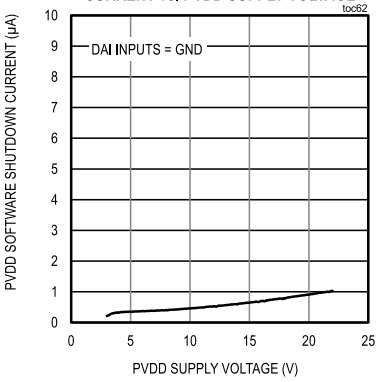
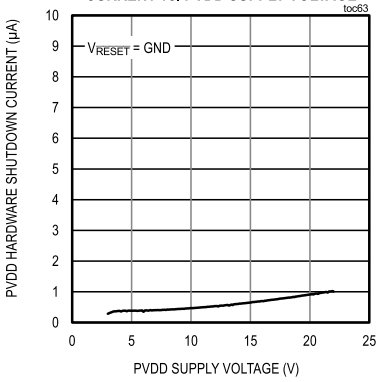
VBAT HARDWARE SHUTDOWN CURRENT vs. VBAT SUPPLY VOLTAGE



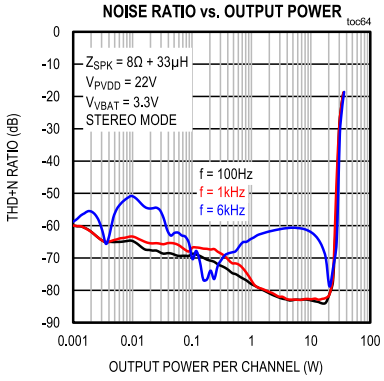
PVDD SOFTWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



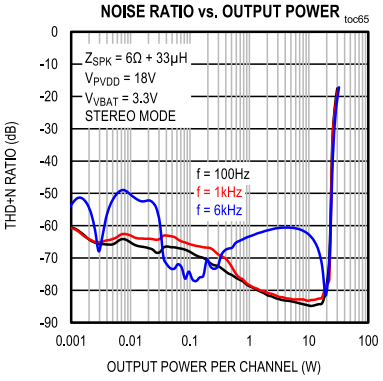
PVDD HARDWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



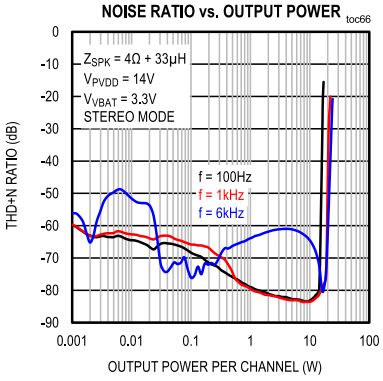
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



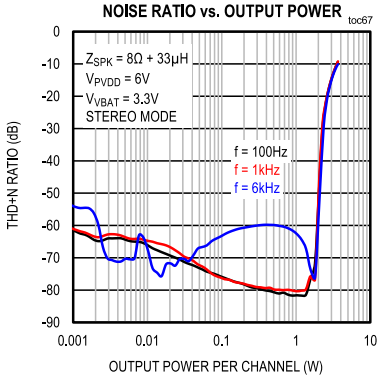
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



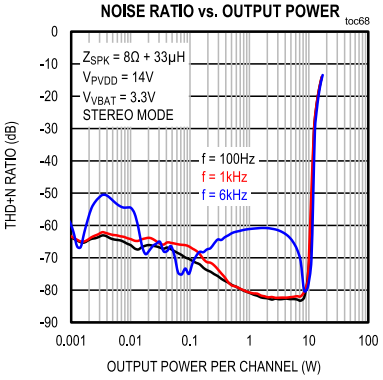
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



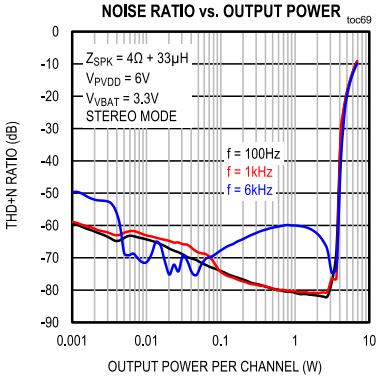
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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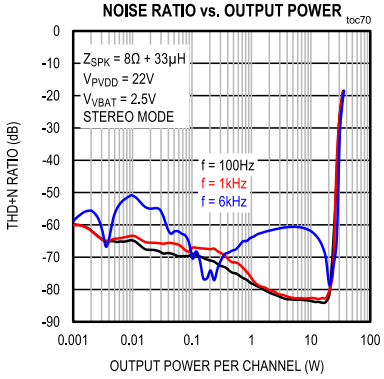
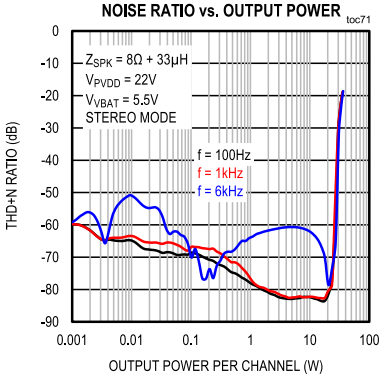
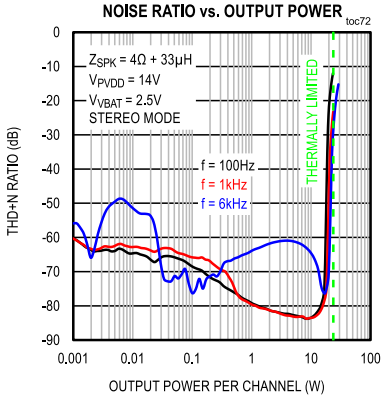
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



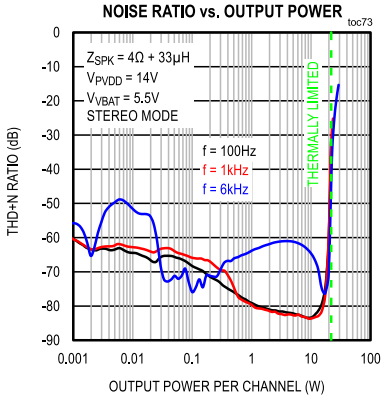
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



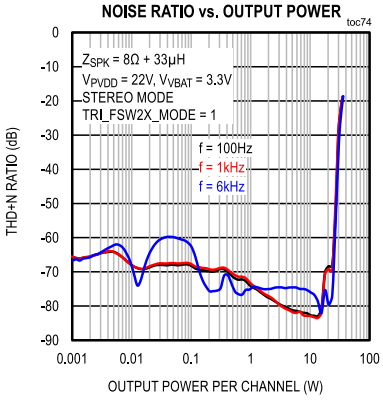
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



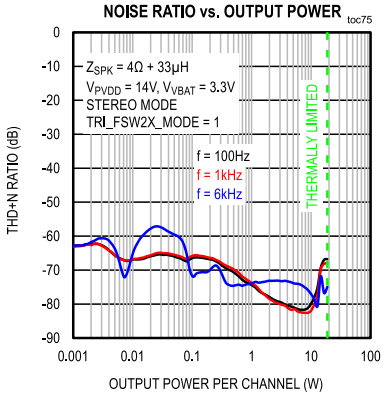
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



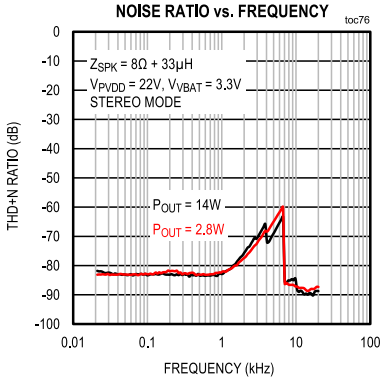
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



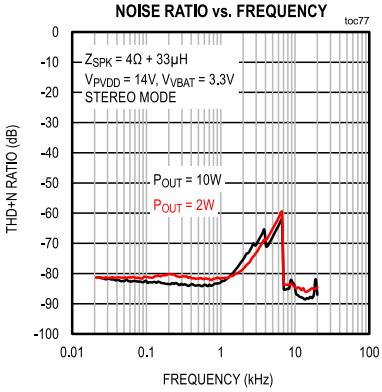
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. OUTPUT POWER



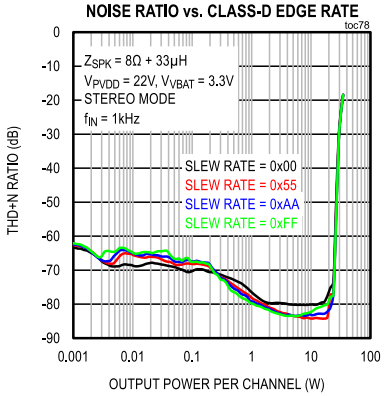
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. CLASS-D EDGE RATE



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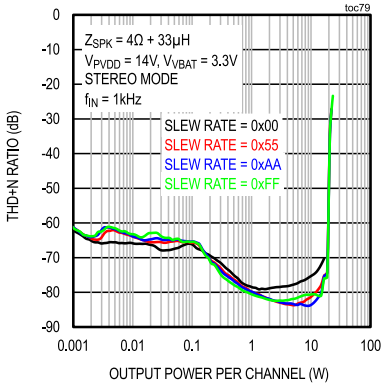
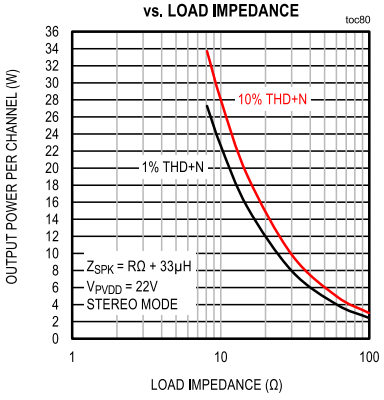
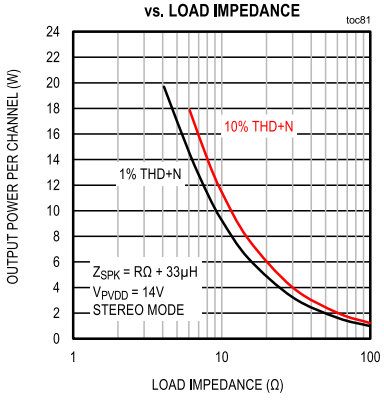
TOTAL HARMONIC DISTORTION PLUS NOISE RATIO vs. CLASS-D EDGE RATE



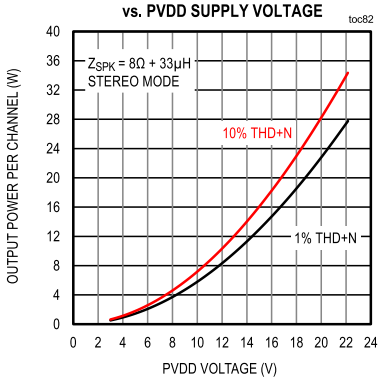
OUTPUT POWER vs. LOAD IMPEDANCE



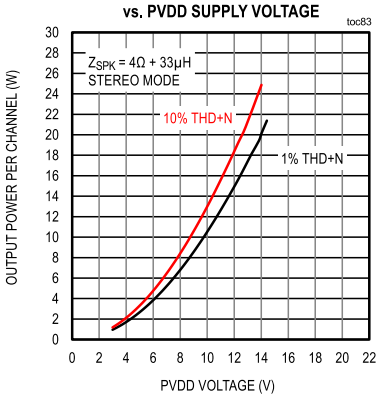
OUTPUT POWER vs. LOAD IMPEDANCE



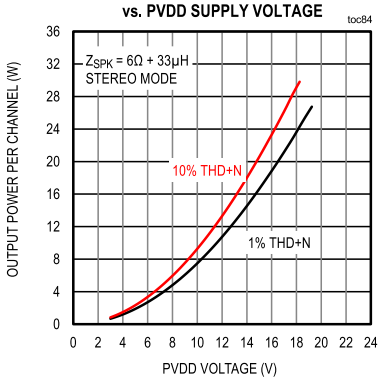
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



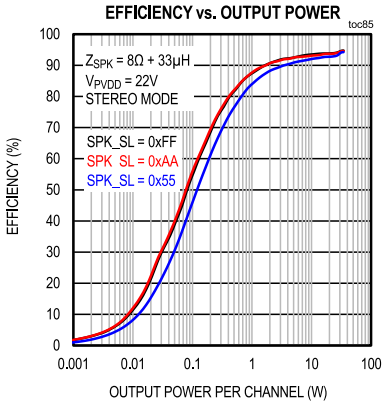
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



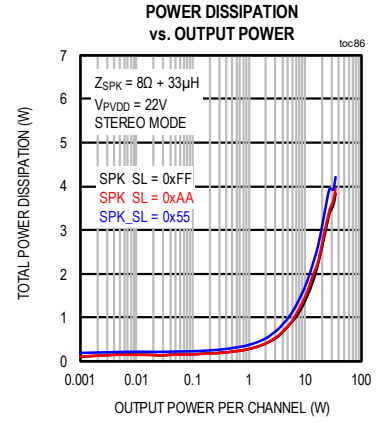
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



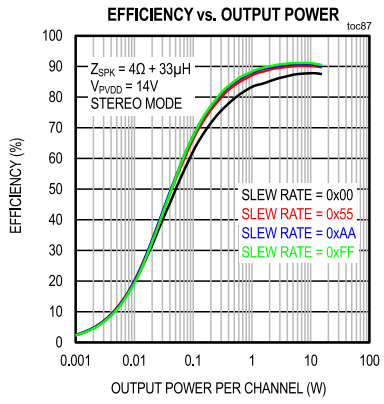
EFFICIENCY vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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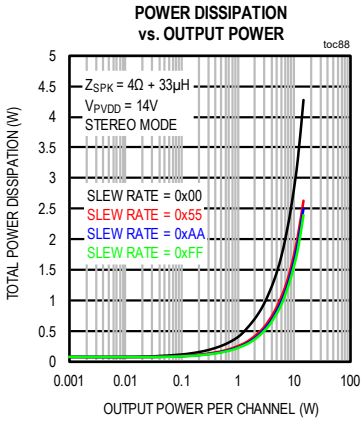

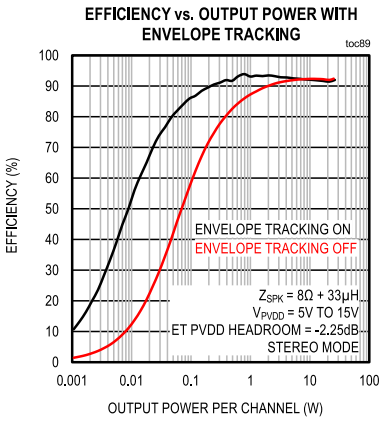

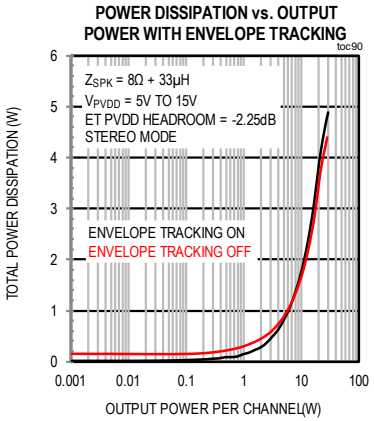

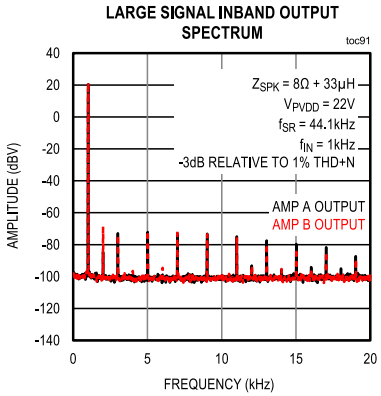

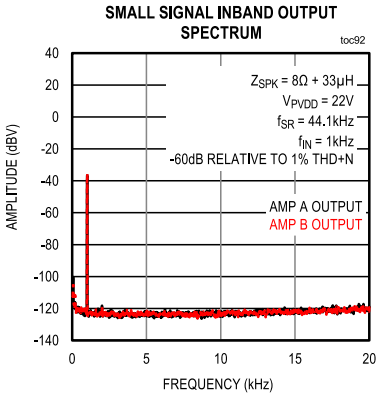

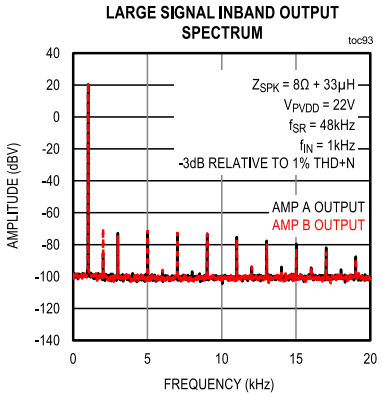

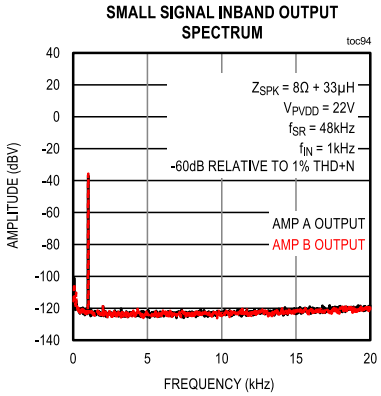

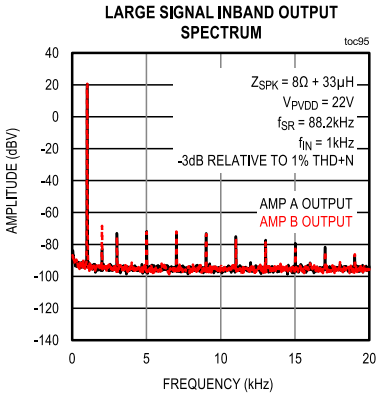

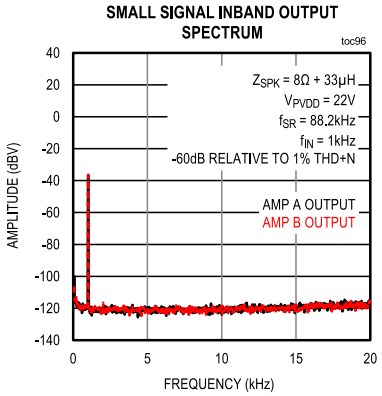

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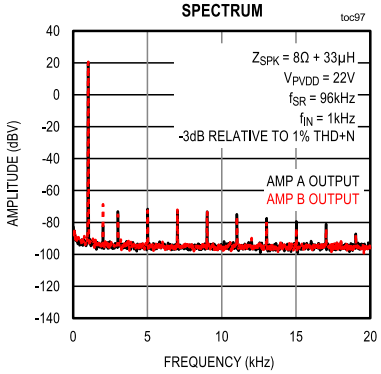
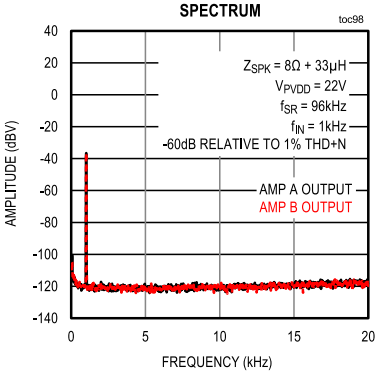
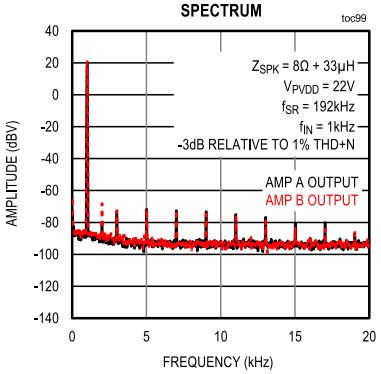
LARGE SIGNAL INBAND OUTPUT SPECTRUM



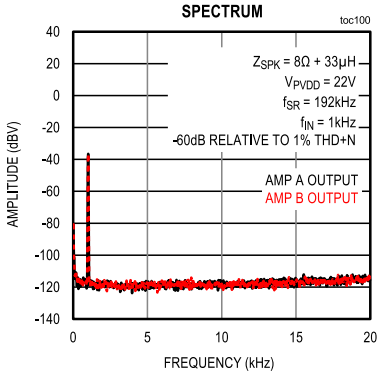
SMALL SIGNAL INBAND OUTPUT SPECTRUM



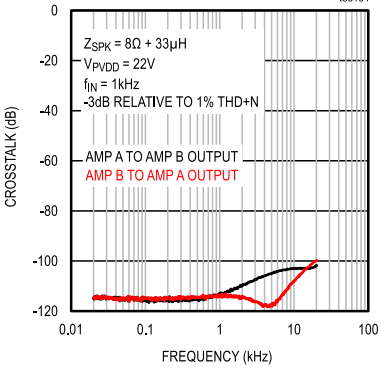
LARGE SIGNAL INBAND OUTPUT SPECTRUM



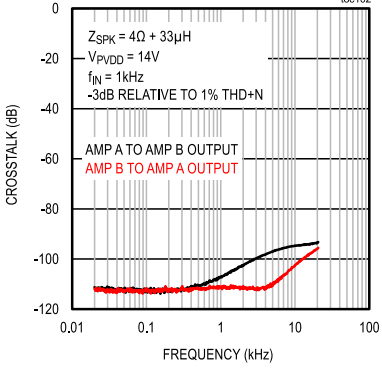
SMALL SIGNAL INBAND OUTPUT SPECTRUM



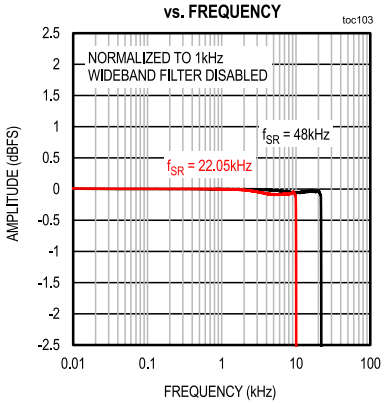
CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



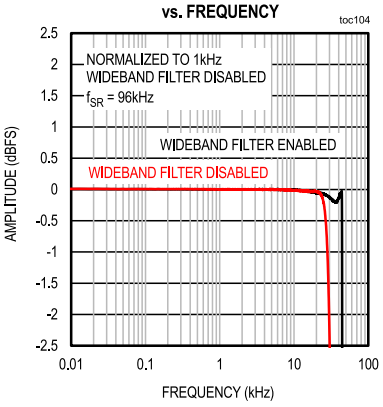
CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



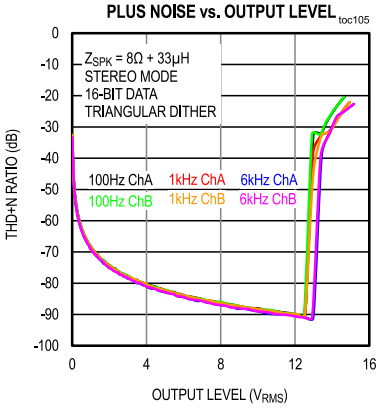
NORMALIZED IMON RESPONSE vs. FREQUENCY



NORMALIZED IMON RESPONSE vs. FREQUENCY



VFB TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL



V_{VBAT} = 3.3V, V_{PVDD} = 20V, V_{AVDD} = 1.8V, C_{VBAT} = 1µF, 10µF, C_{PVDD} = 1 x 220µF, 2 x 10µF, 2 x 0.1µF, C_{AVDD} = 1µF, C_{DVDD} = 1µF, C_{VBOOTP_A} = C_{VBOOTN_A} = C_{VBOOTP_B} = C_{VBOOTN_B} = 0.1µF, Z_{SPK} = Open, AC Measurement Bandwidth = 20Hz to 20kHz, AMPX_SPK_GAIN_MAX = 0x12 (+24dB), SPK Edge Control 1 = 0xAA, Data Width = 24-bit, T_A = 25°C, unless otherwise noted.

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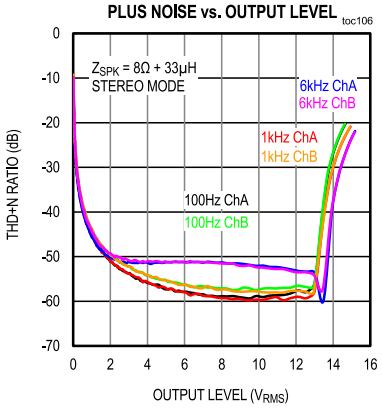
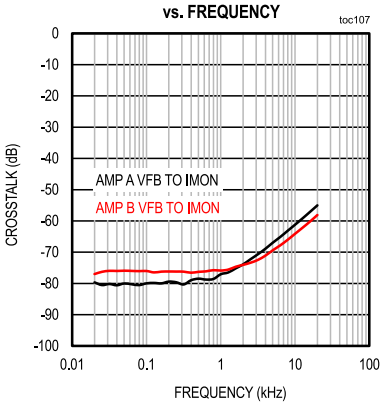
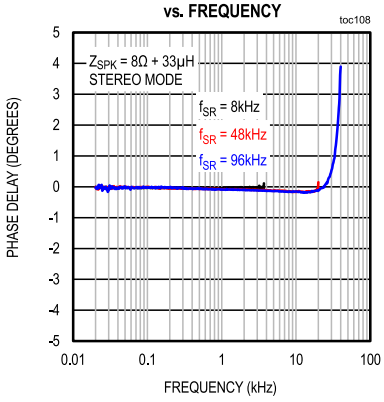
IMON TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT LEVEL



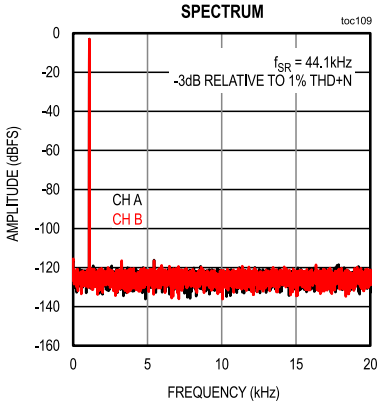
VFB TO IMON CROSSTALK vs. FREQUENCY



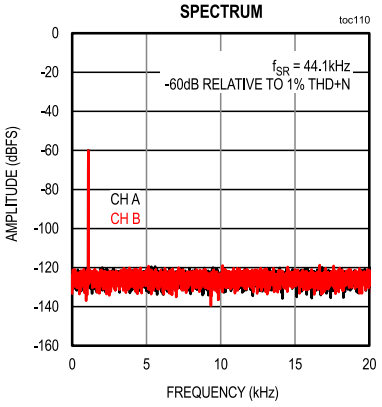
VFB TO IMON PHASE DELAY vs. FREQUENCY



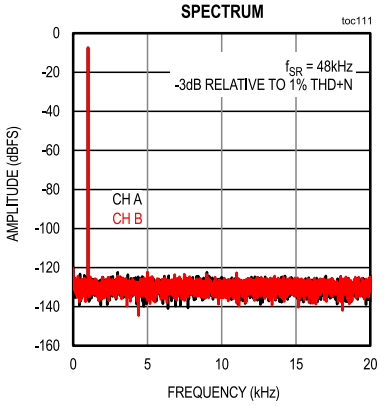
LARGE SIGNAL VFB INBAND SPECTRUM



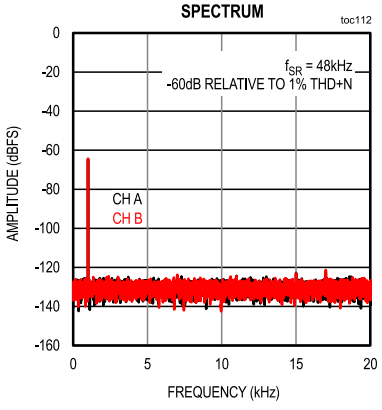
SMALL SIGNAL VFB INBAND SPECTRUM



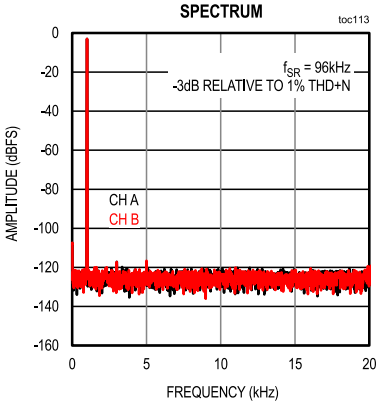
LARGE SIGNAL VFB INBAND SPECTRUM



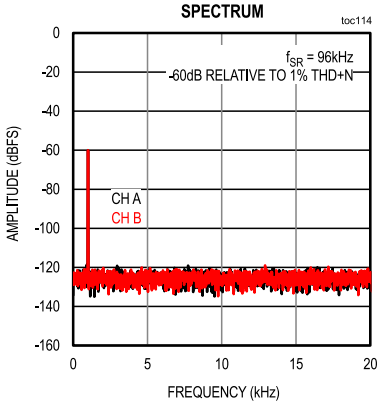
SMALL SIGNAL VFB INBAND SPECTRUM



LARGE SIGNAL VFB INBAND SPECTRUM



SMALL SIGNAL VFB INBAND SPECTRUM



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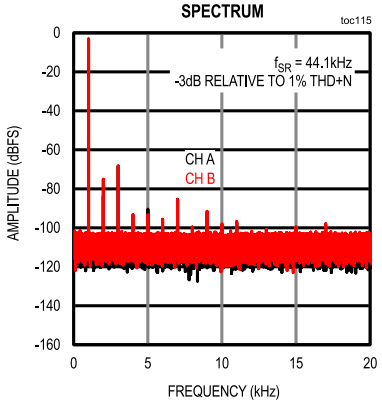
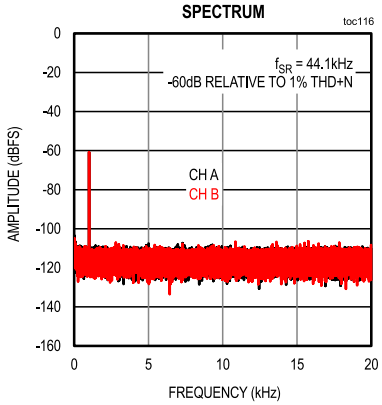
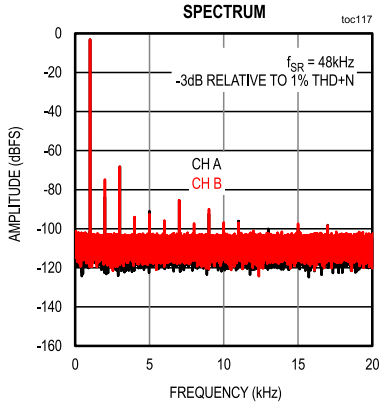
LARGE SIGNAL IMON INBAND SPECTRUM



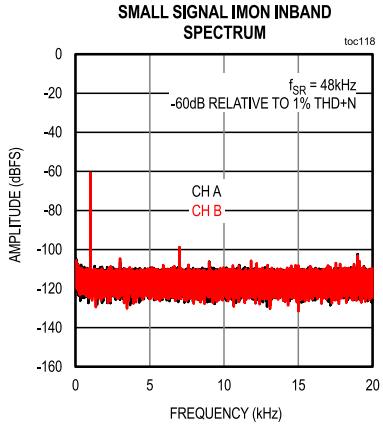
SMALL SIGNAL IMON INBAND SPECTRUM



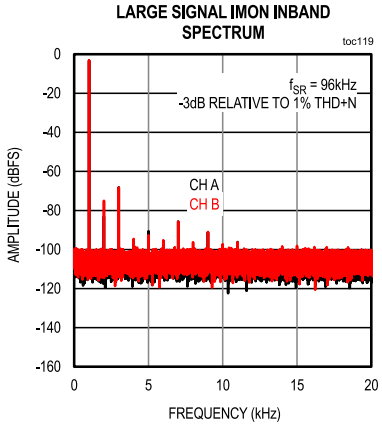
LARGE SIGNAL IMON INBAND SPECTRUM



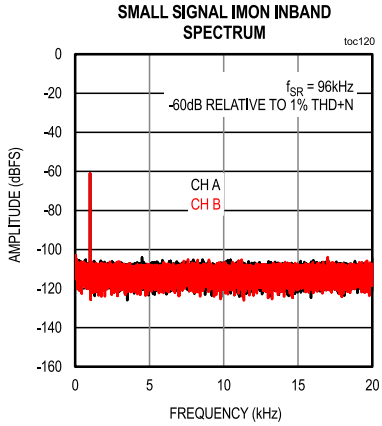
SMALL SIGNAL IMON INBAND SPECTRUM



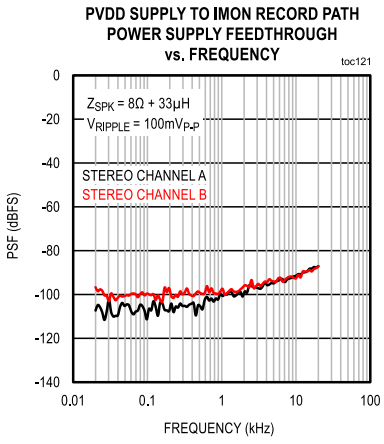
LARGE SIGNAL IMON INBAND SPECTRUM



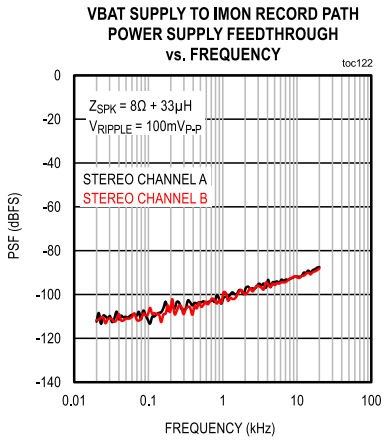
SMALL SIGNAL IMON INBAND SPECTRUM



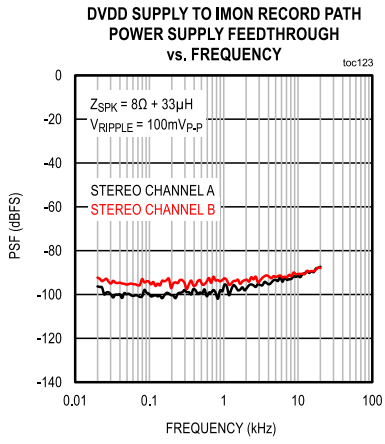
PVDD SUPPLY TO IMON RECORD PATH POWER SUPPLY FEEDTHROUGH vs. FREQUENCY



VBAT SUPPLY TO IMON RECORD PATH POWER SUPPLY FEEDTHROUGH vs. FREQUENCY



DVDD SUPPLY TO IMON RECORD PATH POWER SUPPLY FEEDTHROUGH vs. FREQUENCY



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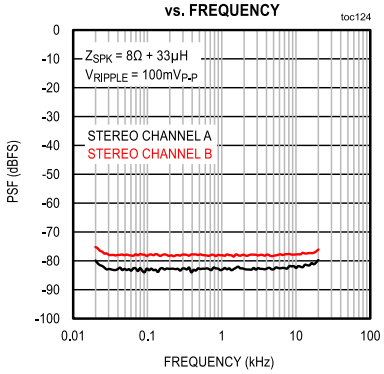
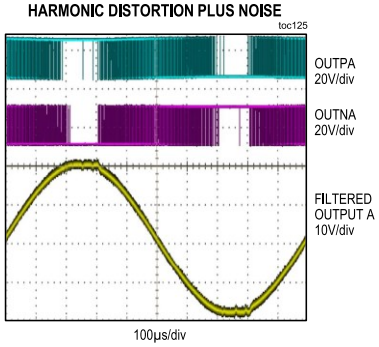
MAX98415A/MAX98425A: SYSTEM

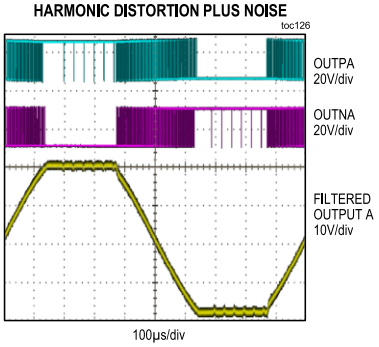
AVDD SUPPLY TO IMONRECORD PATH POWER SUPPLY FEEDTHROUGH vs. FREQUENCY



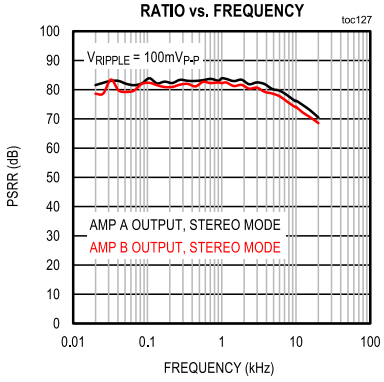
CLIPPING RESPONSE FOR 1% TOTAL HARMONIC DISTORTION PLUS NOISE



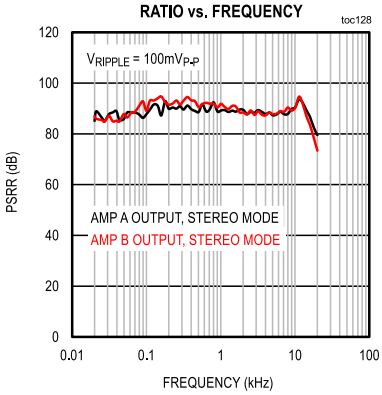
CLIPPING RESPONSE FOR 10% TOTAL HARMONIC DISTORTION PLUS NOISE



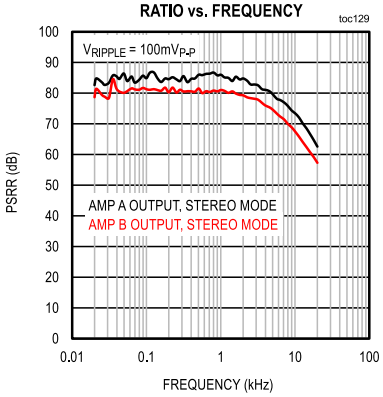
PVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



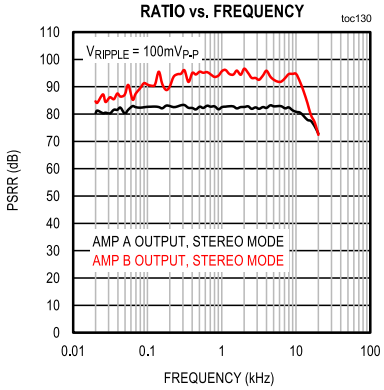
VBAT POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



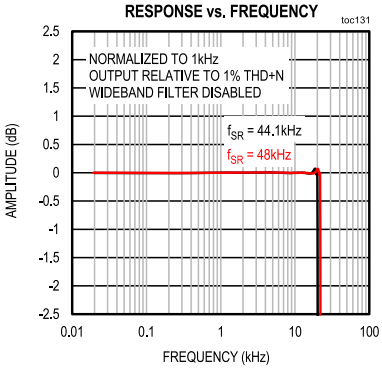
AVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



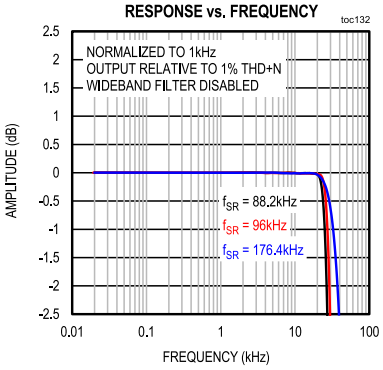
DVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



NORMALIZED OUTPUT SPEAKER RESPONSE vs. FREQUENCY



NORMALIZED OUTPUT SPEAKER RESPONSE vs. FREQUENCY



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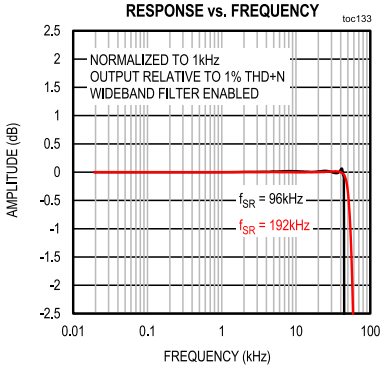
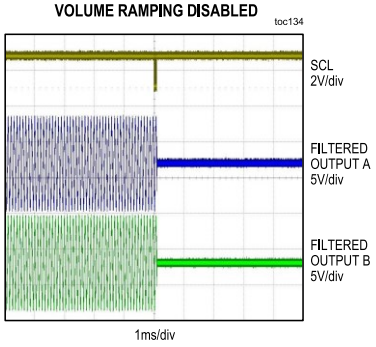
MAX98415A/MAX98425A: SYSTEM

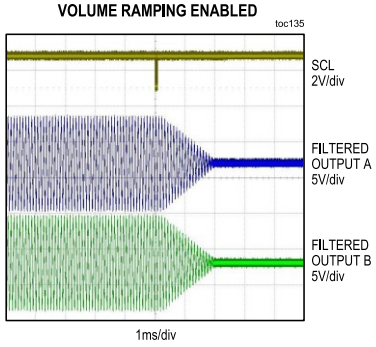
NORMALIZED OUTPUT SPEAKER RESPONSE vs. FREQUENCY



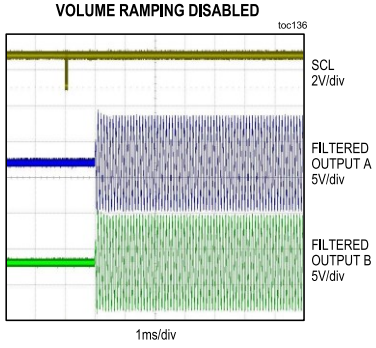
SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING DISABLED



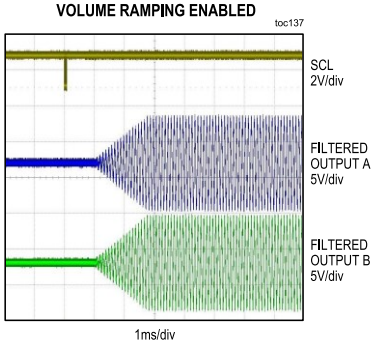
SOFTWARE DISABLE TURN-OFF RESPONSE VOLUME RAMPING ENABLED



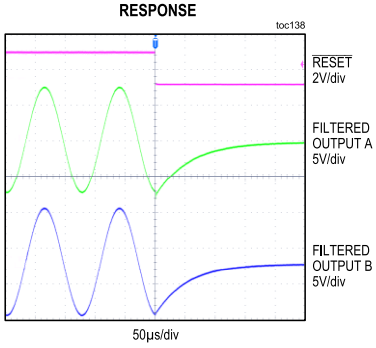
SOFTWARE DISABLE TURN-ON RESPONSE VOLUME RAMPING DISABLED



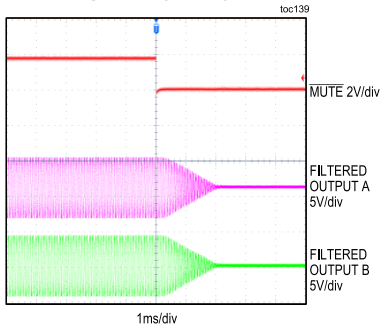
SOFTWARE DISABLE TURN-ON RESPONSE VOLUME RAMPING ENABLED



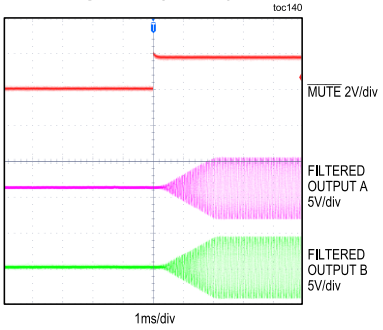
HARDWARE RESET TURN-OFF RESPONSE



ENTERING MUTE WITH MUTE PIN PULLED LOW



EXITING MUTE WITH MUTE PIN PULLED HIGH



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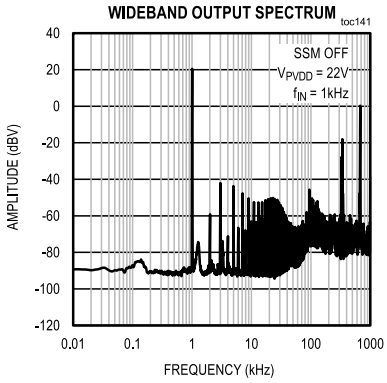
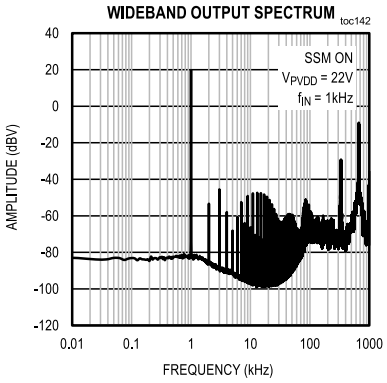
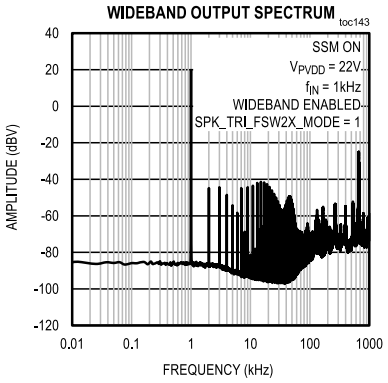
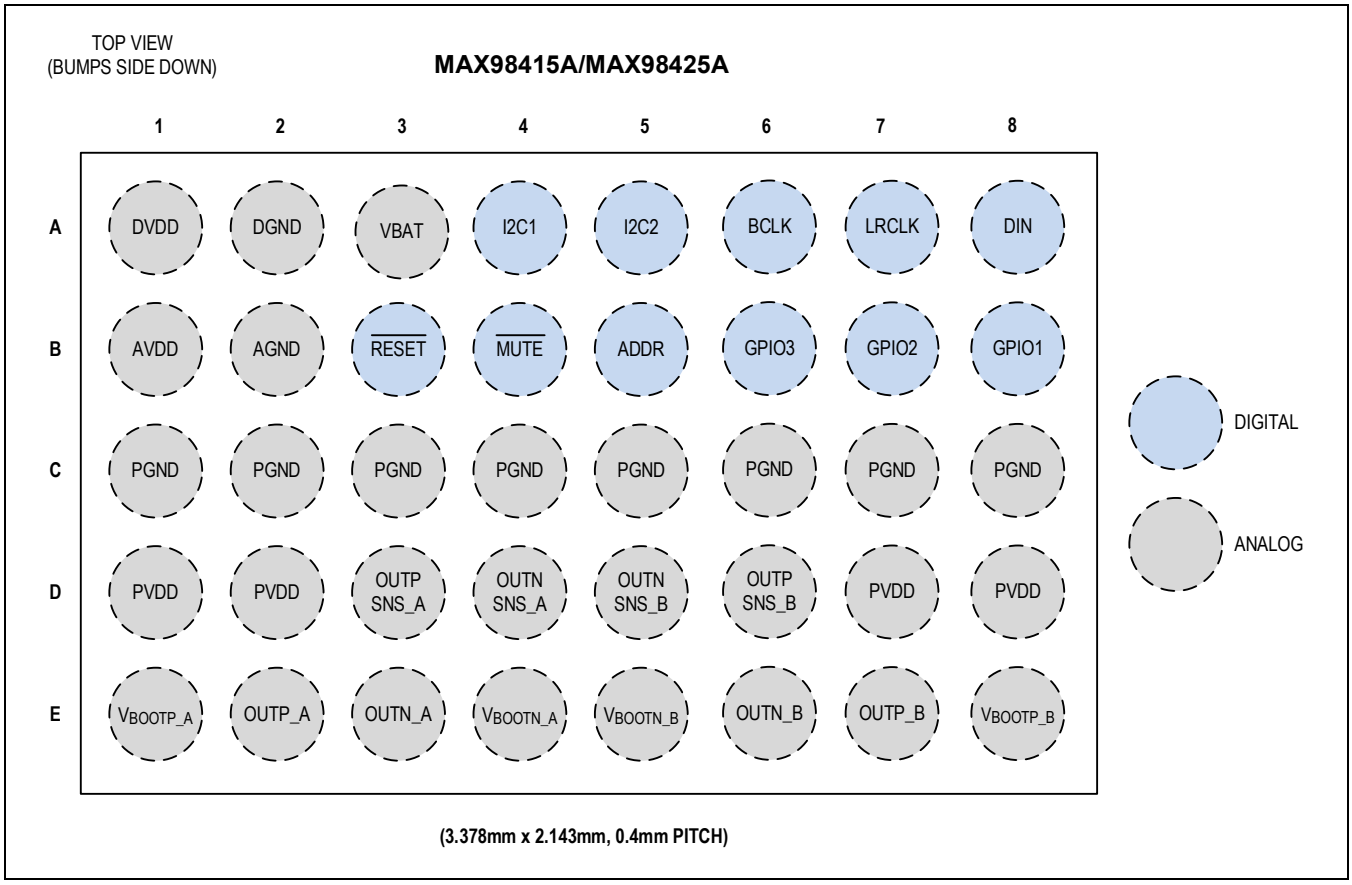
MAX98415A/MAX98425A: SYSTEM







Pin Configurations



Pin Descriptions

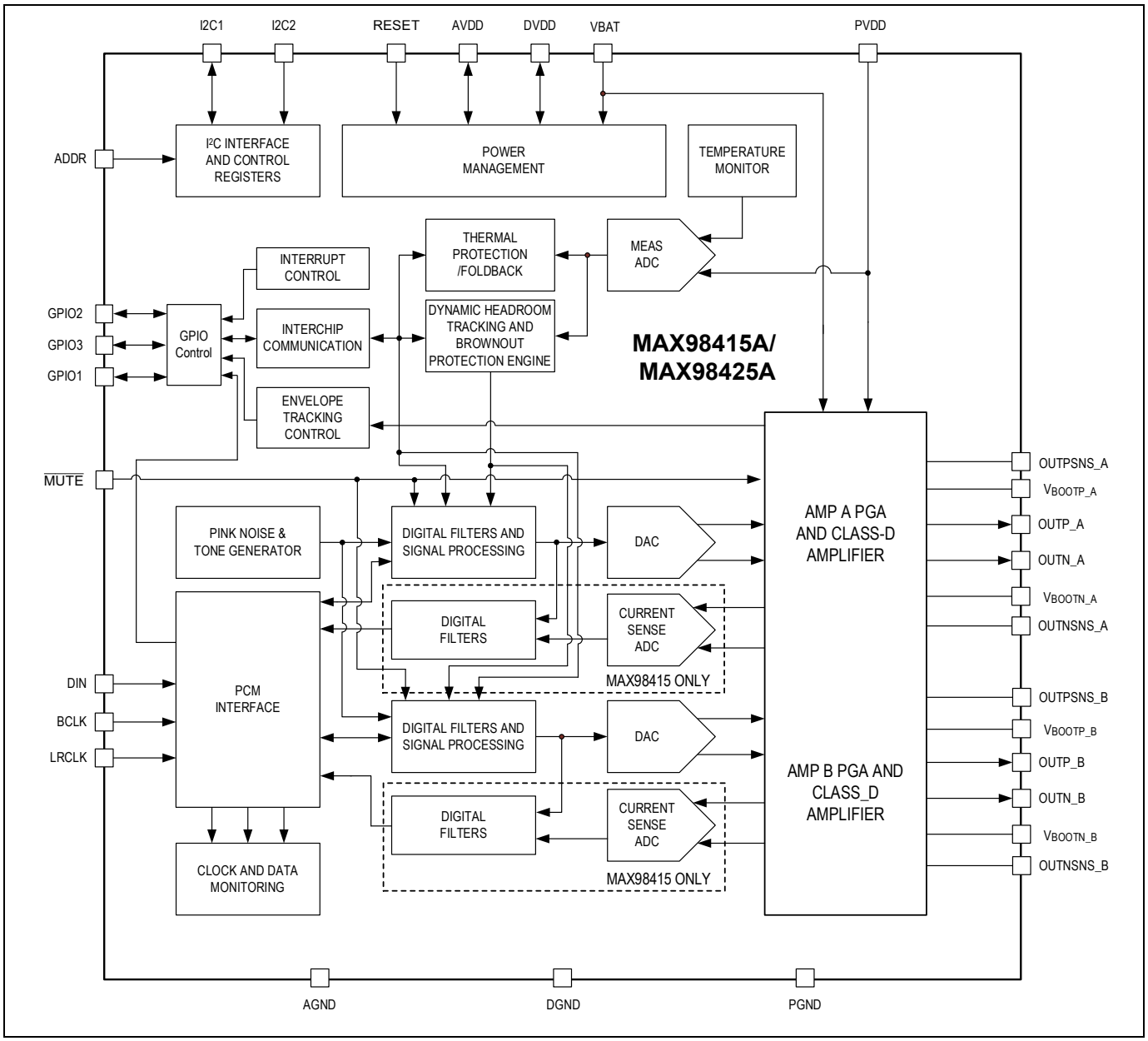
PIN	NAME	FUNCTION	REF SUPPLY	Type
A1	DVDD	Digital Core and Digital I/O Power Supply. Bypass to DGND with a 1µF capacitor.		Supply
A2	DGND	Digital Ground.		Supply
A3	VBAT	Power Supply Input for internal LDOs, gate drive, and digital inputs. Bypass to DGND with a 1µF capacitor placed as close as possible.		Supply
A4	I2C1	I^2C-Compatible Serial-Data/Clock 1. This pin can be configured as either SDA or SCL. Connect a 1.5kΩ pullup resistor to DVDD for a full logic level swing.		Digital I/O (Open Drain)
A5	I2C2	I^2C -Compatible Serial-Data/Clock 1. This pin can be configured as either SDA or SCL. Connect a 1.5kΩ pullup resistor to DVDD for a full logic level swing.		Digital I/O (Open Drain)
A6	BCLK	PCM Interface BCLK Input. Internally pulled down to DGND through R PD.		Digital Input
A7	LRCLK	PCM Interface frame clock Input/Output. LRCLK frequency matches the PCM interface sample rate. Internally pulled down to DGND through R PD.		Digital Input
A8	DIN	PCM Interface Data Input. Internally pulled down to DGND through R PD.		Digital Input
B1	AVDD	Analog Power-Supply. Bypass to AGND with a 1µF capacitor placed as close as possible.		Supply
B2	AGND	Analog Ground. Connect to the common ground plane of the Application.		Supply

B3	$\overline{\text{RESET}}$	Hardware Enable (Active-Low). Resets all digital portions of the device and all registers to default PoR settings.		Supply
B4	$\overline{\text{MUTE}}$	External volume mute pin (Active-Low). A low signal mutes the outputs of both amplifiers.		Digital Input
B5	ADDR	I²C Address Select input. See the *Peripheral Address* section for additional information.		Digital Input
B6	GPIO3	Digital I/O is configurable through the I²C register setting. The pin is configurable as DOUT or, IRQ, or ET_OUT, or ICC. DOUT is PCM Interface Data Output IRQ is Hardware Interrupt Output. Interrupt polarity and pin drive mode are configurable. Connect a 10kΩ pullup resistor to VDD for full logic level swing in open drain mode. The envelope tracker output signal (ET_OUT) is a PWM output signal that controls the external boost output regulation voltage. Interchip Communication Data Bus (ICC). Allows multiple devices to be grouped up to communicate with each other.	DVDD	Digital I/O
B7	GPIO2	Digital I/O is configurable via the I²C register setting. The pin can be configured as DOUT, IRQ, ET_OUT, or ICC. DOUT is PCM Interface Data Output IRQ is Hardware Interrupt Output. Interrupt polarity and pin drive mode are configurable. Connect a 10kΩ pullup resistor to VDD for full logic level swing in open drain mode. The envelope tracker output signal (ET_OUT) is a PWM output signal that controls the external boost output regulation voltage. Interchip Communication Data Bus (ICC). Allows multiple devices to be grouped up to communicate with each other.	DVDD	Digital I/O
B8	GPIO1	Digital I/O is configurable via the I²C register setting. The pin can be configured as DOUT, IRQ, ET_OUT, or ICC. DOUT is PCM Interface Data Output. IRQ is Hardware Interrupt Output. Interrupt polarity and pin drive mode are configurable. Connect a 10kΩ pullup resistor to DVDD for full logic level swing in open drain mode. The envelope tracker output signal (ET_OUT) is a PWM output signal that controls the external boost output regulation voltage. Interchip Communication Data Bus (ICC). Allows multiple devices to be grouped up to communicate with each other.	DVDD	Digital I/O
C1–C8	PGND	Power Ground Speaker Amplifiers A and B.		Supply
D1, D2	PVDD	Power Supply Input for Amplifier A and Amplifier B. Bypass to PGND with a 0.1µF and 10µF capacitor placed as close as possible.		Supply
D3	OUTPSNS_A	Speaker Amplifier A Feedback Positive Input. Connect as close as possible to the positive terminal of the loudspeaker. This pin must form a complete loop with OUTP_A.	PVDD	Analog Input
D4	OUTNSNS_A	Speaker Amplifier A Feedback Negative Input. Connect as close as possible to the negative terminal of the loudspeaker. This pin must form a complete loop with OUTN_A.	PVDD	Analog Input
D5	OUTNSNS_B	Speaker Amplifier B Feedback Negative Input. Connect the pin as close as possible to the negative terminal of the loudspeaker. This pin must form a complete loop with OUTN_B.	PVDD	Analog Input
D6	OUTPSNS_B	Speaker Amplifier B Feedback Positive Input. Connect the pin as close as possible to the positive terminal of the loudspeaker. This pin must form a complete loop with OUTP_B.	PVDD	Analog Input
D7, D8	PVDD	Power Supply Input for Amplifier A & Amplifier B. Bypass to PGND with a 0.1µF and 10µF capacitor placed as close as possible		Supply
E1	V_{BOOTP_A}	Bootstrap for high side gate drive for Speaker Amplifier A. Connect 0.1µF capacitor between V_{BOOTP_A} and OUTP_A.	VBAT	Analog Output

E2	OUTP_A	Positive Speaker Amplifier Output for Amplifier A.	PVDD	Analog Output
E3	OUTN_A	Negative Speaker Amplifier Output for Amplifier A.	PVDD	Analog Output
E4	V_{BOOTN_A}	Bootstrap for high side gate drive for Speaker Amplifier A. Connect 0.1µF capacitor between V_{BOOTN_A} and OUTN_A.	VBAT	Analog Output
E5	V_{BOOTN_B}	Bootstrap for high side gate drive for Speaker Amplifier B. Connect 0.1µF capacitor between V_{BOOTN_B} and OUTN_B.	VBAT	Analog Output
E6	OUTN_B	Negative Speaker Amplifier Output for Amplifier B.	PVDD	Analog Output
E7	OUTP_B	Positive Speaker Amplifier Output for Amplifier B.	PVDD	Analog Output
E8	V_{BOOTP_B}	Bootstrap for high side gate drive for Speaker Amplifier B. Connect 0.1µF capacitor between V_{BOOTP_B} and OUTP_B.	VBAT	Analog Output

Functional Diagrams

Detailed Block Diagram



Detailed Description

Device State Control

The device has three distinct power states: the hardware shutdown state, the software shutdown state, and the active state. When transitioning between states, the device always moves from the hardware shutdown state to the software shutdown state to the active state (or the reverse) based on the state transition requirements. Normal transitions between the software shutdown state and active state are reversible without waiting for an in-progress transition to be completed. State transitions due to fault conditions, supply removal, and reset conditions are not reversible and are always completed (once initiated) to protect the device.

Hardware Shutdown State

When the device is first powered up, or after a hardware reset event, the device always initializes into the hardware shutdown state. In hardware shutdown, the device is configured to its lowest power state. Upon entering hardware shutdown the device is globally placed into a reset condition. As a result, the I^2C control interface is disabled, and all device registers are returned to their PoR states. When exiting the hardware shutdown, the device initializes and then transitions into the software shutdown state. During this transition (as part of initialization), the OTP register trim settings are loaded. If the OTP load routine fails to complete successfully, an OTP_FAIL_* interrupt is generated once the device reaches the software shutdown state.

When the hardware reset input ($\overline{RESET}$) is asserted low, the device enters (or remains in) hardware shutdown. The device is also placed into hardware shutdown anytime the DVDD supply drops below its PoK threshold. The device only exits hardware shutdown when the DVDD supply is above its PoK threshold, and the hardware reset input ($\overline{RESET}$) is asserted high. Once all of these conditions are met, the device automatically exits hardware shutdown and transitions into software shutdown.

Software Shutdown State

The device enters the software shutdown state after it transitions out of the hardware shutdown state and when exiting the active state. In the software shutdown state, all blocks are automatically disabled except for the I^2C control interface. The device successfully enters a software shutdown state from a hardware shutdown state when at least AVDD, DVDD, and PVDD pins exceed their UVLO thresholds, and $\overline{RESET}$ is asserted high. In the software shutdown state, all device registers can be programmed without restriction, and all programmed register states are retained.

The global enable bit (EN) is used to transition the device into and out of software shutdown. When global enable (EN) is set high, the device transitions to the active state, and a power-up done (AMPX_PWRUP_DONE_*) interrupt is generated. Each amplifier has its own power-up done interrupt. When the device is in the active state, and global enable (EN) is set low, the device transitions to the software shutdown state, and a power-down done (PWRDN_DONE_*) interrupt is generated. Additionally, the device is reset and enters software shutdown anytime the global reset bit (RST) is written with a 1.

By default, the device supply configuration is AVDD, PVDD, and VBAT pins being supplied with voltages, and in this scenario, regardless of the state of the global enable bit, the device cannot transition from the software shutdown state to the active state until AVDD, PVDD, and VBAT are all above their UVLO thresholds. If DVDD, PVDD, or VBAT supplies drop below their UVLO levels, or if AVDD supply drops below its PoK threshold while the device is in the active state, the device is forced back into the software shutdown state. If the AVDD and DVDD supplies drop below their UVLO thresholds while the device is in the active state, an appropriate UVLO fault interrupt (AVDD_UVLO_* or DVDD_UVLO_* respectively) is generated.

While in the software shutdown state, the AVDD, PVDD, and VBAT supplies can be powered down safely.

Recovery from Software Shutdown due to Supply Faults

The device provides two forms of fault recovery if either VBAT or PVDD drops below their UVLO thresholds while the device is in its active state. Based on the setting of the VBAT_AUTORESTART_EN and PVDD_AUTORESTART_EN bits, the individual supply fault recovery is either in manual mode or auto restart mode.

If the bit is set low, then the supply UVLO fault recovery is in manual mode. In manual mode, when the supply drops below its UVLO threshold, the device transitions into the software shutdown state (sets EN = 0) and generates the appropriate UVLO fault shutdown interrupt (VBAT_UVLO_SHDN_* or PVDD_UVLO_SHDN_* respectively). Even once the supply recovers (voltage levels exceed the UVLO thresholds), the device remains in the software shutdown state until the global enable bit (EN) is set high by the host software and the AVDD supply is above its UVLO threshold.

If the bit is instead set high, then the supply UVLO fault recovery is in auto restart mode. In auto restart mode, when the supply drops below its UVLO threshold, the device is internally forced into software shutdown (EN state is preserved and remains high) and generates the appropriate UVLO fault shutdown interrupt (VBAT_UVLO_SHDN_* or PVDD_UVLO_SHDN_* respectively). Once the supply recovers (voltage levels exceed the UVLO thresholds), the device is no longer held in software shutdown and (if all other conditions are met) automatically restarts back into the active state. These recovery modes do not apply when the AVDD or DVDD supplies cause a UVLO fault while the device is in the active state. If DVDD drops below its PoK threshold, the device is reset and placed into hardware shutdown.

Active State

The device always enters the active state through a transition from the software shutdown state. In the active state, all enabled device blocks are active, and speaker amplifier playback is possible. In the active state, only dynamic register settings (or those restricted to disabled blocks) can be programmed safely.

The only non-fault state transitions to or from the active state are those initiated through the global enable bit (EN). All other transitions to or from the active state are the result of fault events and can result in audible glitches if they occur during active playback.

Device Sequencing

Table 1 and *Table 2* show the recommended typical device power-up and power-down sequences.

Table 1. Typical Power-Up Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Power-Up Core Supplies	Power the PVDD, VBAT, DVDD, and AVDD supplies above their UVLO thresholds.
2	Exit Hardware Shutdown State	Assert the hardware reset input ($\overline{RESET}$) to a logic high level. If ($\overline{RESET}$) is tied to the DVDD supply, this step is combined with step 1.
3	Enter Software Shutdown State	The device finishes the transition and enters the software shutdown state after the release from reset time ($t_{I^2C\_READY}$) elapses.
4	Program the Device Registers/Enable the External Clocks	The I^2C interface is active, and all registers can be freely configured. Start both external clocks before exiting the software shutdown state.
5	Exit Software Shutdown State	If volume ramping is disabled, the input audio data should be silent. Set the global enable to a logic high (EN = 1).
6	Enter the Active State	The device enters the active state after the turn-on time (t_{ON}) elapses.
7	Active State/Audio Playback	Dynamic bits (and those restricted to disabled blocks) can be programmed. The device is capable of audio playback in the active state.

Table 2. Typical Power-Down Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Exit the Active State	If volume ramping is disabled, the input audio data should be silent. Set the global enable bit to a logic low (EN = 0)
2	Enter Software Shutdown State	The device enters a software shutdown state after the turn-off time (t_{OFF}) elapses.
3	Reprogram Device Registers/Disable the External Clocks	The device is fully programmable and can idle in the software shutdown state. The external clocks and the AVDD, PVDD, and VBAT supplies can be disabled. To return to the active state, resume the power-up sequence from step 4.
4	Enter Hardware Shutdown State	For full hardware shutdown, disable the external clocks first. Assert the reset input ($\overline{RESET}$) to ground or power down the DVDD.

General Purpose Input Output (GPIO) Pins

The MAX98415A/MAX98425A features three general purpose input/output pins, which can be assigned to function as either an Interrupt pin, PCM data path output pin (DOUT), Interchip Communication pin (ICC), or an Envelope Tracking Control output pin. GPIOX_SEL bitfield controls the assignment of the GPIOX pin to one of the four functions.

As an Interrupt, or DOUT, or Envelope Tracking Control function, each GPIO pin operates as an output pin whereas as an ICC function, the GPIO pin functions as an input/output pin. As an Interrupt, the GPIO pin can be configured to operate as an open-drain output or as a push-pull CMOS output. See the *Interrupts* section for more details. For all remaining function assignments, the GPIO output operates as a push-pull CMOS output. As a push-pull output pin, the GPIO pin can be configured for different drive strengths using the GPIOX_DRV bitfield.

PCM Interface

The flexible PCM peripheral interface supports common audio playback sample rates from 16kHz to 192kHz and I/V Feedback sample rates from 8kHz to 96kHz. The PCM interface also supports standard I^2S, left-justified, and TDM data formats. The PCM interface is disabled and powered down when both the PCM data input (DIN) and PCM data output (DOUT) are disabled.

PCM Clock Configuration

The PCM peripheral interface requires the host to supply both BCLK and LRCLK. To configure the PCM interface clock inputs, the host must program both the device interface sample rate (PCM_SR) and BCLK to LRCLK (PCM_BSEL) ratio. The PCM interface sample rate must be configured to match the frequency of the frame clock (LRCLK) using the PCM_SR registers. The speaker path sample rate is also set by the PCM_SR setting. The device supports a range of BCLK to LRCLK clock ratios (PCM_BSEL) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK) frequency, the configured clock ratio cannot result in a BCLK frequency that exceeds 24.576MHz.

The PCM peripheral interface requires the host to supply both BCLK and LRCLK. To configure the PCM interface clock inputs, the host must program both the device interface sample rate (PCM_SR) and BCLK to LRCLK (PCM_BSEL) ratio. The PCM interface sample rate must be configured to match the frequency of the frame clock (LRCLK) using the PCM_SR registers. The speaker path sample rate is also set by the PCM_SR setting. However, the I_{SENSE} ADC path sample rate (IVFB_SR) can be set to the same rate or lower rate than the speaker path sample rate (PCM_SR) according to the restrictions in *Table 3*. When the I_{SENSE} ADC path is set to a lower rate than the speaker amplifier path, the output data contains repeated samples.

Table 3. Sample Rate Selection for I/V Feedback

N/A = Not Available N/S = Not Supported		I_{SENSE} ADC / $V_{FEEDBACK}$ SAMPLE RATE (kHz)												
		192	176.4	96	88.2	48	44.1	32	24	22.05	16	12	11.025	8
PCM Interface and Speaker Path Sample Rate (kHz)	192	N/S	N/S	2	N/S	4	N/S	6	8	N/S	12	16	N/S	24
	176.4	N/S	N/S	N/S	2	N/S	4	N/S	N/S	8	N/S	N/S	16	N/S
	96	N/A	N/A	1	N/S	2	N/S	3	4	N/S	6	8	N/S	12
	88.2	N/A	N/A	N/A	1	N/S	2	N/S	N/S	4	N/S	N/S	8	N/S
	48	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	3	4	N/S	6
	44.1	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4	N/S
	32	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4
	24	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	3
	22.05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S
	16	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2
	12	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S
	11.025	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S
	8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

The device supports a range of BCLK to LRCLK clock ratios (PCM_BSEL) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK frequency), the configured clock ratio cannot result in a BLCK frequency that exceeds 24.576MHz.

PCM Data Format Configuration

The device supports the standard I^2S, left-justified, and TDM data formats. The operating mode is configured using the PCM_FORMAT bit field.

I^2S/Left-Justified Mode

I^2S and left-justified formats support two channels that can be 16-, 24-, or 32-bits in length. The BCLK to LRCLK ratio (PCM_BSEL) must be configured to be twice the desired channel length. The audio data word size is configurable to 16-, 24-, or 32-bits in length (PCM_CHANSZ), but must be programmed to be less than or equal to the channel length. If the resulting channel length exceeds the configured data word size, then the data input LSBs are truncated, and the data output LSBs are padded with either zero or Hi-Z data based on the PCM_TX_EXTRA_HIZ register bit setting.

Table 4. Supported I^2S/Left-Justified Mode Configurations

CHANNELS	CHANNEL LENGTH	BCLK TO LRCLK RATIO (PCM_BSCL)	SUPPORTED DATA WORD SIZES (PCM_CHANSZ)
2	16	32	16
	24	48	16, 24
	32	64	16, 24, 32

With the default PCM settings, falling LRCLK indicates the left channel data (Channel 0) and the start of a new frame, while rising LRCLK indicates the right channel data (Channel 1). In I^2S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

The PCM_BCLKEDGE register bit selects either the rising or falling edge of BCLK as the active edge that is used for data capture (DIN) and data output (DOUT). The PCM_CHANSEL bit configures which LRCLK edge indicates the start of a new frame (Channel 0), and LRCLK transitions always align with the inactive BCLK edge. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as the data input.

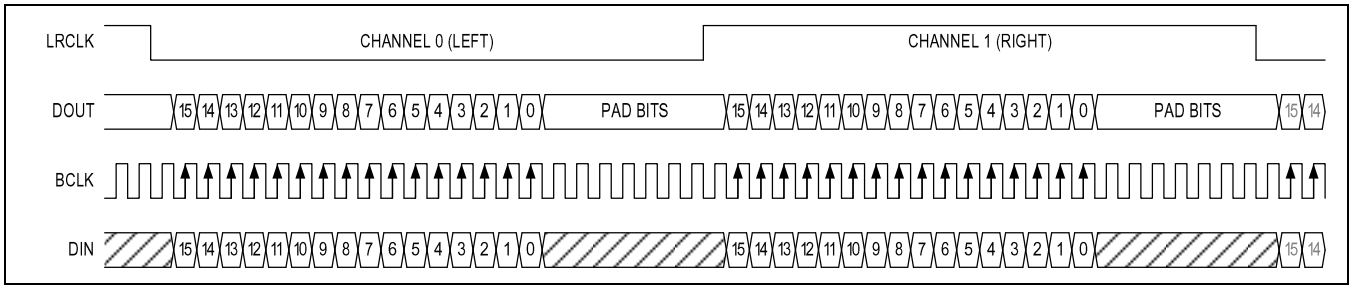


Figure 3. Standard I^2S Mode

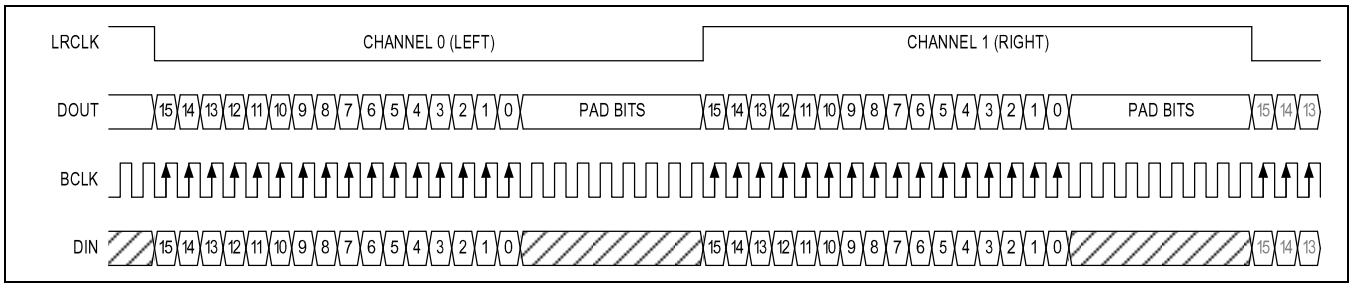


Figure 4. Left-Justified Mode

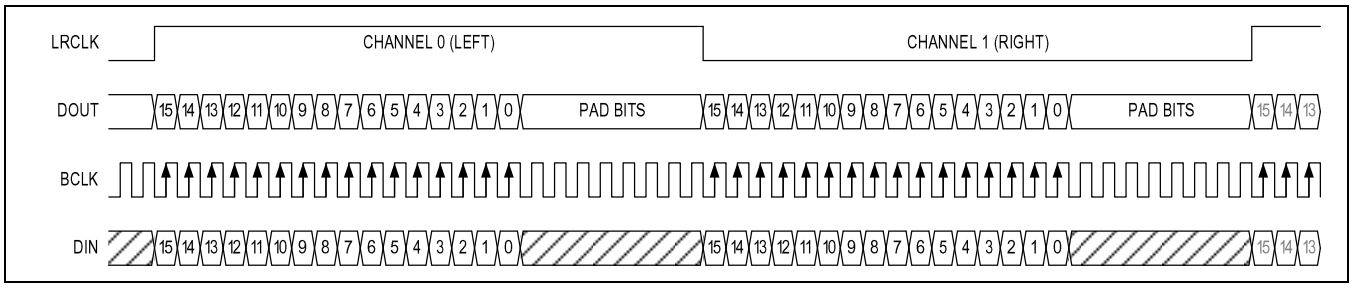


Figure 5. Left-Justified Mode (LRCLK Inverted)

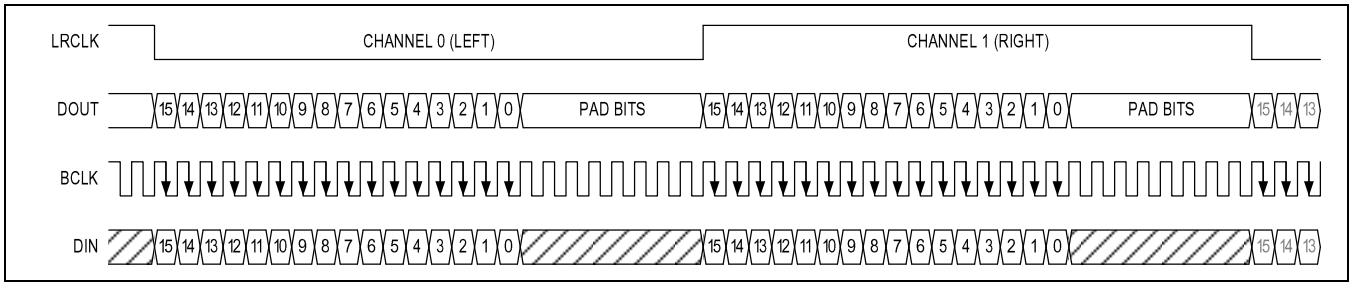


Figure 6. Left-Justified Mode (BCLK Inverted)

TDM Modes

The provided TDM modes support timing for up to 16 digital audio input channels (DIN), each containing 16-, 24-, or 32-bits of data. The digital audio output (DOUT) is structured into 8-bit slots, and the timing can support up to a maximum of 128 data output slots. The number of TDM input channels and output slots is determined by both the selected BCLK to LRCLK ratio (PCM_BSEL) and the selected data word and channel length (PCM_CHANSZ).

For a given valid configuration, the number of available data input channels per frame is calculated as follows:

Number of Available Data Input Channels = BCLK to LRCLK Ratio/Channel Length

For a given valid configuration, the number of available 8-bit data output slots per frame is calculated as follows:

Number of available Data Output Slots = BCLK to LRCLK Ratio/8

Table 5 shows the supported TDM mode configurations for each combination of input data channels and output data slots. In some configurations, the maximum PCM interface and speaker amplifier playback sample rate is limited to less than 96kHz to avoid violating the BCLK frequency limit of 24.576MHz.

Table 5. Supported TDM Mode Configurations

INPUT DATA CHANNELS	OUTPUT DATA SLOTS	DATA WORD SIZES (PCM_DATA_WIDTH)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM SPEAKER PLAYBACK SAMPLE RATE (FLRCLK)
2	4	16	32	192kHz
	6	24	48	
	8	32	64	
3	15	32	125	
4	8	16	64	
	12	24	96	
	16	32	128	
5	15	24	125	
7	15	16	125	
2	4	16	32	96kHz
	6	24	48	
	8	32	64	
3	15	32	125	
4	8	16	64	
	12	24	96	
	16	32	128	
5	15	24	125	
7	15	16	125	
	31	32	250	
8	16	16	128	
	24	24	192	
	32	32	256	
10	31	24	250	
15	31	16	250	
16	32	16	256	
7	31	32	250	48kHz
10	31	24	250	
10	40	32	320	
15	31	16	250	
16	48	24	384	
	64	32	512	

With the default PCM interface settings in TDM mode, a rising frame clock (LRCLK) edge acts as the frame sync pulse and indicates the start of a new frame. The frame sync pulse width must be equal to at least one bit clock period. However, the falling edge can occur at any time as long as it does not violate the setup time of the next frame sync pulse rising edge. The PCM_CHANSEL bit can be used to invert the LRCLK edges (sync pulse) used to start a TDM frame.

In TDM mode, the MSB of the first audio word can be latched on the first (TDM Mode 0), second (TDM Mode 1), or third (TDM Mode 2) active BCLK edge after the sync pulse and is programmed by the PCM_FORMAT bits. Additionally, the PCM_BCLKEDGE register bit allows the BCLK edge (that is used for data capture and data output) to be programmed. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as the data input.

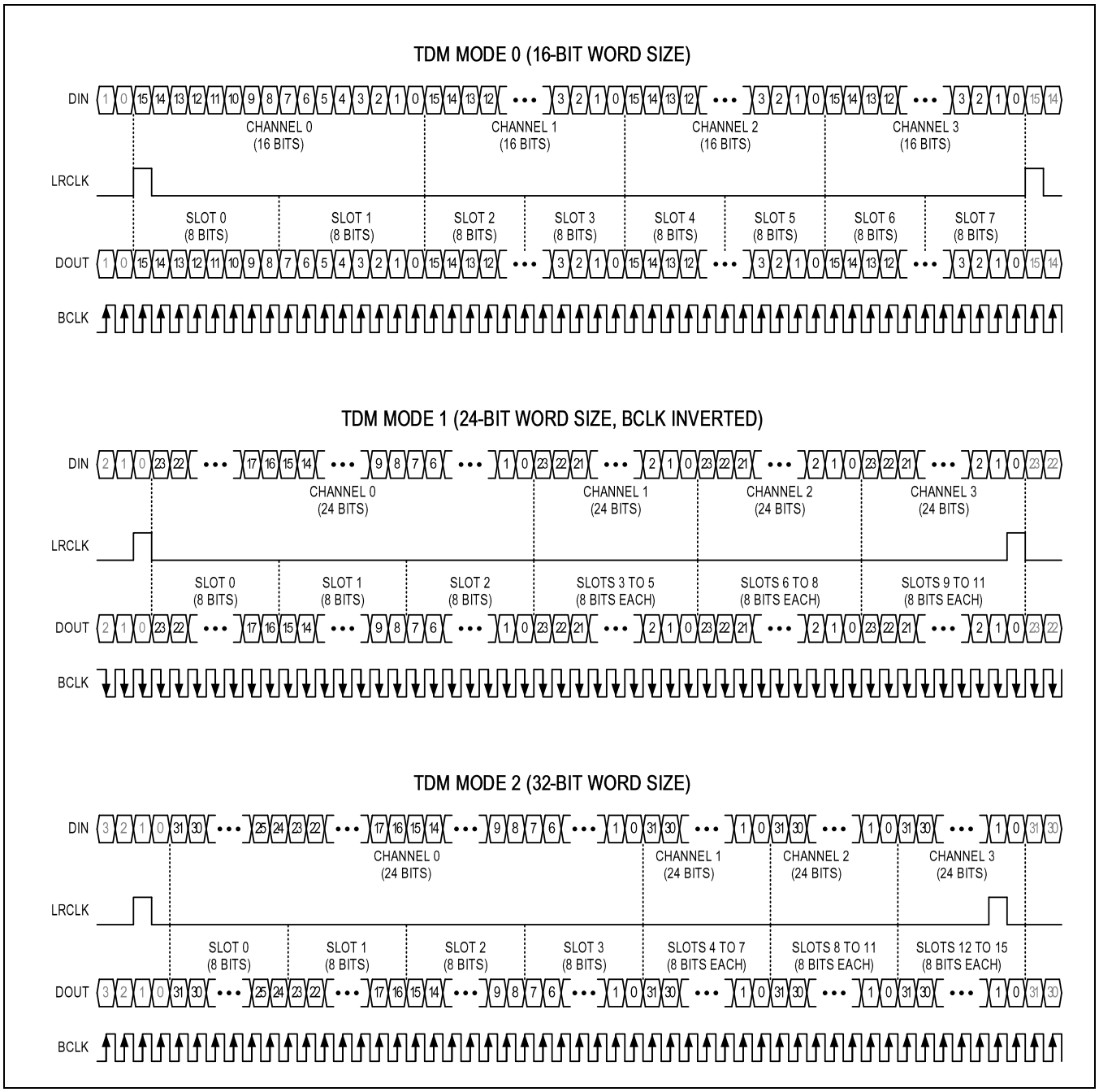


Figure 7. TDM Modes

PCM Data Path Configuration

The PCM interface data input (DIN) receives the source data for the speaker amplifier path, and the data output (DOUT) transmits the data from the I_{SENSE} ADC/$V_{FEEDBACK}$ path in the case of MAX98415A only. In addition, the PCM data output on MAX98415A/MAX98425A can transmit internal diagnostic data such as the speaker DSP monitor path, supply and temperature measurement ADC results, device status reporting, and the DHT attenuation level.

PCM Data Input

The PCM_RX_EN bit enables the data input from the PCM interface to the main PCM playback path. With PCM_RX_EN = 1, the internal playback path accepts data from any valid input data channel on the PCM interface data input (DIN) to the device's internal PCM playback path. The device provides an input digital mono mixer that can route a single channel or mix two PCM input channels to create a mono input to the speaker playback path. The PCM_DMMIX_CFG bit is used to configure the mixer, while the PCM_DMMIX_CH0_SOURCE and PCM_DMMIX_CH1_SOURCE bits select which of the 16 PCM input channels are used as the input to the mono mixer. It is only allowed to set PCM_DMMIX_CFG = 0x0 when PCM_DMMIX_CH0_SOURCE and PCM_DMMIX_CH1_SOURCE bitfields are selected as the same input channel (e.g., value = 0x0 (PCM Input Channel 0)).

In I^2S and left-justified modes, only two input data channels are available, while in TDM mode, up to 16 channels of input data may be available. If the PCM data input is disabled (PCM_RX_EN = 0), a zero-code value is driven into the speaker amplifier path.

PCM Data Output

The PCM interface data output (DOUT) is enabled by the PCM_TX_EN bit field and can transmit any output data type onto any valid output channel or slot. In I^2S and left-justified mode, only two data output channels are available in each output transmit frame (Channel 0 and 1). In TDM mode, each output transmit frame can contain up to 64 sequential 8-bit data output slots, each of which is numbered from 0 up to a maximum of 63.

The PCM data output can transmit several different output data types. In I^2S and left-justified modes, only the speaker amplifier output voltage sense, output current sense, and DSP monitor output data types are available for data output transmission. If the word size of the data output type is longer than the output channel data word (PCM_CHANSZ), the lowest trailing bits are truncated.

In TDM mode, all output data types are available and are individually assigned to data output slots. The output data types vary in word size from 3 bits to 32 bits, and as a result, require from 1 to 4 data output slots to transmit in TDM mode. *Table 6* shows the supported output data types and the parameters of each data type.

Table 6. Supported PCM Data Output Types

OUTPUT DATA TYPE	SYMBOL	DATA WORD SIZE (BITS)	NUMBER OF TDM SLOTS	ENABLE/SLOT ASSIGNMENT
Speaker Amplifier A Output Voltage Feedback	V_{FB}	16	2	PCM_VFB_AMPA_EN/ PCM_AMPA_VFB_SLOT
Speaker Amplifier B Output Voltage Feedback	V_{FB}	16	2	PCM_VFB_AMPA_EN/ PCM_AMPB_VFB_SLOT
Speaker Amplifier A Output Current Sense	IMON	16	2	PCM_IMON_AMPA_EN/ PCM_AMPA_IMON_SLOT
Speaker Amplifier B Output Current Sense	IMON	16	2	PCM_IMON_AMPB_EN/ PCM_AMPB_IMON_SLOT
Speaker Amplifier A DSP Monitor	DSPMON	32	4	PCM_DSPMONITOR_EN/ PCM_AMPA_DSP_MONITOR_SLOT/ PCM_AMPB_DSP_MONITOR_SLOT
Applied DHT Attenuation	DHT_ATN	16	2	PCM_DHT_ATN_EN/ PCM_DHT_ATN_SLOT
PVDD Voltage (VPVDD)	PVDD	16	2	PCM_PVDD_EN/ PCM_PVDD_SLOT
Temperature	TEMP	9	2	PCM_THERM_EN/PCM_THERM_SLOT

OUTPUT DATA TYPE	SYMBOL	DATA WORD SIZE (BITS)	NUMBER OF TDM SLOTS	ENABLE/SLOT ASSIGNMENT
BPE Level	BPELVL	3	1	PCM_BPE_EN/ PCM_BPE_SLOT
Device Status Flags	FLAG	14	2	PCM_STATUS_EN/ PCM_STATUS_SLOT
ICC data	ICCDATA	23	4	ICC_OVER_DOUT_EN/ PCM_ICC_SLOT

An individual enable bit and slot assignment bit field is provided for each output data type. In I^2S and left-justified modes, use output slot 0 to assign data to Channel 0 and output slot 1 to assign data to Channel 1. In TDM mode, the slot assignment selects the slot where the output data type transmit begins for data output types requiring more than one slot to transmit (e.g., a two-slot data type assigned to slot 6 would occupy slots 6 and 7).

In TDM mode, each data type can be assigned to any valid data output slot (or series of slots) with some restrictions. First, it is invalid for data types to be assigned such that the data word extends beyond the end of the data output frame. For example, data types that require two slots to transmit cannot be assigned to the last slot of the frame. Next, it is also invalid to assign a data output type to any slot that overlaps with the slot assignment of another data type (this also applies to channels in I^2S and left-justified modes). Finally, it is invalid to assign a data type to any slots that do not exist in the frame structure of the current PCM interface configuration.

Any data output (DOUT) slots that exist in the current frame structure but have no output data type assigned to them are either Hi-Z or driven with a 0 code (as set by the PCM_TX_SLOT_HIZ bit field). Likewise, if a data output type is disabled, then the assigned data output slot(s) are also either Hi-Z or driven with a 0 code (as set by the PCM_TX_SLOT_HIZ bit field).

Data Output Channel-Interleaved I/V Feedback Data

In I^2S and left-justified use cases, the PCM interface limits the number of available data output channels to two, making it impossible to fit amplifier output current and voltage sense data from stereo devices on a single shared data output (DOUT) line. For these cases, the data output can be configured to allow the current and voltage sense data types from a single device to share a single data output channel. To enable channel-interleaved mode, set the PCM_TX_INTERLEAVE bit high. Then, assign the current and voltage sense data types to the same valid data channel (using PCM_AMPA_VFB_SLOT/PCM_AMPB_VFB_SLOT and PCM_AMPA_IMON_SLOT/PCM_AMPB_IMON_SLOT).

In this configuration, the current and voltage sense data types are frame interleaved on the assigned data output channel. The current and voltage sense data words are both 16-bits in length, and as a result, if the channel length is longer than 16-bits, the trailing padding bits are set to either Hi-Z or zero code depending on the state of the PCM_TX_EXTRA_HIZ bit field.

To identify the data type in channel-interleaved mode, the LSB of the 16-bit data word is dropped (truncated). The data word is then right-shifted by a single bit, and the now vacant MSB is replaced with either a 0 to indicate voltage sense data or a 1 to indicate current sense data. For phase alignment, the voltage sense data for a single sampling instant is always transmitted in the assigned channel on the first frame, followed by the current sense data on the second frame. The MSB value and the transmission order allow the host to identify and phase-align the output data across frames.

Since the I/V feedback data is frame interleaved, the sample rate for the PCM interface must be greater than that of the I/V feedback by an integer ratio of 2. *Figure 8* shows a basic case where the sample rate of the PCM interface is twice that of the I/V feedback path.

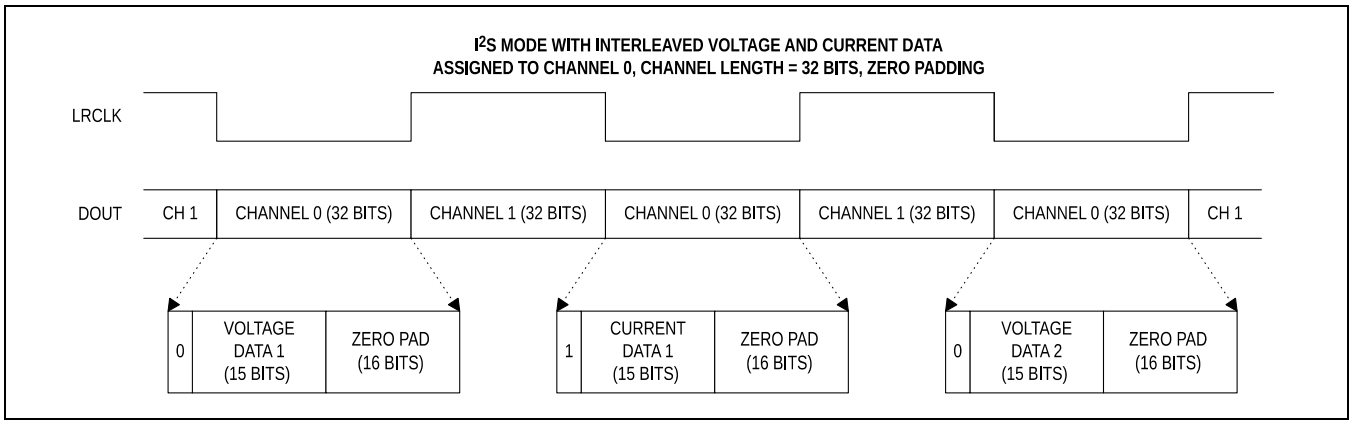


Figure 8. I/V Feedback Path Data Interleaved on a Single Data Output Channel

Data Output Shared Channel - I/V Feedback Data

In I²S and left justified use cases, the PCM interface limits the number of available data output channels to 2, making it impossible to fit amplifier output current and voltage sense data from stereo devices on a single shared data output (DOUT) line. For these cases, the data output can be configured to allow the current and voltage sense data types from a single device to share a single data output channel. To enable channel-shared mode, assign the current and voltage sense data types to the same valid data channel (using PCM_AMPX_VFB_SLOT = PCM_AMPX_IMON_SLOT). The voltage sense data is always transmitted first, followed by the current sense data in the same assigned channel.

In this configuration, the BCLK/LRCLK ratio has to be configured for 64 or higher as the current and voltage sense data words are both 16-bits in length. If the BCLK/LRCLK ratio is less than 64 the current and voltage sense data will not be decoded properly.

Data Output Status Bits

The following interrupt information is reported in the status slots:

- Bit 15: 0
- Bit 14: 0
- Bit 13: BPE level 0 begin
- Bit 12: BPE level change
- Bit 11: BPE active begins
- Bit 10: BPE active end
- Bit 9: Thermal warning 1 begins
- Bit 8: Thermal warning 1 end
- Bit 7: Thermal warning 2 begin
- Bit 6: Thermal warning 2 end
- Bit 5: Thermal foldback begins
- Bit 4: Thermal foldback end
- Bit 3: DHT active end
- Bit 2: DHT active begins
- Bit 1: Speaker overcurrent
- Bit 0: Power-up done

Each of the interrupt information above corresponds to a raw interrupt and is 1 bit wide. Thermal warning, Thermal foldback, and Speaker overcurrent status flags refer to logical OR of raw interrupts corresponding to each amplifier. The Speaker overcurrent status flag is triggered only in Stereo Mode (AMPA_SPK_EN = 1, AMPB_SPK_EN = 1, and EN = 1). The Power-Up done status flag gets triggered in Stereo Mode (AMPA_SPK_EN = 1, AMPB_SPK_EN = 1, and EN = 1) and in amplifier A enabled only modes (AMPA_SPK_EN = 1, AMPB_SPK_EN = 0, and EN = 1).

When a raw interrupt has a rising edge, the corresponding status bit goes high during the next LRCLK frame. The status bit goes low during the next LRCLK frame even if the raw interrupt has remained high.

PCM Interface Timing

Figure 9 and *Figure 10* shows timing for BCLK, LRCLK, DIN, and DOUT. See the *Electrical Characteristics* table for more details.

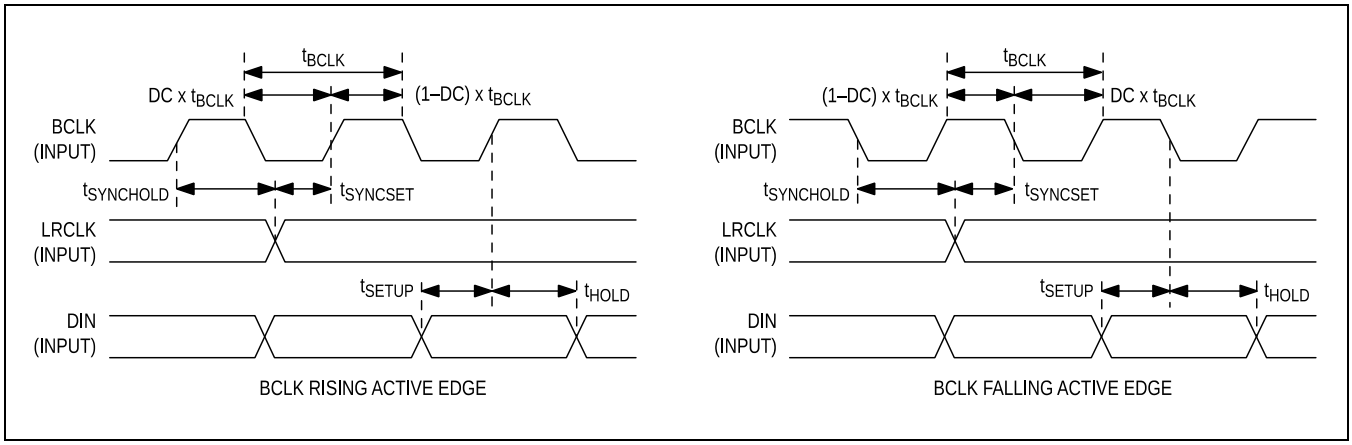


Figure 9. PCM Interface Timing/Peripheral Mode—LRCLK, BCLK, DIN Timing Diagram

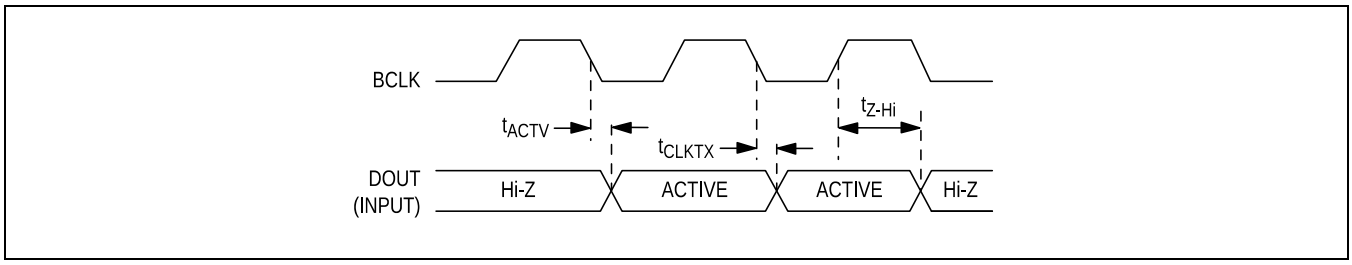


Figure 10. PCM Interface Timing/DOUT Timing Diagram

Interrupts

The device supports individually enabled status interrupts for sending feedback to the host about events that have occurred on-chip. When enabled, interrupts are transmitted on the IRQ output.

Interrupt Bit Field Composition

Each interrupt source has five individual bit field components. The function of each component is detailed as follows, and the corresponding bit fields for each source can be identified by the appended suffix (shown in parentheses).

- Raw Status (RAW): Each interrupt source has a read-only bit to indicate the real-time raw status of the interrupt source.
- State (STATE): Each interrupt source has a read-only state bit that is set whenever a rising edge occurs on the associated raw status bit. The state bit is set regardless of the setting of the source enable bit.
- Flag (FLAG): Each interrupt source has a read-only flag bit. If the source enable bit is set, then the flag bit is set and an interrupt can be generated whenever the source state bit is set.
- Enable (EN): Each interrupt source has a dynamic read/write enable bit. When the enable bit is set, the associated flag bit is set, and an interrupt can be generated whenever the source state bit is set.
- Clear (CLR): Each interrupt source has a dynamic write-only clear bit. Writing a 1 to a clear bit resets the associated state and flag bits to 0. Writing a 0 to a clear bit has no effect. In I^2C control mode, the IRQ output is deasserted if all flag bits are 0.

Interrupt Output Configuration

The device allows the user to configure the drive mode, and polarity of the IRQ output. Any of the three GPIO pins can be configured for IRQ output. The IRQ_MODE bit controls the drive mode. If IRQ_MODE is 0, the pin is configured as an open-drained output and requires an external pullup resistor. If IRQ_MODE is 1, then IRQ is configured as a push-pull CMOS output.

Additionally, when IRQ is configured as a push-pull CMOS output, the drive strength control (GPIOX_DRV) bits set the drive strength of the IRQ output. Four different CMOS drive strengths are available. The IRQ_POL bit controls the polarity of the IRQ bus. Interrupt events (a flag bit is set high) assert the IRQ bus low if IRQ_POL = 0 and high if IRQ_POL = 1. The IRQ bus deasserts if all flag bits are cleared (set low).

Interrupt Sources

Table 7. Interrupt Sources

INTERRUPT SOURCES	BIT FIELD	DESCRIPTION
Thermal Shutdown Begin Event	AMPA_THERMSHDN_BGN_* AMPB_THERMSHDN_BGN_*	Indicates when the thermal-shutdown threshold temperature has been exceeded. A separate interrupt for each of the amplifiers indicates which amplifier exceeds the thermal-shutdown threshold temperature.
Thermal Shutdown End Event	AMPA_THERMSHDN_END_* AMPB_THERMSHDN_END_*	Indicates that the die temperature was previously above the thermal-shutdown threshold and has now dropped below the threshold. A separate interrupt for each of the amplifiers indicates which amplifier dropped below the thermal-shutdown temperature threshold.
Thermal Warning 1 Begin Event	AMPA_THERMWARN1_BGN_* AMPB_THERMWARN1_BGN_*	Indicates when the thermal-warning1 threshold temperature has been exceeded. A separate interrupt for each of the amplifiers indicates which amplifier exceeds the thermal-warning1 threshold temperature. It is recommended that both AMPA_THERMWARN1_BGN_EN and AMPB_THERMWARN1_BGN_EN are enabled to toggle the corresponding *_FLAG bits and generate an interrupt on the IRQ pin.
Thermal Warning 1 End Event	AMPA_THERMWARN1_END_* AMPB_THERMWARN1_END_*	Indicates that the die temperature was previously above the thermal-warning1 threshold and has now dropped below the threshold. A separate interrupt for each of the amplifiers indicates which amplifier dropped below the thermal-warning1 threshold temperature. It is recommended that both AMPA_THERMWARN1_END_EN and AMPB_THERMWARN1_END_EN are enabled to toggle the corresponding *_FLAG bits and generate an interrupt on the IRQ pin.
Thermal Warning 2 Begin Event	AMPA_THERMWARN2_BGN_* AMPB_THERMWARN2_BGN_*	Indicates when the thermal-warning2 threshold temperature has been exceeded. A separate interrupt for each of the amplifiers indicates which amplifier exceeds the thermal-warning2 threshold temperature. It is recommended that both AMPA_THERMWARN2_BGN_EN and AMPB_THERMWARN2_BGN_EN are enabled to toggle the corresponding *_FLAG bits and generate an interrupt on the IRQ pin.
Thermal Warning 2 End Event	AMPA_THERMWARN2_END_* AMPB_THERMWARN2_END_*	Indicates that the die temperature was previously above the thermal-warning2 threshold and has now dropped below the threshold. A separate interrupt for each of the amplifiers indicates which amplifier dropped below the thermal-warning2 threshold temperature. It is recommended that both AMPA_THERMWARN2_END_EN and AMPB_THERMWARN2_END_EN are enabled to toggle the corresponding *_FLAG bits and generate an interrupt on the IRQ pin.
Thermal Foldback Begin Event	AMPA_THERMFB_BGN_* AMPB_THERMFB_BGN_*	Indicates that the die temperature is above the thermal-warning1 threshold and the device is attenuating the output. A separate interrupt for each of the amplifiers indicates which amplifier

INTERRUPT SOURCES	BIT FIELD	DESCRIPTION
		exceeds the thermal-warning1 threshold and is currently attenuating the output.
Thermal Foldback End Event	AMPA_THERMFB_END_* AMPB_THERMFB_END_*	Indicates that the die temperature is below the thermal-warning1 threshold and the device has stopped attenuating the output. A separate interrupt for each of the amplifiers indicates which amplifier dropped below the thermal-warning1 threshold and is releasing the output.
BPE Level Change Event	BPE_LEVEL_*	Indicates that the BPE has transitioned between thresholds.
BPE Active Begin Event	BPE_ACTIVE_BGN_*	Indicates that the BPE is active.
BPE Active End Event	BPE_ACTIVE_END_*	Indicates that the BPE is no longer active.
BPE Level 0 Begin Event	BPE_L0_*	Indicates that the BPE has transitioned into L0.
OTP Load Fail Event	OTP_FAIL_*	Indicates when the OTP load routine that runs when exiting hardware shutdown has failed to complete successfully. If the OTP load routine fails, the device is held in software shutdown.
Speaker Over Current Event	AMPA_SPK_OVC_* AMPB_SPK_OVC_*	Indicates that the speaker amplifier current limit has been exceeded.
Internal CLK Error	INT_CLK_ERR_*	Indicates a clock stop error in the internal clocks of the device.
External CLK (BCLK/LRCLK) Error	CLK_ERR_*	Indicates a frequency or framing error in the input BCLK or LRCLK.
External CLK (BCLK/LRCLK) Recover	CLK_RECOVER_*	Indicates that the input BCLK or LRCLK has recovered after an error event.
Speaker Amplifier Monitor Error	AMPA_INT_SPKMON_ERR_* AMPB_INT_SPKMON_ERR_*	Indicates an amplifier output stuck high or low error. A separate interrupt for each amplifier indicates which amplifier output is showing the output error.
Power-Up Done Event	AMPA_PWRUP_DONE_* AMPB_PWRUP_DONE_*	Indicates when the device has entered the active state and the device is ready to play audio. A separate interrupt for each amplifier indicates which amplifier output is ready to play audio.
Power-Down Done Event	PWRDN_DONE_*	Indicates when the device has entered the software shutdown state.
PVDD UVLO Shutdown Event	PVDD_UVLO_SHDN_*	Indicates that PVDD is below the minimum allowed voltage when the device is in an active state.
VBAT UVLO Shutdown Event	VBAT_UVLO_SHDN_*	Indicates that VBAT is below the minimum allowed voltage when the device is in an active state.
AVDD UVLO Event	AVDD_UVLO_*	Indicates that AVDD is below the minimum allowed voltage when the device is in an active state.
DVDD UVLO Event	DVDD_UVLO_*	Indicates that DVDD is below the minimum allowed voltage when the device is in an active state.
DHT Active Begin Event	DHT_ACTIVE_BGN_*	Indicates that the DHT circuit is active and is applying attenuation to the signal.
DHT Active End Event	DHT_ACTIVE_END_*	Indicates that the DHT circuit has stopped applying attenuation to the signal.
RMS Limiter Active Begin Event	AMPA_RMS_LIM_ACTIVE_BGN_* AMPB_RMS_LIM_ACTIVE_BGN_*	Indicates that the RMS Limiter is active on the amplifier output. A separate interrupt is available for each amplifier.
RMS Limiter Active End Event	AMPA_RMS_LIM_ACTIVE_END_* AMPB_RMS_LIM_ACTIVE_END_*	Indicates that the input has dropped below the RMS Limiter threshold and RMS Limiter activity has ended. A separate interrupt is available for each amplifier.
Speaker Output Clip Indicator	AMPA_SPK_CLIP_* AMPB_SPK_CLIP_*	Indicates that the amplifier output is clipped. A separate interrupt is available for each amplifier output.
Mute Pin Assertion Indicator	EXT_MUTE_*	Indicates that MUTE is asserted.

NOTE: *The bit fields are shown without the component suffixes. For example, OTP_FAIL_*. refers to OTP_FAIL_RAW, OTP_FAIL_STATE, OTP_FAIL_FLAG, OTP_FAIL_EN, and OTP_FAIL_CLR. All interrupt sources have these five component bit fields.*

Speaker Path

Speaker Audio Processing Bypass Path

In applications where the audio processing in the main speaker path is not desired, the device provides a bypass path. The bypass path is selected with the PCM_BYPASS_EN bit field. The PCM data input channel for the speaker audio processing bypass path is selected with the PCM_BYPASS_SOURCE bit field.

The data from the speaker audio processing bypass path is mixed with the data from the main PCM playback path to the speaker outputs. If PCM_RX_EN = 0 and BYP_AMP_SEL = 1, the data in the main PCM playback path is zero, and the data from the PCM bypass path is routed through the speaker amplifier path. If PCM_RX_EN = 1 and BYP_AMP_SEL = 1, the data from the main PCM playback path is mixed with the PCM bypass path and is routed through the speaker amplifier path.

Bypass Path Data Inversion

The input data to the audio processing bypass path can optionally be inverted by setting the BYP_INVERT bit to 1.

Speaker Playback Path

The source input data to the speaker amplifier path is routed from either the PCM interface or the tone generator. The data is then routed through digital filters, signal processing, and volume/gain control blocks before reaching the Class-D speaker amplifier.

Speaker Path Noise Gate

The speaker path noise gate function is enabled when the device is in the active state, and the noise gate enable (NOISEGATE_EN) is set to 1. The noise gate enable can be programmed dynamically. However, if the noise gate function is disabled (NOISEGATE_EN is set to 0) while the noise gate is active (speaker path actively muted), the noise gate function remains active until after it deactivates normally (unmutes the speaker path).

When the noise gate is enabled, the noise gate activates whenever the amplitude of the input audio data to the speaker path (from the PCM interface) is below the configured mute threshold (MUTE_THRESH) for more than 1024 consecutive data samples. When the noise gate is active, the amplifier path is muted, the current sense ADC and voltage feedback paths output zero code data, and the device idles in a reduced power state.

The noise gate deactivates immediately if the amplitude of a single sample from the input audio data exceeds the configured unmute threshold (UNMUTE_THRESH). When the noise gate deactivates, the speaker path is unmuted, and returns to normal operation before the input audio data (that triggered deactivation) reaches the speaker output. Once noise gate deactivation is complete, the current sense ADC and voltage feedback paths resume operation and output data normally.

The noise gate mute and unmute threshold settings are selected in terms of the number of bits (starting from the LSB) that must be toggling (or active) for the input signal amplitude to exceed the thresholds. It is invalid to set the noise gate unmute threshold (UNMUTE_THRESH) such that it is less than the configured mute threshold (MUTE_THRESH). The location of the audio data LSB within the PCM input data channel is determined by the configured PCM data word size (PCM_CHANSZ). The supported combinations are shown in *Table 8*.

Table 8. Noise Gate/Idle Mode Threshold LSB Location by Input Data Configuration

INPUT DATA WORD SIZE (PCM_CHANSZ)	NOISE GATE FUNCTION LSB LOCATION
16	16
24	24
32	

It is not valid to enable the speaker path noise gate function when the tone generator is enabled or when the speaker idle mode is enabled.

Speaker Path Dither

The input data to the speaker path can optionally have dither (±1LSB peak-to-peak) applied if SPK_DITH_EN is set to 1. No dither is applied when SPK_DITH_EN is set to 0.

Speaker Path Data Inversion

The input data to each speaker amplifier path can optionally be inverted by setting the corresponding AMPX_SPK_INVERT bit to 1. The input data to the speaker path can only be inverted when the speaker DC blocking filter is also enabled by setting AMPX_SPK_DCBLK_EN to 1.

Speaker Path DC Blocking Filter

A DC blocking filter can be enabled on the speaker path of each amplifier by setting the corresponding AMPX_SPK_DCBLK_EN bit to 1. The device offers four DC Blocker corner frequency selection settings for each amplifier (AMPX_SPK_IVF_DCBLK_CFG), which sets the DC blocking filter for playback and IVFeedback paths.

Speaker Path Digital Volume Control

The device has a dynamically programmable speaker path digital volume control with independent controls for each amplifier path. The digital volume control provides an attenuation range of 0dB to -90dB in 0.5dB steps that is configured with the AMPX_SPK_VOL bit field. A volume change can only be applied to the respective speaker outputs by writing a 1 to the AMPX_VOL_UPDATE bit fields. AMPX_VOL_UPDATE bits are dynamic clear-on-write bits.

A digital mute is also provided, which is enabled when AMPX_SPK_VOL is set to 0xFF. The ramp rate of the speaker path digital volume control is programmable and provided individually for each amplifier (AMPX_SPK_VOL_RMP_RATE). With multiple MAX98415A/MAX98425A on the same I^2C bus, the synchronization of volume change on the devices can be easily achieved by configuring and enabling the I^2C group write address feature, digital volume ramp rate, and applying the volume change by setting the AMPX_VOL_UPDATE bits using the group write address.

Digital volume ramping during speaker path start-up and speaker path shutdown is disabled by default. However, both the volume ramp-up and ramp-down can be individually enabled with the AMPX_SPK_VOL_RMPUP_BYPASS and AMPX_SPK_VOL_RMPDN_BYPASS bit fields, respectively. When volume ramp-up or ramp-down is enabled, the device turn-on and turn-off times are longer.

Speaker Path Digital Gain Control

The device provides a programmable speaker path digital gain control that is independent of each amplifier path. The digital gain control provides a range of 0dB to +6dB, with 0.5dB fine step in the range of 0dB to +4dB, and 1dB steps thereafter. It is configured with the AMPX_SPK_CLIP bit field. Digital gain changes are applied immediately and can produce clicks and pops when changed dynamically. It is recommended to change AMPx_SPK_CLIP only when EN = 0 or AMPX_SPK_EN = 0.

Speaker Path DSP Data Feedback Path

The speaker path DSP data for each amplifier can be routed from just before the DAC input back to the PCM interface and can be assigned to any valid data output channel. The speaker path DSP data feedback path is enabled with the AMPX_SPK_FB_EN bits.

Speaker Safe Mode

The device provides a safe mode bit (AMPX_SPK_SAFE_EN) for each amplifier output which applies a -18dB attenuation to the input signal when set to 1. By default, speaker safe mode is enabled to protect any speaker connected to the device on power-up. While speaker safe mode is enabled, the amplifier analog gain setting (AMPx_SPK_GAIN_MAX), digital volume control (AMPX_SPK_VOL), and speaker digital gain control (AMPX_SPK_CLIP) settings are ignored.

External Mute Pin Control

The device provides a $\overline{\text{MUTE}}$ pin to digitally mute both the amplifier output paths using external pin control. For normal audio playback on any of the channels, it is required that the $\overline{\text{MUTE}}$ pin is pulled to logic high, as specified in the *Electrical Characteristics* table.

When the $\overline{\text{MUTE}}$ pin is asserted, the ramping of the digital volume of the device output can be bypassed using the MUTE_RMPDN_BYPASS bit. When the $\overline{\text{MUTE}}$ pin is deasserted, the ramping up of the digital volume of the device output can be bypassed using the UNMUTE_RMPUP_BYPASS bit.

Speaker Maximum Peak Output Voltage Scaling

The device operates over a large PVDD supply voltage range, and as a result, the full-scale speaker amplifier output amplitude level is configurable to allow it to be scaled. As a baseline, the full-scale output of the speaker path DAC is 3.40dBV (typ). The speaker path no-load maximum peak output voltage level (V_{MPO}) is then programmable relative to this baseline level. The peak output scaling range is from +6dB to +24dB and is set with the AMPX_SPK_GAIN_MAX bit field.

The speaker output signal level (in dBV) for a given digital input signal level (in dBFS) is calculated as follows:

Output Signal Level (dBV) = Input Signal Level (dBFS) + 0.39 (dBV) + SPK_GAIN_MAX (dB)

(0dBFS is referenced to 0dBV)

The peak output voltage scaling is applied to the signal path using a combination of digital gain and analog gain adjustments.

Dynamic-Headroom Tracking (DHT)

The device features dynamic-headroom tracking that can preserve consistent signal distortion and listening levels in the presence of a varying supply level. The DHT block provides both a dynamic range compressor (DRC) and a limiter. The limiter can operate either as a signal distortion limiter (SDL) or a standard signal level limiter (SLL). These three functions can be used independently (modes 1 through 3). The DHT block is enabled with the DHT_EN bit. Before enabling the DHT, the measurement ADC PVDD channel should be configured and enabled as required based on the amplifier mode of operation. The DHT block uses the measured supply levels and the current signal level to calculate the attenuation (if any) that is applied to the signal path. Also, the DHT block should not be disabled by setting the DHT_EN bit to 0 when the DHT is active (i.e., attenuation is being applied).

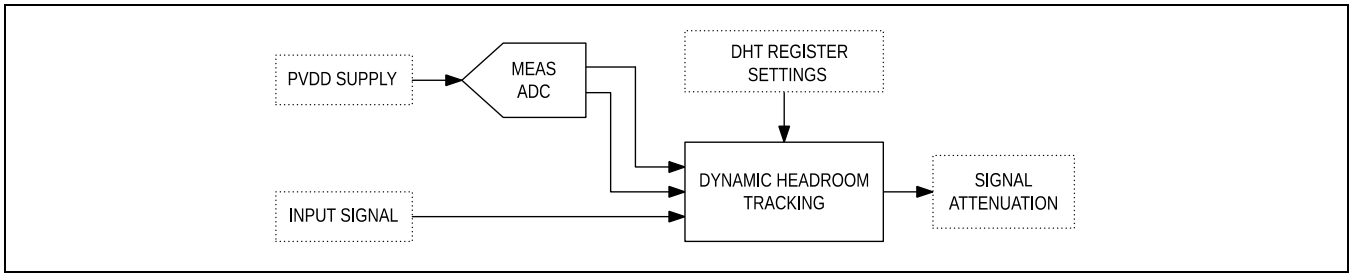


Figure 11. Simplified Dynamic Headroom Tracking System Block Diagram

DHT Supply Tracking and Headroom

The DHT block uses three parameters to track the target peak output level (V_{TPO}) relative to the maximum peak output voltage (V_{MPO}) as the active speaker amplifier supply level varies.

The first is the speaker amplifier full-scale gain setting (SPK_GAIN_MAX bit field). This control selects the maximum (no load) peak output voltage level (V_{MPO}) that is output by the Class-D amplifier with a full-scale input signal (0dBFS). Most DHT thresholds and parameters are calculated relative to the full-scale V_{MPO}.

The second parameter is the measured speaker amplifier supply voltage level (V_{SUP}). The measurement ADC provides the DHT block with the current PVDD supply voltage level.

The third parameter is the speaker amplifier supply headroom (SUP_{HR}). The supply headroom is a positive or negative percentage offset relative to the measured V_{SUP} conversion result. It is configured using the DHT_HR bit field and can be set from +20% to -20% of V_{SUP} in 2.5% step sizes.

The DHT target peak output voltage level (V_{TPO}) is equal to the measured supply voltage (V_{SUP}) scaled to include the selected supply headroom percentage. It is actively calculated with the following equation:

$$V_{TPO} = V_{SUP} \times (100\% - SUP_{HR})$$

The target peak output attenuation (or ratio) from V_{TPO} to V_{MPO} is calculated as follows:

$$A_{TPO} = 20 \times \log (V_{TPO}/V_{MPO})$$

If A_{TPO} exceeds 0dB (V_{SUP} with headroom > V_{MPO}), then the DHT block assumes that there is sufficient supply voltage to reproduce the audio signals as configured without attenuation. In this case, A_{TPO} = 0dB is used for all further calculations. This is important as the DHT functions only ever apply attenuation and do not apply positive gain. Once the calculated V_{TPO} drops below V_{MPO}, the calculated target peak output attenuation (A_{TPO}) is less than 0dB, and the DHT functions are applied appropriately as the input signal level changes.

For example, if V_{MPO} = 13.63V, V_{SUP} = 8.04V, and SUP_{HR} = -20%, then solving for V_{TPO} yields a target peak output level of approximately 9.65V. Next, solving for the target peak output attenuation (A_{TPO}) yields approximately -3dB.

Figure 12 shows the default transfer function (with no DHT attenuation applied), where the current target peak output level (V_{TPO}) is based on the current V_{SUP} and the supply headroom settings. The tracked V_{TPO} and the resulting peak output attenuation (A_{TPO}) are then used in the attenuation calculations for the DHT functions. Note that this and all subsequent figures are not drawn to a precise scale and that the x-axis is the input signal level (dBFS) on a linear scale, while the y-axis is the peak output voltage level on a log scale.

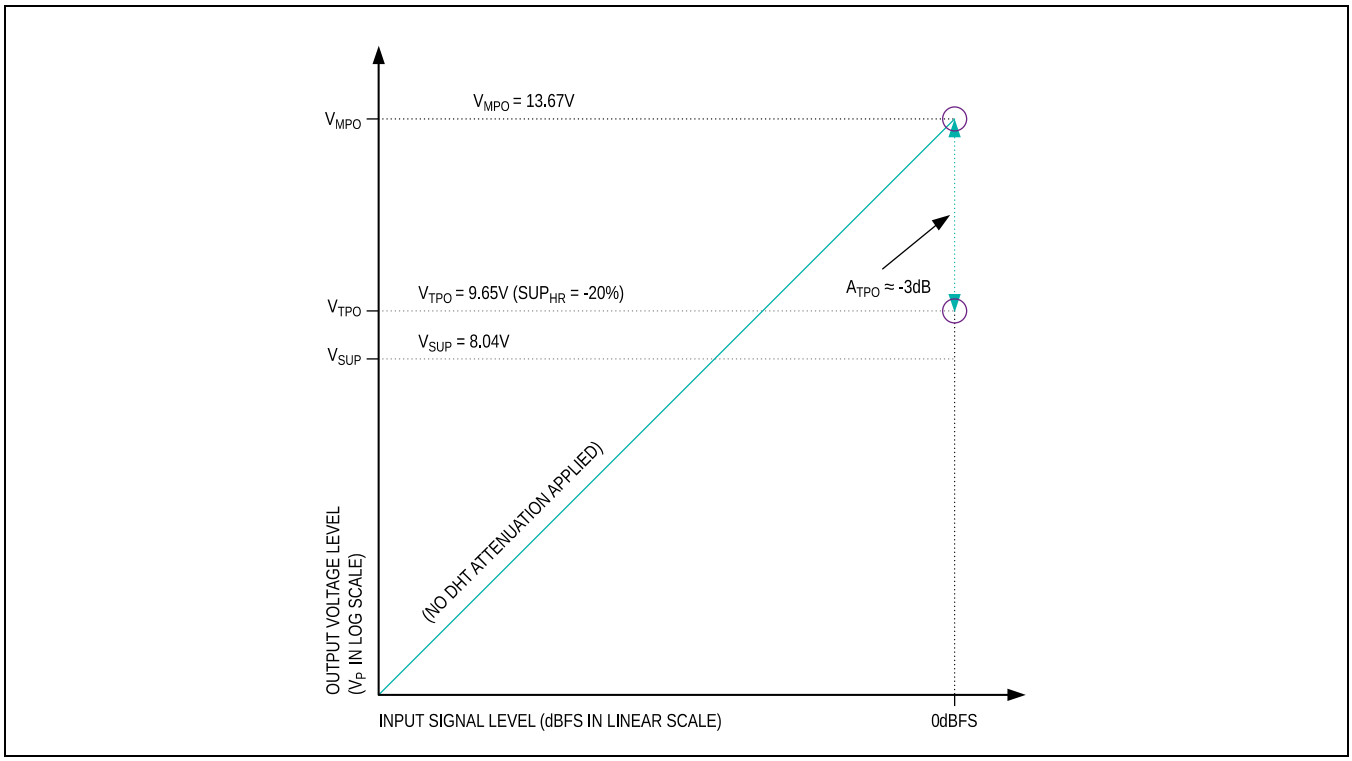


Figure 12. V_{TPO} and A_{TPO} Calculation Example

DHT Mode 1–Signal Distortion Limiter

The DHT signal distortion limiter (SDL) maintains a consistent level of signal distortion at the amplifier output as the supply voltage (V_{SUP}) changes. To use DHT mode 1 (just the signal distortion limiter active), set the DHT_LIM_MODE bit low (default) to place the limiter function in supply tracking mode (SDL), and set the dynamic range compressor rotation point (DHT_VROT_PNT) to 0dBFS (effectively disabling the DRC). The signal distortion limiter function is a compressor with a ratio of infinity to one that actively sets its threshold (V_{SDL} in voltage) equal to the calculated target peak output voltage level (V_{TPO}). The output-referred SDL threshold (SDL_{THR}) and the input-referred SDL knee or rotation point (SDL_{RP}) are equal in mode 1, and can be calculated relative to full-scale (in dBFS) as a ratio of V_{TPO} to V_{MPO}:

$$SDL_{RP} = SDL_{THR} = 20 \times \log(A_{TPO}) = 20 \times \log(V_{TPO} / V_{MPO})$$

The transfer function for input signal levels below the SDL rotation point (SDL_{RP}) is unchanged. When the input signal level exceeds SDL_{RP}, the signal distortion limiter function is applied to the signal path. As the input signal level increases,

the distortion limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) as follows:

$$SDL\ ATTENUATION = SDL_{RP} - A_{INPUT}$$

By actively recalculating SDL_{RP} (or SDL_{THR}) as the target peak output level (V_{TPO}) changes, the DHT SDL maintains a consistent limit and level of amplifier output distortion relative to the available supply voltage (V_{SUP}).

When the target peak output voltage exceeds the amplifier's maximum peak output voltage (V_{MPO}), no SDL attenuation is applied as there is sufficient headroom. However, as soon as V_{TPO} falls below V_{MPO}, the input signal amplitude can exceed the calculated SDL_{RP}. The following examples, *Figure 13*, *Figure 14*, and *Figure 15*, show the transfer of the input signal amplitude that can exceed when $V_{SUP} \geq V_{MPO}$ with the minimum (-20%), without (0%), and maximum (+20%) supply headroom (SUP_{HR}) settings. Note that in the case with positive headroom (+20%), the SDL_{RP} falls below the input signal full-scale level even though $V_{SUP} = V_{MPO}$.

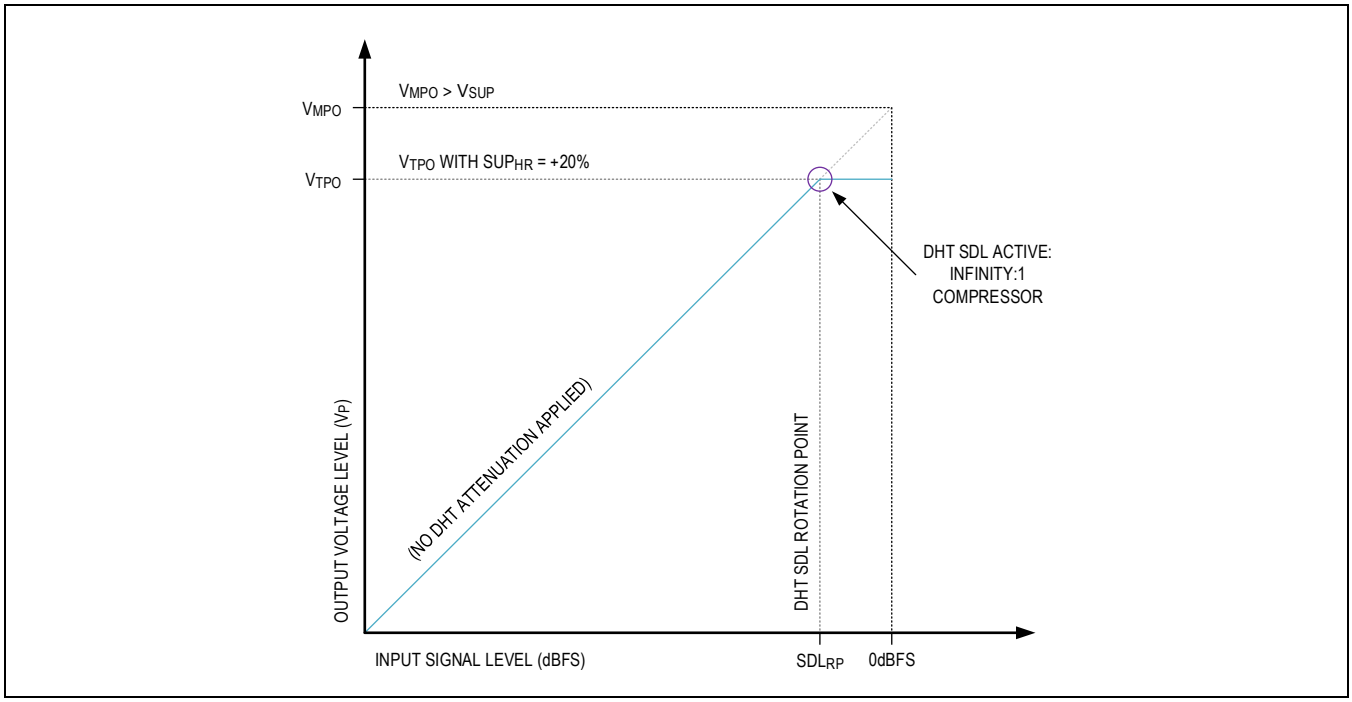


Figure 13. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and +20% Headroom (SUP_{HR})

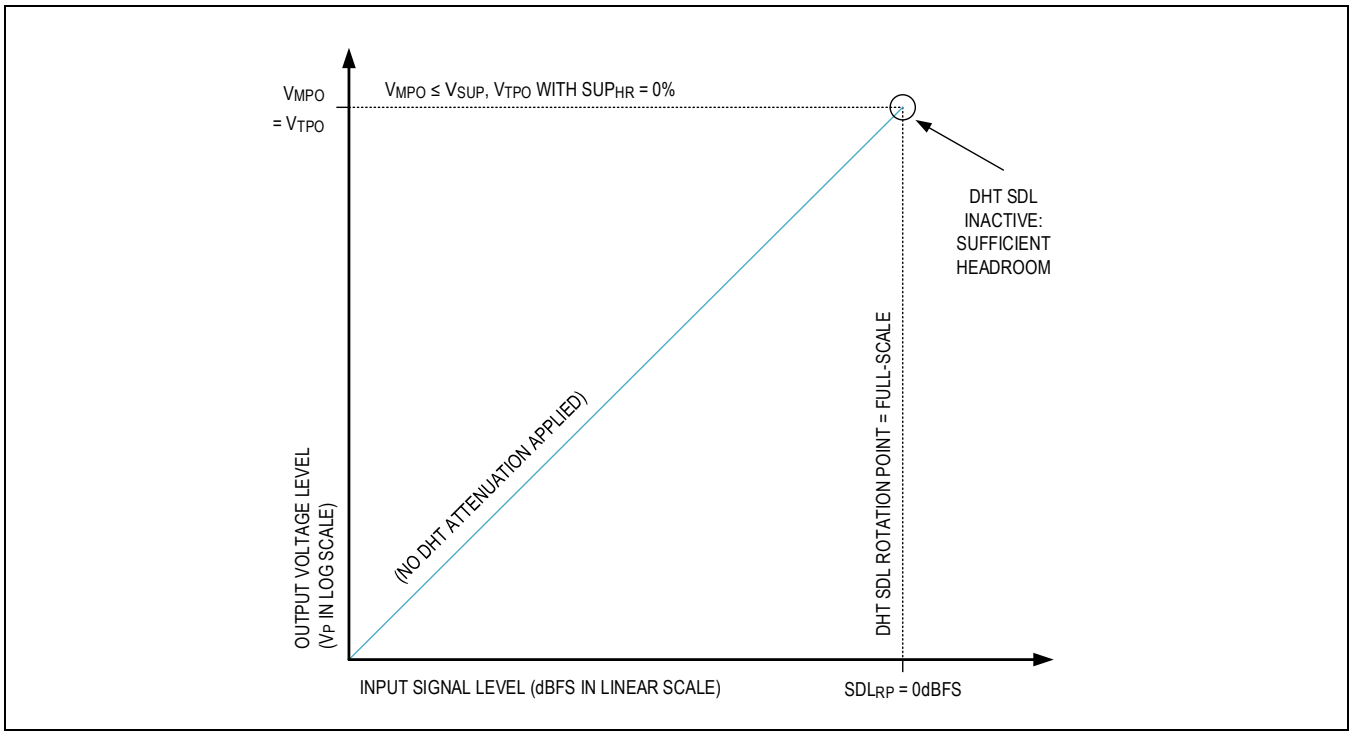


Figure 14. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and 0% Headroom (SUP_{HR})

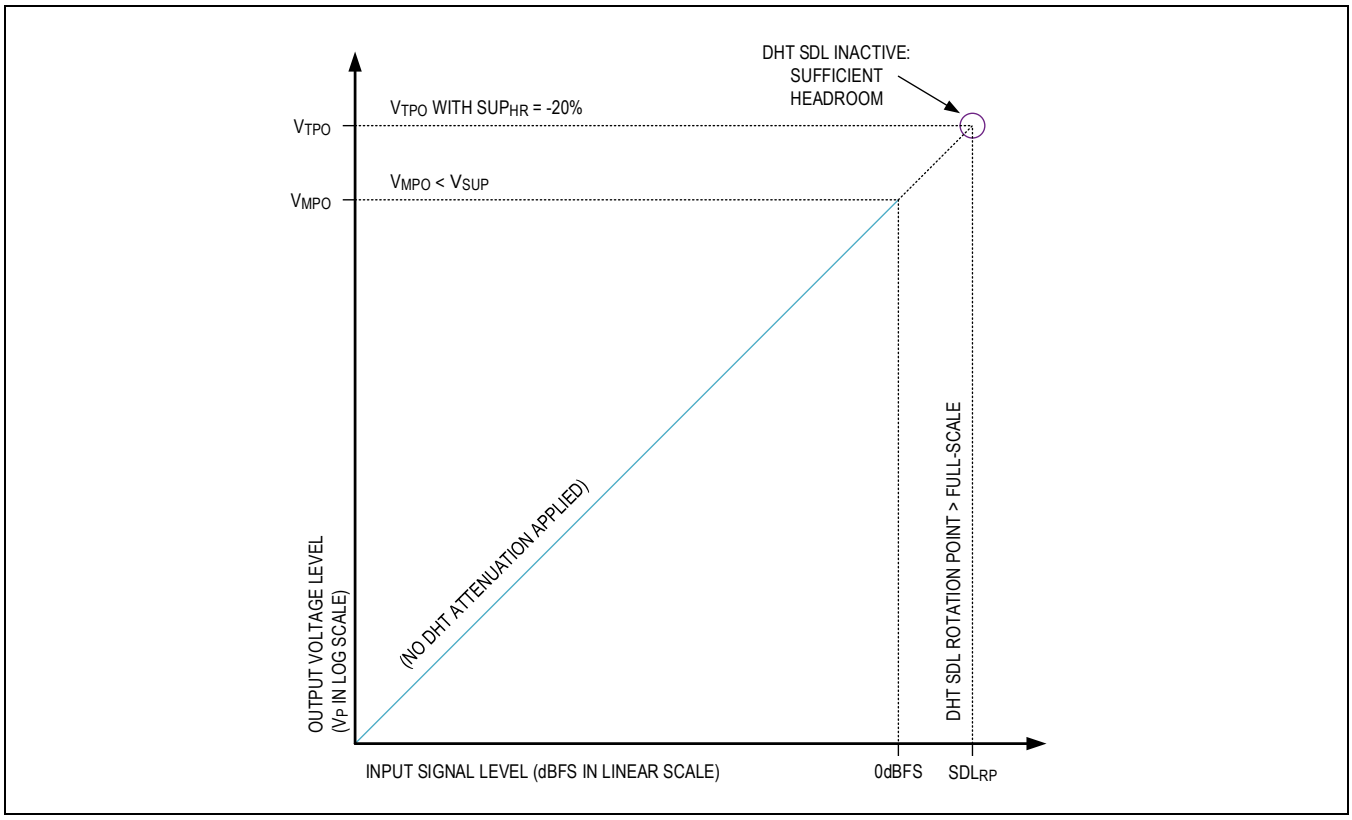


Figure 15. Signal Distortion Limiter with $V_{MPO} \leq V_{SUP}$ and -20% Headroom (SUP_{HR})

As the supply voltage (V_{SUP}) drops further below the maximum peak output voltage (V_{MPO}), the DHT target peak out voltage (V_{TPO}) proportionally scales down. In cases with zero or positive amplifier supply headroom settings (+20% ≥ SUP_{HR} ≥ 0%), the input signal level can exceed the SDL rotation point (SDL_{RP}) before the peak output exceeds V_{SUP}. In this case, amplifier output clipping can be prevented.

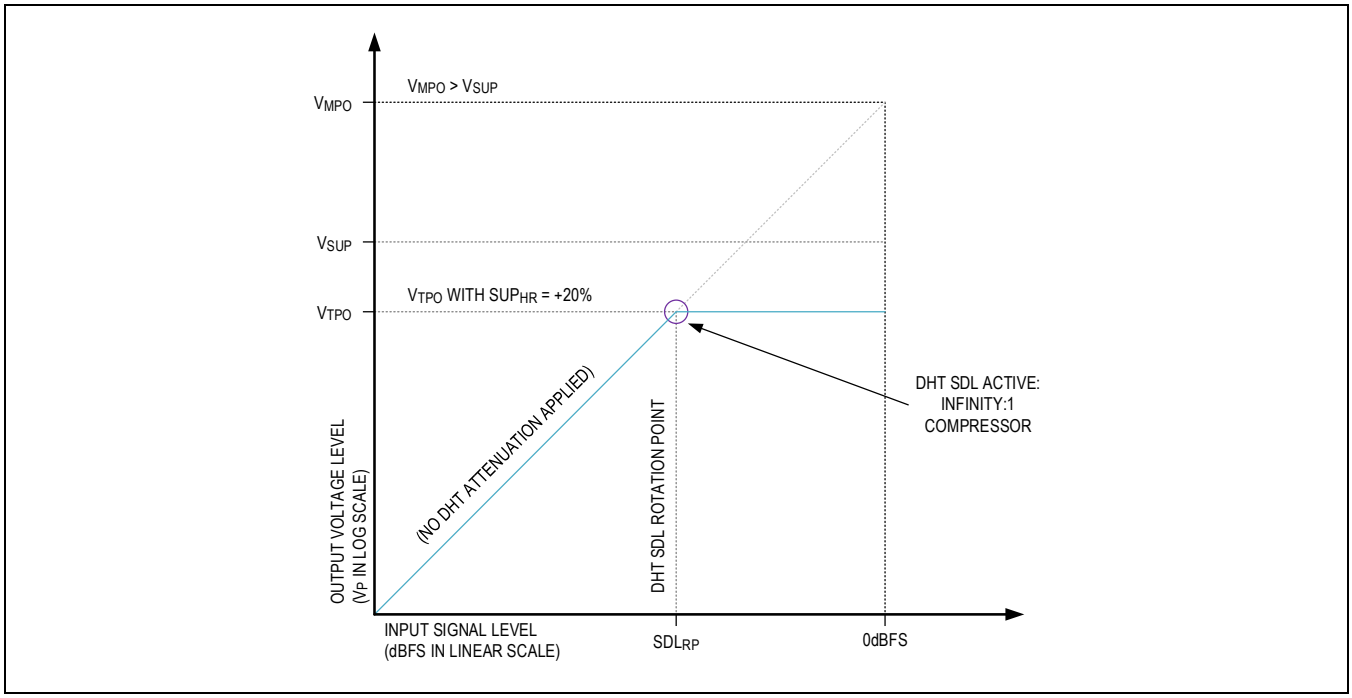


Figure 16. Signal Distortion Limiter with V_{MPO} > V_{SUP} and +20% Headroom (SUP_{HR})

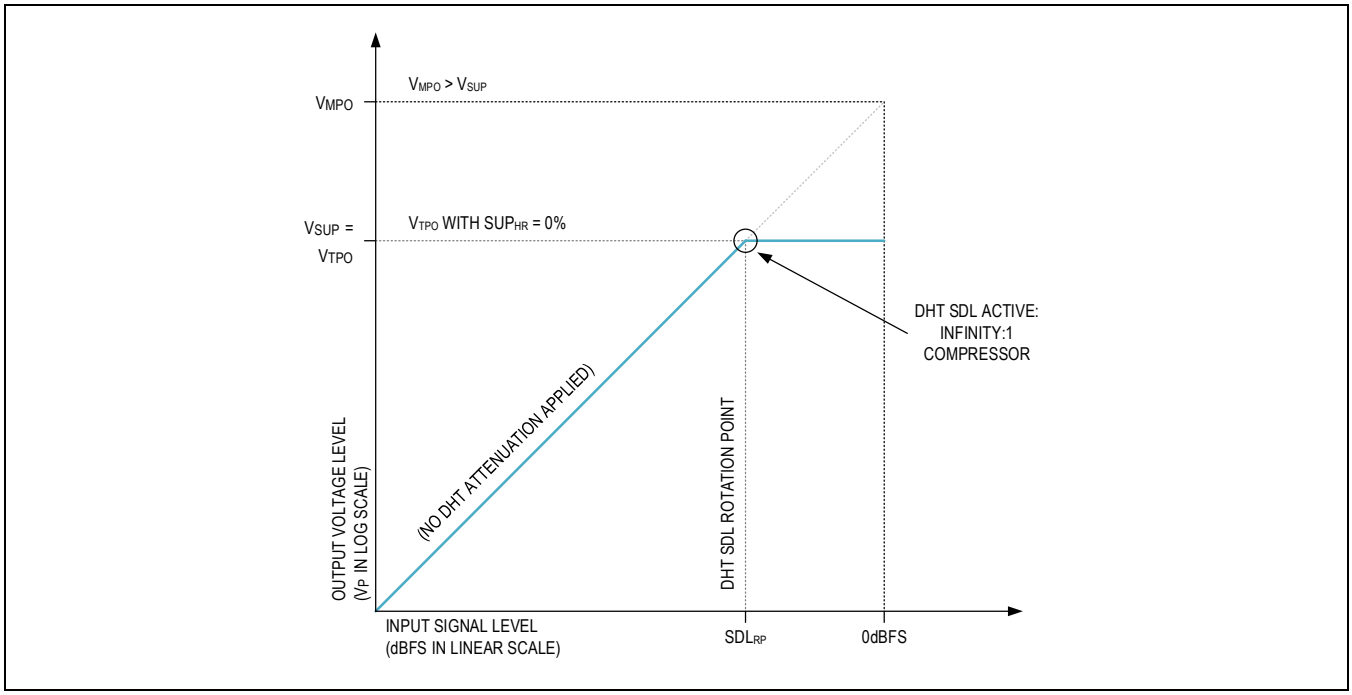


Figure 17. Signal Distortion Limiter with V_{MPO} > V_{SUP} and 0% Headroom (SUP_{HR})

In cases with a negative supply headroom setting (0% > SUP_{HR} ≥ -20%), the input signal does not exceed the SDL_{RP} until after the peak output reaches V_{SUP}. As a result, clipping occurs at the amplifier output. However, once the input

signal level exceeds the SDL_{RP}, the audio signal level is digitally limited by the SDL preventing the amplifier output clipping from worsening further.

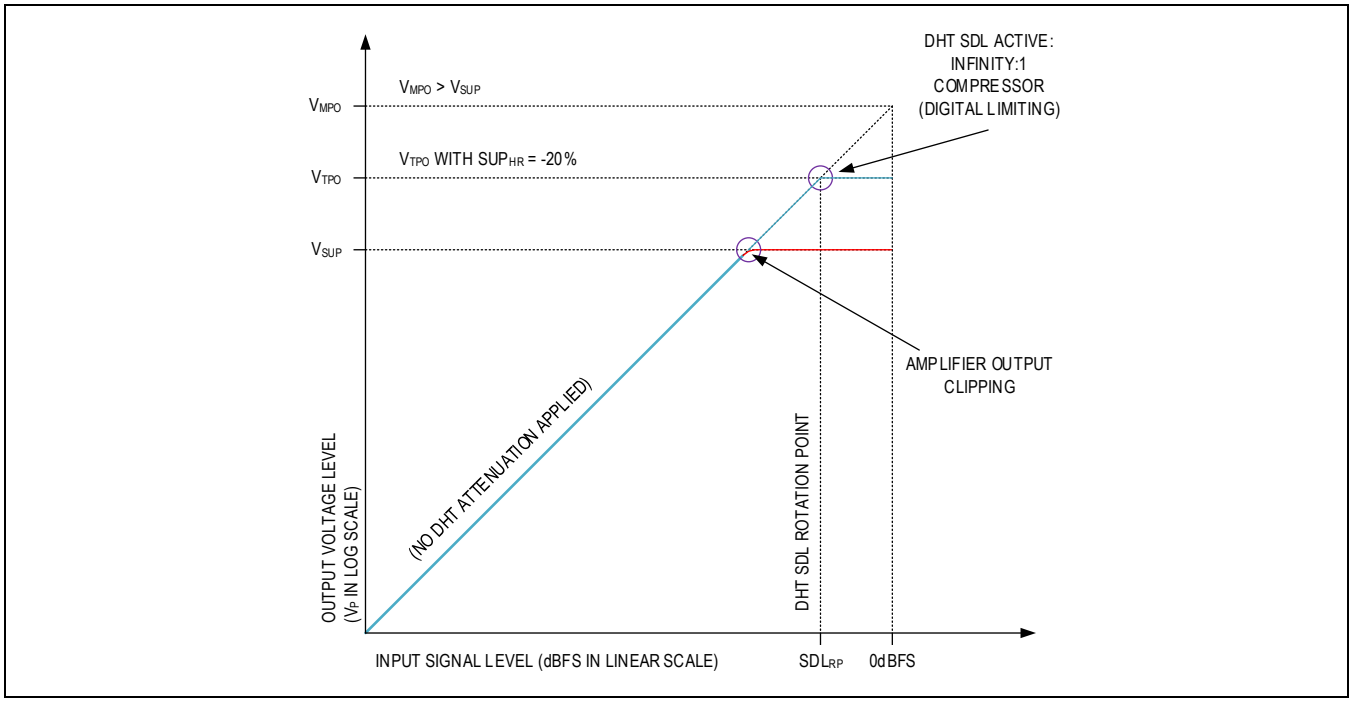


Figure 18. Signal Distortion Limiter with V_{MPO} > V_{SUP} and -20% Headroom (SUP_{HR})

DHT Mode 2–Signal Level Limiter

In DHT mode 2, the limiter is configured as a fixed threshold signal level limiter (SLL). Set the DHT_LIM_MODE bit high to place the limiter function in SLL mode, and set the dynamic range compressor rotation point to 0dBFS (effectively disabling the DRC).

Like the signal distortion limiter, the signal level limiter function is a compressor with a ratio of infinity to 1. However, unlike the SDL, the SLL output referred threshold (SLL_{THR}) is configured to a set level. The SLL_{THR} is selected with the DHT_LIM_THRESH bit field from a range of 0dBFS to -15dBFS. The SLL threshold can also be expressed as an input referred knee or rotation point (SLL_{RP}) which is equal to SLL_{THR} in mode 2. The SLL amplifier peak output voltage limit (V_{SLL}) is calculated from the selected SLL threshold (SLL_{THR}) and maximum peak output voltage (V_{MPO}) with the following equation:

$$\text{SLL PEAK OUTPUT VOLTAGE LIMIT} = V_{SLL} = V_{MPO} \times 10\text{^}(SLL_{THR} / 20)$$

The transfer function for signal levels below the SLL threshold (SLL_{THR}) is unchanged. When the signal level exceeds the SLL_{THR}, the signal level limiter function is applied to the signal path. As the input signal level increases, the limiter attenuation continues to increase as well and can be calculated for a given input signal level (A_{INPUT} in dBFS) relative to SLL_{RP} (= SLL_{THR}) as follows:

$$\text{SLL ATTENUATION} = SLL_{RP} - A_{INPUT}$$

When V_{TPO} is greater than V_{SLL}, the amplifier peak output level is limited to V_{SLL} whenever the signal amplitude exceeds the SLL threshold (SLL_{THR}). As a result of the fixed SLL threshold and rotation point, the transfer function is identical for any V_{SUP} level and corresponding V_{TPO} that is greater than V_{SLL}.

This is illustrated in *Figure 19* for decreasing V_{SUP} and V_{TPO} levels. As V_{SUP} decreases, V_{TPO} is recalculated and decreases as well. Three different progressively lower V_{TPO} levels are shown (V_{TPO1}, V_{TPO2}, and V_{TPO3}). Due to the fixed SLL threshold, V_{SLL} is the same in all three cases. Since all three V_{TPO} values are greater than V_{SLL}, the transfer function for each case is identical and is limited at V_{SLL}.

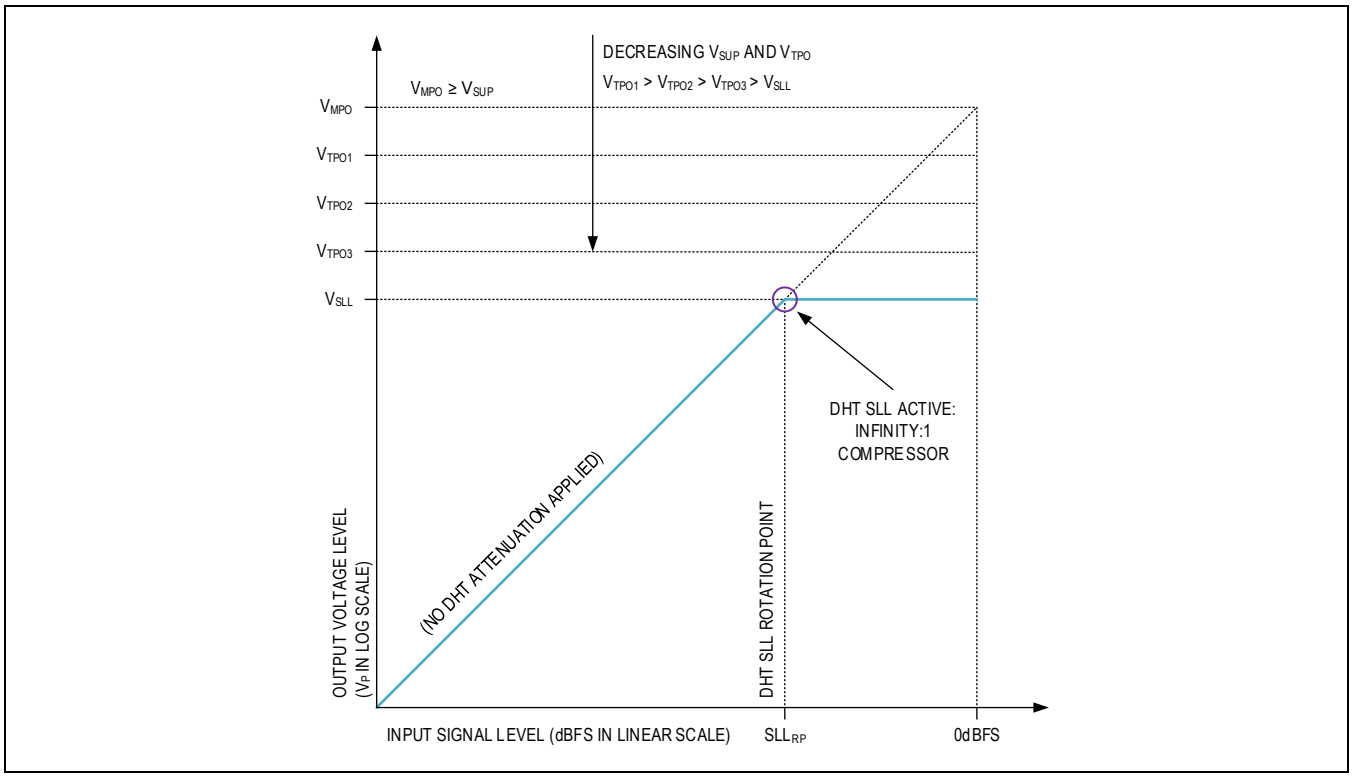


Figure 19. Signal Level Limiter with $V_{TPO} > V_{SLL}$ as V_{SUP} Decreases

When V_{TPO} is less than V_{SLL}, the amplifier output can clip before the input signal amplitude exceeds the SLL rotation point ($SLL_{RP} = SLL_{THR}$). As the input signal level continues to increase and exceed SLL_{RP}, the signal level is digitally limited which prevents the amplifier output clipping from worsening further. Because both the SLL threshold and rotation point are fixed relative to full-scale, the clipping at the amplifier output grows progressively worse before the input signal exceeding SLL_{RP} (= SLL_{THR}) as V_{SUP} continues to decrease.

Figure 20 has the same SLL settings as *Figure 19* (same SLL_{THR}). For simplicity, $V_{TPO} = V_{SUP}$ (SUP_{HR} = 0%), and V_{TPO} has decreased further and is now less than V_{SLL}. As a result, the amplifier output clips before the SLL digitally limits the signal level.

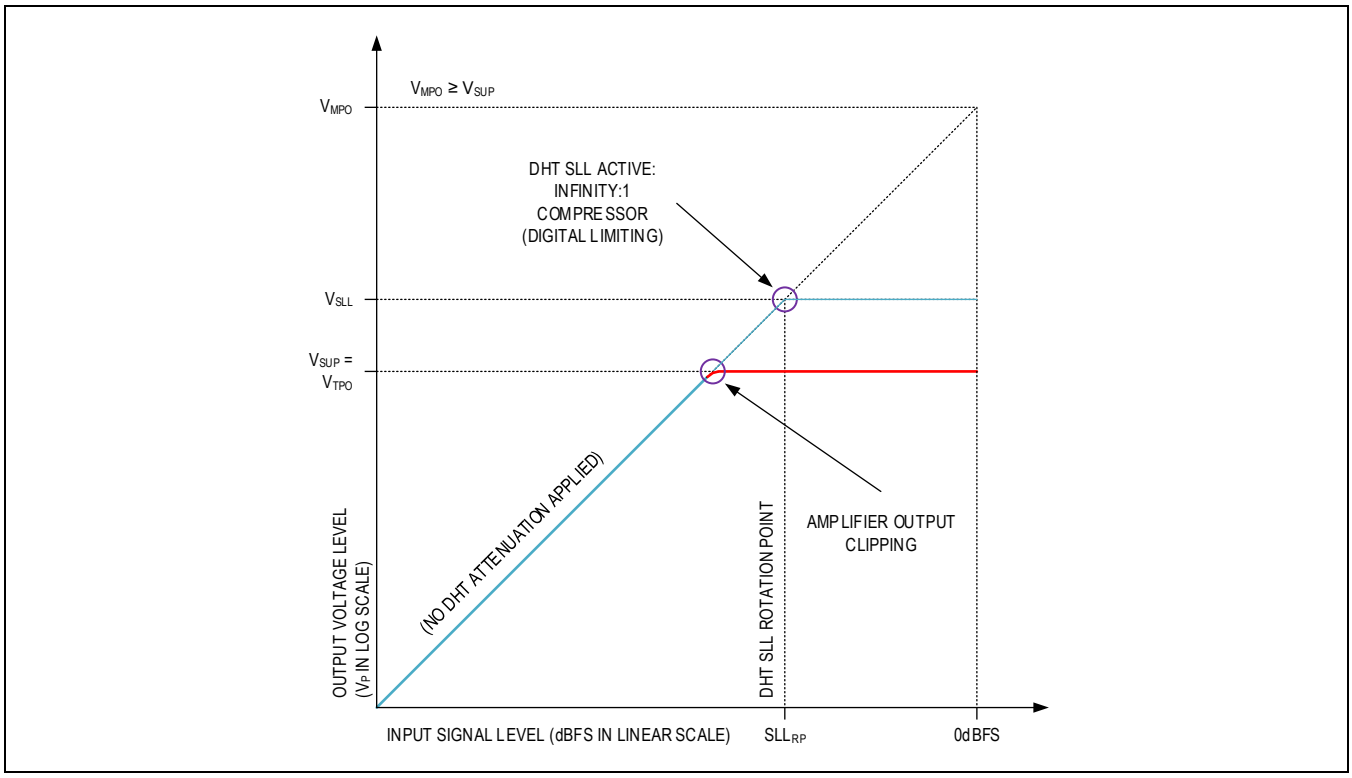


Figure 20. Signal Level Limiter with V_{TPO} < V_{SLL} Showing Amplifier Output Clipping

DHT Mode 3–Dynamic Range Compressor

The DHT dynamic range compressor (DRC) is configured by setting the input referred rotation point (DRC_{RP} in dBFS). The DRC_{RP} can be selected from a range from 0dBFS to -15dBFS with the DHT_VROT_PNT bit field. To calculate the DRC output referred voltage threshold (V_{DRC}), use the following equation:

$$V_{DRC} = V_{MPO} \times 10(DRC_{RP}/20)$$

For mode 3 operation, set the DRC rotation point (DRC_{RP}) to any level lower than 0dBFS. Next, to disable limiter functions, place DHT into signal level limiter mode (DHT_LIM_MODE = 1) and set the fixed SLL threshold (SLL_{THR}) to 0dBFS (using the DHT_LIM_THRESH bit field).

Once configured, the dynamic range compressor rotation point (DRC_{RP}) is fixed at the selected level (or ratio) relative to the input full-scale. As V_{SUP} and V_{TPO} change, the DRC compression ratio for input signals that exceed DRC_{RP} changes as well. However, the transfer function remains unchanged for input signals below DRC_{RP}.

The DHT tracks the target peak output voltage (V_{TPO}) and attenuation (A_{TPO}). As they change, the adaptive DRC compression ratio smoothly scales the listening level of the amplifier for any input signals that exceed DRC_{RP}. The DRC compression ratio is actively calculated with the following formula:

$$\text{DRC COMPRESSION RATIO} = DRC_{RP}/(A_{TPO} - DRC_{RP})$$

The DRC attenuation for a given input signal level (A_{INPUT} in dBFS) is calculated as follows:

$$\text{DRC ATTENUATION} = A_{TPO} - A_{INPUT} \times (A_{TPO} / DRC_{RP})$$

The following example shows the DRC transfer function with SUP_{HR} ≥ 0% as V_{SUP} (and thus V_{TPO}) decreases. As the V_{TPO} level decreases (from V_{TPO1} to V_{TPO2} to V_{TPO3}), the DRC compression ratio increases.

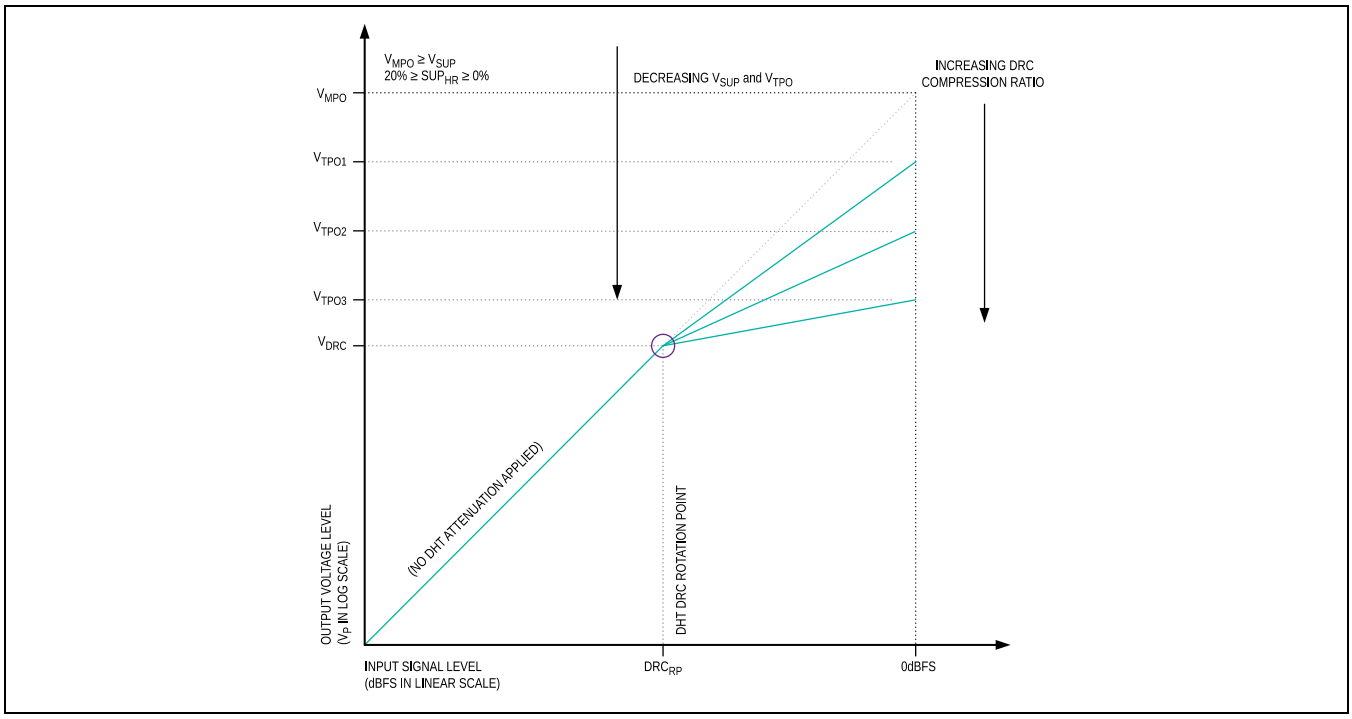


Figure 21. Dynamic Range Compression with Decreasing V_{SUP} and SUP_{HR} ≥ 0%

Figure 22 shows the DRC transfer function with SUP_{HR} < 0%. Due to the negative supply headroom, V_{TPO} is greater than V_{SUP}, and the amplifier output clips before the input signal reaches full scale.

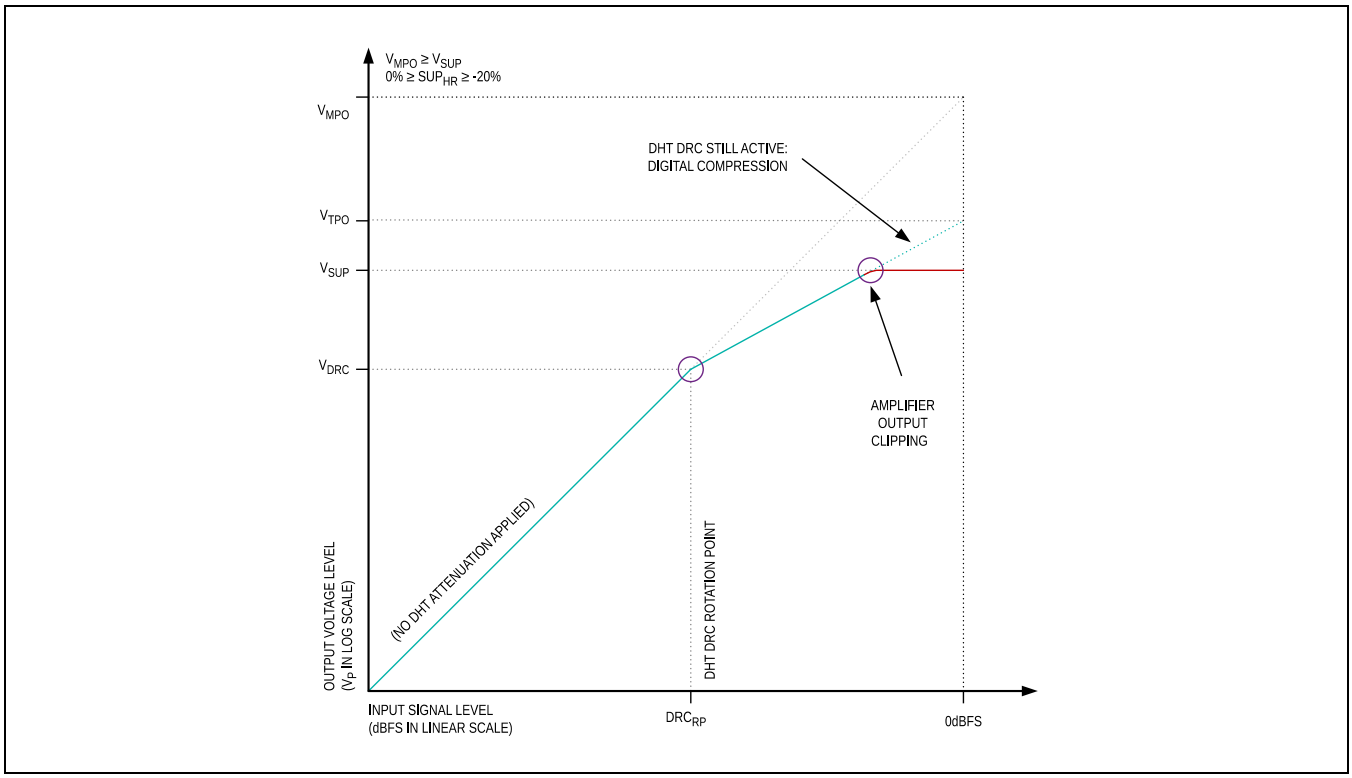


Figure 22. Dynamic Range Compressor with SUP_{HR} < 0% and Output Clipping

DHT Attenuation

An interrupt is generated (DHT_ACTIVE_BGN_*) when the DHT block first applies attenuation. When the DHT block fully releases all applied attenuation (i.e., DHT is inactive), an interrupt is generated (DHT_ACTIVE_END_*). Interrupts are not generated when DHT is actively adjusting the level of attenuation.

The maximum attenuation (A_{MAX}) applied to the audio signal by the DHT functions is selected with the DHT_MAX_ATN bit field. The maximum attenuation can be set from -1dB to -15dB with a 1dB step size. The configured DHT functions stop further attenuation of the audio signal once the calculated attenuation (relative to the un-attenuated input signal level) reaches the selected maximum attenuation (A_{MAX}). If the calculated attenuation (based on input signal level and measured V_{SUP}) exceeds the selected maximum attenuation (A_{MAX}), the applied attenuation is set equal to (limited at) A_{MAX}. This can occur anytime when the target peak output (V_{TPO}) to maximum peak output (V_{MPO}) ratio or peak output attenuation (denoted A_{TPO}) is less than (or has a larger absolute value than) A_{MAX}.

All previous examples show cases where the peak output attenuation (A_{TPO}) did not exceed the selected maximum attenuation (A_{MAX}). The following figures show signal distortion limiter use cases where V_{SUP} has decreased until $A_{TPO} < A_{MAX}$ (the DHT DRC function DRC_{RP} is set to 0dbFS as in use case 1).

In *Figure 23*, the SUP_{HR} is set to -20%. Since ATPO < A_{MAX}, the attenuation applied by the distortion limiter reaches the programmed maximum attenuation level before the input signal reaches full scale. For input signals past the point where calculated attenuation is equal to A_{MAX}, the attenuation stops increasing and is now fixed at A_{MAX}. As a result, the audio signal (in the digital domain) begins to increase past this point. This results in the distortion increasing at the amplifier output (which was already clipping at the limited level of distortion).

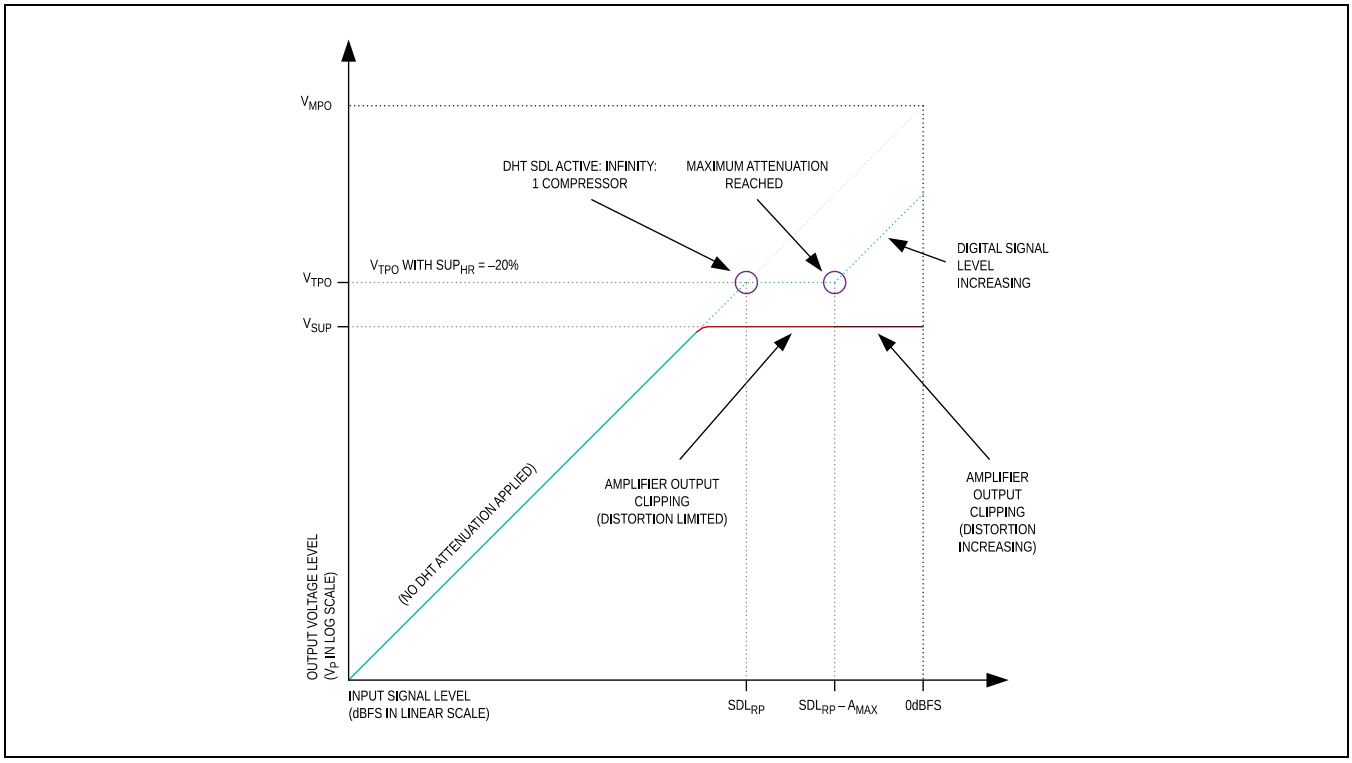


Figure 23. Distortion Limiter Case with -20% Headroom and A_{MAX} Exceeded

In *Figure 24*, the supply headroom is set to +20%. As before, the attenuation applied by the SDL reaches the selected maximum attenuation (A_{MAX}) before the input signal reaches full scale. The audio signal (in the digital domain) begins increasing past this point, and the signal level (and any distortion) at the amplifier output increases as well. In this case, the amplifier output did not clip until after A_{MAX} was exceeded.

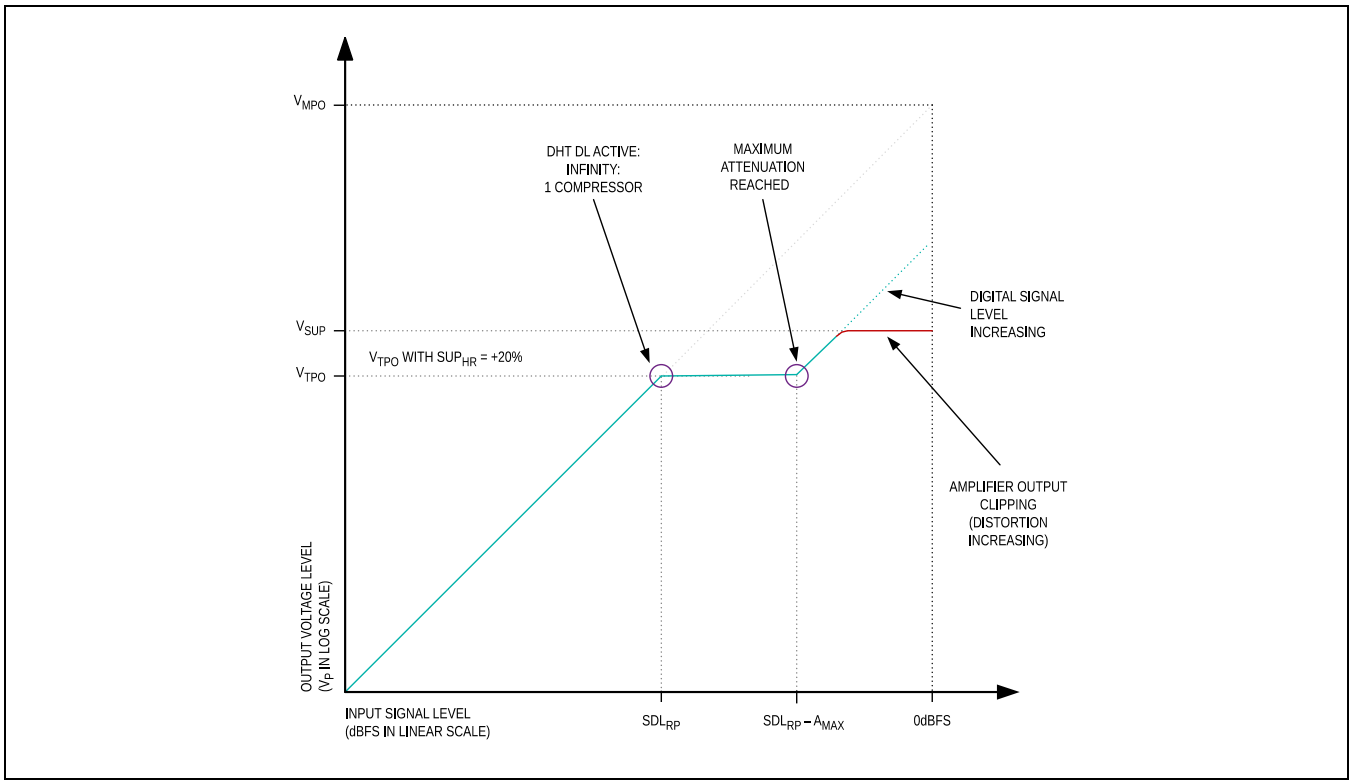


Figure 24. Distortion Limiter Case with +20% Headroom and AMAX Exceeded

DHT Attenuation Reporting

In TDM mode, the current level of DHT attenuation is reported on the PCM data output (DOUT) when the DHT attenuation transmit enable bit is set high (PCM_DHT_ATN_EN = 1). The DHT attenuation level output is transmitted as a 14-bit unsigned binary attenuation level:

DOUT CURRENT DHT ATTENUATION (dB) = 20 x log(14-bit DOUT Value/16383)

If enabled, the DHT attenuation target (in dB) is also shared between devices on the interchip communication (ICC) bus. In this case, the DHT attenuation level output requires two ICC output slots (8 bits each) and is transmitted as a 10-bit unsigned binary attenuation level (DHT_ATN) followed by 6 bits of zero padding.

The current DHT attenuation (in dB) is calculated from the 10-bit value (DHT_ATN) with the following equation:

ICC CURRENT DHT ATTENUATION (dB) = - (DHT_ATN[9:0] x 0.015625dB)

The current DHT attenuation level cannot exceed the selected DHT maximum attenuation (A_{MAX}). Additionally, when the DHT is inactive, the reported attenuation is 0x0.

DHT Ballistics

When the signal level exceeds the rotation point or threshold for a configured DHT function (SDL, SLL, and/or DRC) or continues to increase beyond this point, the appropriate level of attenuation is applied to the signal level at the programmed attack rate. The DHT attack rate is selected with the DHT_ATK_RATE bit field.

The change in input signal level is detected by a peak detect circuit, which has a fixed 3.5ms release time. When the signal level decreases or drops below the rotation point or threshold for a configured DHT function (SDL, SLL, and/or DRC), the appropriate level of applied attenuation is released. The DHT release rate is selected with the DHT_RLS_RATE bit field. However, due to the 3.5ms/dB peak detector, the 2ms/dB release rate is effectively 3.5ms/dB. All other release rates have a fixed delta of 3.5ms compared to the programmed release rate.

The attack and release behavior is slightly different when triggered by a change in the active amplifier supply level. When the supply level decreases and triggers a DHT function attack, the attenuation is applied quickly at the configured attack rate. Likewise, as the supply level increases, the attenuation is released at the configured release rate. However, if DHT

supply hysteresis is enabled (DHT_SUPPLY_HYST_EN = 1), then as the supply increases, the applied DHT function does not release attenuation until the increase in the supply level exceeds the programmed DHT supply hysteresis level (DHT_SUPPLY_HYST). Once the supply increase exceeds the hysteresis, the appropriate level of applied attenuation is released at the configured release rate.

Speaker Amplifier

The device features a Class-D speaker amplifier output stage. The speaker amplifier playback path is enabled and disabled using the SPK_EN bit. The Class-D amplifier generates a rail-to-rail output, pulse-width modulated (PWM) signal. By varying the PWM duty cycle, the amplifier modulates the output with the audio input signal. Because the switching frequency of the amplifier is 330kHz (typ), when the output signal is filtered by the speaker, only the audio component remains. Rail-to-rail operation ensures that power dissipation at the output is dominated by the on-resistance (R_{ON}) of the output power MOSFETs', the brief saturation current draw as the output switches, and the current draw necessary to charge the output stage gates.

Speaker Amplifier Operating Modes

The speaker amplifier operates as a fixed supply Class-D amplifier using V_{PVDD} as the output supply rail.

Stereo Mode

In this mode, the MAX98415A/MAX98425A processes two channels of digital audio input data to produce amplified Class-D output signals that can drive two independent loads at the output. The OUTPA/OUTNA drives the Amplifier A output speaker load, whereas OUTPB/OUTNB drives the Amplifier B output speaker load.

Idle Mode

In customer systems where an external LC filter is used for electromagnetic interference (EMI) reduction, the quiescent power consumption and power consumption for low signal levels can be reduced by setting the IDLE_MODE_EN bit field to 1.

When the idle mode is enabled, the idle mode activates whenever the amplitude of the input audio data to the speaker path (from the PCM interface) is below the configured idle mode active/noise gate mute threshold (MUTE_THRESH) for more than 1024 consecutive data samples. The idle mode deactivates immediately if the amplitude of a single sample from the input audio data exceeds the configured Idle Mode inactive/noise gate unmute threshold (UNMUTE_THRESH).

The idle mode active/noise gate mute and idle mode inactive/unmute threshold settings are selected in terms of the number of bits (starting from the LSB) that must be toggling (or active) for the input signal amplitude to exceed the thresholds. It is invalid to set the idle mode inactive/noise gate unmute threshold (NG_UNMUTE_THRESH) such that it is less than the configured idle mode active/mute threshold (NG_MUTE_THRESH). The location of the audio data LSB within the PCM input data channel is determined by the configured PCM data word size (PCM_CHANSZ). The supported combinations are shown in *Table 8*.

It is not valid to enable the idle mode and noise gate function simultaneously.

Speaker Amplifier Ultra-Low EMI Filterless Operation

Traditional Class-D amplifiers require the use of external LC filters or shielding to meet electromagnetic interference (EMI) regulation standards. However, the device features emissions-limiting circuitry that limits the output switching harmonics that can directly contribute to EMI and radiated emissions.

The programmable speaker amplifier edge rate control bits are used to adjust the switching edge rate to help tune EMI performance. As the edge rate increases, the efficiency improves slightly, while as the edge rate decreases, the efficiency drops slightly. The speaker amplifier edge rate is configured with the SPK_SL_RATE_LS and SPK_SL_RATE_HS bit fields.

The speaker amplifier output also supports spread-spectrum modulation (SSM). SSM is enabled by default to optimize the suppression and control of the output switching harmonics that can contribute to EMI and radiated emissions. The modulation index in spread-spectrum mode is controlled by the SPK_SSM_MOD_INDEX bit field, and the maximum modulation index (MMI) varies accordingly. Higher percentage settings of the modulation index result in the switching frequency of the amplifier being modulated by a wider range, spreading out-of-band energy across a wider bandwidth. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Speaker Amplifier Overcurrent Protection

The device features amplifier current limit protection that protects the amplifier output from both high current and short circuit events. If the OVC_RETRY_EN bit is set to 1 and the speaker amplifier output current exceeds the current limit

threshold (6.0A min), the device generates an interrupt and disables the amplifier output. After approximately 20ms, the amplifier output is re-enabled. If the overcurrent condition still exists, the device continues to disable and re-enable the amplifier output automatically until the fault condition is removed.

If the OVC_RETRY_EN bit is set to 0, the device still generates an interrupt, and disables the amplifier output when a speaker amplifier overcurrent event occurs. However, in this case, the device is placed into software shutdown and the software enable (EN) bit is set to 0. As a result, the host must manually re-enable the device after an overcurrent event.

Note: In systems with large cable lengths (>6”), an overcurrent event may trigger VBAT_UVLO_XXX interrupt. To enable auto restart of the amplifier, it is recommended to keep VBAT_AUTORESTART_EN=1. In this case, the amplifier outputs are re-enabled at a faster than 20ms rate, based on VBAT recovery.

Speaker Current ADC and Voltage Feedback Path

The device provides a 16-bit ADC to monitor the speaker amplifier output current for each amplifier and a digitally compensated voltage feedback path to represent the speaker output. The current and voltage feedback paths are independently enabled with the IVFB_I_EN and IVFB_V_EN bits, respectively.

The voltage and current digital data output are routed to the host through the PCM interface data output (DOUT), which is enabled by the PCM_TX_EN bit field. Both I and V data can be formatted in 16-, 24-, or 32-bit 2's complement format and have a voltage feedback range of ±24V and a current sense range of ±6.0A.

When configured in 16-bit mode for $V_{FEEDBACK}$, if MSB is zero, then the voltage would be 12/(2^15) x DIG CODE.

For example, a $V_{FEEDBACK}$ reading of 0111 1111 1111 1111 translates to a voltage of +24V, and a reading of 1000 0000 0000 0000 would be -24V.

For 16-bit I_{SENSE}, if MSB is zero, then the current would be 3/(2^15) x DIG CODE.

For example, an I_{SENSE} reading of 0111 1111 1111 1111 translates to a voltage of +6A, and a reading of 1000 0000 0000 0000 would be -6A.

See the *PCM Interface* section for details on configuring I/V feedback-data output on DOUT. Both the current and voltage sense ADC output data can optionally have dither applied (±1 LSB peak-to-peak) by setting the IVFB_DITH_EN bit field to 1. No dither is applied when IVFB_DITH_EN is set to 0.

The I/V feedback path provides separate optional DC blocking filters (first-order highpass) in the current and voltage sense paths. The current and voltage path filters are enabled by setting the IVFB_I_DCBLK_EN and IVFB_V_DCBLK_EN bit fields to 1, respectively.

To ensure phase alignment, the current and voltage sense ADCs should be enabled either with a single write to the IVFB_I_EN and IVFB_V_EN bits (EN = 1) or by setting both bits high before exiting software shutdown.

When laying out the PCB, the OUTPSNS and OUTNSNS pins should be Kelvin connected as closely as possible to the load connected between OUTP and OUTN for accurate voltage measurements. If a filter comprised of a ferrite bead and capacitor is installed between the speaker amplifier output pins and the load, then the sense lines should be connected between the filter and the load and as close to the load as possible. If an LC filter is installed between the amplifier output pins and the load, the OUTPSNS and OUTNSNS lines should be connected to the OUTP and OUTN lines before the filter. The OUTPSNS and OUTNSNS pins are not intended to be driven by an external source. The speaker amplifier current is measured internally and requires no external connections.

Brownout-Prevention Engine

The brownout-prevention engine (BPE) allows the device to reduce its contribution to the overall system power consumption by attenuating the amplifier output when the supply drops below a set of programmable thresholds. The BPE is enabled and disabled using the BPE_EN bit. The BPE can be enabled anytime by setting the BPE_EN bit high. However, the BPE must not be disabled when it is active (in critical supply levels 0 through 3). The BPE can be disabled safely at any time that it is inactive. The input to the BPE controller is selected using the BPE_SRC_SEL bit. By default, the input to the BPE controller is the measurement ADC PVDD channel. If the PVDD measurement ADC channel is not already active, enabling the BPE automatically, enables it. The sample rate and filter settings for the measurement ADC determine the speed at which the BPE updates.

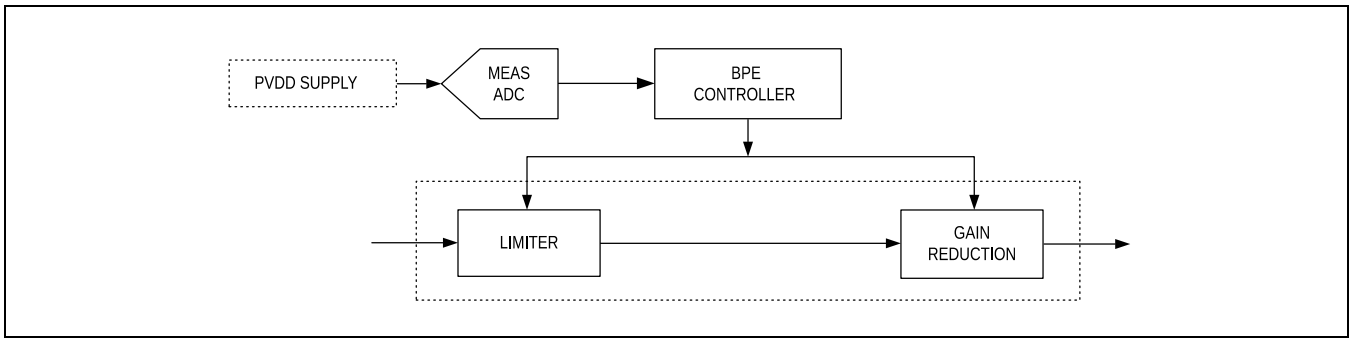


Figure 25. BPE Block Diagram

BPE State Controller and Level Thresholds

There are four BPE critical supply levels, each with individually programmable thresholds. The thresholds for each level are configured with the BPE_L0_VTHRESH to BPE_L3_VTHRESH bit fields, respectively. The BPE state controller monitors the measurement ADC channel results and automatically makes state changes.

Table 9. Brownout-Prevention Engine Levels

THRESHOLD NAME	CONDITION
BPE Inactive	V_{SUPPLY} > Critical Supply Level 3
Critical Supply Level 3	Critical Supply 3 ≥ V_{SUPPLY} > Critical Supply Level 2 + Hysteresis
Critical Supply Level 2	Critical Supply Level 2 ≥ V_{SUPPLY} > Critical Supply Level 1 + Hysteresis
Critical Supply Level 1	Critical Supply Level 1 ≥ V_{SUPPLY} > Critical Supply Level 0 + Hysteresis
Critical Supply Level 0	V_{SUPPLY} ≤ Critical Supply Level 0

The brownout engine supports hysteresis on the levels. This behaves as follows:

- When in level N, transition to level N + 1 when V_{SUPPLY} stays above (level N threshold) + (hysteresis)
- When in level N, transition to level N - 1 when V_{SUPPLY} falls below the level N threshold

The BPE_VTHRESH_HYST register defines the amount of hysteresis. The hysteresis is only applied to the thresholds when the supply voltage increases. The amount of hysteresis can be defined as larger than the distance between two levels.

Thresholds must be configured so that the level N threshold is greater than the sum of the level N - 1 threshold and the hysteresis. For example, if the level 2 threshold is set to 6.3359V and hysteresis is set to 43.99mV, then the level 3 threshold must be set to 6.3799V or higher.

The current level of the BPE can be read back using the BPE_STATE register. The BPE_LOWEST register contains the lowest BPE level that the controller has visited since the last time the BPE_LOWEST register was read.

BPE Level Configuration Options

For a given BPE level, the following options are configurable to reduce the overall device current draw:

- Gain Attenuation Function
- Limiter Function

Each of these configuration options is individually configurable for each BPE level.

BPE Gain Attenuation Function

The speaker gain attenuation block reduces the overall current drawn by the device at low supply voltages by applying smooth digital gain changes to the signal path. The maximum attenuation that can be applied can be independently configured for each BPE level. The maximum attenuation that can be applied for each level is programmable from 0 to -31dB in 1dB steps and is configured using the BPE_Lx_MAXATTN bits.

When the V_{SUPPLY} voltage level falls below the programmed level, the brownout controller waits for a time equal to the programmed dwell time for the level before applying attenuation at the programmed attack rate. The brownout controller then enters the hold time phase when the V_{SUPPLY} voltage increases and causes the brownout controller to enter the next level. After the programmed hold time for a BPE level expires, the controller enters the release phase where the

controller releases the attenuation at the programmed release rate. Additionally, each BPE level has independent programmable settings for dwell time (BPE_Lx_DWELL), hold time (BPE_Lx_HOLD), attack and release step size (BPE_Lx_STEP), attack rate (BPE_Lx_GAIN_ATK), and release rate (BPE_Lx_GAIN_RLS). While the attack and release rates are independently configurable for the gain attenuation and limiter block, the attack and release step size settings are common.

The BPE_LOWEST_GAIN register contains the lowest gain (highest attenuation) applied to the brownout controller. The register is updated upon reading to show the current attenuation applied by the BPE.

BPE Limiter Function

The BPE limiter function allows the device to reduce the overall current draw at low supply levels by quickly attenuating (12µs) input signals that exceed a programmed threshold. When the BPE limiter is enabled (BPE_LIM_EN = 1), the device ignores the Signal Distortion Limiter and Signal Level Limiter settings in the DHT. In this state, the limiter knee threshold is determined solely by the BPE limiter setting of the current BPE level. Each BPE level has an individually configured limiter threshold (set by BPE_Ln_LIM) that is programmable from 0dBFS and -15dBFS in 1dB steps.

Input signals that exceed the limiter knee threshold are attenuated, while input signals below the threshold are not. Each BPE level has an individually configured attack and release step size (BPE_Lx_STEP), attack rates (BPE_Lx_LIM_ATK), and release rates (BPE_Lx_LIM_RLS). While the attack and release rates are independently configurable for the gain attenuation and limiter block, the attack and release step size settings are common. The BPE_LOWEST_LIMIT register contains the lowest limiter setting applied to the brownout controller. The register is updated upon reading to show the current limiter setting applied by the BPE.

Brownout Interrupts

The BPE can generate interrupts triggered by the following conditions:

- The BPE controller enters level 0 (BPE_L0_*)
- The BPE controller changes from one level to another (BPE_LEVEL_*)
- The BPE controller is active (BPE_ACTIVE_BGN_*)
- The BPE controller is no longer active (BPE_ACTIVE_END_*)

See the *Interrupts* section for more information.

Measurement ADC

The device features a configurable 9-bit measurement ADC. The measurement ADC has three channels: two channels for die temperature measurement (measurement ADC thermal channels) close to each amplifier output, and a third channel for PVDD supply voltage measurement (measurement ADC PVDD channel). Enabled channels are measured sequentially and continuously. The programmable measurement ADC sample rate can be set independently for each channel. Each channel separately provides an optional programmable lowpass IIR filter.

Measurement ADC Thermal Channels

When the device is clocked in the active state (EN = 1), the measurement ADC thermal channels automatically activate. When active, they continuously measure and report the device die temperature over the range from -29°C to +150°C.

The output of the thermal ADC channels can be readback through the MEAS_ADC_AMPX_THERM_DATA bit fields and these are the inputs to both the thermal protection, and thermal foldback blocks. By default (MEAS_ADC_THERM_RD_MODE = 0), the thermal readback values are automatically updated after each conversion is completed. Setting MEAS_ADC_THERM_RD_MODE = 1 places the thermal readback into manual mode. In manual mode, the thermal readback results are updated manually when 1 is written to the MEAS_ADC_THERM_UPD bit field. The ADC thermal channels data readback in manual mode and the data streamed through the PCM interface is 9 bits. In automatic mode, since the 9-bit data readback is from two registers, the LSB register is not guaranteed to be synchronous with the MSB register and can result in higher noise.

The highest measured temperature measurement results are readback through the HIGHEST_AMPX_THERMAL_DATA_MSB and HIGHEST_AMPX_THERMAL_DATA_LSB bit fields. These bit fields automatically clear and are reset to the value of the current measurement result immediately after the LSB readback is completed.

The thermal ADC channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_AMPX_TEMP_FILT_EN bit field, and the bandwidth is set with the MEAS_ADC_AMPX_TEMP_FILT_COEFF bit field.

Measurement ADC PVDD Channel

When the device is clocked and in the active state (EN = 1), the measurement ADC PVDD channel can be enabled. The PVDD channel is manually enabled by setting the MEAS_ADC_PVDD_EN bit to 1 and must be manually enabled for the DHT to operate. When the channel is enabled, it continuously measures and reports the PVDD supply voltage level over the range of 2.5V to 22.5V.

The output of the measurement ADC PVDD channel can be read back through the MEAS_ADC_PVDD_DATA bit field and is routed to the DHT. By default (MEAS_ADC_PVDD_RD_MODE = 0), the PVDD readback value is automatically updated after each conversion is completed. Setting MEAS_ADC_PVDD_RD_MODE to 1 places PVDD readback into manual mode. In manual mode, the readback result is updated when 1 is written to the MEAS_ADC_PVDD_RD_UPD bit field. The ADC PVDD channel data readback in manual mode, and the data streamed through the PCM interface is 9 bits. In automatic mode, since the 9-bit data readback is from two registers, the LSB register is not guaranteed to be synchronous with the MSB register and can result in higher noise.

The lowest PVDD measurement is readback through the LOWEST_PVDD_DATA_MSB and LOWEST_PVDD_DATA_LSB bit fields. These bit fields both automatically clear and are reset to the value of the current measurement result immediately after the LSB readback is completed.

The PVDD channel also provides an optional lowpass IIR filter with a programmable bandwidth that scales relative to the measurement ADC sample rate. The filter is enabled with the MEAS_ADC_PVDD_FILT_EN bit and the bandwidth is set with the MEAS_ADC_PVDD_FILT_COEFF bit field.

Clock Monitor

The device has external clock monitors that detect host and system-level faults. The clock monitor detects external clock failures and invalid clock configurations. Upon fault detection, this monitor automatically places the device into software shutdown to stop glitches and unwanted signals at the amplifier output and speaker load.

Clock Monitor

The device provides an optional clock monitor that is enabled by setting CMON_EN to 1. Once enabled, it actively monitors the input BCLK and LRCLK anytime the device exits software shutdown (EN = 1). When the tone generator is enabled, the clock monitor is automatically disabled. When active, the clock monitor detects clock activity, clock frequency, and frame timing (clock ratio). If faults are detected, the clock monitor automatically places the device into software shutdown and generates a clock error interrupt (CLK_ERR_*).

The clock monitor operates in automatic mode when CMON_AUTORESTART_EN = 1 and manual mode when CMON_AUTORESTART_EN = 0. In automatic mode, when a clock error places the device into software shutdown, the global enable bit (EN) is not changed (remains 1), and the device automatically recovers from all clock errors. In automatic mode, both clock error (CLK_ERR_*) and clock recovery (CLK_RECOVER_*) interrupts are generated in pairs (a clock recovery interrupt is not possible until after a clock error has occurred).

In manual mode, when a clock error places the device into software shutdown, the global enable bit (EN) is set to 0. Clock recovery (CLK_RECOVER_*) interrupts are never generated in manual mode, and the device remains in software shutdown until the host sets EN back to 1. Once the device is re-enabled (EN set to 1), the clock monitor is active and detects any new (or persisting) clock errors. If a clock error is detected, the device returns to software shutdown (EN = 0), and a new clock error interrupt (CLK_ERR_*) is generated. Clock errors are fault conditions, and audible glitches may occur on clock monitor-based transitions into and out of software shutdown. When the clock monitor is enabled, no false clock error or clock recovery interrupts are generated when the host software transitions the device normally into and out of software shutdown.

Clock Monitor is enabled by default, and it is highly recommended that the block be kept enabled to allow Speaker Monitor to function correctly in the absence of BCLK and LRCLK.

Clock Activity and Frequency Detection

When the clock monitor is enabled, the bit clock (BCLK) and frame clock (LRCLK) frequencies are monitored. The expected LRCLK frequency is equal to the PCM sample rate (PCM_SR). The expected BCLK frequency is based on the BCLK to LRCLK ratio (PCM_BSEL) relative to the PCM sample rate (PCM_SR).

The current frequency of each clock is measured relative to (and once per interval of) the programmed frame period (as set by PCM_SR). A clock frequency error is detected when the measured clock frequencies differ from programmed clock

frequencies (faster or slower) by more than the frequency error threshold (45% typ). If either clock stops high or low, the frequency measurement result allows detection of the clock stop event.

The CMON_ERRTOL bit field sets the clock frequency error tolerance. The tolerance is the required number of consecutive frame clock periods (PCM_SR) with an incorrect clock frequency before a clock error is generated. If the error persists for the selected number of frame periods, a clock error interrupt (CLK_ERR_*) is generated, and the device is placed on software shutdown.

In automatic mode, the CMON_ERRTOL bit field also sets the number of consecutive frame clock periods without clock frequency errors (LRCLK or BCLK) that are required for automatic restart to occur. Once the selected number of consecutive error-free frames are detected, a clock recovery interrupt (CLK_RECOVER_*) is generated, and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated. The clock monitor remains disabled, and the device remains in software shutdown until the host software sets EN back to 1.

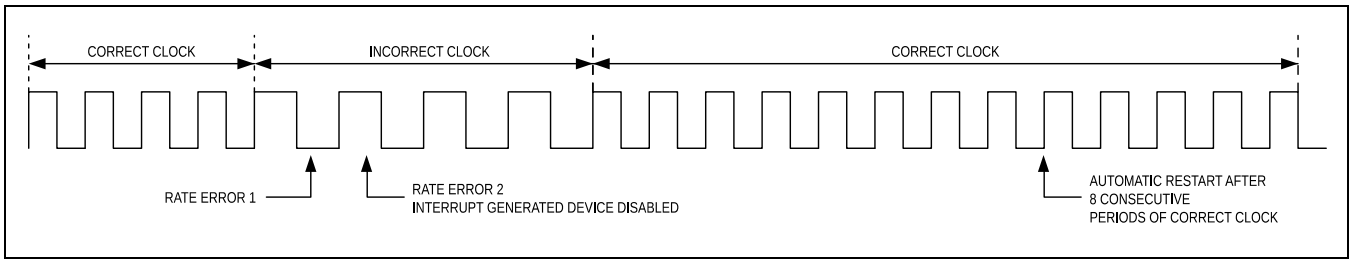


Figure 26. Clock Monitor LRCLK Rate Error Example with CMON_ERRTOL = 0x1

Clock Frame Error Detection

When the clock monitor is enabled, the bit clock (BCLK) to frame clock (LRCLK) ratio is monitored. The clock monitor counts the number of BCLK periods per frame (LRCLK period) and then compares the count to the configured clock ratio (PCM_BSEL). In addition, in I^2S and left-justified modes, the clock monitor verifies the LRCLK duty cycle by checking that the number of BCLK periods per channel is equal. In TDM mode, data transport is synchronized to the active frame clock (LRCLK) edge, so no duty cycle restrictions are enforced.

A frame error is detected in each frame where the monitored clock ratio (and duty cycle in I^2S and left-justified modes) differs from the configured settings. The CMON_BSELTOL bit field sets the number of consecutive frames with frame errors that are required before a clock error interrupt is generated (CLK_ERR_*) and the device is placed on software shutdown.

In automatic mode, the CMON_BSELTOL bit field also sets the number of consecutive frames without frame errors that are required for automatic restart to occur. Once the selected number of consecutive error-free frames are detected, a clock recover interrupt (CLK_RECOVER_*) is generated, and the device automatically exits software shutdown.

In manual mode, no clock recovery interrupts are generated; the clock monitor remains disabled, and the device remains in software shutdown until the host software sets EN back to 1.

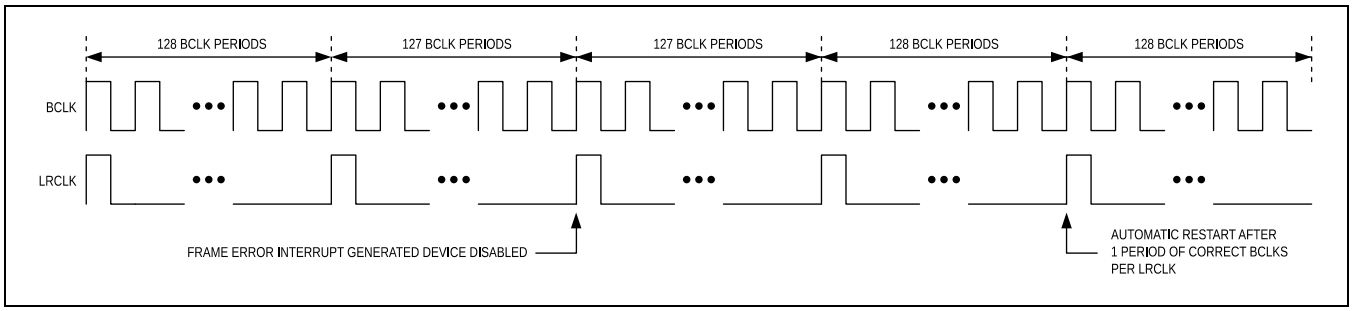


Figure 27. Clock Monitor Framing Error Example in TDM Mode with PCM_BSEL = 0x6 and CMON_BSELTOL = 0x0

RMS Limiter

The MAX98415A/MAX98425A features a Root Mean Square (RMS) Limiter that limits the speaker output signal based on the RMS value of the input signal, thereby allowing the speaker outputs to play the higher dynamic audio signals without compression. The RMS Limiter is enabled and disabled on each amplifier using AMPA_RMS_LIM_EN and AMPB_RMS_LIM_EN bits, and these bits can only be configured when the device is in software shutdown.

The RMS Limiter block requires configuration of the RMS Limiter threshold for each amplifier (AMPA_RMS_LIM_THRESH and AMPB_RMS_LIM_THRESH) to set the threshold level for attack of the limiter. The RMS Limiter thresholds are configurable in steps of 0.25dBFS to cover a range from 0dBFS to -57dBFS. *Table 10* shows input-referred RMS limiter thresholds for DC and sinewave input signals. In addition to setting the RMS thresholds, the RMS Limiter requires setting the time constant of attack and release of the limiter. AMPA_RMS_LIM_TIME_CONST [19:0] and AMPB_RMS_LIM_TIME_CONST [19:0] bitfields set the time constant coefficients for each of the amplifier outputs for the RMS Limiter.

Table 10. RMS Limiter Threshold Decode

REGISTER VALUE	DECODE (ACTUAL RMS THRESHOLD)	DECODE (DC INPUT)	DECODE (SINE-WAVE INPUT)
0x0–0x18	From 0dBFs, in 0.25dBFs steps	RESERVED	RESERVED
0x19	-6.25dBFs	-3.125dBFs	-0.125dBFs
0x1A	-6.5dBFs	-3.25dBFs	-0.25dBFs
..	..	in 0.125dBFs steps	in 0.125dBFs steps
0x20	-8dBFs	-4dBFs	-1dBFs
..	..	in 0.125dBFs steps	in 0.125dBFs steps
0x28	-10dBFs	-4dBFs	-2dBFs
..	..	..	..
0xE4	-57dBFs	-28.5dBFs	-25dBFs
0xE5–0xFF	RESERVED	RESERVED	RESERVED

When the RMS limiter is active on an amplifier output, it sets the corresponding AMPX_RMS_LIM_ACTIVE_BGN_* interrupt bit, whereas when the RMS limiter releases the amplifier output, the device sets the corresponding AMPX_RMS_LIM_ACTIVE_END_* interrupt bit.

Envelope Tracking Control for Speaker Output Supply

The device features an envelope tracking control circuit that adjusts an external DC-DC converter's regulated output level according to the PVDD supply level required by the Class-D amplifier on the device. The envelope tracking control is enabled by the ET_EN bit, and the envelope tracking output signal can be configured on any of the GPIO pins using the GPIOX_SEL bitfield.

The envelope tracking output signal is a Pulse-width modulation (PWM) signal that is inversely proportional to the incoming audio sample and the overall gain of the amplifier. The PWM output is driven by V_{DVDD} supply and operates at 192kHz fixed frequency for the 48kHz sample rate family (176.4kHz for the 44.1kHz sample rate family). The signal requires low-pass filtering and an appropriately matched series resistor before connecting to the FB pin of the external DC-DC converter. The low pass-filtered PWM signal, in combination with a series resistor, raises or lowers the FB pin voltage from its internally regulated level thereby changing the regulated output level (V_{PVDD}) of the DC-DC converter. *Figure 28* shows typical envelope tracker behavior in the presence of an audio signal.

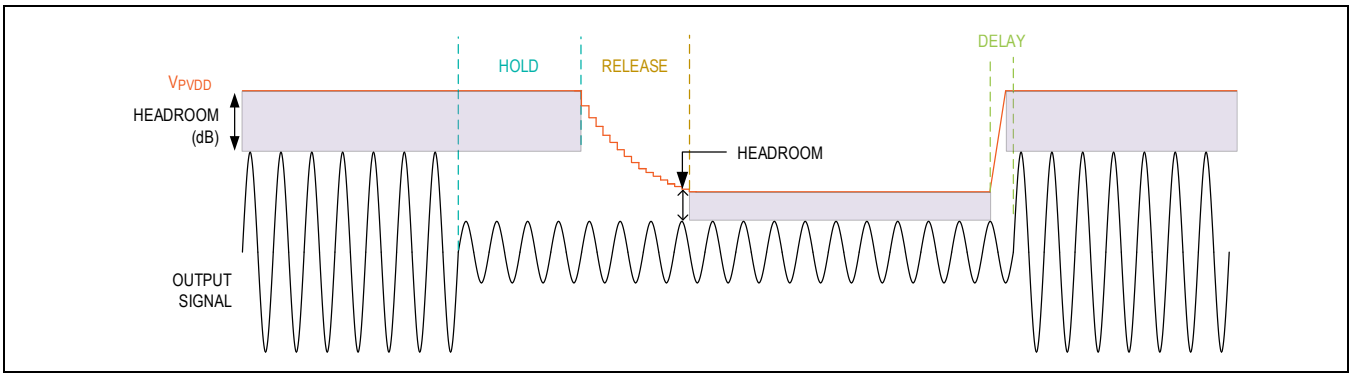


Figure 28. Envelope Tracker Operation

Envelope Tracking Algorithm

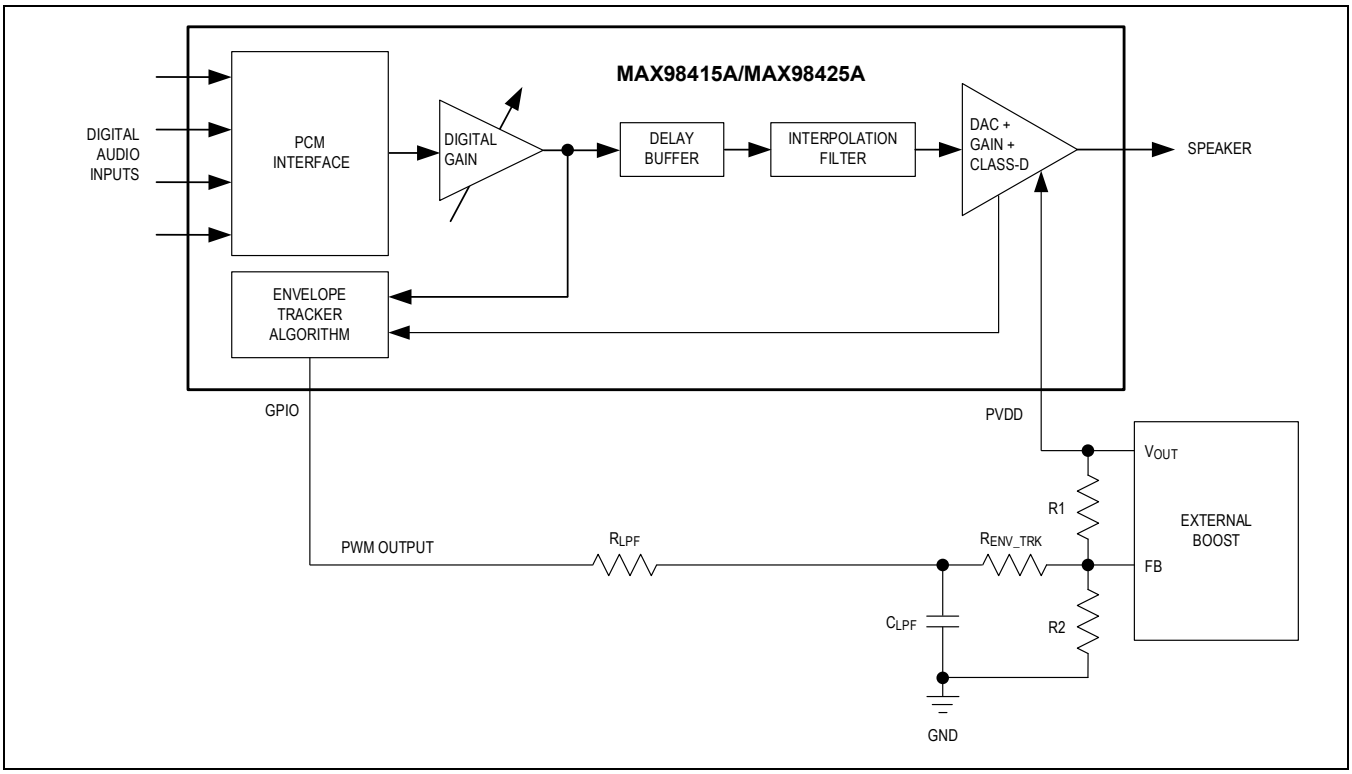


Figure 29. Envelope Tracking Control Block Diagram and External Connections

Figure 29 shows a device block diagram with envelope tracking control and the external components required to interface the envelope tracking output signal to the external DC-DC converter. The resistors R1 and R2 set the regulated output level of the DC-DC converter when there is no PWM output from MAX98415A/MAX98425A and are chosen based on the DC-DC converter's application circuit. The components R_{LPF} and C_{LPF} form a low-pass filter for the envelope tracking PWM output signal. R_{LPF} is chosen such that R_{LPF} << R_{ET} and R_{LPF} can support the drive current selected by the GPIOX_DRV setting. C_{LPF} is chosen such that the low-pass filter frequency is much lower than the PWM frequency (192kHz) of the envelope tracker signal. The value of R_{ET} determines the PWM duty cycle range required to control the external
DC-DC converter is chosen so that the combination of R1, R2, R_{ET}, and V_{FB} can set a valid PWM duty cycle range (from 0 to 100%) to get the desired PVDD supply range from the external converter.

Envelope Tracking Attack

The envelope tracking algorithm is in attack mode when the peak detection circuit determines that the incoming audio sample, along with the gain of the amplifier, exceeds the current PVDD level. The attack begins immediately after the detection is complete, and the algorithm starts decreasing the PWM duty cycle at the rate of 20.883µs/step.

Envelope Tracking Release

At the end of the envelope tracking hold time, the device enters envelope tracking release mode. In this mode, the envelope tracker output starts decreasing the PVDD level until it reaches the target PVDD level based on the PVDD level + Envelope tracking PVDD Headroom level. The release rate is fixed, and the maximum release time is 92.3ms for the PVDD supply to change from 22V to 3V.

Envelope Tracking Hold

When the peak detector circuit determines that incoming audio input has dropped below the threshold of the envelope tracker step, the algorithm enters in a hold state. In this state, the algorithm maintains the current PVDD level until the envelope tracking hold timer expires.

Envelope Tracking Configuration

The envelope tracking algorithm on MAX98415A/MAX98425A requires configuration of PVDD Headroom, Envelope Tracking Levels, PWM Step size, PVDD step size, maximum PWM duty cycle, minimum PVDD level, and playback delay to be setup and valid to be able to control the external DC-DC converter according to PVDD level required by the device.

Envelope Tracking PVDD Headroom

The Envelope Tracking PVDD Headroom allows the algorithm to calculate a threshold below the PVDD level for each envelope tracker step. The Envelope Tracking PVDD Headroom is set by configuring the ET_PVDD_HDRM bitfield.

The PVDD headroom prevents loss of headroom at the output due to resistive losses in the PVDD supply to the speaker load path. The envelope tracker algorithm uses the PVDD level for each envelope tracker step, PVDD headroom, and peak level of incoming audio samples to determine the envelope tracker attack threshold.

Envelope Tracking Hold Time

The envelope tracking hold time is set by configuring the ET_HOLD_TIME bitfield.

Envelope Tracking Levels and Step Size Configuration

A maximum of 16 steps of the PWM signal allows finer control of the external DC-DC converter regulation voltage, thereby improving overall system efficiency. The envelope tracking levels are configured by setting the ET_LEVEL_SEL bitfield.

The envelope tracker level step-size refers to the PWM steps between each level and the resulting PVDD level step, which is based on external components (R_{ET} and V_{FB}) of the system. The step-size in terms of duty cycle is configured by setting the 9-bit ET_LVL_STEPSIZE bitfield which allows the duty cycle to be set from 0% to 50%. The PVDD level step size in terms of voltage is set by ET_PVDD_STEPSIZE bitfield.

Playback Delay for Envelope Tracking

MAX98415A/MAX98425A provides up to 4.0ms of delay buffer to allow external PVDD voltage to update to the new level determined by the PWM control signal and avoid clipping the audio sample at the load. The maximum delay depends on the programmed PCM sample rate. *Table 11* provides the delay step size, maximum programmable code, and the resultant maximum programmable playback delay available for each sample rate.

Table 11. Envelope Tracking Maximum Playback Delay Time

PCM SAMPLE RATE (kHz)	MAXIMUM PROGRAMMABLE DELAY CODE	MAXIMUM PROGRAMMABLE DELAY (ms)
8	0x7F	4.0
11.025	0x7F	4.35
12	0x7F	4.0
16	0x7F	4.0
22.05	0x7F	4.35
24	0x7F	4.0
32	0x60	3.0
44.1	0x40	2.18
48	0x40	2.0
88.2	0x20	1.09
96	0x20	1.0
176.4	0x10	0.544
192	0x10	0.5

Envelope Tracking Maximum PWM Duty Cycle

The PWM maximum duty cycle is set by configuring the ET_MAXDUTY_CYC bitfield. The maximum duty cycle can be set from 0% to 100% and sets the minimum PVDD level (output level) of the external DC-DC converter.

Envelope Tracking Minimum PVDD Voltage

The minimum PVDD voltage is set by configuring the MIN_PVDD_LVL bitfield. The minimum PVDD level, PVDD step size, and number of levels inform the algorithm PVDD level for each envelope tracker step.

Recommended Device Sequencing with Envelope Tracking Control Enabled

The *Device Sequencing* section describes a generally recommended power-up and power-down sequence for MAX98415A/MAX98425A). When Envelope Tracking Control is enabled on the device, it is recommended to follow the device power-up and power-down sequences provided in *Table 12* and *Table 13*, respectively.

Table 12. Power-Up Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Power-Up Core Supplies	Power the PVDD, VBAT, DVDD, and AVDD supplies above their UVLO thresholds. Enable the external boost before exiting the hardware shutdown state on the device.
2	Exit Hardware Shutdown State	Assert the hardware reset input ($\overline{RESET}$) to a logic high level. If ($\overline{RESET}$) is tied to the DVDD supply, this step is combined with step 1.
3	Enter Software Shutdown State	The device finishes the transition and enters the software shutdown state after the release from reset time ($t_{I^2C\_READY}$) elapses.
4	Program the Device Registers/Enable the External Clocks	The I^2C interface is active, and all registers can be freely configured. Assign appropriate GPIO pin for envelope tracking function. Start both external clocks before exiting the software shutdown state.
5	Exit Software Shutdown State	If volume ramping is disabled, the input audio data should be silent. Set the global enable to a logic high (EN = 1).
6	Enter the Active State	The device enters the active state after the turn-on time (t_{ON}) elapses.
7	Active State/Audio Playback	Dynamic bits (and those restricted to disabled blocks) can be programmed. The device is capable of audio playback in the active state.

Table 13. Power-Down Sequence

STEP	ACTION	DETAILED DESCRIPTION
1	Exit the Active State and Disable the Envelope Tracking Function	If volume ramping is disabled, the input audio data should be silent. Set the global enable bit to a logic low (EN = 0) followed immediately by disabling the envelope tracking function on the device (ET_EN = 0) to avoid overshoot of the external boost output.
2	Enter Software Shutdown State	The device enters a software shutdown state after the turn-off time (t_{OFF}) elapses.
3	Reprogram Device Registers/Disable the External Clocks	The device is fully programmable and can idle in the software shutdown state. The external clocks and the AVDD, PVDD, and VBAT supplies can be disabled. To return to the active state, resume the power-up sequence from step 4.
4	Enter Hardware Shutdown State	For full hardware shutdown, disable the external clocks first. Assert the reset input ($\overline{RESET}$) to ground or power down the DVDD.

Speaker Monitor

The speaker monitor is a circuit that is designed to protect the speaker against amplifier signals that could damage it. The speaker monitor is enabled by default and can be disabled by setting the SPKMON_EN bit to zero. The circuit monitors the amplifier's PWM signal and shuts down the amplifier output when the DC signal goes above a programmed speaker monitor threshold (set by SPKMON_THRESH). Additionally, the device also generates an INT_SPKMON_ERR interrupt. The speaker monitor accuracy is typically less than 5% but varies with speaker load impedance. It is recommended to set a speaker monitor threshold based on the actual load (DC) of the speaker.

For the speaker monitor to operate, PCM clocks must be available.

Thermal Protection

The MAX98415A/MAX98425A has two measurement ADC thermal channels, one for each amplifier, to monitor the die temperature. When the device is active, the measurement ADC thermal channels are automatically enabled, and they

monitor the die temperature to ensure that the device does not exceed the configured thermal thresholds. Interrupt registers are provided so that the device can notify the host when the die temperature crosses either the thermal warning or thermal-shutdown threshold, or when thermal foldback starts and stops. Each measurement ADC thermal channel has its own interrupts to indicate which amplifier output causes dissipation on the die to exceed the programmed threshold.

Thermal Warning and Thermal Shutdown Configuration

The device features two thermal-warning thresholds. The thermal-warning thresholds are configured by THERMWARN1_THRESH[6:0], and THERMWARN2_THRESH[6:0] bit fields, and the thermal shutdown threshold is configured by the THERMSHDN_THRESH[5:0] bit field. The thermal-warning2 threshold should always be set to a temperature higher than or equal to thermal-warning1 temperature. Additionally, the thermal-warning2 threshold temperature should never be configured higher than the thermal shutdown threshold temperature minus hysteresis. When the die temperature is decreasing, hysteresis is applied to thermal-shutdown, thermal-warning1, and thermal-warning2 thresholds. The temperature hysteresis is configured with the THERM_HYST bit field. Thermal-warning1, thermal-warning2, and thermal shutdown thresholds are compared to the maximum of the die temperature reported by each of the measurement ADC thermal channels.

Thermal Shutdown Recovery Configuration

The device thermal-shutdown recovery behavior is determined by the state of the THERM_AUTORESTART_EN bit. When the THERM_AUTORESTART_EN bit is set to 0, the thermal shutdown recovery is in manual mode. In manual mode, when the highest temperature between the measurements from the two measurement ADC thermal channels exceeds the thermal-shutdown threshold, the device generates appropriate interrupts, and both amplifier outputs are automatically disabled. There are separate thermal-shutdown interrupts available for each measurement ADC thermal channel to indicate which measurement ADC channel resulted in a thermal-shutdown event.

When the temperature on both measurement ADC thermal channels drops below the thermal-shutdown threshold minus the hysteresis and the thermal-warning2 threshold minus the hysteresis, the appropriate interrupts are generated to notify the host. In addition, once the die temperature drops below the thermal-warning2 threshold minus the hysteresis, the device is placed into software shutdown (EN is set to 0) and remains in that state until the host manually re-enables the device.

When the THERM_AUTORESTART_EN bit is set to 1, the thermal shutdown recovery is in automatic mode. In automatic mode, when the temperature, measured by any of the measurement ADC thermal channels, exceeds the thermal-shutdown threshold, the device generates appropriate interrupts, and both the amplifiers are automatically disabled. When the temperature on both measurement ADC thermal channels drops below the thermal-shutdown threshold minus the hysteresis, an interrupt is generated, but the amplifier remains disabled. When the temperature on both measurement ADC thermal channels drops below the thermal-warning2 threshold minus the hysteresis, another set of interrupts is generated, and (unlike manual mode) both the amplifier outputs are then automatically re-enabled.

Thermal Foldback

The device features a thermal foldback to allow for a smoother audio response to high-temperature events. Thermal foldback is enabled by setting the THERMFB_EN bit to 1. The device provides two thermal-warning thresholds that are configured by the THERMWARN1_THRESH[6:0] and THERMWARN2_THRESH[6:0] bit fields. They should be set such that the thermal-warning2 threshold temperature is higher than or equal to the thermal-warning1 threshold temperature. Additionally, the thermal-warning2 threshold temperature should never be configured higher than the thermal shutdown threshold temperature minus hysteresis.

Once enabled, thermal foldback begins when the die temperature measured by the Amp A temperature monitor or Amp B temperature monitor exceeds the configured thermal-warning1 threshold. Interrupts are generated by each of the amplifier temperature monitors (AMP*_THERMFB_BGN_* and AMP*_THERMWARN1_BGN_*), and attenuation is applied to both speaker amplifier paths (in Stereo Mode) based on the highest temperature measured by the temperature monitors. The slope of the thermal foldback attenuation is programmed with the THERMFB_SLOPE1 bit field.

If the die temperature continues to increase and exceeds the configured thermal-warning2 threshold, the appropriate amplifier temperature monitor generates an interrupt (AMP*_THERMWARN2_BGN_*) and attenuation continues to be applied to both speaker amplifier paths. The slope of the attenuation applied to the speaker amplifier paths is programmed with the THERMFB_SLOPE2 bit field. As the die temperature increases, the level of attenuation also increases proportionally up to a maximum level of -12dB (unless the thermal shutdown threshold is exceeded first). When thermal foldback is active, the attack time for a gain change can be a maximum of two samples. Additionally, there is a sample delay in the signal path attenuation due to the group delay of the amplifier.

When the die temperature starts to decrease, and the measured temperature from both temperature monitors drops below the thermal-warning2 threshold minus the programmed hysteresis level and remains there for longer than the programmed hold time (set with the THERMFB_HOLD bit field), the attenuation starts to release and an interrupt (AMP*_THERMWARN2_END_*) is generated. If the die temperature continues to reduce and the measured temperature from both temperature monitors drops below the thermalwarning1 threshold temperature minus the programmed hysteresis level, thermal foldback ends and interrupts (AMP*_THERMFB_END_* and AMP*_THERMWARN1_END_*) are generated. The attenuation release rate (for decreasing temperature) is programmable and configured with the THERMFB_RLS bit field.

Tone Generator

The device includes a tone generator which is enabled using the TONE_EN bit field and replaces the PCM interface as the input source to the speaker playback path. When the tone generator is enabled, both it and the speaker playback path operate without the need for any external clocks.

The tone generator output is configured to generate sine wave or DC tones (using the TONE_CONFIG bit field).

The tone generator can create sine waves with either a 1kHz fixed frequency or a variable sample rate-dependent frequency. When a sample rate-based sinewave output is selected, the tone generator output frequency is set by the playback sample rate setting (PCM_SR) divided by the selected ratio (as set by TONE_CONFIG). For the playback sample rate of 44.1kHz and its multiples, the tone generator output frequency can vary by up to 9%. The tone generator supports all available sample rate settings (PCM_SR). The amplitude of the output sine wave relative to full-scale is selected with the TONE_AMPLITUDE bit field.

The tone generator can output either a fixed or a programmable DC output level (as set by TONE_CONFIG). Fixed DC output levels of zero code, positive half-scale, and negative half-scale are provided for quick configuration. If the programmable DC output level is selected (TONE_CONFIG), the DC level is configured as a signed two's complement value with the TONE_DC bit field.

Pink Noise Generator

The device includes a pink noise generator, which is enabled using the PINK_NOISE_EN bit field and replaces the PCM interface as the input source to the speaker playback path. The pink noise generator and the tone generator cannot be enabled at the same time. When the pink noise generator is enabled, both it and the speaker playback path operate without the need for any external clocks. The output level of the generator is fixed, so the amplifier gain and speaker volume must be used to adjust the level.

Interchip Communication

The device features an interchip communication (ICC) interface that uses a shared data bus to facilitate synchronized speaker amplifier path attenuation adjustments across groups of devices. Depending on the configuration, the ICC interface can synchronize brownout-prevention engine (BPE), DHT, and thermal foldback. Each device receives the data of the other grouped devices and reacts accordingly.

ICC Operation and Data Format

The bidirectional ICC bus is used to synchronize the responses of grouped devices. To create the ICC bus, the ICC interface pins of each device are externally connected (whether or not the devices are in the same group). The ICC bus operates with the same clock sources and data format configuration as the PCM interface data input (DIN) and can support a maximum of 16 channels. For a given valid PCM interface configuration, the number of available ICC data channels per frame is calculated as follows (based on the PCM_CHANSZ, PCM_BSEL, and PCM_FORMAT settings):

Number of Available Data Input Channels = BCLK to LRCLK Ratio / Channel Length

The ICC interface is disabled when both the ICC data transmit output (ICC_TX_EN) and the ICC data link (ICC_LINK_EN) are disabled. To enable the ICC interface, both ICC_TX_EN and ICC_LINK_EN must be set to 1. It is invalid to set these controls to different values, and both must always be set to the same state (either enabled or disabled). Once the ICC link and data transmit are enabled, the ICC data output channel is assigned with the ICC_TX_DEST bit field. The ICC pin is Hi-Z during all other data channels and can be configured (with the ICC_RX_CHn_EN bits) to accept data from the output data channels of grouped devices.

The transmitted ICC data is always the same size as the configured PCM data input word size (set by PCM_CHANSZ). When a 16-bit data word is selected, the ICC data word is not long enough to synchronize BPE, DHT, and thermal foldback. In this case, the ICC_DATA_SEL bit is used to choose whether the DHT function or thermal foldback function

is synchronized in addition to the BPE state. When a 24-bit or 32-bit data word size is selected, ICC can synchronize BPE, DHT, and thermal foldback across a given group. In these cases, the ICC_DATA_SEL bit has no effect. Active ICC data channels always contain ICC data words followed by zero padding bits up to the ICC data channel length (which is equal to PCM input data channel length). If BPE, DHT, or thermal foldback is disabled for any given group, then the transmitted ICC data for the disabled function(s) is always zero code.

Multiamplifier Grouping

The ICC interface allows multiple devices to be grouped so that BPE, DHT, and thermal foldback behavior can be synchronized. The receive channel enables (ICC_RX_CHn_EN) are used to define groups. A given device monitors all selected channels (when ICC_RX_CHn_EN = 1, and n denotes the channel number) on the ICC data bus. The configured set of receive channels must also include the assigned transmit channel (as set by ICC_TX_DEST) for any given device. Each device in a given group must have identical settings for all ICC receive channel enables (ICC_RX_CHn_EN). Furthermore, all devices in the same group must have identical DHT, thermal protection, and thermal foldback settings to achieve a synchronized response across the group. The behavior of a group as a whole is undefined if any given device in a group has different settings.

The ICC bus can support a maximum of 16 data channels. The minimum size of a group is two devices, and as a result, the maximum number of concurrent groups on a single ICC bus is eight. A group can contain as many as 16 devices, but then only a single group is possible on a single ICC bus.

ICC Multi-Group Example

Consider a system design that includes four devices that require DHT synchronization, and that two distinct groups of two devices each (with different DHT settings) share a single ICC bus. The PCM interface (and thus the ICC bus) is configured in TDM mode 1 with four 16-bit data channels available. One possible configuration (among many) is to assign devices 1 and 3 to the first group (denoted group A) and to assign devices 2 and 4 to the second group (denoted group B).

To configure group A, both devices 1 and 3 are set to monitor channels 0 and 2 by programming ICC_RX_CH0_EN = 1 and ICC_RX_CH2_EN = 1 on both devices (all other ICC receive bit fields are 0). Device 1 transmits on channel 0 (ICC_TX_DEST = 0x0) and device 3 transmits on channel 2 (ICC_TX_DEST = 0x2).

To configure group B, both devices 2 and 4 are set to monitor channels 1 and 3 by programming ICC_RX_CH1_EN = 1 and ICC_RX_CH3_EN = 1 on both devices (all other ICC receive bit fields are 0). Device 2 transmits on channel 1 (ICC_TX_DEST= 0x1), and device 4 transmits on channel 3 (ICC_TX_DEST = 0x3).

Since the ICC channel length and data word size are limited to 16 bits, the ICC_DATA_SEL bit field in all four devices, must be set to 0 to select DHT target attenuation synchronization. Finally, on all four devices set ICC_LINK_EN = 1 and ICC_TX_EN = 1 to enable the ICC interfaces.

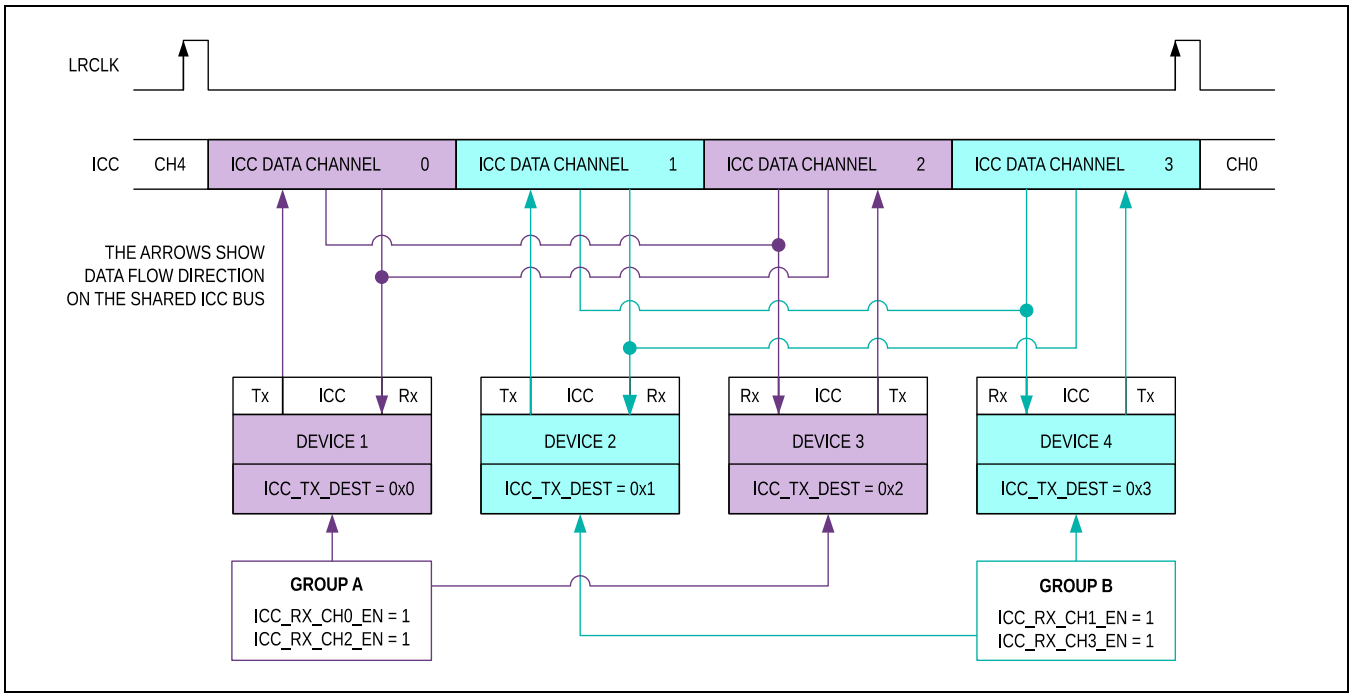


Figure 30. ICC Multi-Group Example with 2 Groups and 4 Total Devices

I²C Serial Interface

The I²C serial control interface is activated when the device detects a valid I²C start condition at the I2C1 and I2C2 pins. The I2C1 and I2C2 pins can each act as either SCL or SDA, respectively, and the start condition configures the device address and state of each pin. After the first I²C transaction, the I²C interface configuration i.e., I2C1, I2C2, and ADDR pins connections should not change.

Peripheral Address

The peripheral address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The seven most significant bits are programmable through the ADDR connection, and the required I2C1 and I2C2 connections for each address as shown in *Table 14*. The device does not communicate if ADDR is floating. Setting the read/write bit to 1 configures the device for read mode. Setting the read/write bit to 0 configures the device for write mode. The address is the first byte of information sent to the IC after the START condition.

In addition to the address set by the ADDR input, the device features a configurable seven-bit group write address (GRP_WR_ADDR[6:0]) available for cases where synchronized write transactions are needed across multiple devices. The group write address is enabled by setting the GRP_WR_EN = 1. When enabled, the device (or a group of devices) accepts write transactions through the group address regardless of the ADDR connection. Group read transactions are not supported (and should not be attempted to avoid data collisions).

Table 14. I²C Peripheral Address

I2C1	I2C2	CONDITIONS	I²C PERIPHERAL ADDRESS (BINARY)	I²C WRITE ADDRESS (BINARY)	I²C READ ADDRESS (BINARY)
SCL	SDA	ADDR connected to VBAT/DVDD	0111000x	01110000	01110001
SCL	SDA	ADDR connected to GND	0111001x	01110010	01110011
SCL	SDA	ADDR connected to SDA	0111010x	01110100	01110101
SCL	SDA	ADDR connected to SCL	0111011x	01110110	01110111

I2C1	I2C2	CONDITIONS	I²C PERIPHERAL ADDRESS (BINARY)	I²C WRITE ADDRESS (BINARY)	I²C READ ADDRESS (BINARY)
SCL	SDA	GRP_WR_EN=1 GRP_WR_ADDR = xxxxxx0	Same as GRP_WR_ADDR	Same as GRP_WR_ADDR	N/A
SDA	SCL	ADDR connected to VBAT/DVDD	0111100x	01111000	01111001
SDA	SCL	ADDR connected to GND	0111101x	01111010	01111011
SDA	SCL	ADDR connected to SDA	0111110x	01111100	01111101
SDA	SCL	ADDR connected to SCL	0111111x	01111110	01111111
SDA	SCL	GRP_WR_EN = 1 GRP_WR_ADDR = xxxxxx0	Same as GRP_WR_ADDR	Same as GRP_WR_ADDR	N/A

The IC features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the IC and the I²C manager at clock rates up to 1MHz. *Figure 31* shows the 2-wire interface timing diagram. The manager generates SCL and initiates data transfer on the bus. The I²C manager writes data to the IC by transmitting the proper peripheral address followed by two register address bytes (the most significant byte first) and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the IC is 8 bits long and is followed by an acknowledge clock pulse. A controller reading data from the IC transmits the proper peripheral address followed by a series of nine SCL pulses. The IC transmits data on SDA in sync with the controller-generated SCL pulses. The controller acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not-acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pull-up resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pull-up resistor, typically greater than 500Ω, is required on SCL if there are multiple controllers on the bus, or if the single controller has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the IC from high voltage spikes on the bus lines and minimize crosstalk and undershooting of the bus signals.

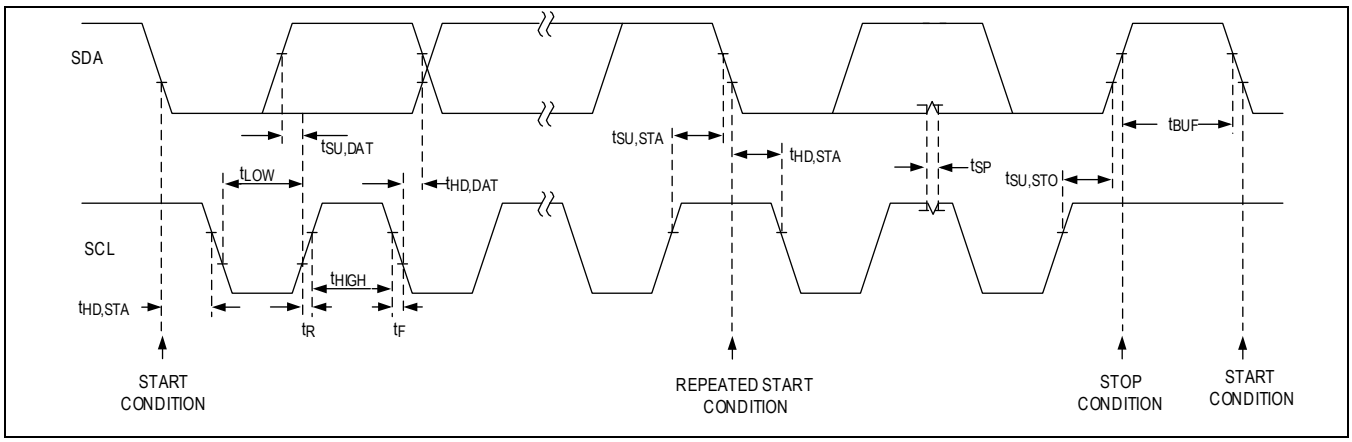


Figure 31. I²C Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A manager initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the manager signals the beginning of a transmission to the IC. The manager terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

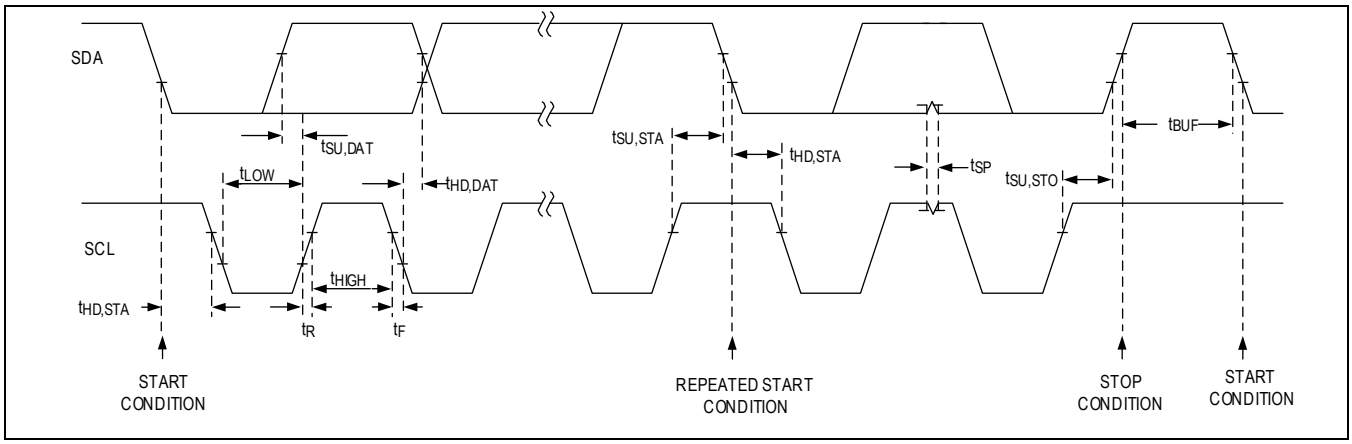


Figure 32. I^2C START, STOP, and REPEATED START Conditions

Early STOP Conditions

The IC recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the IC uses to handshake receipt each byte of data when in write mode. The IC pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The I2C manager pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the IC is in read mode. An acknowledge bit is sent by the I2C manager after each read byte to allow data transfer to continue. A not acknowledge (NACK) is sent when the I2C manager reads the final byte of data from the IC, followed by a STOP condition.

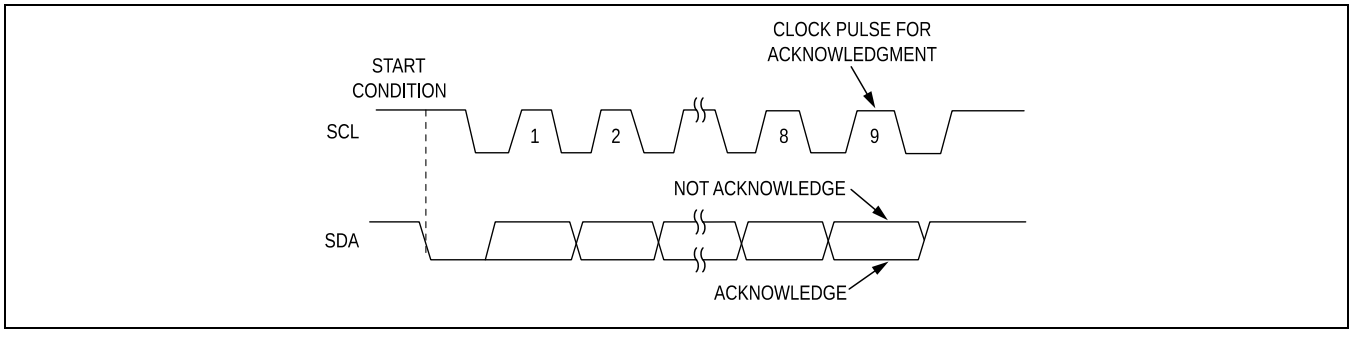


Figure 33. I^2C Acknowledge

Write Data Format

A write to the IC includes the transmission of a START condition, the peripheral address with the R/$\overline{W}$ bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

The peripheral address with the R/$\overline{W}$ bit set to 0 indicates that the manager intends to write data to the IC. The IC acknowledges receipt of the address byte during the I²C manager-generated 9th SCL pulse.

The second and third bytes transmitted by the manager are configured by the IC's internal register address pointer. The pointer tells the IC where to write the next byte of data. An acknowledge pulse is sent by the IC upon receipt of the address pointer data.

The third byte sent to the IC contains the data that is written to the chosen register. An acknowledge pulse from the IC signals receipt of the data byte. The address pointer auto-increments to the next register address after each received data byte. This auto-increment feature allows the manager to write to sequential registers within one continuous frame. The manager signals the end of transmission by issuing a STOP condition.

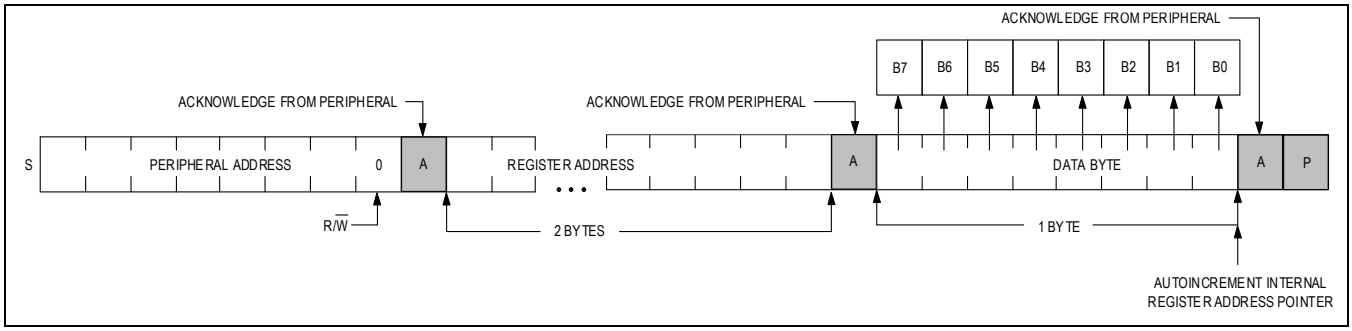


Figure 34. I²C Writing One Byte of Data to the Peripheral

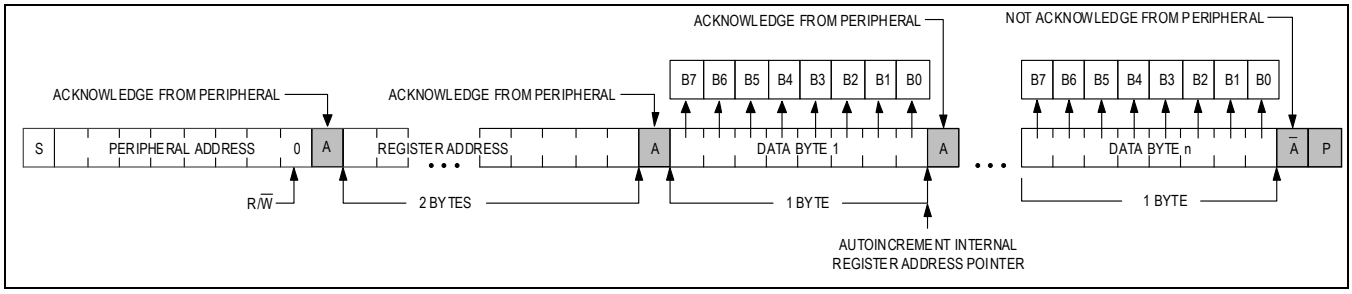


Figure 35. I²C Writing n-Bytes of Data to the Peripheral

Read Data Format

Initiate a read operation by sending the peripheral address with the R/$\overline{W}$ bit set to 1. The IC acknowledges receipt of its peripheral address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x2000. The first byte transmitted from the IC is the content of register 0x2000. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x2000.

The I²C register address pointer must be preset to a specific target register address before a read command is issued. The manager presets the peripheral register address pointer by first sending the device's peripheral address with the R/$\overline{W}$ bit set to 0 (write command), followed by two commands containing the target register address for the address pointer.

A REPEATED START condition is then sent, followed by the read command (peripheral address with the R/$\overline{W}$ bit set to 1). This begins a read command with the internal register address pointer set to the target register address. The first byte transmitted from the device contains the contents of the register to which the address pointer is set. Transmitted data is valid on the rising edge of SCL. The manager acknowledges (ACK) receipt of each read byte during the acknowledge

clock pulse. The address pointer then auto-increments after each acknowledged read data byte. This auto-increment feature allows multiple registers to be read sequentially within one continuous frame.

The manager must issue an acknowledge (ACK) for all correctly received bytes except the last byte. To terminate the read operation, the final byte must be followed by a not-acknowledge (NACK) from the manager and then a STOP condition. A not-acknowledge (NACK) followed by a STOP condition can be issued after any number of read data bytes.

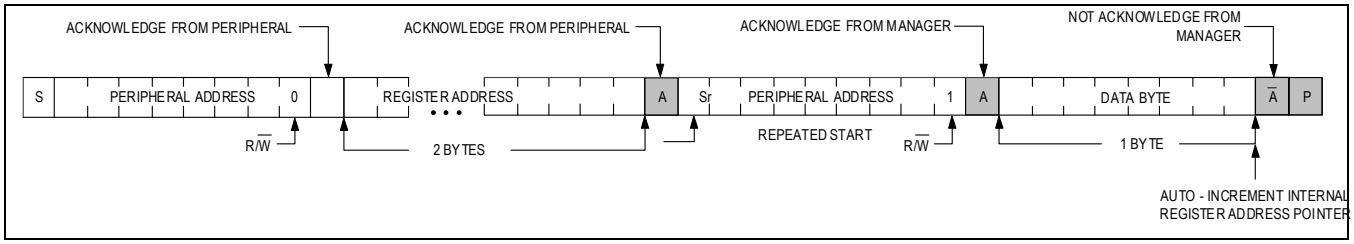


Figure 36. I²C Reading One Byte of Data from the Peripheral

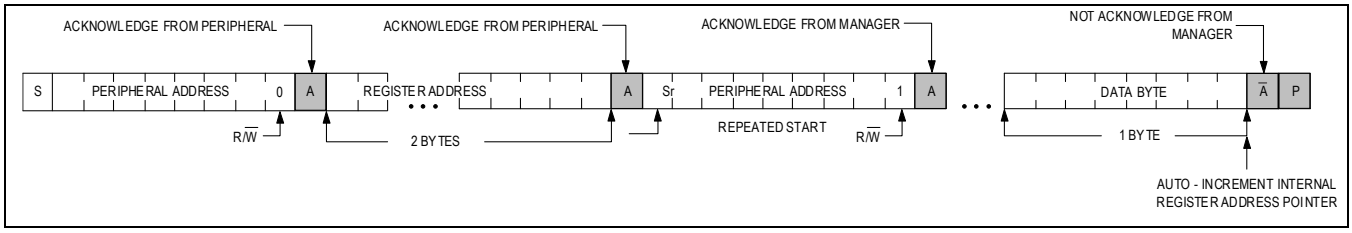


Figure 37. I²C Reading n-Bytes of Data from the Peripheral

I²C Register Map

Control Bit Field Types and Write Access Restrictions

The device control bit fields fall into one of three basic types: read, write, or read and write. There are no read restrictions, and any read-enabled bit field can be read back anytime the I²C control interface is active. However, there are write restrictions, and every write-enabled bit field falls into one of two write access subtypes.

The first write access subtype is dynamic. Dynamic bit fields effectively have no write access restrictions and can be safely changed (written) in any device state where the I²C control interface is active. The second-bit field access subtype is restricted. Restricted bit fields should only be changed (written) when the related functional block (as shown in *Table 15*) is powered down.

If the write access is restricted to the global enable (restrictions EN and ENL), then the restricted bit field should only be changed (written) when the device is in software shutdown. As a form of system protection, write access to some critical global enable restricted bit fields (ENL) is locked out by the hardware when the device is not in the software-shutdown state. Attempting to change (write to) these locked restricted bit fields when the device is not in the software-shutdown state has no effect (read access is still allowed).

The bit field type and write access subtype are provided for every bit field in the detailed register description tables. For all bit fields with the restricted subtype, the dependency is also denoted in the "RES" column.

Table 15 provides a detailed description of all device register types, access subtypes, and restriction dependencies used by this device. The write access restrictions describe the specific device condition(s) that should be met (and the corresponding bit field settings) before the system attempts to change (write to) bit fields with that restriction type.

Table 15. Control Bit Types and Write Access Restrictions

BIT FIELD TYPE	WRITE ACCESS	WRITE ACCESS RESTRICTIONS		"RES" SYMBOL
		DESCRIPTION	CONDITION	
Read	Read Only	—	—	**—**
Write or Read/Write	Dynamic	—	—	**—**
	Restricted	Device in Software Shutdown	EN = 0	**EN**
		Write Access Locked Out by Hardware Unless the Device in Software Shutdown	EN = 0	**ENL**
		Speaker Amplifier Output and Feedback Disabled	SPK_AMPA_EN = 0, SPK_AMPA_EN = 0, SPK_AMPA_FB_EN = 0 SPK_AMPB_FB_EN = 0	**SPK**
		Voltage Feedback and Current Sense ADC Disabled	IVF_AMPA_V_EN = 0, IVF_AMPB_V_EN = 0 and IVF_AMPA_I_EN = 0, IVF_AMPB_I_EN = 0	**IVS**
		Thermal Foldback Disabled	THERMFB_EN = 0	**TFB**
		Noise Gate Disabled	NOISEGATE_EN = 0	**NG**
		Dynamic-Headroom Tracking Disabled	DHT_EN = 0	**DHT**
		Brownout-Prevention Engine Disabled	BPE_EN = 0	**BPE**
		PCM Interface Data Input and Output Disabled	PCM_RX_EN = 0 and PCM_TX_EN = 0	**PCM**
		PCM Data Output Disabled	PCM_TX_EN = 0	**TXEN**
		IRQ Bus Output Disabled	IRQ_EN = 0	**IRQ**
		Interchip Communication (ICC) Interface Disabled	ICC_LINK_EN = 0 and ICC_TX_EN = 0	**ICC**

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
Reset									
0x1000	Software Reset[7:0]	–	–	–	–	–	–	–	RST
Interrupt Raw Bits									
0x2000	Supply and OTP Interrupts Raw[7:0]	–	–	PVDD_UVLO_SHDN_RAW	VBAT_UVLO_SHDN_RAW	–	AVDD_UVLO_RAW	DVDD_UVLO_RAW	OTP_FAIL_RAW
0x2001	Power Up and Down Interrupts Raw[7:0]	PWRDN_DONE_RAW	–	–	–	–	–	AMPB_PWRUP_DONE_RAW	AMPA_PWRUP_DONE_RAW
0x2003	Clock and Data Interrupts Raw[7:0]	–	–	–	–	CLK_RECOVER_RAW	–	INT_CLK_ERR_RAW	CLK_ERR_RAW
0x2005	Amplifier Output Fault Interrupts Raw[7:0]	–	–	AMPB_INT_SPKMON_ERR_RAW	AMPA_INT_SPKMON_ERR_RAW	–	–	AMPB_SPK_OVC_RAW	AMPA_SPK_OVC_RAW
0x2006	Amp A Thermal Warning Interrupts Raw[7:0]	AMPA_THERMSHDN_END_RAW	AMPA_THERMSHDN_BGN_RAW	AMPA_THERMFB_END_RAW	AMPA_THERMFB_BGN_RAW	AMPA_THERMWARN2_END_RAW	AMPA_THERMWARN2_BGN_RAW	AMPA_THERMWARN1_END_RAW	AMPA_THERMWARN1_BGN_RAW
0x2007	Amp B Thermal Warning Interrupts Raw[7:0]	AMPB_THERMSHDN_END_RAW	AMPB_THERMSHDN_BGN_RAW	AMPB_THERMFB_END_RAW	AMPB_THERMFB_BGN_RAW	AMPB_THERMWARN2_END_RAW	AMPB_THERMWARN2_BGN_RAW	AMPB_THERMWARN1_END_RAW	AMPB_THERMWARN1_BGN_RAW
0x200A	BPE and DHT Interrupts Raw[7:0]	BPE_L0_RAW	BPE_LEVEL_RAW	BPE_ACTIVE_END_RAW	BPE_ACTIVE_BGN_RAW	–	–	DHT_ACTIVE_END_RAW	DHT_ACTIVE_BGN_RAW
0x200B	RMS Limiter Interrupts Raw[7:0]	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_RAW	AMPB_RMS_LIM_ACTIVE_BGN_RAW	AMPA_RMS_LIM_ACTIVE_END_RAW	AMPA_RMS_LIM_ACTIVE_BGN_RAW
0x200E	Miscellaneous Interrupts Raw[7:0]	EXT_MUTE_RAW	–	–	–	–	–	AMPB_SPK_CLIP_RAW	AMPA_SPK_CLIP_RAW
Interrupts State Bits									
0x2010	Supply and OTP Interrupts State[7:0]	–	–	PVDD_UVLO_SHDN_STATE	VBAT_UVLO_SHDN_STATE	–	AVDD_UVLO_STATE	DVDD_UVLO_STATE	OTP_FAIL_STATE
0x2011	Power Up and Down Interrupts State[7:0]	PWRDN_DONE_STATE	–	–	–	–	–	AMPB_PWRUP_DONE_STATE	AMPA_PWRUP_DONE_STATE
0x2013	Clock and Data Interrupts State[7:0]	–	–	–	–	CLK_RECOVER_STATE	–	INT_CLK_ERR_STATE	CLK_ERR_STATE
0x2015	Amplifier Output Fault Interrupts State[7:0]	–	–	AMPB_INT_SPKMON_ERR_STATE	AMPA_INT_SPKMON_ERR_STATE	–	–	AMPB_SPK_OVC_STATE	AMPA_SPK_OVC_STATE

ADDRESS	NAME	MSB							LSB
0x2016	Amp A Thermal Warning Interrupts State[7:0]	AMPA_THERMSHDN_END_STATE	AMPA_THERMSHDN_BGN_STATE	AMPA_THERMFB_END_STATE	AMPA_THERMFB_BGN_STATE	AMPA_THERMWARN2_END_STATE	AMPA_THERMWARN2_BGN_STATE	AMPA_THERMWARN1_END_STATE	AMPA_THERMWARN1_BGN_STATE
0x2017	Amp B Thermal Warning Interrupts State[7:0]	AMPB_THERMSHDN_END_STATE	AMPB_THERMSHDN_BGN_STATE	AMPB_THERMFB_END_STATE	AMPB_THERMFB_BGN_STATE	AMPB_THERMWARN2_END_STATE	AMPB_THERMWARN2_BGN_STATE	AMPB_THERMWARN1_END_STATE	AMPB_THERMWARN1_BGN_STATE
0x201A	BPE and DHT Interrupts State[7:0]	BPE_L0_STATE	BPE_LEVEL_STATE	BPE_ACTIVE_END_STATE	BPE_ACTIVE_BGN_STATE	–	–	DHT_ACTIVE_END_STATE	DHT_ACTIVE_BGN_STATE
0x201B	RMS Limiter Interrupts State[7:0]	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_STATE	AMPB_RMS_LIM_ACTIVE_BGN_STATE	AMPA_RMS_LIM_ACTIVE_END_STATE	AMPA_RMS_LIM_ACTIVE_BGN_STATE
0x201E	Miscellaneous Interrupts State[7:0]	EXT_MUTE_STATE	–	–	–	–	–	AMPB_SPK_CLIP_STATE	AMPA_SPK_CLIP_STATE
Interrupt Flag Registers									
0x2020	Supply and OTP Interrupts Flag[7:0]	–	–	PVDD_UVLO_SHDN_FLAG	VBAT_UVLO_SHDN_FLAG	–	AVDD_UVLO_FLAG	DVDD_UVLO_FLAG	OTP_FAIL_FLAG
0x2021	Power Up and Down Interrupts Flag[7:0]	PWRDN_DONE_FLAG	–	–	–	–	–	AMPB_PWRUP_DONE_FLAG	AMPA_PWRUP_DONE_FLAG
0x2023	Clock and Data Interrupts Flag[7:0]	–	–	–	–	CLK_RECOVER_FLAG	–	INT_CLK_ERR_FLAG	CLK_ERR_FLAG
0x2025	Amplifier Output Fault Interrupts Flag[7:0]	–	–	AMPB_INT_SPKMON_ERR_FLAG	AMPA_INT_SPKMON_ERR_FLAG	–	–	AMPB_SPK_OVC_FLAG	AMPA_SPK_OVC_FLAG
0x2026	Amp A Thermal Interrupts Flag[7:0]	AMPA_THERMSHDN_END_FLAG	AMPA_THERMSHDN_BGN_FLAG	AMPA_THERMFB_END_FLAG	AMPA_THERMFB_BGN_FLAG	AMPA_THERMWARN2_END_FLAG	AMPA_THERMWARN2_BGN_FLAG	AMPA_THERMWARN1_END_FLAG	AMPA_THERMWARN1_BGN_FLAG
0x2027	Amp B Thermal Interrupts Flag[7:0]	AMPB_THERMSHDN_END_FLAG	AMPB_THERMSHDN_BGN_FLAG	AMPB_THERMFB_END_FLAG	AMPB_THERMFB_BGN_FLAG	AMPB_THERMWARN2_END_FLAG	AMPB_THERMWARN2_BGN_FLAG	AMPB_THERMWARN1_END_FLAG	AMPB_THERMWARN1_BGN_FLAG
0x202A	BPE and DHT Interrupts Flag[7:0]	BPE_L0_FLAG	BPE_LEVEL_FLAG	BPE_ACTIVE_END_FLAG	BPE_ACTIVE_BGN_FLAG	–	–	DHT_ACTIVE_END_FLAG	DHT_ACTIVE_BGN_FLAG
0x202B	RMS Limiter Interrupts Flag[7:0]	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_FLAG	AMPB_RMS_LIM_ACTIVE_BGN_FLAG	AMPA_RMS_LIM_ACTIVE_END_FLAG	AMPA_RMS_LIM_ACTIVE_BGN_FLAG
0x202E	Miscellaneous Device Interrupts Flag[7:0]	EXT_MUTE_FLAG	–	–	–	–	–	AMPB_SPK_CLIP_FLAG	AMPA_SPK_CLIP_FLAG
Interrupt Enable									
0x2030	Supply and OTP Interrupts Enable[7:0]	–	–	PVDD_UVLO_SHDN_EN	VBAT_UVLO_SHDN_EN	–	AVDD_UVLO_EN	DVDD_UVLO_EN	OTP_FAIL_EN

ADDRESS	NAME	MSB							LSB
0x2031	Power Up and Down Interrupts Enable[7:0]	PWRDN_DONE_EN	–	–	–	–	–	AMPB_PWRUP_DONE_EN	AMPA_PWRUP_DONE_EN
0x2033	Clock and Data Interrupts Enable[7:0]	–	–	–	–	CLK_RECOVER_EN	–	INT_CLK_ERR_EN	CLK_ERR_EN
0x2035	Amplifier Output Fault Interrupts Enable[7:0]	–	–	AMPB_INT_SPKMON_ERR_EN	AMPA_INT_SPKMON_ERR_EN	–	–	AMPB_SPK_OVC_EN	AMPA_SPK_OVC_EN
0x2036	Amp A Thermal Interrupts Enable[7:0]	AMPA_THERMSHDN_END_EN	AMPA_THERMSHDN_BGN_EN	AMPA_THERMFB_END_EN	AMPA_THERMFB_BGN_EN	AMPA_THERMWARN2_END_EN	AMPA_THERMWARN2_BGN_EN	AMPA_THERMWARN1_END_EN	AMPA_THERMWARN1_BGN_EN
0x2037	Amp B Thermal Interrupts Enable[7:0]	AMPB_THERMSHDN_END_EN	AMPB_THERMSHDN_BGN_EN	AMPB_THERMFB_END_EN	AMPB_THERMFB_BGN_EN	AMPB_THERMWARN2_END_EN	AMPB_THERMWARN2_BGN_EN	AMPB_THERMWARN1_END_EN	AMPB_THERMWARN1_BGN_EN
0x203A	BPE and DHT Interrupts Enable[7:0]	BPE_L0_EN	BPE_LEVEL_EN	BPE_ACTIVE_END_EN	BPE_ACTIVE_BGN_EN	–	–	DHT_ACTIVE_END_EN	DHT_ACTIVE_BGN_EN
0x203B	RMS Limiter Interrupts Enable[7:0]	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_EN	AMPB_RMS_LIM_ACTIVE_BGN_EN	AMPA_RMS_LIM_ACTIVE_END_EN	AMPA_RMS_LIM_ACTIVE_BGN_EN
0x203E	Miscellaneous Device Interrupts Enable[7:0]	EXT_MUTE_EN	–	–	–	–	–	AMPB_SPK_CLIP_EN	AMPA_SPK_CLIP_EN
Interrupt Flag Clear									
0x2040	Supply and OTP Interrupts Clear[7:0]	–	–	PVDD_UVLO_SHDN_CLR	VBAT_UVLO_SHDN_CLR	–	AVDD_UVLO_CLR	DVDD_UVLO_CLR	OTP_FAIL_CLR
0x2041	Power Up and Down Interrupts Clear[7:0]	PWRDN_DONE_CLR	–	–	–	–	–	AMPB_PWRUP_DONE_CLR	AMPA_PWRUP_DONE_CLR
0x2043	Clock and Data Interrupts Clear[7:0]	–	–	–	–	CLK_RECOVER_CLR	–	INT_CLK_ERR_CLR	CLK_ERR_CLR
0x2045	Amplifier Output Fault Interrupts Clear[7:0]	–	–	AMPB_INT_SPKMON_ERR_CLR	AMPA_INT_SPKMON_ERR_CLR	–	–	AMPB_SPK_OVC_CLR	AMPA_SPK_OVC_CLR
0x2046	Amp A Thermal Interrupts Clear[7:0]	AMPA_THERMSHDN_END_CLR	AMPA_THERMSHDN_BGN_CLR	AMPA_THERMFB_END_CLR	AMPA_THERMFB_BGN_CLR	AMPA_THERMWARN2_END_CLR	AMPA_THERMWARN2_BGN_CLR	AMPA_THERMWARN1_END_CLR	AMPA_THERMWARN1_BGN_CLR
0x2047	Amp B Thermal Interrupts Clear[7:0]	AMPB_THERMSHDN_END_CLR	AMPB_THERMSHDN_BGN_CLR	AMPB_THERMFB_END_CLR	AMPB_THERMFB_BGN_CLR	AMPB_THERMWARN2_END_CLR	AMPB_THERMWARN2_BGN_CLR	AMPB_THERMWARN1_END_CLR	AMPB_THERMWARN1_BGN_CLR
0x204A	BPE and DHT Interrupts Clear[7:0]	BPE_L0_CLR	BPE_LEVEL_CLR	BPE_ACTIVE_END_CLR	BPE_ACTIVE_BGN_CLR	–	–	DHT_ACTIVE_END_CLR	DHT_ACTIVE_BGN_CLR
0x204B	RMS Limiter Interrupts Clear[7:0]	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_CLR	AMPB_RMS_LIM_ACTIVE_BGN_CLR	AMPA_RMS_LIM_ACTIVE_END_CLR	AMPA_RMS_LIM_ACTIVE_BGN_CLR
0x204E	Miscellaneous Device Interrupts Clear[7:0]	EXT_MUTE_CLR	–	–	–	–	–	AMPB_SPK_CLIP_CLR	AMPA_SPK_CLIP_CLR
GPIO Pin Control									

ADDRESS	NAME	MSB							LSB
0x2050	GPIO Select[7:0]	–	–	GPIO3_SEL[1:0]		GPIO2_SEL[1:0]		GPIO1_SEL[1:0]	
0x2052	Pin Config[7:0]	–	–	GPIO3_DRV[1:0]		GPIO2_DRV[1:0]		GPIO1_DRV[1:0]	
0x205F	IRQ Control[7:0]	–	–	–	–	–	IRQ_MODE	IRQ_POL	IRQ_EN
MUTE Pin Volume Control									
0x2060	Mute Ramp Control[7:0]	–	–	–	–	–	–	MUTE_RMPDN_BYPASS	UNMUTE_RMPUP_BYPASS
Clock and Speaker Monitor Control									
0x21F0	Clock Monitor Control[7:0]	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
0x21F2	Speaker Monitor Threshold[7:0]	–	–	–	–	SPKMON_THRESH[3:0]			
0x21F7	Enable Controls[7:0]	–	–	–	–	SPKMON_EN	–	–	CMON_EN
PCM Registers									
0x2201	PCM Mode Config[7:0]	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
0x2202	PCM Clock Setup[7:0]	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
0x2203	PCM Sample Rate Setup 1[7:0]	IVFB_SR[3:0]				PCM_SR[3:0]			
0x2209	PCM TX Control 6[7:0]	–	–	PCM_THERM_SLOT[5:0]					
0x220A	PCM TX Control 7[7:0]	–	–	PCM_DHT_ATN_SLOT[5:0]					
0x220B	PCM TX Control 8[7:0]	–	–	PCM_STATUS_SLOT[5:0]					
0x220C	PCM TX Control 9[7:0]	–	–	PCM_AMPA_DSP_MONITOR_SLOT[5:0]					
0x220D	PCM TX Control 10[7:0]	–	–	PCM_AMPB_DSP_MONITOR_SLOT[5:0]					
0x220E	PCM TX Control 11[7:0]	–	–	PCM_BPE_SLOT[5:0]					
0x220F	PCM TX Control 12[7:0]	–	–	PCM_ICC_SLOT[5:0]					
0x2210	PCM TX Control 1[7:0]	–	–	PCM_AMPA_VFB_SLOT[5:0]					
0x2211	PCM TX Control 2[7:0]	–	–	PCM_AMPB_VFB_SLOT[5:0]					
0x2212	PCM TX Control 3[7:0]	–	–	PCM_AMPA_IMON_SLOT[5:0]					
0x2213	PCM TX Control 4[7:0]	–	–	PCM_AMPB_IMON_SLOT[5:0]					
0x2214	PCM TX Control 5[7:0]	–	–	PCM_PVDD_SLOT[5:0]					
0x2220	PCM Tx HiZ Control 1[7:0]	PCM_TX_SLOT_HIZ[63:56]							
0x2221	PCM Tx HiZ Control 2[7:0]	PCM_TX_SLOT_HIZ[55:48]							
0x2222	PCM Tx HiZ Control 3[7:0]	PCM_TX_SLOT_HIZ[47:40]							
0x2223	PCM Tx HiZ Control 4[7:0]	PCM_TX_SLOT_HIZ[39:32]							

ADDRESS	NAME	MSB							LSB
0x2224	PCM Tx HiZ Control 5[7:0]	PCM_TX_SLOT_HIZ[31:24]							
0x2225	PCM Tx HiZ Control6[7:0]	PCM_TX_SLOT_HIZ[23:16]							
0x2226	PCM Tx HiZ Control 7[7:0]	PCM_TX_SLOT_HIZ[15:8]							
0x2227	PCM Tx HiZ Control 8[7:0]	PCM_TX_SLOT_HIZ[7:0]							
0x2229	PCM RX Source 1[7:0]	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
0x222A	PCM RX Source 2[7:0]	PCM_DMMIX_CH1_SOURCE[3:0]				PCM_DMMIX_CH0_SOURCE[3:0]			
0x222B	PCM Bypass Source[7:0]	–	–	–	–	PCM_BYPASS_SOURCE[3:0]			
0x222C	PCM TX Source Enables 1[7:0]	PCM_BPE_EN	PCM_STATUS_EN	PCM_DHT_ATN_EN	PCM_THERM_EN	PCM_PVDD_EN	PCM_DSPMONITOR_EN	PCM_IMON_AMPA_EN	PCM_VFB_AMPA_EN
0x222D	PCM TX Source Enables 2[7:0]	–	–	–	–	–	–	PCM_IMON_AMPB_EN	PCM_VFB_AMPB_EN
0x222E	PCM Rx Enables[7:0]	–	–	–	–	–	–	PCM_BYP_EN	PCM_RX_EN
0x222F	PCM Tx Enables[7:0]	–	–	–	–	–	–	–	PCM_TX_EN
Interchip Communication									
0x2270	ICC Rx Enables A[7:0]	ICC_RX_CH7_EN	ICC_RX_CH6_EN	ICC_RX_CH5_EN	ICC_RX_CH4_EN	ICC_RX_CH3_EN	ICC_RX_CH2_EN	ICC_RX_CH1_EN	ICC_RX_CH0_EN
0x2271	ICC Rx Enables B[7:0]	ICC_RX_CH15_EN	ICC_RX_CH14_EN	ICC_RX_CH13_EN	ICC_RX_CH12_EN	ICC_RX_CH11_EN	ICC_RX_CH10_EN	ICC_RX_CH9_EN	ICC_RX_CH8_EN
0x2272	ICC Tx Control[7:0]	–	ICC_INTERLEAVE_MODE	ICC_DATA_SEL	ICC_TX_EXTRA_HIZ	ICC_TX_DEST[3:0]			
0x227F	ICC Enables[7:0]	–	–	–	–	–	ICC_OVER_DOUT_EN	ICC_LINK_EN	ICC_TX_EN
Tone Generator Control									
0x2283	Tone Generator and DC Config[7:0]	–	–	TONE_AMPLITUDE[1:0]		TONE_CONFIG[3:0]			
0x2284	Tone Generator DC Level 1[7:0]	TONE_DC[23:16]							
0x2285	Tone Generator DC Level 2[7:0]	TONE_DC[15:8]							
0x2286	Tone Generator DC Level 3[7:0]	TONE_DC[7:0]							
0x228F	Tone Generator Enable[7:0]	–	–	–	–	–	–	PINK_NOISE_EN	TONE_EN
Noise Gate and Idle Mode									
0x22E0	Noise Gate/Idle Mode Control[7:0]	NG_UNMUTE_THRESH[3:0]				NG_MUTE_THRESH[3:0]			
0x22E3	Noise Gate/Idle Mode Enables[7:0]	–	–	–	–	–	–	IDLE_MODE_EN	NOISEGATE_EN

ADDRESS	NAME	MSB							LSB
Amplifier Volume Control									
0x22F0	AMP A Volume Level Control[7:0]	AMPA_SPK_VOL[7:0]							
0x22F1	AMP B Volume Level Control[7:0]	AMPB_SPK_VOL[7:0]							
0x22FF	Amplifier Volume Update Control[7:0]	–	–	–	–	–	–	AMPB_VOL_UPDATE	AMPA_VOL_UPDATE
AMP A Playback Path Control									
0x2300	AMP A Volume Ramp Control[7:0]	–	–	AMPA_SPK_VOL_RMP_RATE[1:0]		–	–	AMPA_SPK_VOL_RMPDN_BYPASS	AMPA_SPK_VOL_RMPUP_BYPASS
0x2302	AMP A Path Gain[7:0]	–	–	–	AMPA_SPK_GAIN_MAX[4:0]				
0x2303	AMP A DSP Config[7:0]	–	AMPA_SPK_WBAND_FILT_EN	AMPA_SPK_SAFE_EN	AMPA_SPK_INVERT	AMPA_SPK_DITH_EN	AMPA_SPK_IVF_DCBLK_CFG[1:0]		AMPA_SPK_DCBLK_EN
0x230B	AMP A SPK Path Wideband Only Enable[7:0]	–	–	–	–	–	–	–	AMPA_SPK_WIDEBAND_ONLY_EN
0x230E	AMP A Clip Gain[7:0]	–	–	–	–	AMPA_SPK_CLIP[3:0]			
AMP B Playback Path Control									
0x2320	AMP B Volume Ramp Control[7:0]	–	–	AMPB_SPK_VOL_RMP_RATE[1:0]		–	–	AMPB_SPK_VOL_RMPDN_BYPASS	AMPB_SPK_VOL_RMPUP_BYPASS
0x2322	AMP B Path Gain[7:0]	–	–	–	AMPB_SPK_GAIN_MAX[4:0]				
0x2323	AMP B DSP Config[7:0]	–	AMPB_SPK_WBAND_FILT_EN	AMPB_SPK_SAFE_EN	AMPB_SPK_INVERT	AMPB_SPK_DITH_EN	AMPB_SPK_IVF_DCBLK_CFG[1:0]		AMPB_SPK_DCBLK_EN
0x232B	AMP B SPK Path Wideband Only Enable[7:0]	–	–	–	–	–	–	–	AMPB_SPK_WIDEBAND_ONLY_EN
0x232E	AMP B Clip Gain[7:0]	–	–	–	–	AMPB_SPK_CLIP[3:0]			
Class-D Modulator and Output Edge Control									
0x23D3	SSM Configuration[7:0]	–	–	–	–	SPK_TRI_SSM_EN	–	SPK_TRI_SSM_MOD[1:0]	
0x23DA	SPK Switching Frequency[7:0]	–	–	–	–	–	SPK_TRI_FSW2X_MODE	–	–
0x23DD	SPK Edge Control 1[7:0]	SPK_SL_RATE_LS[3:0]				SPK_SL_RATE_HS[3:0]			
Bypass Path Channel Control									
0x23E0	Bypass Path Config[7:0]	–	–	–	–	–	–	BYP_WBAND_FILT_EN	BYP_INVERT

ADDRESS	NAME	MSB							LSB
0x23E1	Bypass Path Routing Config[7:0]	–	–	–	–	–	–	BYP_PATH_AMP_SEL[1:0]	
AMP Mode Select and Enable									
0x23F0	AMP output mode select[7:0]	–	–	–	–	–	–	–	AMP_MODE
0x23FF	AMP enables[7:0]	–	–	–	–	AMPB_SPK_FB_EN	AMPA_SPK_FB_EN	AMPB_SPK_EN	AMPA_SPK_EN
I_V Feedback Path Control (For MAX98415 Only)									
0x2400	I_V Sense Path Config[7:0]	IVF_WBAND_FILT_EN	VFB_DITH_EN	IMON_DITH_EN	–	AMPB_IVF_I_DCBLK_EN	AMPB_IVF_V_DCBLK_EN	AMPA_IVF_I_DCBLK_EN	AMPA_IVF_V_DCBLK_EN
0x2404	I_V Sense Path Enables[7:0]	–	IVF_AMPB_IM_EN	IVF_AMPB_I_EN	IVF_AMPB_V_EN	–	IVF_AMPA_IM_EN	IVF_AMPA_I_EN	IVF_AMPA_V_EN
Meas ADC									
0x2700	Meas ADC Sample Rate[7:0]	MEAS_ADC_AMPB_TEMP_SR[1:0]		MEAS_ADC_AMPA_TEMP_SR[1:0]		–	–	MEAS_ADC_PVDD_SR[1:0]	
0x2702	Meas ADC Optimal Mode[7:0]	–	–	–	–	MEAS_ADC_OPT_AVE_SEL[1:0]		MEAS_ADC_OPT_MODE[1:0]	
0x2704	Meas ADC Readback Control 1[7:0]	–	–	–	–	MEAS_ADC_AMPB_TEMP_RD_MODE	MEAS_ADC_AMPA_TEMP_RD_MODE	–	MEAS_ADC_PVDD_RD_MODE
0x2705	Meas ADC Readback Control 2[7:0]	–	–	–	–	MEAS_ADC_AMPB_TEMP_RD_UPD	MEAS_ADC_AMPA_TEMP_RD_UPD	–	MEAS_ADC_PVDD_RD_UPD
0x2710	Meas ADC PVDD Config[7:0]	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
0x2712	Meas ADC AMPA Thermal Config[7:0]	–	–	–	MEAS_ADC_AMPA_TEMP_FILT_EN	MEAS_ADC_AMPA_TEMP_FILT_COEFF[3:0]			
0x2713	Meas ADC AMPB Thermal Config[7:0]	–	–	–	MEAS_ADC_AMPB_TEMP_FILT_EN	MEAS_ADC_AMPB_TEMP_FILT_COEFF[3:0]			
0x2720	Meas ADC PVDD Readback MSB[7:0]	MEAS_ADC_PVDD_DATA[8:1]							
0x2721	Meas ADC PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
0x2724	Meas ADC AMPA Thermal Readback MSB[7:0]	MEAS_ADC_AMPA_THERM_DATA[8:1]							
0x2725	Meas ADC AMPA Thermal Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_AMPA_THERM_DATA[0]

ADDRESS	NAME	MSB							LSB
0x2726	Meas ADC AMPB Thermal Readback MSB[7:0]	MEAS_ADC_AMPB_THERM_DATA[8:1]							
0x2727	Meas ADC AMPB Thermal Readback LSB[7:0]	–	–	–	–	–	–	–	MEAS_ADC_AMPB_THERM_DATA[0]
0x2730	Meas ADC Lowest PVDD Readback MSB[7:0]	LOWEST_PVDD_DATA[8:1]							
0x2731	Meas ADC Lowest PVDD Readback LSB[7:0]	–	–	–	–	–	–	–	LOWEST_PVDD_DATA[0]
0x2732	Meas ADC AMPA Highest Thermal Readback MSB[7:0]	HIGHEST_AMPA_THERMAL_DATA_MSB[7:0]							
0x2733	Meas ADC AMPA Highest Thermal Readback LSB[7:0]	–	–	–	–	–	–	–	HIGHEST_AMPA_THERMAL_DATA_LSB
0x2734	Meas ADC AMPB Highest Thermal Readback MSB[7:0]	HIGHEST_AMPB_THERMAL_DATA_MSB[7:0]							
0x2735	Meas ADC AMPB Highest Thermal Readback LSB[7:0]	–	–	–	–	–	–	–	HIGHEST_AMPB_THERMAL_DATA_LSB
0x273F	Meas ADC Config[7:0]	–	–	–	–	–	–	–	MEAS_ADC_PVDD_EN
Thermal Protection									
0x2750	Thermal Warning Threshhold[7:0]	–	THERMWARN1_THRESH[6:0]						
0x2754	Warning Threshold 2 Amp 1[7:0]	–	THERMWARN2_THRESH[6:0]						
0x2758	Thermal Shutdown Threshold[7:0]	–	THERMSHDN_THRESH[6:0]						
0x275C	Thermal Hysteresis[7:0]	–	–	–	–	–	–	THERM_HYST[1:0]	
0x275F	Thermal Foldback Settings[7:0]	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE2[1:0]		THERMFB_SLOPE1[1:0]	
0x276F	Thermal Foldback Enable[7:0]	–	–	–	–	–	–	–	THERMFB_EN
Brownout Protection Engine									
0x2800	BPE State[7:0]	–	–	–	–	–	BPE_STATE[2:0]		
0x2801	BPE L3 Threshold MSB[7:0]	BPE_L3_VTHRESH[8:1]							
0x2802	BPE L3 Threshold LSB[7:0]	–	–	–	–	–	–	–	BPE_L3_VTHRESH[0]
0x2803	BPE L2 Threshold MSB[7:0]	BPE_L2_VTHRESH[8:1]							

ADDRESS	NAME	MSB							LSB
0x2804	BPE L2 Threshold LSB[7:0]	–	–	–	–	–	–	–	BPE_L2_VTHRESH[0]
0x2805	BPE L1 Threshold MSB[7:0]	BPE_L1_VTHRESH[8:1]							
0x2806	BPE L1 Threshold LSB[7:0]	–	–	–	–	–	–	–	BPE_L1_VTHRESH[0]
0x2807	BPE L0 Threshold MSB[7:0]	BPE_L0_VTHRESH[8:1]							
0x2808	BPE L0 Threshold LSB[7:0]	–	–	–	–	–	–	–	BPE_L0_VTHRESH[0]
0x2809	BPE L3 Dwell and Hold Time[7:0]	–	–	BPE_L3_DWELL[2:0]			BPE_L3_HOLD[2:0]		
0x280A	BPE L2 Dwell and Hold Time[7:0]	–	–	BPE_L2_DWELL[2:0]			BPE_L2_HOLD[2:0]		
0x280B	BPE L1 Dwell and Hold Time[7:0]	–	–	BPE_L1_DWELL[2:0]			BPE_L1_HOLD[2:0]		
0x280C	BPE L0 Hold Time[7:0]	–	–	–	–	–	BPE_L0_HOLD[2:0]		
0x280D	BPE L3 Attack and Release Step[7:0]	–	–	–	–	BPE_L3_STEP[3:0]			
0x280E	BPE L2 Attack and Release Step[7:0]	–	–	–	–	BPE_L2_STEP[3:0]			
0x280F	BPE L1 Attack and Release Step[7:0]	–	–	–	–	BPE_L1_STEP[3:0]			
0x2810	BPE L0 Attack and Release Step[7:0]	–	–	–	–	BPE_L0_STEP[3:0]			
0x2811	BPE L3 Max Gain Attn[7:0]	–	–	–	BPE_L3_MAXATTN[4:0]				
0x2812	BPE L2 Max Gain Attn[7:0]	–	–	–	BPE_L2_MAXATTN[4:0]				
0x2813	BPE L1 Max Gain Attn[7:0]	–	–	–	BPE_L1_MAXATTN[4:0]				
0x2814	BPE L0 Max Gain Attn[7:0]	–	–	–	BPE_L0_MAXATTN[4:0]				
0x2815	BPE L3 Gain Attack and Rls Rates[7:0]	–	–	BPE_L3_GAIN_RLS[2:0]			BPE_L3_GAIN_ATK[2:0]		
0x2816	BPE L2 Gain Attack and Rls Rates[7:0]	–	–	BPE_L2_GAIN_RLS[2:0]			BPE_L2_GAIN_ATK[2:0]		
0x2817	BPE L1 Gain Attack and Rls Rates[7:0]	–	–	BPE_L1_GAIN_RLS[2:0]			BPE_L1_GAIN_ATK[2:0]		
0x2818	BPE L0 Gain Attack and Rls Rates[7:0]	–	–	BPE_L0_GAIN_RLS[2:0]			BPE_L0_GAIN_ATK[2:0]		
0x2819	BPE L3 Limiter Config[7:0]	–	–	–	–	BPE_L3_LIM[3:0]			
0x281A	BPE L2 Limiter Config[7:0]	–	–	–	–	BPE_L2_LIM[3:0]			
0x281B	BPE L1 Limiter Config[7:0]	–	–	–	–	BPE_L1_LIM[3:0]			
0x281C	BPE L0 Limiter Config[7:0]	–	–	–	–	BPE_L0_LIM[3:0]			

ADDRESS	NAME	MSB							LSB
0x281D	BPE L3 Limiter Attack and Release Rates[7:0]	–	–	BPE_L3_LIM_RLS[2:0]			BPE_L3_LIM_ATK[2:0]		
0x281E	BPE L2 Limiter Attack and Release Rates[7:0]	–	–	BPE_L2_LIM_RLS[2:0]			BPE_L2_LIM_ATK[2:0]		
0x281F	BPE L1 Limiter Attack and Release Rates[7:0]	–	–	BPE_L1_LIM_RLS[2:0]			BPE_L1_LIM_ATK[2:0]		
0x2820	BPE L0 Limiter Attack and Release Rates[7:0]	–	–	BPE_L0_LIM_RLS[2:0]			BPE_L0_LIM_ATK[2:0]		
0x2821	BPE Threshold Hysteresis[7:0]	BPE_VTHRESH_HYST[7:0]							
0x2822	BPE Infinite Hold Clear[7:0]	–	–	–	–	–	–	–	BPE_HLD_RLS
0x2824	BPE Lowest State[7:0]	–	–	–	–	–	BPE_LOWEST[2:0]		
0x2825	BPE Lowest Gain[7:0]	BPE_LOWEST_GAIN[7:0]							
0x2826	BPE Lowest Limiter[7:0]	BPE_LOWEST_LIMIT[7:0]							
0x283F	BPE Enable[7:0]	–	–	–	–	–	–	BPE_LIM_EN	BPE_EN
Dynamic Headroom Tracking									
0x2840	DHT Configuration 1[7:0]	–	–	–	–	DHT_VROT_PNT[3:0]			
0x2841	Limiter Configuration 1[7:0]	–	–	–	DHT_HR[4:0]				
0x2842	Limiter Configuration 2[7:0]	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
0x2843	DHT Configuration 2[7:0]	–	–	–	DHT_MAX_ATN[4:0]				
0x2844	DHT Configuration 3[7:0]	–	–	–	–	DHT_ATK_RATE[3:0]			
0x2845	DHT Configuration 4[7:0]	–	–	–	–	DHT_RLS_RATE[3:0]			
0x2846	DHT Supply Hysteresis Configuration[7:0]	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
0x284F	DHT Enable[7:0]	–	–	–	–	–	–	–	DHT_EN
Envelope Tracking Control									
0x2860	ET Levels[7:0]	–	–	–	–	ET_LEVEL_SEL[3:0]			
0x2861	ET Level Step Size MSB[7:0]	ET_LVL_STEPSIZE[8:1]							
0x2862	ET Level Step Size LSB[7:0]	–	–	–	–	–	–	–	ET_LVL_STEPSIZE[0]
0x2863	ET Level PVDD Step Size MSB[7:0]	ET_PVDD_STEPSIZE[8:1]							
0x2864	ET Level PVDD Step Size LSB[7:0]	–	–	–	–	–	–	–	ET_PVDD_STEPSIZE[0]
0x2866	Maximum Duty Cycle MSB[7:0]	ET_MAXDUTY_CYC[9:2]							

ADDRESS	NAME	MSB							LSB
0x2867	Maximum Duty Cycle LSB[7:0]	–	–	–	–	–	–	ET_MAXDUTY_CYC[1:0]	
0x2868	Minimum PVDD Level MSB[7:0]	MIN_PVDD_LVL[8:1]							
0x2869	Minimum PVDD Level LSB[7:0]	–	–	–	–	–	–	–	MIN_PVDD_LVL[0]
0x286A	ET PVDD headroom[7:0]	–	–	ET_PVDD_HDRM[5:0]					
0x286C	ET Delay Time[7:0]	–	ET_PB_DELAY_TIME[6:0]						
0x286E	ET Level Hold Time[7:0]	–	–	–	–	–	ET_HOLD_TIME[2:0]		
RMS Limiter									
0x2890	AMP A Limiter Threshold 1[7:0]	AMPA_RMS_LIM_THRESH[7:0]							
0x2893	AMP A Limiter Time Constant MSB[7:0]	–	–	–	–	AMPA_RMS_LIM_TIME_CONST[19:16]			
0x2894	AMP A Limiter Time Constant MSB[7:0]	AMPA_RMS_LIM_TIME_CONST[15:8]							
0x2895	AMP A Limiter Time Constant LSB[7:0]	AMPA_RMS_LIM_TIME_CONST[7:0]							
0x2898	AMP B Limiter Threshold 1[7:0]	AMPB_RMS_LIM_THRESH[7:0]							
0x289B	AMP B Limiter Time Constant MSB[7:0]	–	–	–	–	AMPB_RMS_LIM_TIME_CONST[19:16]			
0x289C	AMP B Limiter Time Constant MSB[7:0]	AMPB_RMS_LIM_TIME_CONST[15:8]							
0x289D	AMP B Limiter Time Constant LSB[7:0]	AMPB_RMS_LIM_TIME_CONST[7:0]							
0x28AF	RMS Limiter Enable[7:0]	–	–	–	–	–	–	AMPB_RMS_LIM_EN	AMPA_RMS_LIM_EN
System Configuration									
0x29F1	Group Write Address Ctrl[7:0]	GRP_WR_ADDR[6:0]							GRP_WR_EN
0x29FD	Device Ramp Control[7:0]	–	–	–	–	–	–	SHTDWN_RMPDN_BYPASS	STARTUP_RMPUP_BYPASS
0x29FE	Auto-Restart Behavior[7:0]	–	–	–	–	OVC_AUTORESTART_EN	THERM_AUTORESTART_EN	VBAT_AUTORESTART_EN	PVDD_AUTORESTART_EN
0x29FF	Global Enable[7:0]	–	–	–	–	–	–	–	EN
Device and Revision ID									
0x3FFD	Device ID MSB[7:0]	DEVICE_ID_MSB[7:0]							
0x3FFE	Device ID LSB[7:0]	DEVICE_ID_LSB[7:0]							
0x3FFF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

Software Reset (0x1000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
RST	0	–	This bit field is used to trigger a software reset event. Writing a 1 resets the device and returns the control registers to their power-on reset states. Writing a 0 has no effect, and readback always returns 0.	0: No action 1: Triggers a software reset event

Supply and OTP Interrupts Raw (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PVDD_UVLO_SHDN_RAW	VBAT_UVLO_SHDN_RAW	–	AVDD_UVLO_RAW	DVDD_UVLO_RAW	OTP_FAIL_RAW
Reset	–	–	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PVDD_UVLO_SHDN_RAW	5	–	Raw value of PVDD UVLO error indicator.	0: No PVDD UVLO error. 1: PVDD below the UVLO threshold in the active state.
VBAT_UVLO_SHDN_RAW	4	–	Raw value of VBAT UVLO error indicator.	0: No VBAT UVLO error. 1: VBAT below the UVLO threshold in the active state.
AVDD_UVLO_RAW	2	–	Raw value of AVDD UVLO error indicator.	0: No AVDD UVLO error. 1: AVDD below the UVLO threshold in the active state.
DVDD_UVLO_RAW	1	–	Raw value of DVDD UVLO error indicator.	0: No DVDD UVLO error. 1: DVDD below the UVLO threshold in the active state.
OTP_FAIL_RAW	0	–	Raw status of OTP load fail.	0: No OTP Load Failure. 1: The OTP Load Routine was not completed successfully.

Power Up and Down Interrupts Raw (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	PWRDN_DONE_RAW	–	–	–	–	–	AMPB_PWRUP_DONE_RAW	AMPA_PWRUP_DONE_RAW
Reset	0b0	–	–	–	–	–	0b0	0b0

BIT	7	6	5	4	3	2	1	0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_RAW	7	–	Raw value of Power-Down done.	0: The device is not reporting a power-down into a software shutdown event. 1: The device is reporting a power-down into a software shutdown event.
AMPB_PWRUP_DONE_RAW	1	–	Raw value of Power-Up Done for Amplifier B.	0: The device is not reporting a power-up event. 1: The device is reporting a power-up into the active state with the speaker amplifier 2 enabled.
AMPA_PWRUP_DONE_RAW	0	–	Raw value of Power-Up Done for Amplifier A.	0: The device is not reporting a power-up event. 1: The device is reporting a power-up into the active state with the speaker amplifier enabled.

Clock and Data Interrupts Raw (0x2003)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_RECOVER_RAW	–	INT_CLK_ERR_RAW	CLK_ERR_RAW
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Read Only	–	Read Only	Read Only
Restriction	–	–	–	–	Normal	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLK_RECOVER_RAW	3	–	Raw value of the external clock monitor error recovery indicator.	0: The clock monitor is not reporting clock error recovery. 1: The clock monitor is reporting clock error recovery.
INT_CLK_ERR_RAW	1	–	Raw value of internal clock error indicator.	0: The internal clock monitor is not reporting clock error. 1: The internal clock is monitor reporting clock error.
CLK_ERR_RAW	0	–	Raw value of the external clock monitor error indicator.	0: No external clock error was detected. 1: Clock monitor reporting clock error.

Amplifier Output Fault Interrupts Raw (0x2005)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_INT_SPKMON_ERR_RAW	AMPA_INT_SPKMON_ERR_RAW	–	–	AMPB_SPK_OVC_RAW	AMPA_SPK_OVC_RAW
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_INT_SPKMON_ERR_RAW	5	–	Raw value of the Amp B internal speaker monitor status indicator.	0: The internal speaker monitor is not reporting data errors. 1: The internal speaker monitor reporting data errors.
AMPA_INT_SPKMON_ERR_RAW	4	–	Raw value of the internal speaker monitor status indicator for Amp A.	0: The internal speaker monitor not reporting data errors. 1: The internal speaker monitor reporting data errors.
AMPB_SPK_OVC_RAW	1	–	Raw value of speaker overcurrent limit for Amplifier B.	0: Speaker overcurrent limit is inactive. 1: Speaker overcurrent limit is active.
AMPA_SPK_OVC_RAW	0	–	Raw value of speaker overcurrent limit on Amplifier A.	0: Speaker overcurrent limit is inactive. 1: Speaker overcurrent limit is active.

Amp A Thermal Warning Interrupts Raw (0x2006)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_THERMSHDN_END_RAW	AMPA_THERMSHDN_BGN_RAW	AMPA_THERMFB_END_RAW	AMPA_THERMFB_BGN_RAW	AMPA_THERMWARN2_END_RAW	AMPA_THERMWARN2_BGN_RAW	AMPA_THERMWARN1_END_RAW	AMPA_THERMWARN1_BGN_RAW
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMSHDN_END_RAW	7	–	Raw value of Amp A thermal shutdown end indicator.	0: The die temperature above the thermal shutdown limit. 1: The die temperature has dropped below the thermal shutdown limit.
AMPA_THERMSHDN_BGN_RAW	6	–	Raw value of Amp A thermal shutdown begin indicator.	0: The die temperature is below the thermal shutdown limit. 1: The die temperature is above the thermal shutdown limit.
AMPA_THERMFB_END_RAW	5	–	Raw value of Amp A thermal foldback end.	0: The thermal foldback is active. 1: The thermal foldback has ended.
AMPA_THERMFB_BGN_RAW	4	–	Raw value of Amp A thermal foldback begin.	0: The thermal foldback is not active. 1: The thermal foldback is active.
AMPA_THERMWARN2_END_RAW	3	–	Raw value of Amp A thermal-warning2 end indicator.	0: The die temperature above the thermal-warning2 limit. 1: The die temperature has dropped below the thermal-warning2 limit.
AMPA_THERMWARN2_BGN_RAW	2	–	Raw value of thermal-warning2 begin indicator for Amplifier A.	0: The die temperature is below the thermal-warning2 limit. 1: The die temperature is above the thermal-warning2 limit.
AMPA_THERMWARN1_END_RAW	1	–	Raw value of thermal-warning1 end indicator for Amplifier A.	0: The die temperature is above the thermal-warning1 limit. 1: The die temperature has dropped below the thermal-warning1 limit.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMWARN1_BGN_RAW	0	–	Raw value of thermal-warning1 begin indicator for Amplifier A.	0: The die temperature is below the thermal-warning1 limit. 1: The die temperature is above the thermal-warning1 limit.

Amp B Thermal Warning Interrupts Raw (0x2007)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_THERMSHDN_END_RAW	AMPB_THERMSHDN_BGN_RAW	AMPB_THERMFB_END_RAW	AMPB_THERMFB_BGN_RAW	AMPB_THERMWARN2_END_RAW	AMPB_THERMWARN2_BGN_RAW	AMPB_THERMWARN1_END_RAW	AMPB_THERMWARN1_BGN_RAW
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMSHDN_END_RAW	7	–	Raw value of Amp B thermal shutdown end indicator.	0: The die temperature is above the thermal shutdown limit. 1: The die temperature has dropped below the thermal shutdown limit.
AMPB_THERMSHDN_BGN_RAW	6	–	Raw value of Amp B thermal shutdown begin indicator.	0: The die temperature is below the thermal shutdown limit. 1: The die temperature is above the thermal shutdown limit.
AMPB_THERMFB_END_RAW	5	–	Raw value of Amp B thermal foldback end.	0: The thermal foldback is active. 1: The thermal foldback has ended.
AMPB_THERMFB_BGN_RAW	4	–	Raw value of Amp B thermal foldback begin.	0: The thermal foldback is not active. 1: The thermal foldback is active.
AMPB_THERMWARN2_END_RAW	3	–	Raw value of Amp B thermal-warning2 end indicator.	0: The die temperature is above the thermal-warning2 limit. 1: The die temperature has dropped below the thermal-warning2 limit.
AMPB_THERMWARN2_BGN_RAW	2	–	Raw value of Amp Bthermal-warning2 begin indicator.	0: The die temperature is below the thermal-warning2 limit. 1: The die temperature is above the thermal-warning2 limit.
AMPB_THERMWARN1_END_RAW	1	–	Raw value of Amp B thermal-warning1 end indicator.	0: The die temperature is above the thermal-warning1 limit. 1: The die temperature has dropped below the thermal-warning1 limit.
AMPB_THERMWARN1_BGN_RAW	0	–	Raw value of Amp B thermal-warning1 begin indicator.	0: The die temperature is below the thermal-warning1 limit. 1: The die temperature is above the thermal-warning1 limit.

BPE and DHT Interrupts Raw (0x200A)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_RAW	BPE_LEVEL_RAW	BPE_ACTIVE_END_RAW	BPE_ACTIVE_BGN_RAW	–	–	DHT_ACTIVE_END_RAW	DHT_ACTIVE_BGN_RAW
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_RAW	7	–	Indicates that BPE has transitioned into level 0.	0: The BPE controller is not in level 0. 1: The BPE controller has transitioned into level 0.
BPE_LEVEL_RAW	6	–	Indicates that BPE has transitioned between levels.	0: The BPE is static. 1: The BPE level is changing.
BPE_ACTIVE_END_RAW	5	–	Indicates that the BPE is no longer active.	0: The Brownout Protection Engine is active. 1: The Brownout Protection Engine is inactive.
BPE_ACTIVE_BGN_RAW	4	–	Indicates that the BPE is active.	0: The Brownout Protection Engine is inactive. 1: The Brownout Protection Engine is active.
DHT_ACTIVE_END_RAW	1	–	Raw value of DHT active end.	0: DHT is currently active or has not yet applied attenuation. 1: DHT activity has ended.
DHT_ACTIVE_BGN_RAW	0	–	Raw value of DHT active begin.	0: DHT is not active. 1: DHT is active.

RMS Limiter Interrupts Raw (0x200B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_RAW	AMPB_RMS_LIM_ACTIVE_BGN_RAW	AMPA_RMS_LIM_ACTIVE_END_RAW	AMPA_RMS_LIM_ACTIVE_BGN_RAW
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_ACTIVE_END_RAW	3	–	Raw value of Amplifier B RMS Limiter end.	0: RMS Limiter is currently active or has not applied attenuation. 1: RMS Limiter activity has ended.
AMPB_RMS_LIM_ACTIVE_BGN_RAW	2	–	Raw value of Amplifier B RMS Limiter begin.	0: RMS Limiter is not active. 1: RMS Limiter is active.
AMPA_RMS_LIM_ACTIV	1	–	Raw value of Amplifier A RMS Limiter end.	0: RMS Limiter is currently active or has not applied attenuation. 1: RMS Limiter activity has ended.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
E_END_RAW				
AMPA_RMS_LIM_ACTIVE_BGN_RAW	0	–	Raw value of Amplifier A RMS Limiter begin.	0: RMS Limiter is not active. 1: RMS Limiter is active.

Miscellaneous Interrupts Raw (0x200E)

BIT	7	6	5	4	3	2	1	0
Field	EXT_MUTE_RAW	–	–	–	–	–	AMPB_SPK_CLIP_RAW	AMPA_SPK_CLIP_RAW
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EXT_MUTE_RAW	7	–	Raw value of external mute indicator.	0: Not externally muted. 1: Speaker amplifier outputs are muted via pin control.
AMPB_SPK_CLIP_RAW	1	–	Speaker amplifier B output clipping monitor raw bit.	0: The speaker amplifier output clipping is not detected. 1: The speaker amplifier output clipping is detected.
AMPA_SPK_CLIP_RAW	0	–	Speaker amplifier A output clipping monitor raw bit.	0: The speaker amplifier output clipping is not detected. 1: The speaker amplifier output clipping is detected.

Supply and OTP Interrupts State (0x2010)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PVDD_UVLO_SHDN_STATE	VBAT_UVLO_SHDN_STATE	–	AVDD_UVLO_STATE	DVDD_UVLO_STATE	OTP_FAIL_STATE
Reset	–	–	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PVDD_UVLO_SHDN_STATE	5	–	Unmaskable interrupt state, cleared by PVDD_UVLO_SHDN_CLR.	0: No rising edge of PVDD_UVLO_SHDN_RAW since the last PVDD_UVLO_SHDN_CLR. 1: The rising edge of PVDD_UVLO_SHDN_RAW since the last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_STATE	4	–	Unmaskable interrupt state, cleared by VBAT_UVLO_SHDN_CLR.	0: No rising edge of VBAT_UVLO_SHDN_RAW since the last VBAT_UVLO_SHDN_CLR. 1: The rising edge of VBAT_UVLO_SHDN_RAW since the last VBAT_UVLO_SHDN_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AVDD_UVLO_STATE	2	–	Unmaskable interrupt state, cleared by AVDD_UVLO_CLR.	0: No rising edge of AVDD_UVLO_RAW since the last AVDD_UVLO_CLR. 1: The rising edge of AVDD_UVLO_RAW since the last AVDD_UVLO_CLR.
DVDD_UVLO_STATE	1	–	Unmaskable interrupt state, cleared by DVDD_UVLO_CLR.	0: No rising edge of DVDD_UVLO_RAW since the last DVDD_UVLO_CLR. 1: The rising edge of DVDD_UVLO_RAW since the last DVDD_UVLO_CLR.
OTP_FAIL_STATE	0	–	Unmaskable interrupt state, cleared by OTP_FAIL_CLR.	0: No rising edge of OTP_FAIL_RAW since the last OTP_FAIL_CLR. 1: The rising edge of OTP_FAIL_RAW since the last OTP_FAIL_CLR.

Power Up and Down Interrupts State (0x2011)

BIT	7	6	5	4	3	2	1	0
Field	PWRDN_DONE_STATE	–	–	–	–	–	AMPB_PWRUP_DONE_STATE	AMPA_PWRUP_DONE_STATE
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_STATE	7	–	Unmaskable interrupt state, cleared by PWRDN_DONE_CLR.	0: No rising edge of PWRDN_DONE_RAW since the last PWRDN_DONE_CLR. 1: The rising edge of PWRDN_DONE_RAW since the last PWRDN_DONE_CLR.
AMPB_PWRUP_DONE_STATE	1	–	Unmaskable interrupt state, cleared by AMPB_PWRUP_DONE_CLR.	0: No rising edge of AMPB_PWRUP_DONE_RAW since last the AMPB_PWRUP_DONE_CLR. 1: The rising edge of AMPB_PWRUP_DONE_RAW since last the AMPB_PWRUP_DONE_CLR.
AMPA_PWRUP_DONE_STATE	0	–	Unmaskable interrupt state, cleared by AMPA_PWRUP_DONE_CLR.	0: No rising edge of PWRUP_DONE_RAW since the last AMPA_PWRUP_DONE_CLR. 1: The rising edge of PWRUP_DONE_RAW since the last AMPA_PWRUP_DONE_CLR.

Clock and Data Interrupts State (0x2013)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_RECOVER_STATE	–	INT_CLK_ERR_STATE	CLK_ERR_STATE
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Read Only	–	Read Only	Read Only
Restriction	–	–	–	–	Normal	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLK_RECOVER_STATE	3	–	Unmaskable interrupt state, cleared by CLK_RECOVER_CLR.	0: No rising edge of CLK_RECOVER_RAW since the last CLK_RECOVER_CLR. 1: The rising edge of CLK_RECOVER_RAW since the last CLK_RECOVER_CLR.
INT_CLK_ERR_STATE	1	–	Unmaskable interrupt state, cleared by INT_CLK_ERR_CLR.	0: No rising edge of INT_CLK_ERR_RAW since the last INT_CLK_ERR_CLR. 1: The rising edge of INT_CLK_ERR_RAW since the last INT_CLK_ERR_CLR.
CLK_ERR_STATE	0	–	Unmaskable interrupt state, cleared by CLK_ERR_CLR.	0: No rising edge of the CLK_ERR_RAW since the last CLK_ERR_CLR. 1: The rising edge of CLK_ERR_RAW since the last CLK_ERR_CLR.

Amplifier Output Fault Interrupts State (0x2015)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_INT_SPKMON_ERR_STATE	AMPA_INT_SPKMON_ERR_STATE	–	–	AMPB_SPK_OVC_STATE	AMPA_SPK_OVC_STATE
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_INT_SPKMON_ERR_STATE	5	–	Unmaskable interrupt state, cleared by AMPB_INT_SPKMON_ERR_CLR.	0: No rising edge of AMPB_INT_SPKMON_ERR_RAW since the last AMPB_INT_SPKMON_ERR_CLR. 1: The rising edge of AMPB_INT_SPKMON_ERR_RAW since the last AMPB_INT_SPKMON_ERR_CLR.
AMPA_INT_SPKMON_ERR_STATE	4	–	Unmaskable interrupt state, cleared by AMPA_INT_SPKMON_ERR_CLR.	0: No rising edge of AMPA_INT_SPKMON_ERR_RAW since last the AMPA_INT_SPKMON_ERR_CLR. 1: The rising edge of AMPA_INT_SPKMON_ERR_RAW since the last AMPA_INT_SPKMON_ERR_CLR.
AMPB_SPK_OVC_STATE	1	–	Unmaskable interrupt state, cleared by AMPB_SPK_OVC_CLR.	0: No rising edge of AMPB_SPK_OVC_RAW since the last AMPB_SPK_OVC_CLR 1: The rising edge of AMPB_SPK_OVC_RAW since the last AMPB_SPK_OVC_CLR.
AMPA_SPK_OVC_STATE	0	–	Unmaskable interrupt state, cleared by AMPA_SPK_OVC_CLR.	0: No rising edge of AMPA_SPK_OVC_RAW since the last AMPA_SPK_OVC_CLR. 1: The rising edge of AMPA_SPK_OVC_RAW since the last AMPA_SPK_OVC_CLR.

Amp A Thermal Warning Interrupts State (0x2016)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_THERMSHDN_END_STATE	AMPA_THERMSHDN_BGN_STATE	AMPA_THERMFB_END_STATE	AMPA_THERMFB_BGN_STATE	AMPA_THERMWARN2_END_STATE	AMPA_THERMWARN2_BGN_STATE	AMPA_THERMWARN1_END_STATE	AMPA_THERMWARN1_BGN_STATE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0

BIT	7	6	5	4	3	2	1	0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMSHDN_END_STATE	7	–	Unmaskable interrupt state, cleared by AMPA_THERMSHDN_END_CLR.	0: No rising edge of AMPA_THERMSHDN_END_RAW since the last AMPA_THERMSHDN_END_CLR. 1: The rising edge of AMPA_THERMSHDN_END_RAW since the last AMPA_THERMSHDN_END_CLR.
AMPA_THERMSHDN_BGN_STATE	6	–	Unmaskable interrupt state, cleared by AMPA_THERMSHDN_BGN_CLR.	0: No rising edge of AMPA_THERMSHDN_BGN_RAW since the last AMPA_THERMSHDN_BGN_CLR. 1: The rising edge of AMPA_THERMSHDN_BGN_RAW since the last AMPA_THERMSHDN_BGN_CLR.
AMPA_THERMFB_END_STATE	5	–	Unmaskable interrupt state, cleared by AMPA_THERMFB_END_CLR.	0: No rising edge of AMPA_THERMFB_END_RAW since the last AMPA_THERMFB_END_CLR. 1: The rising edge of AMPA_THERMFB_END_RAW since the last AMPA_THERMFB_END_CLR.
AMPA_THERMFB_BGN_STATE	4	–	Unmaskable interrupt state, cleared by AMPA_THERMFB_BGN_CLR.	0: No rising edge of AMPA_THERMFB_BGN_RAW since the last AMPA_THERMFB_BGN_CLR. 1: The rising edge of AMPA_THERMFB_BGN_RAW since the last AMPA_THERMFB_BGN_CLR.
AMPA_THERMWARN2_END_STATE	3	–	Unmaskable interrupt state, cleared by AMPA_THERMWARN2_END_CLR.	0: No rising edge of AMPA_THERMWARN2_END_RAW since the last AMPA_THERMWARN2_END_CLR. 1: The rising edge of AMPA_THERMWARN2_END_RAW since the last AMPA_THERMWARN2_END_CLR.
AMPA_THERMWARN2_BGN_STATE	2	–	Unmaskable interrupt state, cleared by AMPA_THERMWARN2_BGN_CLR.	0: No rising edge of AMPA_THERMWARN2_BGN_RAW since the last AMPA_THERMWARN2_BGN_CLR. 1: The rising edge of AMPA_THERMWARN2_BGN_RAW since the last AMPA_THERMWARN2_BGN_CLR.
AMPA_THERMWARN1_END_STATE	1	–	Unmaskable interrupt state, cleared by AMPA_THERMWARN1_END_CLR.	0: No rising edge of AMPA_THERMWARN1_END_RAW since the last AMPA_THERMWARN1_END_CLR. 1: The rising edge of AMPA_THERMWARN1_END_RAW since the last AMPA_THERMWARN1_END_CLR.
AMPA_THERMWARN1_BGN_STATE	0	–	Unmaskable interrupt state, cleared by AMPA_THERMWARN1_BGN_CLR.	0: No rising edge of AMPA_THERMWARN1_BGN_RAW since the last AMPA_THERMWARN1_BGN_CLR. 1: The rising edge of AMPA_THERMWARN1_BGN_RAW since the last AMPA_THERMWARN1_BGN_CLR.

Amp B Thermal Warning Interrupts State (0x2017)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_THERMSHDN_END_STATE	AMPB_THERMSHDN_BGN_STATE	AMPB_THERMFB_END_STATE	AMPB_THERMFB_BGN_STATE	AMPB_THERMWARN2_END_STATE	AMPB_THERMWARN2_BGN_STATE	AMPB_THERMWARN1_END_STATE	AMPB_THERMWARN1_BGN_STATE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMSHDN_END_STATE	7	–	Unmaskable interrupt state, cleared by AMPB_THERMSHDN_END_CLR.	0: No rising edge of AMPB_THERMSHDN_END_RAW since the last AMPB_THERMSHDN_END_CLR. 1: The rising edge of AMPB_THERMSHDN_END_RAW since the last AMPB_THERMSHDN_END_CLR.
AMPB_THERMSHDN_BGN_STATE	6	–	Unmaskable interrupt state, cleared by AMPB_THERMSHDN_BGN_CLR.	0: No rising edge of AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR. 1: The rising edge of AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR.
AMPB_THERMFB_END_STATE	5	–	Unmaskable interrupt state, cleared by AMPB_THERMFB_END_CLR.	0: No rising edge of AMPB_THERMFB_END_RAW since the last AMPB_THERMFB_END_CLR. 1: The rising edge of AMPB_THERMFB_END_RAW since the last AMPB_THERMFB_END_CLR.
AMPB_THERMFB_BGN_STATE	4	–	Unmaskable interrupt state, cleared by AMPB_THERMFB_BGN_CLR.	0: No rising edge of AMPB_THERMFB_BGN_RAW since the last AMPB_THERMFB_BGN_CLR. 1: The rising edge of AMPB_THERMFB_BGN_RAW since the last AMPB_THERMFB_BGN_CLR.
AMPB_THERMWARN2_END_STATE	3	–	Unmaskable interrupt state, cleared by AMPB_THERMWARN2_END_CLR.	0: No rising edge of AMPB_THERMWARN2_END_RAW since the last AMPB_THERMWARN2_END_CLR. 1: The rising edge of AMPB_THERMWARN2_END_RAW since the last AMPB_THERMWARN2_END_CLR.
AMPB_THERMWARN2_BGN_STATE	2	–	Unmaskable interrupt state, cleared by AMPB_THERMWARN2_BGN_CLR.	0: No rising edge of AMPB_THERMWARN2_BGN_RAW since the last AMPB_THERMWARN2_BGN_CLR. 1: The rising edge of AMPB_THERMWARN2_BGN_RAW since the last AMPB_THERMWARN2_BGN_CLR.
AMPB_THERMWARN1_END_STATE	1	–	Unmaskable interrupt state, cleared by AMPB_THERMWARN1_END_CLR.	0: No rising edge of AMPB_THERMWARN1_END_RAW since the last AMPB_THERMWARN1_END_CLR. 1: The rising edge of AMPB_THERMWARN1_END_RAW since the last AMPB_THERMWARN1_END_CLR.
AMPB_THERMWARN1_BGN_STATE	0	–	Unmaskable interrupt state, cleared by AMPB_THERMWARN1_BGN_CLR.	0: No rising edge of AMPB_THERMWARN1_BGN_RAW since the last AMPB_THERMWARN1_BGN_CLR. 1: The rising edge of

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				AMPB_THERMWARN1_BGN_RAW since the last AMPB_THERMWARN1_BGN_CLR.

BPE and DHT Interrupts State (0x201A)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_STATE	BPE_LEVEL_STATE	BPE_ACTIVE_END_STATE	BPE_ACTIVE_BGN_STATE	–	–	DHT_ACTIVE_END_STATE	DHT_ACTIVE_BGN_STATE
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_STATE	7	–	Unmaskable interrupt state, cleared by BPE_L0_CLR.	0: No rising edge of BPE_L0_RAW since the last BPE_L0_CLR. 1: The rising edge of BPE_L0_RAW since the last BPE_L0_CLR.
BPE_LEVEL_STATE	6	–	Unmaskable interrupt state, cleared by BPE_LEVEL_CLR.	0: No rising edge of BPE_LEVEL_RAW since the last BPE_LEVEL_CLR. 1: The rising edge of BPE_LEVEL_RAW since the last BPE_LEVEL_CLR.
BPE_ACTIVE_END_STATE	5	–	Unmaskable interrupt state, cleared by BPE_ACTIVE_END_CLR.	0: No rising edge of BPE_ACTIVE_END_RAW since the last BPE_ACTIVE_END_CLR. 1: The rising edge of BPE_ACTIVE_END_RAW since the last BPE_ACTIVE_END_CLR.
BPE_ACTIVE_BGN_STATE	4	–	Unmaskable interrupt state, cleared by BPE_ACTIVE_END_CLR.	0: No rising edge of BPE_ACTIVE_BGN_RAW since the last BPE_ACTIVE_BGN_CLR. 1: The rising edge of BPE_ACTIVE_BGN_RAW since the last BPE_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_STATE	1	–	Unmaskable interrupt state, cleared by DHT_ACTIVE_END_CLR.	0: No rising edge of DHT_ACTIVE_END_RAW since the last DHT_ACTIVE_END_CLR. 1: The rising edge of DHT_ACTIVE_END_RAW since the last DHT_ACTIVE_END_CLR.
DHT_ACTIVE_BGN_STATE	0	–	Unmaskable interrupt state, cleared by DHT_ACTIVE_BGN_CLR.	0: No rising edge of DHT_ACTIVE_BGN_RAW since the last DHT_ACTIVE_BGN_CLR. 1: The rising edge of DHT_ACTIVE_BGN_RAW since the last DHT_ACTIVE_BGN_CLR.

RMS Limiter Interrupts State (0x201B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_STATE	AMPB_RMS_LIM_ACTIVE_BGN_STATE	AMPA_RMS_LIM_ACTIVE_END_STATE	AMPA_RMS_LIM_ACTIVE_BGN_STATE
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_ACTIVE_END_STATE	3	–	Unmaskable interrupt state, cleared by AMPB_RMS_LIM_ACTIVE_END_CLR.	0: No rising edge of AMPB_RMS_LIM_ACTIVE_END_RAW since the last AMPB_RMS_LIM_ACTIVE_END_CLR. 1: The rising edge of AMPB_RMS_LIM_ACTIVE_END_RAW since the last AMPB_RMS_LIM_ACTIVE_END_CLR.
AMPB_RMS_LIM_ACTIVE_BGN_STATE	2	–	Unmaskable interrupt state, cleared by AMPB_RMS_LIM_ACTIVE_BGN_CLR.	0: No rising edge of AMPB_RMS_LIM_ACTIVE_BGN_RAW since the last AMPB_RMS_LIM_ACTIVE_BGN_CLR. 1: The rising edge of AMPB_RMS_LIM_ACTIVE_BGN_RAW since the last AMPB_RMS_LIM_ACTIVE_BGN_CLR.
AMPA_RMS_LIM_ACTIVE_END_STATE	1	–	Unmaskable interrupt state, cleared by AMPA_RMS_LIM_ACTIVE_BGN_CLR.	0: No rising edge of AMPA_RMS_LIM_ACTIVE_END_RAW since the last AMPA_RMS_LIM_ACTIVE_END_CLR. 1: The rising edge of AMPA_RMS_LIM_ACTIVE_END_RAW since the last AMPA_RMS_LIM_ACTIVE_END_CLR.
AMPA_RMS_LIM_ACTIVE_BGN_STATE	0	–	Unmaskable interrupt state, cleared by AMPA_RMS_LIM_ACTIVE_BGN_CLR.	0: No rising edge of AMPA_RMS_LIM_ACTIVE_BGN_RAW since the last AMPA_RMS_LIM_ACTIVE_BGN_CLR. 1: The rising edge of AMPA_RMS_LIM_ACTIVE_BGN_RAW since the last AMPA_RMS_LIM_ACTIVE_BGN_CLR.

Miscellaneous Interrupts State (0x201E)

BIT	7	6	5	4	3	2	1	0
Field	EXT_MUTE_STATE	–	–	–	–	–	AMPB_SPK_CLIP_STATE	AMPA_SPK_CLIP_STATE
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EXT_MUTE_STATE	7	–	Unmaskable interrupt state, cleared by EXT_MUTE_CLR.	0: No rising edge of EXT_MUTE_RAW since the last EXT_MUTE_CLR. 1: The rising edge of EXT_MUTE_RAW since the last EXT_MUTE_CLR.
AMPB_SPK_CLIP_STATE	1	–	Unmaskable interrupt state, cleared by AMPB_SPK_CLIP_CLR.	0: No rising edge of AMPB_SPK_CLIP_RAW since the last AMPB_SPK_CLIP_CLR. 1: The rising edge of AMPB_SPK_CLIP_RAW since the last AMPB_SPK_CLIP_CLR.
AMPA_SPK_CLIP_STATE	0	–	Unmaskable interrupt state, cleared by AMPA_SPK_CLIP_CLR.	0: No rising edge of AMPA_SPK_CLIP_RAW since the last AMPA_SPK_CLIP_CLR. 1: The rising edge of AMPA_SPK_CLIP_RAW since the last AMPA_SPK_CLIP_CLR.

Supply and OTP Interrupts Flag (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PVDD_UVLO_SHDN_FLAG	VBAT_UVLO_SHDN_FLAG	–	AVDD_UVLO_FLAG	DVDD_UVLO_FLAG	OTP_FAIL_FLAG

BIT	7	6	5	4	3	2	1	0
Reset	–	–	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	Read Only	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PVDD_UVLO_SHDN_FLAG	5	–	PVDD supply UVLO event maskable interrupt flag. Masked by PVDD_UVLO_SHDN_EN and cleared by PVDD_UVLO_SHDN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of PVDD_UVLO_SHDN_RAW since the last PVDD_UVLO_SHDN_CLR or PVDD_UVLO_SHDN_EN is low. 1: PVDD_UVLO_SHDN_EN is a high and rising edge of PVDD_UVLO_SHDN_RAW since the last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_FLAG	4	–	VBAT supply UVLO event maskable interrupt flag. Masked by VBAT_UVLO_SHDN_EN and cleared by VBAT_UVLO_SHDN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of VBAT_UVLO_SHDN_RAW since the last VBAT_UVLO_SHDN_CLR or VBAT_UVLO_SHDN_EN is low. 1: VBAT_UVLO_SHDN_EN is a high and rising edge of VBAT_UVLO_SHDN_RAW since the last VBAT_UVLO_SHDN_CLR.
AVDD_UVLO_FLAG	2	–	AVDD supply UVLO event maskable interrupt flag. Masked by AVDD_UVLO_EN and cleared by AVDD_UVLO_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AVDD_UVLO_RAW since the last AVDD_UVLO_CLR or AVDD_UVLO_EN is low. 1: AVDD_UVLO_EN is a high and rising edge of AVDD_UVLO_RAW since the last AVDD_UVLO_CLR.
DVDD_UVLO_FLAG	1	–	DVDD supply UVLO event maskable interrupt flag. Masked by DVDD_UVLO_EN and cleared by DVDD_UVLO_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DVDD_UVLO_RAW since the last DVDD_UVLO_CLR or DVDD_UVLO_EN is low. 1: DVDD_UVLO_EN is a high and rising edge of DVDD_UVLO_RAW since the last DVDD_UVLO_CLR.
OTP_FAIL_FLAG	0	–	OTP load routine fail event maskable interrupt flag. Masked by OTP_FAIL_EN and cleared by OTP_FAIL_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of OTP_FAIL_RAW since the last OTP_FAIL_CLR or OTP_FAIL_EN is low. 1: OTP_FAIL_EN is the high and rising edge of OTP_FAIL_RAW since the last OTP_FAIL_CLR.

Power Up and Down Interrupts Flag (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	PWRDN_DONE_FLAG	–	–	–	–	–	AMPB_PWRUP_DONE_FLAG	AMPA_PWRUP_DONE_FLAG
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_FLAG	7	–	Device power down done event maskable interrupt flag. Masked by PWRDN_DONE_EN and cleared by PWRDN_DONE_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of PWRDN_DONE_RAW since the last PWRDN_DONE_CLR or PWRDN_DONE_EN is low. 1: PWRDN_DONE_EN is the high and rising edge of PWRDN_DONE_RAW since the last PWRDN_DONE_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_PWRUP_DONE_FLAG	1	–	Device power up done event maskable interrupt flag. Masked by AMPB_PWRUP_DONE_EN and cleared by AMPB_PWRUP_DONE_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_PWRUP_DONE_RAW since the last AMPB_PWRUP_DONE_CLR or AMPB_PWRUP_DONE_EN is low. 1: AMPB_PWRUP_DONE_EN is the high and rising edge of AMPB_PWRUP_DONE_RAW since the last AMPB_PWRUP_DONE_CLR.
AMPA_PWRUP_DONE_FLAG	0	–	Device power up done event maskable interrupt flag. Masked by AMPA_PWRUP_DONE_EN and cleared by AMPA_PWRUP_DONE_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_PWRUP_DONE_RAW since the last AMPA_PWRUP_DONE_CLR or PWRUP_DONE_EN is low. 1: AMPA_PWRUP_DONE_EN is the high and rising edge of AMPA_PWRUP_DONE_RAW since the last AMPA_PWRUP_DONE_CLR.

Clock and Data Interrupts Flag (0x2023)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_RECOVER_FLAG	–	INT_CLK_ERR_FLAG	CLK_ERR_FLAG
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Read Only	–	Read Only	Read Only
Restriction	–	–	–	–	Normal	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLK_RECOVER_FLAG	3	–	PCM input clock error recovery event maskable interrupt flag. Masked by CLK_RECOVER_EN and cleared by CLK_RECOVER_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of CLK_RECOVER_RAW since the last CLK_RECOVER_CLR or CLK_RECOVER_EN is low. 1: BCLK_RECOVER_EN high and rising edge of BCLK_RECOVER_RAW since the last BCLK_RECOVER_CLR.
INT_CLK_ERR_FLAG	1	–	Internal clock monitor error event maskable interrupt flag. Masked by INT_CLK_ERR_EN and cleared by INT_CLK_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of INT_CLK_ERR_RAW since the last INT_CLK_ERR_CLR or INT_CLK_ERR_EN is low. 1: INT_CLK_ERR_EN high and rising edge of INT_CLK_ERR_RAW since the last INT_CLK_ERR_CLR.
CLK_ERR_FLAG	0	–	PCM input clock error event maskable interrupt flag. Masked by CLK_ERR_EN and cleared by CLK_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of CLK_ERR_RAW since the last CLK_ERR_CLR or CLK_ERR_EN is low. 1: CLK_ERR_EN high and rising edge of CLK_ERR_RAW since the last CLK_ERR_CLR.

Amplifier Output Fault Interrupts Flag (0x2025)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_INT_SPKMON_ERR_FLAG	AMPA_INT_SPKMON_ERR_FLAG	–	–	AMPB_SPK_OVC_FLAG	AMPA_SPK_OVC_FLAG
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	–	–	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_INT_SPKMON_ERR_FLAG	5	–	Internal speaker data monitor error event maskable interrupt flag. Masked by AMPB_INT_SPKMON_ERR_EN and cleared by AMPB_INT_SPKMON_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_INT_SPKMON_ERR_RAW since the last AMPB_INT_SPKMON_ERR_CLR or AMPB_INT_SPKMON_ERR_EN is low. 1: AMPB_INT_SPKMON_ERR_EN high and rising edge of AMPB_INT_SPKMON_ERR_RAW since the last AMPB_INT_SPKMON_ERR_CLR.
AMPA_INT_SPKMON_ERR_FLAG	4	–	Internal speaker data monitor error event maskable interrupt flag. Masked by AMPA_INT_SPKMON_ERR_EN and cleared by AMPA_INT_SPKMON_ERR_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_INT_SPKMON_ERR_RAW since the last AMPA_INT_SPKMON_ERR_CLR or AMPA_INT_SPKMON_ERR_EN is low 1: AMPA_INT_SPKMON_ERR_EN high and rising edge of AMPA_INT_SPKMON_ERR_RAW since the last AMPA_INT_SPKMON_ERR_CLR.
AMPB_SPK_OVC_FLAG	1	–	Speaker overcurrent event maskable interrupt flag. Masked by SPK_OVC_EN and cleared by SPK_OVC_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_SPK_OVC_RAW since the last AMPB_SPK_OVC_CLR or AMPB_SPK_OVC_EN is low. 1: AMPB_SPK_OVC_EN is the high and rising edge of AMPB_SPK_OVC_RAW since the last AMPB_SPK_OVC_CLR.
AMPA_SPK_OVC_FLAG	0	–	Speaker overcurrent event maskable interrupt flag. Masked by SPK_OVC_EN and cleared by SPK_OVC_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_SPK_OVC_RAW since the last AMPA_SPK_OVC_CLR or AMPA_SPK_OVC_EN is low. 1: AMPA_SPK_OVC_EN is the high and rising edge of AMPA_SPK_OVC_RAW since the last AMPA_SPK_OVC_CLR.

Amp A Thermal Interrupts Flag (0x2026)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_THERMSHDN_END_FLAG	AMPA_THERMSHDN_BGN_FLAG	AMPA_THERMFB_END_FLAG	AMPA_THERMFB_BGN_FLAG	AMPA_THERMWARN2_END_FLAG	AMPA_THERMWARN2_BGN_FLAG	AMPA_THERMWARN1_END_FLAG	AMPA_THERMWARN1_BGN_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMSHDN_END_FLAG	7	–	Amp A Thermal shutdown end event maskable interrupt flag. Masked by AMPA_THERMSHDN_END_EN and cleared by AMPA_THERMSHDN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMSHDN_END_RAW since the last AMPA_THERMSHDN_END_CLR or AMPA_THERMSHDN_END_EN is low. 1: AMPA_THERMSHDN_END_EN is the high and rising edge of AMPA_THERMSHDN_END_RAW since the last AMPA_THERMSHDN_END_CLR.
AMPA_THERMSHDN_BGN_FLAG	6	–	Amp A Thermal shutdown begin event maskable interrupt flag. Masked by AMPA_THERMSHDN_END_EN and cleared by AMPA_THERMSHDN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMSHDN_BGN_RAW since the last AMPA_THERMSHDN_BGN_CLR or AMPA_THERMSHDN_BGN_EN is low. 1: AMPA_THERMSHDN_BGN_EN is a high and rising edge of AMPA_THERMSHDN_BGN_RAW since the last AMPA_THERMSHDN_BGN_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMFB_END_FLAG	5	–	Amp A Thermal foldback end event maskable interrupt flag. Masked by AMPA_THERMFB_END_EN and cleared by AMPA_THERMFB_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMFB_END_RAW since the last AMPA_THERMFB_END_CLR or AMPA_THERMFB_END_EN is low. 1: AMPA_THERMFB_END_EN is the high and rising edge of AMPA_THERMFB_END_RAW since the last AMPA_THERMFB_END_CLR.
AMPA_THERMFB_BGN_FLAG	4	–	Amp A Thermal foldback begin event maskable interrupt flag. Masked by AMPA_THERMFB_BGN_EN and cleared by AMPA_THERMFB_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMFB_BGN_RAW since the last AMPA_THERMFB_BGN_CLR or AMPA_THERMFB_BGN_EN is low. 1: AMPA_THERMFB_BGN_EN is a high and rising edge of AMPA_THERMFB_BGN_RAW since the last AMPA_THERMFB_BGN_CLR.
AMPA_THERMWARN2_END_FLAG	3	–	Amp A Thermal-warning2 end event maskable interrupt flag. Masked by AMPA_THERMWARN2_END_EN and cleared by AMPA_THERMWARN2_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMWARN2_END_RAW since the last AMPA_THERMWARN2_END_CLR or AMPA_THERMWARN2_END_EN is low. 1: THERMWARN2_END_EN is the high and rising edge of THERMWARN2_END_RAW since the last THERMWARN2_END_CLR.
AMPA_THERMWARN2_BGN_FLAG	2	–	Amp A Thermal-warning2 begin event maskable interrupt flag. Masked by AMPA_THERMWARN2_BGN_EN and cleared by AMPA_THERMWARN2_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMWARN2_BGN_RAW since the last AMPA_THERMWARN2_BGN_CLR or THERMWARN2_BGN_EN is low. 1: AMPA_THERMWARN2_BGN_EN is the high and rising edge of AMPA_THERMWARN2_BGN_RAW since the last AMPA_THERMWARN2_BGN_CLR.
AMPA_THERMWARN1_END_FLAG	1	–	Amp A Thermal-warning1 end event maskable interrupt flag. Masked by AMPA_THERMWARN1_END_EN and cleared by AMPA_THERMWARN1_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMWARN1_END_RAW since the last AMPA_THERMWARN1_END_CLR or AMPA_THERMWARN1_END_EN is low. 1: AMPA_THERMWARN1_END_EN is the high and rising edge of AMPA_THERMWARN1_END_RAW since the last AMPA_THERMWARN1_END_CLR.
AMPA_THERMWARN1_BGN_FLAG	0	–	Amp A Thermal-warning1 begin event maskable interrupt flag. Masked by AMPA_THERMWARN1_BGN_EN and cleared by AMPA_THERMWARN1_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_THERMWARN1_BGN_RAW since the last AMPA_THERMWARN1_BGN_CLR or AMPA_THERMWARN1_BGN_EN is low. 1: AMPA_THERMWARN1_BGN_EN is the high and rising edge of AMPA_THERMWARN1_BGN_RAW since the last AMPA_THERMWARN1_BGN_CLR.

Amp B Thermal Interrupts Flag (0x2027)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_THERMSHDN_END_FLAG	AMPB_THERMSHDN_BGN_FLAG	AMPB_THERMFB_END_FLAG	AMPB_THERMFB_BGN_FLAG	AMPB_THERMWARN2_END_FLAG	AMPB_THERMWARN2_BGN_FLAG	AMPB_THERMWARN1_END_FLAG	AMPB_THERMWARN1_BGN_FLAG
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMSHDN_END_FLAG	7	–	Amp B Thermal shutdown end event maskable interrupt flag. Masked by AMPB_THERMSHDN_END_EN and cleared by AMPB_THERMSHDN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMSHDN_END_RAW since the last AMPB_THERMSHDN_END_CLR or AMPB_THERMSHDN_END_EN is low. 1: AMPB_THERMSHDN_END_EN is the high and rising edge of AMPB_THERMSHDN_END_RAW since the last AMPB_THERMSHDN_END_CLR.
AMPB_THERMSHDN_BGN_FLAG	6	–	Amp B Thermal shutdown begins event maskable interrupt flag. Masked by AMPB_THERMSHDN_END_EN and cleared by AMPB_THERMSHDN_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR or AMPB_THERMSHDN_BGN_EN is low. 1: AMPB_THERMSHDN_BGN_EN is the high and rising edge of AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR.
AMPB_THERMFB_END_FLAG	5	–	Amp B Thermal foldback end event maskable interrupt flag. Masked by AMPB_THERMFB_END_EN and cleared by AMPB_THERMFB_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMFB_END_RAW since the last AMPB_THERMFB_END_CLR or AMPB_THERMFB_END_EN is low. 1: AMPB_THERMFB_END_EN is the high and rising edge of AMPB_THERMFB_END_RAW since the last AMPB_THERMFB_END_CLR.
AMPB_THERMFB_BGN_FLAG	4	–	Amp B Thermal foldback begin event maskable interrupt flag. Masked by AMPB_THERMFB_BGN_EN and cleared by AMPB_THERMFB_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMFB_BGN_RAW since the last AMPB_THERMFB_BGN_CLR or AMPB_THERMFB_BGN_EN is low. 1: AMPB_THERMFB_BGN_EN is the high and rising edge of AMPB_THERMFB_BGN_RAW since the last AMPB_THERMFB_BGN_CLR.
AMPB_THERMWARN2_END_FLAG	3	–	Amp B Thermal-warning2 end event maskable interrupt flag. Masked by AMPB_THERMWARN2_END_EN and cleared by AMPB_THERMWARN2_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMWARN2_END_RAW since the last AMPB_THERMWARN2_END_CLR or AMPB_THERMWARN2_END_EN is low. 1: AMPB_THERMWARN2_END_EN is the high and rising edge of AMPB_THERMWARN2_END_RAW since the last AMPB_THERMWARN2_END_CLR.
AMPB_THERMWARN2_BGN_FLAG	2	–	Amp B Thermal-warning2 begin event maskable interrupt flag. Masked by AMPB_THERMWARN2_BGN_EN and cleared by AMPB_THERMWARN2_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMWARN2_BGN_RAW since the last AMPB_THERMWARN2_BGN_CLR or AMPB_THERMWARN2_BGN_EN is low. 1: AMPB_THERMWARN2_BGN_EN is the high and rising edge of AMPB_THERMWARN2_BGN_RAW since the last AMPB_THERMWARN2_BGN_CLR.
AMPB_THERMWARN1_END_FLAG	1	–	Amp B Thermal-warning1 end event maskable interrupt flag. Masked by AMPB_THERMWARN1_END_EN and cleared by AMPB_THERMWARN1_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMWARN1_END_RAW since the last AMPB_THERMWARN1_END_CLR or AMPB_THERMWARN1_END_EN is low. 1: AMPB_THERMWARN1_END_EN is the high and rising edge of AMPB_THERMWARN1_END_RAW since the last AMPB_THERMWARN1_END_CLR.
AMPB_THERMWARN1_BGN_FLAG	0	–	Amp B Thermal-warning1 begin event maskable interrupt flag. Masked by AMPB_THERMWARN1_BGN_EN and cleared by AMPB_THERMWARN1_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_THERMWARN1_BGN_RAW since the last AMPB_THERMWARN1_BGN_CLR or AMPB_THERMWARN1_BGN_EN is low. 1: AMPB_THERMWARN1_BGN_EN is the high and rising edge of AMPB_THERMWARN1_BGN_RAW since the last AMPB_THERMWARN1_BGN_CLR.

BPE and DHT Interrupts Flag (0x202A)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_FLAG	BPE_LEVEL_FLAG	BPE_ACTIVE_END_FLAG	BPE_ACTIVE_BGN_FLAG	–	–	DHT_ACTIVE_END_FLAG	DHT_ACTIVE_BGN_FLAG
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	Read Only	Read Only
Restriction	Normal	Normal	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_FLAG	7	–	Brownout-protection engine level 0 entry event maskable interrupt flag. Masked by BPE_L0_EN and cleared by BPE_L0_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of BPE_L0_RAW since the last BPE_L0_CLR or BPE_L0_EN is low. 1: BPE_L0_EN high and rising edge of BPE_L0_RAW since the last BPE_L0_CLR.
BPE_LEVEL_FLAG	6	–	Brownout-protection engine level change maskable interrupt flag. Masked by BPE_LEVEL_EN and cleared by BPE_LEVEL_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of BPE_LEVEL_RAW since the last BPE_LEVEL_CLR or BPE_LEVEL_EN is low. 1: BPE_LEVEL_EN high and rising edge of BPE_LEVEL_RAW since the last BPE_LEVEL_CLR.
BPE_ACTIVE_END_FLAG	5	–	Brownout-protection engine active end maskable interrupt flag. Masked by BPE_ACTIVE_END_EN and cleared by BPE_ACTIVE_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of BPE_ACTIVE_END_RAW since the last BPE_ACTIVE_END_CLR or BPE_ACTIVE_END_EN is low. 1: BPE_ACTIVE_END_EN high and rising edge of BPE_ACTIVE_END_RAW since the last BPE_ACTIVE_END_CLR.
BPE_ACTIVE_BGN_FLAG	4	–	Brownout-protection engine active end maskable interrupt flag. Masked by BPE_ACTIVE_BGN_EN and cleared by BPE_ACTIVE_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of BPE_ACTIVE_BGN_RAW since the last BPE_ACTIVE_BGN_CLR or BPE_ACTIVE_BGN_EN is low. 1: BPE_ACTIVE_BGN_EN high and rising edge of BPE_ACTIVE_BGN_RAW since the last BPE_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_FLAG	1	–	DHT active end event maskable interrupt flag. Masked by DHT_ACTIVE_END_EN and cleared by DHT_ACTIVE_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DHT_ACTIVE_END_RAW since the last DHT_ACTIVE_END_CLR or DHT_ACTIVE_END_EN is low. 1: DHT_ACTIVE_END_EN is the high and rising edge of DHT_ACTIVE_END_RAW since the last DHT_ACTIVE_END_CLR.
DHT_ACTIVE_BGN_FLAG	0	–	DHT active begin event maskable interrupt flag. Masked by DHT_ACTIVE_BGN_EN and cleared by DHT_ACTIVE_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of DHT_ACTIVE_BGN_RAW since the last DHT_ACTIVE_BGN_CLR or DHT_ACTIVE_BGN_EN is low. 1: DHT_ACTIVE_BGN_EN is the high and rising edge of DHT_ACTIVE_BGN_RAW since the last DHT_ACTIVE_BGN_CLR.

RMS Limiter Interrupts Flag (0x202B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_FLAG	AMPB_RMS_LIM_ACTIVE_BGN_FLAG	AMPA_RMS_LIM_ACTIVE_END_FLAG	AMPA_RMS_LIM_ACTIVE_BGN_FLAG
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_ACTIVE_END_FLAG	3	–	Amplifier B RMS Limiter Active End event maskable interrupt flag. Masked by AMPB_RMS_LIM_ACTIVE_END_EN and cleared by AMPB_RMS_LIM_ACTIVE_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_RMS_LIM_ACTIVE_END_RAW since the last AMPB_RMS_LIM_ACTIVE_END_CLR or AMPB_RMS_LIM_ACTIVE_END_EN is low. 1: AMPB_RMS_LIM_ACTIVE_END_EN high and rising edge of AMPB_RMS_LIM_ACTIVE_END_RAW since the last AMPB_RMS_LIM_ACTIVE_END_CLR.
AMPB_RMS_LIM_ACTIVE_BGN_FLAG	2	–	Amplifier B RMS Limiter Active event maskable interrupt flag. Masked by AMPB_RMS_LIM_ACTIVE_BGN_EN and cleared by AMPB_RMS_LIM_ACTIVE_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_RMS_LIM_ACTIVE_BGN_RAW since the last AMPB_RMS_LIM_ACTIVE_BGN_CLR or AMPB_RMS_LIM_ACTIVE_BGN_EN is low. 1: AMPB_RMS_LIM_ACTIVE_BGN_EN high and rising edge of AMPB_RMS_LIM_ACTIVE_BGN_RAW since the last AMPB_RMS_LIM_ACTIVE_BGN_CLR.
AMPA_RMS_LIM_ACTIVE_END_FLAG	1	–	Amplifier A RMS Limiter Active End event maskable interrupt flag. Masked by AMPA_RMS_LIM_ACTIVE_END_EN and cleared by AMPA_RMS_LIM_ACTIVE_END_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_RMS_LIM_ACTIVE_END_RAW since the last AMPA_RMS_LIM_ACTIVE_END_CLR or AMPA_RMS_LIM_ACTIVE_END_EN is low. 1: AMPA_RMS_LIM_ACTIVE_END_EN high and rising edge of AMPA_RMS_LIM_ACTIVE_END_RAW since the last AMPA_RMS_LIM_ACTIVE_END_CLR.
AMPA_RMS_LIM_ACTIVE_BGN_FLAG	0	–	Amplifier A RMS Limiter Active event maskable interrupt flag. Masked by AMPA_RMS_LIM_ACTIVE_BGN_EN and cleared by AMPA_RMS_LIM_ACTIVE_BGN_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_RMS_LIM_ACTIVE_BGN_RAW since the last AMPA_RMS_LIM_ACTIVE_BGN_CLR or AMPA_RMS_LIM_ACTIVE_BGN_EN is low. 1: AMPA_RMS_LIM_ACTIVE_BGN_EN high and rising edge of AMPA_RMS_LIM_ACTIVE_BGN_RAW since the last AMPA_RMS_LIM_ACTIVE_BGN_CLR.

Miscellaneous Device Interrupts Flag (0x202E)

BIT	7	6	5	4	3	2	1	0
Field	EXT_MUTE_FLAG	–	–	–	–	–	AMPB_SPK_CLIP_FLAG	AMPA_SPK_CLIP_FLAG
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Read Only	–	–	–	–	–	Read Only	Read Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EXT_MUTE_FLAG	7	–	AVDD supply UVLO event maskable interrupt flag. Masked by AVDD_UVLO_EN and cleared by AVDD_UVLO_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of EXT_MUTE_RAW since the last EXT_MUTE_CLR or EXT_MUTE_EN is low. 1: EXT_MUTE_EN is the high and rising edge of EXT_MUTE_RAW since the last EXT_MUTE_CLR.
AMPB_SPK_CLIP_FLAG	1	–	Amp B Internal speaker data monitor error event maskable interrupt flag. Masked by AMPB_SPK_CLIP_EN and cleared by AMPB_SPK_CLIP_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPB_SPK_CLIP_RAW since the last AMPB_SPK_CLIP_CLR or AMPB_SPK_CLIP_EN is low. 1: AMPB_SPK_CLIP_EN high and rising edge of AMPB_SPK_CLIP_RAW since the last AMPB_SPK_CLIP_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_CLIP_FLAG	0	–	Amp A Internal speaker data monitor error event maskable interrupt flag. Masked by AMPA_SPK_CLIP_EN and cleared by AMPA_SPK_CLIP_CLR. If IRQ is enabled, an interrupt is generated on a flag bit rising edge.	0: No rising edge of AMPA_SPK_CLIP_RAW since the last AMPA_SPK_CLIP_CLR or AMPA_SPK_CLIP_EN is low. 1: AMPA_SPK_CLIP_EN high and rising edge of AMPA_SPK_CLIP_RAW since the last AMPA_SPK_CLIP_CLR.

Supply and OTP Interrupts Enable (0x2030)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PVDD_UVLO_SHDN_EN	VBAT_UVLO_SHDN_EN	–	AVDD_UVLO_EN	DVDD_UVLO_EN	OTP_FAIL_EN
Reset	–	–	0b0	0b0	–	0b0	0b0	0b1
Access Type	–	–	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read
Restriction	–	–	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PVDD_UVLO_SHDN_EN	5	–	Enable (unmask) control for PVDD_UVLO_SHDN_FLAG.	0: PVDD_UVLO_SHDN_FLAG cannot go high. 1: PVDD_UVLO_SHDN_FLAG goes high if there is a rising edge on PVDD_UVLO_SHDN_RAW since the last PVDD_UVLO_SHDN_CLR.
VBAT_UVLO_SHDN_EN	4	–	Enable (unmask) control for VBAT_UVLO_SHDN_FLAG.	0: VBAT_UVLO_SHDN_FLAG cannot go high. 1: VBAT_UVLO_SHDN_FLAG goes high if there is a rising edge on VBAT_UVLO_SHDN_RAW since the last VBAT_UVLO_SHDN_CLR.
AVDD_UVLO_EN	2	–	Enable (unmask) control for AVDD_UVLO_FLAG.	0: AVDD_UVLO_FLAG cannot go high. 1: AVDD_UVLO_FLAG goes high if there is a rising edge on AVDD_UVLO_RAW since the last AVDD_UVLO_CLR.
DVDD_UVLO_EN	1	–	Enable (unmask) control for DVDD_UVLO_FLAG.	0: DVDD_UVLO_FLAG cannot go high. 1: DVDD_UVLO_FLAG goes high if there is a rising edge on DVDD_UVLO_RAW since the last DVDD_UVLO_CLR.
OTP_FAIL_EN	0	–	Enable (unmask) control for OTP_FAIL_FLAG.	0: OTP_FAIL_FLAG cannot go high. 1: OTP_FAIL_FLAG goes high if there is a rising edge on OTP_FAIL_RAW since the last OTP_FAIL_CLR.

Power Up and Down Interrupts Enable (0x2031)

BIT	7	6	5	4	3	2	1	0
Field	PWRDN_DONE_EN	–	–	–	–	–	AMPB_PWRUP_DONE_EN	AMPA_PWRUP_DONE_EN
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Write, Read	–	–	–	–	–	Write, Read	Write, Read
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_EN	7	–	Enable (unmask) control for PWRDN_DONE_FLAG.	0: PWRDN_DONE_FLAG cannot go high. 1: PWRDN_DONE_FLAG goes high if there is a rising edge on PWRDN_DONE_RAW since the last PWRDN_DONE_CLR.
AMPB_PWRUP_DONE_EN	1	–	Enable (unmask) control for AMPB_PWRUP_DONE_FLAG.	0: AMPB_PWRUP_DONE_FLAG cannot go high. 1: AMPB_PWRUP_DONE_FLAG goes high if there is a rising edge on AMPB_PWRUP_DONE_RAW since the last AMPB_PWRUP_DONE_CLR.
AMPA_PWRUP_DONE_EN	0	–	Enable (unmask) control for AMPA_PWRUP_DONE_FLAG.	0: AMPA_PWRUP_DONE_FLAG cannot go high. 1: AMPA_PWRUP_DONE_FLAG goes high if there is a rising edge on AMPA_PWRUP_DONE_RAW since the last AMPA_PWRUP_DONE_CLR.

Clock and Data Interrupts Enable (0x2033)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_RECOVER_EN	–	INT_CLK_ERR_EN	CLK_ERR_EN
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Write, Read	–	Write, Read	Write, Read
Restriction	–	–	–	–	Normal	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLK_RECOVER_EN	3	–	Enable (unmask) control for CLK_RECOVER_FLAG.	0: CLK_RECOVER_FLAG cannot go high. 1: CLK_RECOVER_FLAG goes high if there is a rising edge on CLK_RECOVER_RAW since the last CLK_RECOVER_CLR.
INT_CLK_ERR_EN	1	–	Enable (unmask) control for INT_CLK_ERR_FLAG.	0: INT_CLK_ERR_FLAG cannot go high. 1: INT_CLK_ERR_FLAG goes high if there is a rising edge on INT_CLK_ERR_RAW since the last INT_CLK_ERR_CLR.
CLK_ERR_EN	0	–	Enable (unmask) control for CLK_ERR_FLAG.	0: CLK_ERR_FLAG cannot go high. 1: CLK_ERR_FLAG goes high if there is a rising edge on CLK_ERR_RAW since the last CLK_ERR_CLR.

Amplifier Output Fault Interrupts Enable (0x2035)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_INT_SPKMON_ERR_EN	AMPA_INT_SPKMON_ERR_EN	–	–	AMPB_SPK_OVC_EN	AMPA_SPK_OVC_EN
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	–	–	Write, Read	Write, Read
Restriction	–	–	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_INT_SPKMON_ERR_EN	5	–	Enable (unmask) control for AMPB_INT_SPKMON_ERR_FLAG.	0: AMPB_INT_SPKMON_ERR_FLAG cannot go high. 1: AMPB_INT_SPKMON_ERR_FLAG goes high if there is a rising edge on AMPB_INT_SPKMON_ERR_RAW since the last AMPB_INT_SPKMON_ERR_CLR..
AMPA_INT_SPKMON_ERR_EN	4	–	Enable (unmask) control for AMPA_INT_SPKMON_ERR_FLAG.	0: AMPA_INT_SPKMON_ERR_FLAG cannot go high. 1: AMPA_INT_SPKMON_ERR_FLAG goes high if there is a rising edge on AMPA_INT_SPKMON_ERR_RAW since the last AMPA_INT_SPKMON_ERR_CLR..
AMPB_SPK_OVC_EN	1	–	Enable (unmask) control for AMPB_SPK_OVC_FLAG.	0: AMPB_SPK_OVC_FLAG cannot go high. 1: AMPB_SPK_OVC_FLAG goes high if there is a rising edge on AMPB_SPK_OVC_RAW since the last AMPB_SPK_OVC_CLR.
AMPA_SPK_OVC_EN	0	–	Enable (unmask) control for AMPA_SPK_OVC_FLAG.	0: AMPA_SPK_OVC_FLAG cannot go high. 1: AMPA_SPK_OVC_FLAG goes high if there is a rising edge on AMPA_SPK_OVC_RAW since the last AMPA_SPK_OVC_CLR.

Amp A Thermal Interrupts Enable (0x2036)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_THERMSHDN_END_EN	AMPA_THERMSHDN_BGN_EN	AMPA_THERMFB_END_EN	AMPA_THERMFB_BGN_EN	AMPA_THERMWARN2_END_EN	AMPA_THERMWARN2_BGN_EN	AMPA_THERMWARN1_END_EN	AMPA_THERMWARN1_BGN_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMSHDN_END_EN	7	–	Enable (unmask) control for THERMSHDN_END_FLAG.	0: AMPA_THERMSHDN_END_FLAG cannot go high. 1: AMPA_THERMSHDN_END_FLAG goes high if there is a rising edge on AMPA_THERMSHDN_END_RAW since the last AMPA_THERMSHDN_END_CLR..
AMPA_THERMSHDN_BGN_EN	6	–	Enable (unmask) control for AMPA_THERMSHDN_BGN_FLAG.	0: AMPA_THERMSHDN_BGN_FLAG cannot go high. 1: AMPA_THERMSHDN_BGN_FLAG goes high if there is a rising edge on AMPA_THERMSHDN_BGN_RAW since the last AMPA_THERMSHDN_BGN_CLR..
AMPA_THERMFB_END_EN	5	–	Enable (unmask) control for AMPA_THERMFB_END_FLAG.	0: AMPA_THERMFB_END_FLAG cannot go high. 1: AMPA_THERMFB_END_FLAG goes high if there is a rising edge on AMPA_THERMFB_END_RAW since the last AMPA_THERMFB_END_CLR.
AMPA_THERMFB_BGN_EN	4	–	Enable (unmask) control for AMPA_THERMFB_BGN_FLAG.	0: AMPA_THERMFB_BGN_FLAG cannot go high. 1: AMPA_THERMFB_BGN_FLAG goes high if there is a rising edge on THERMFB_BGN_RAW since the last THERMFB_BGN_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMWARN2_END_EN	3	–	Enable (unmask) control for AMPA_THERMWARN2_END_FLAG.	0: AMPA_THERMWARN2_END_FLAG cannot go high. 1: AMPA_THERMWARN2_END_FLAG goes high if there is a rising edge on AMPA_THERMWARN2_END_RAW since the last AMPA_THERMWARN2_END_CLR.
AMPA_THERMWARN2_BGN_EN	2	–	Enable (unmask) control for AMPA_THERMWARN2_BGN_FLAG.	0: AMPA_THERMWARN2_BGN_FLAG cannot go high. 1: AMPA_THERMWARN2_BGN_FLAG goes high if there is a rising edge on AMPA_THERMWARN2_BGN_RAW since the last AMPA_THERMWARN2_BGN_CLR.
AMPA_THERMWARN1_END_EN	1	–	Enable (unmask) control for AMPA_THERMWARN1_END_FLAG.	0: AMPA_THERMWARN1_END_FLAG cannot go high. 1: AMPA_THERMWARN1_END_FLAG goes high if there is a rising edge on AMPA_THERMWARN1_END_RAW since the last AMPA_THERMWARN1_END_CLR.
AMPA_THERMWARN1_BGN_EN	0	–	Enable (unmask) control for AMPA_THERMWARN1_BGN_FLAG.	0: AMPA_THERMWARN1_BGN_FLAG cannot go high. 1: AMPA_THERMWARN1_BGN_FLAG goes high if there is a rising edge on AMPA_THERMWARN1_BGN_RAW since the last AMPA_THERMWARN1_BGN_CLR.

Amp B Thermal Interrupts Enable (0x2037)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_THERMSHDN_END_EN	AMPB_THERMSHDN_BGN_EN	AMPB_THERMFB_END_EN	AMPB_THERMFB_BGN_EN	AMPB_THERMWARN2_END_EN	AMPB_THERMWARN2_BGN_EN	AMPB_THERMWARN1_END_EN	AMPB_THERMWARN1_BGN_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMSHDN_END_EN	7	–	Enable (unmask) control for AMPB_THERMSHDN_BGN_FLAG.	0: AMPB_THERMSHDN_BGN_FLAG cannot go high. 1: AMPB_THERMSHDN_BGN_FLAG goes high if there is a rising edge on AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR.
AMPB_THERMSHDN_BGN_EN	6	–	Enable (unmask) control for AMPB_THERMSHDN_BGN_FLAG.	0: AMPB_THERMSHDN_BGN_FLAG cannot go high. 1: AMPB_THERMSHDN_BGN_FLAG goes high if there is a rising edge on AMPB_THERMSHDN_BGN_RAW since the last AMPB_THERMSHDN_BGN_CLR.
AMPB_THERMFB_END_EN	5	–	Enable (unmask) control for AMPB_THERMFB_END_FLAG.	0: AMPB_THERMFB_END_FLAG cannot go high. 1: AMPB_THERMFB_END_FLAG goes high if there is a rising edge on AMPB_THERMFB_END_RAW since the last AMPB_THERMFB_END_CLR.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMFB_BGN_EN	4	–	Enable (unmask) control for AMPB_THERMFB_BGN_FLAG.	0: AMPB_THERMFB_BGN_FLAG cannot go high. 1: AMPB_THERMFB_BGN_FLAG goes high if there is a rising edge on AMPB_THERMFB_BGN_RAW since the last AMPB_THERMFB_BGN_CLR.
AMPB_THERMWARN2_END_EN	3	–	Enable (unmask) control for AMPB_THERMWARN2_END_FLAG.	0: AMPB_THERMWARN2_END_FLAG cannot go high. 1: AMPB_THERMWARN2_END_FLAG goes high if there is a rising edge on AMPB_THERMWARN2_END_RAW since the last AMPB_THERMWARN2_END_CLR.
AMPB_THERMWARN2_BGN_EN	2	–	Enable (unmask) control for AMPB_THERMWARN2_BGN_FLAG.	0: AMPB_THERMWARN2_BGN_FLAG cannot go high. 1: AMPB_THERMWARN2_BGN_FLAG goes high if there is a rising edge on AMPB_THERMWARN2_BGN_RAW since the last AMPB_THERMWARN2_BGN_CLR.
AMPB_THERMWARN1_END_EN	1	–	Enable (unmask) control for AMPB_THERMWARN1_END_FLAG.	0: AMPB_THERMWARN1_END_FLAG cannot go high. 1: AMPB_THERMWARN1_END_FLAG goes high if there is a rising edge on AMPB_THERMWARN1_END_RAW since the last AMPB_THERMWARN1_END_CLR.
AMPB_THERMWARN1_BGN_EN	0	–	Enable (unmask) control for AMPB_THERMWARN1_BGN_FLAG.	0: AMPB_THERMWARN1_BGN_FLAG cannot go high. 1: AMPB_THERMWARN1_BGN_FLAG goes high if there is a rising edge on AMPB_THERMWARN1_BGN_RAW since the last AMPB_THERMWARN1_BGN_CLR.

BPE and DHT Interrupts Enable (0x203A)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_EN	BPE_LEVEL_EN	BPE_ACTIVE_END_EN	BPE_ACTIVE_BGN_EN	–	–	DHT_ACTIVE_END_EN	DHT_ACTIVE_BGN_EN
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_EN	7	–	Enable (unmask) control for BPE_L0_FLAG.	0: BPE_L0_FLAG cannot go high. 1: BPE_L0_FLAG goes high if there is a rising edge on BPE_L0_RAW since the last BPE_L0_CLR.
BPE_LEVEL_EN	6	–	Enable (unmask) control for BPE_LEVEL_FLAG.	0: BPE_LEVEL_FLAG cannot go high. 1: BPE_LEVEL_FLAG goes high if there is a rising edge on BPE_LEVEL_RAW since the last BPE_LEVEL_CLR.
BPE_ACTIVE_END_EN	5	–	Enable (unmask) control for BPE_ACTIVE_END_FLAG.	0: BPE_ACTIVE_END_FLAG cannot go high. 1: BPE_ACTIVE_END_FLAG goes high if there is a rising edge on BPE_ACTIVE_END_RAW since the last BPE_ACTIVE_END_CLR.
BPE_ACTIVE_BGN_EN	4	–	Enable (unmask) control for BPE_ACTIVE_BGN_FLAG.	0: BPE_ACTIVE_BGN_FLAG cannot go high. 1: BPE_ACTIVE_BGN_FLAG goes high if there

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				is a rising edge on BPE_ACTIVE_BGN_RAW since the last BPE_ACTIVE_BGN_CLR.
DHT_ACTIVE_END_EN	1	–	Enable (unmask) control for DHT_ACTIVE_END_FLAG.	0: DHT_ACTIVE_END_FLAG cannot go high. 1: DHT_ACTIVE_END_FLAG goes high if there is a rising edge on DHT_ACTIVE_END_RAW since the last DHT_ACTIVE_END_CLR.
DHT_ACTIVE_BGN_EN	0	–	Enable (unmask) control for DHT_ACTIVE_BGN_FLAG.	0: DHT_ACTIVE_BGN_FLAG cannot go high. 1: DHT_ACTIVE_BGN_FLAG goes high if there is a rising edge on DHT_ACTIVE_BGN_RAW since the last DHT_ACTIVE_BGN_CLR.

RMS Limiter Interrupts Enable (0x203B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_EN	AMPB_RMS_LIM_ACTIVE_BGN_EN	AMPA_RMS_LIM_ACTIVE_END_EN	AMPA_RMS_LIM_ACTIVE_BGN_EN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_ACTIVE_END_EN	3	–	Enable (unmask) control for AMPB_RMS_LIM_ACTIVE_END_FLAG.	0: AMPB_RMS_LIM_ACTIVE_END_FLAG cannot go high. 1: AMPB_RMS_LIM_ACTIVE_END_FLAG goes high if there is a rising edge on AMPB_RMS_LIM_ACTIVE_END_RAW since the last AMPB_RMS_LIM_ACTIVE_END_CLR.
AMPB_RMS_LIM_ACTIVE_BGN_EN	2	–	Enable (unmask) control for AMPB_RMS_LIM_ACTIVE_BGN_FLAG.	0: AMPB_RMS_LIM_ACTIVE_BGN_FLAG cannot go high. 1: AMPB_RMS_LIM_ACTIVE_BGN_FLAG goes high if there is a rising edge on AMPB_RMS_LIM_ACTIVE_BGN_RAW since the last AMPB_RMS_LIM_ACTIVE_BGN_CLR.
AMPA_RMS_LIM_ACTIVE_END_EN	1	–	Enable (unmask) control for AMPA_RMS_LIM_ACTIVE_END_FLAG.	0: AMPA_RMS_LIM_ACTIVE_END_FLAG cannot go high. 1: AMPA_RMS_LIM_ACTIVE_END_FLAG goes high if there is a rising edge on AMPA_RMS_LIM_ACTIVE_END_RAW since the last AMPA_RMS_LIM_ACTIVE_END_CLR.
AMPA_RMS_LIM_ACTIVE_BGN_EN	0	–	Enable (unmask) control for AMPA_RMS_LIM_ACTIVE_BGN_FLAG.	0: AMPA_RMS_LIM_ACTIVE_BGN_FLAG cannot go high. 1: AMPA_RMS_LIM_ACTIVE_BGN_FLAG goes high if there is a rising edge on AMPA_RMS_LIM_ACTIVE_BGN_RAW since the last AMPA_RMS_LIM_ACTIVE_BGN_CLR.

Miscellaneous Device Interrupts Enable (0x203E)

BIT	7	6	5	4	3	2	1	0
Field	EXT_MUTE_EN	–	–	–	–	–	AMPB_SPK_CLIP_EN	AMPA_SPK_CLIP_EN
Reset	0b0	–	–	–	–	–	0b0	0b0

BIT	7	6	5	4	3	2	1	0
Access Type	Write, Read	–	–	–	–	–	Write, Read	Write, Read
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EXT_MUTE_EN	7	–	Enable (unmask) control for EXT_MUTE_FLAG.	0: EXT_MUTE_FLAG cannot go high. 1: EXT_MUTE_FLAG goes high if there is a rising edge on EXT_MUTE_RAW since the last EXT_MUTE_CLR.
AMPB_SPK_CLIP_EN	1	–	Enable (unmask) control for AMPB_SPK_CLIP_FLAG.	0: AMPB_SPK_CLIP_FLAG cannot go high. 1: AMPB_SPK_CLIP_FLAG goes high if there is a rising edge on AMPB_SPK_CLIP_RAW since the last AMPB_SPK_CLIP_CLR.
AMPA_SPK_CLIP_EN	0	–	Enable (unmask) control for AMPA_SPK_CLIP_FLAG.	0: AMPA_SPK_CLIP_FLAG cannot go high. 1: AMPA_SPK_CLIP_FLAG goes high if there is a rising edge on AMPA_SPK_CLIP_RAW since the last AMPA_SPK_CLIP_CLR.

Supply and OTP Interrupts Clear (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PVDD_UVLO_SHDN_CLR	VBAT_UVLO_SHDN_CLR	–	AVDD_UVLO_CLR	DVDD_UVLO_CLR	OTP_FAIL_CLR
Reset	–	–	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	–	Write Only	Write Only	–	Write Only	Write Only	Write Only
Restriction	–	–	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PVDD_UVLO_SHDN_CLR	5	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears PVDD_UVLO_SHDN_STATE and PVDD_UVLO_SHDN_FLAG to zero.
VBAT_UVLO_SHDN_CLR	4	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears VBAT_UVLO_SHDN_STATE and VBAT_UVLO_SHDN_FLAG to zero.
AVDD_UVLO_CLR	2	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AVDD_UVLO_STATE and AVDD_UVLO_FLAG to zero.
DVDD_UVLO_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DVDD_UVLO_STATE and DVDD_UVLO_FLAG to zero.
OTP_FAIL_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears OTP_FAIL_STATE and OTP_FAIL_FLAG to zero.

Power Up and Down Interrupts Clear (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	PWRDN_DONE_CLR	–	–	–	–	–	AMPB_PWRUP_DONE_CLR	AMPA_PWRUP_DONE_CLR

BIT	7	6	5	4	3	2	1	0
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Write Only	–	–	–	–	–	Write Only	Write Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_CLR	7	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears PWRDN_DONE_STATE and PWRDN_DONE_FLAG to zero.
AMPB_PWRUP_DONE_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_PWRUP_DONE_STATE and AMPB_PWRUP_DONE_FLAG to zero.
AMPA_PWRUP_DONE_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect 1: Writing one clears AMPA_PWRUP_DONE_STATE and. AMPA_PWRUP_DONE_FLAG to zero.

Clock and Data Interrupts Clear (0x2043)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLK_RECOVER_CLR	–	INT_CLK_ERR_CLR	CLK_ERR_CLR
Reset	–	–	–	–	0b0	–	0b0	0b0
Access Type	–	–	–	–	Write Only	–	Write Only	Write Only
Restriction	–	–	–	–	Normal	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLK_RECOVER_CLR	3	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears CLK_RECOVER_STATE and CLK_RECOVER_FLAG to zero.
INT_CLK_ERR_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears INT_CLK_ERR_STATE and INT_CLK_ERR_FLAG to zero.
CLK_ERR_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears CLK_ERR_STATE and CLK_ERR_FLAG to zero.

Amplifier Output Fault Interrupts Clear (0x2045)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_INT_SPKMON_ERR_CLR	AMPA_INT_SPKMON_ERR_CLR	–	–	AMPB_SPK_OVC_CLR	AMPA_SPK_OVC_CLR
Reset	–	–	0b0	0b0	–	–	0b0	0b0
Access Type	–	–	Write Only	Write Only	–	–	Write Only	Write Only
Restriction	–	–	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_INT_SPKMON_ERR_CLR	5	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_INT_SPKMON_ERR_STATE and AMPB_INT_SPKMON_ERR_FLAG to zero.
AMPA_INT_SPKMON_ERR_CLR	4	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_INT_SPKMON_ERR_STATE and AMPA_INT_SPKMON_ERR_FLAG to zero.
AMPB_SPK_OVC_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_SPK_OVC_STATE and AMPB_SPK_OVC_FLAG to zero.
AMPA_SPK_OVC_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_SPK_OVC_STATE and AMPA_SPK_OVC_FLAG to zero.

Amp A Thermal Interrupts Clear (0x2046)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_THERMSHDN_END_CLR	AMPA_THERMSHDN_BGN_CLR	AMPA_THERMFB_END_CLR	AMPA_THERMFB_BGN_CLR	AMPA_THERMWARN2_END_CLR	AMPA_THERMWARN2_BGN_CLR	AMPA_THERMWARN1_END_CLR	AMPA_THERMWARN1_BGN_CLR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMSHDN_END_CLR	7	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMSHDN_END_STATE and AMPA_THERMSHDN_END_FLAG to zero.
AMPA_THERMSHDN_BGN_CLR	6	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMSHDN_BGN_STATE and AMPA_THERMSHDN_BGN_FLAG to zero.
AMPA_THERMFB_END_CLR	5	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMFB_END_STATE and AMPA_THERMFB_END_FLAG to zero.
AMPA_THERMFB_BGN_CLR	4	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMFB_BGN_STATE and AMPA_THERMFB_BGN_FLAG to zero.
AMPA_THERMWARN2_END_CLR	3	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMWARN2_END_STATE and AMPA_THERMWARN2_END_FLAG to zero.
AMPA_THERMWARN2_BGN_CLR	2	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMWARN2_BGN_STATE and AMPA_THERMWARN2_BGN_FLAG to zero.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_THERMWARN1_END_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMWARN1_END_STATE and AMPA_THERMWARN1_END_FLAG to zero.
AMPA_THERMWARN1_BGN_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_THERMWARN1_BGN_STATE and AMPA_THERMWARN1_BGN_FLAG to zero.

Amp B Thermal Interrupts Clear (0x2047)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_THERMSHDN_END_CLR	AMPB_THERMSHDN_BGN_CLR	AMPB_THERMFB_END_CLR	AMPB_THERMFB_BGN_CLR	AMPB_THERMWARN2_END_CLR	AMPB_THERMWARN2_BGN_CLR	AMPB_THERMWARN1_END_CLR	AMPB_THERMWARN1_BGN_CLR
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only	Write Only
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_THERMSHDN_END_CLR	7	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMSHDN_END_STATE and AMPB_THERMSHDN_END_FLAG to zero.
AMPB_THERMSHDN_BGN_CLR	6	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMSHDN_BGN_STATE and AMPB_THERMSHDN_BGN_FLAG to zero.
AMPB_THERMFB_END_CLR	5	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMFB_END_STATE and AMPB_THERMFB_END_FLAG to zero.
AMPB_THERMFB_BGN_CLR	4	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMFB_BGN_STATE and AMPB_THERMFB_BGN_FLAG to zero.
AMPB_THERMWARN2_END_CLR	3	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMWARN2_END_STATE and AMPB_THERMWARN2_END_FLAG to zero.
AMPB_THERMWARN2_BGN_CLR	2	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMWARN2_BGN_STATE and AMPB_THERMWARN2_BGN_FLAG to zero.
AMPB_THERMWARN1_END_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMWARN1_END_STATE and AMPB_THERMWARN1_END_FLAG to zero.
AMPB_THERMWARN1_BGN_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_THERMWARN1_BGN_STATE and AMPB_THERMWARN1_BGN_FLAG to zero.

BPE and DHT Interrupts Clear (0x204A)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_CLR	BPE_LEVEL_CLR	BPE_ACTIVE_END_CLR	BPE_ACTIVE_BGN_CLR	–	–	DHT_ACTIVE_END_CLR	DHT_ACTIVE_BGN_CLR
Reset	0b0	0b0	0b0	0b0	–	–	0b0	0b0
Access Type	Write Only	Write Only	Write Only	Write Only	–	–	Write Only	Write Only
Restriction	Normal	Normal	Normal	Normal	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_CLR	7	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears BPE_L0_STATE and BPE_L0_FLAG to zero.
BPE_LEVEL_CLR	6	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears BPE_LEVEL_STATE and BPE_LEVEL_FLAG to zero.
BPE_ACTIVE_END_CLR	5	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears BPE_ACTIVE_END_STATE and BPE_ACTIVE_END_FLAG to zero.
BPE_ACTIVE_BGN_CLR	4	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears BPE_ACTIVE_BGN_STATE and BPE_ACTIVE_BGN_FLAG to zero.
DHT_ACTIVE_END_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DHT_ACTIVE_END_STATE and DHT_ACTIVE_END_FLAG to zero.
DHT_ACTIVE_BGN_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears DHT_ACTIVE_BGN_STATE and DHT_ACTIVE_BGN_FLAG to zero.

RMS Limiter Interrupts Clear (0x204B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_ACTIVE_END_CLR	AMPB_RMS_LIM_ACTIVE_BGN_CLR	AMPA_RMS_LIM_ACTIVE_END_CLR	AMPA_RMS_LIM_ACTIVE_BGN_CLR
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write Only	Write Only	Write Only	Write Only
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_ACTIVE_END_CLR	3	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_RMS_LIM_ACTIVE_END_STATE and AMPB_RMS_LIM_ACTIVE_END_FLAG to zero.
AMPB_RMS_LIM_ACTIVE_BGN_CLR	2	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_RMS_LIM_ACTIVE_BGN_STATE and

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				AMPB_RMS_LIM_ACTIVE_BGN_FLAG to zero.
AMPA_RMS_LIM_ACTIVE_END_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_RMS_LIM_ACTIVE_END_STATE and AMPA_RMS_LIM_ACTIVE_END_FLAG to zero.
AMPA_RMS_LIM_ACTIVE_BGN_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_RMS_LIM_ACTIVE_BGN_STATE and AMPA_RMS_LIM_ACTIVE_BGN_FLAG to zero.

Miscellaneous Device Interrupts Clear (0x204E)

BIT	7	6	5	4	3	2	1	0
Field	EXT_MUTE_CLR	–	–	–	–	–	AMPB_SPK_CLIP_CLR	AMPA_SPK_CLIP_CLR
Reset	0b0	–	–	–	–	–	0b0	0b0
Access Type	Write Only	–	–	–	–	–	Write Only	Write Only
Restriction	Normal	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EXT_MUTE_CLR	7	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears EXT_MUTE_STATE and EXT_MUTE_FLAG to zero.
AMPB_SPK_CLIP_CLR	1	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPB_SPK_CLIP_STATE and AMPB_SPK_CLIP_FLAG to zero.
AMPA_SPK_CLIP_CLR	0	–	Clears associated FLAG and STATE bits.	0: Writing zero has no effect. 1: Writing one clears AMPA_SPK_CLIP_STATE and AMPA_SPK_CLIP_FLAG to zero.

GPIO Select (0x2050)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO3_SEL[1:0]		GPIO2_SEL[1:0]		GPIO1_SEL[1:0]	
Reset	–	–	0b01		0b00		0b11	
Access Type	–	–	Write, Read		Write, Read		Write, Read	
Restriction	–	–	Normal		Normal		Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
GPIO3_SEL	5:4	EN	Selects I/O function for GPIO3 pin.	0: GPIO is configured as IRQ output. 1: GPIO is configured as an ICC pin. 2: GPIO is configured as an Envelope Tracking Output pin. 3: GPIO is configured as DOUT.
GPIO2_SEL	3:2	EN	Selects I/O function for GPIO2 pin.	0: GPIO is configured as IRQ output. 1: GPIO is configured as an ICC pin. 2: GPIO is configured as an Envelope Tracking

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				Output pin. 3: GPIO is configured as DOUT.
GPIO1_SEL	1:0	EN	Selects I/O function for GPIO1 pin	0: GPIO is configured as IRQ output. 1: GPIO is configured as an ICC pin. 2: GPIO is configured as an Envelope Tracking Output pin. 3: GPIO is configured as DOUT.

Pin Config (0x2052)

BIT	7	6	5	4	3	2	1	0
Field	–	–	GPIO3_DRV[1:0]		GPIO2_DRV[1:0]		GPIO1_DRV[1:0]	
Reset	–	–	0b01		0b01		0b01	
Access Type	–	–	Write, Read		Write, Read		Write, Read	
Restriction	–	–	Normal		Normal		Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
GPIO3_DRV	5:4	EN	Configures the output drive strength of GPIO pin.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode
GPIO2_DRV	3:2	EN	Configures the output drive strength of GPIO pin.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode
GPIO1_DRV	1:0	EN	Configures the output drive strength of GPIO pin.	00: Reduced drive mode 01: Normal drive mode 10: High drive mode 11: Maximum drive mode

IRQ Control (0x205F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	IRQ_MODE	IRQ_POL	IRQ_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read
Restriction	–	–	–	–	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IRQ_MODE	2	IRQ	Controls the drive mode of the IRQ output.	0: Open-drain output (an external pull-up resistor is required) 1: CMOS push-pull output
IRQ_POL	1	IRQ	Controls the IRQ output assert polarity.	0: IRQ output is low when any interrupt FLAG bits are high (i.e., active low). 1: IRQ output is high when any interrupt FLAG bits are high (i.e., active high).
IRQ_EN	0	–	Enables the IRQ Output.	0: IRQ output is disabled and is Hi-Z 1: IRQ output is enabled and controlled by the interrupt controller

Mute Ramp Control (0x2060)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	MUTE_RMPDN_BYPASS	UNMUTE_RMPUP_BYPASS
Reset	–	–	–	–	–	–	0b1	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MUTE_RMPDN_BYPASS	1	–	Controls whether the speaker amplifier path volume is internally ramped down during volume changes.	0: Volume ramp enabled 1: Volume ramp bypassed
UNMUTE_RMPUP_BYPASS	0	–	Controls whether the speaker amplifier path volume is ramped up during unmute event	0: Volume ramp enabled 1: Volume ramp bypassed

Clock Monitor Control (0x21F0)

BIT	7	6	5	4	3	2	1	0
Field	–	CMON_BSELTOL[2:0]			CMON_ERRTOL[2:0]			CMON_AUTORESTART_EN
Reset	–	0b000			0b000			0b0
Access Type	–	Write, Read			Write, Read			Write, Read
Restriction	–	Normal			Normal			Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CMON_BSELTOL	6:4	EN	The number of frames of incorrect or correct clock ratio (BCLKs per LRCLK) needed to trigger or recover from a framing error.	0x0: Trigger after 1 incorrect LRCLK frame, recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames. 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frames. 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames. 0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames.
CMON_ERRTOL	3:1	EN	Selects the number of incorrect or correct LRCLK periods needed to trigger or recover from a frame clock rate error.	0x0: Trigger after 1 incorrect LRCLK frame, recover after 1 correct LRCLK frame. 0x1: Trigger after 2 incorrect LRCLK frames, recover after 16 correct LRCLK frames 0x2: Trigger after 3 incorrect LRCLK frames, recover after 24 correct LRCLK frames. 0x3: Trigger after 4 incorrect LRCLK frames, recover after 32 correct LRCLK frames. 0x4: Trigger after 5 incorrect LRCLK frames, recover after 40 correct LRCLK frames. 0x5: Trigger after 6 incorrect LRCLK frames, recover after 48 correct LRCLK frames.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x6: Trigger after 7 incorrect LRCLK frames, recover after 56 correct LRCLK frames. 0x7: Trigger after 8 incorrect LRCLK frames, recover after 64 correct LRCLK frames.
CMON_AUTORESTART_EN	0	EN	Controls whether or not the device automatically resumes playback when the clocks become valid after the device is disabled due to a clock monitor error.	0: The device does not automatically restart after valid clocks are reapplied. 1: The device automatically restarts after valid clocks are reapplied.

Speaker Monitor Threshold (0x21F2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_THRESH[3:0]			
Reset	–	–	–	–	0x3			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPKMON_THRESH	3:0	–	Sets the speaker power threshold. If the signal power recovered by the circuit is above this threshold, a speaker monitor error will be asserted. The minimum threshold is 0.25V, and the maximum is 4V, 0.25V per step.	0x0: 0.25V 0x1: 0.5V .....: ..... 0.25V per step 0xE: 3.75V 0xF: 4.0V

Enable Controls (0x21F7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_EN	–	–	CMON_EN
Reset	–	–	–	–	0b1	–	–	0b1
Access Type	–	–	–	–	Write, Read	–	–	Write, Read
Restriction	–	–	–	–	Normal	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPKMON_EN	3	ENL	Enables the internal speaker protection monitor.	0x0: Disable the internal speaker data monitor. 0x1: Enable the internal speaker data monitor.
CMON_EN	0	ENL	Enables the clock monitor to monitor PCM input clocks for clock errors.	0: The clock monitor is disabled. 1: The clock monitor is enabled.

PCM Mode Config (0x2201)

BIT	7	6	5	4	3	2	1	0
Field	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
Reset	0b11		0b000			0b0	0b0	0b0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read
Restriction	Normal		Normal			Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_CHANSZ	7:6	ENL	Configures the PCM data word size for each channel.	00: Reserved 01: 16-bit 10: 24-bit 11: 32-bit
PCM_FORMAT	5:3	ENL	Selects the PCM data format.	0x0: I^2S Mode 0x1: Left-justified 0x2: Reserved 0x3: TDM Mode 0 (0 BCLK delay from LRCLK) 0x4: TDM Mode 1 (1 BCLK delay from LRCLK) 0x5: TDM Mode 2 (2 BCLK delay from LRCLK) 0x6 to 0x7: Reserved
PCM_TX_INTERLEAVE	2	ENL	Controls whether or not the I/V sense data assigned to the same channel is frame interleaved on the PCM data output (DOUT).	0: Disable Interleave mode. 1: Enable Interleave mode.
PCM_CHANSEL	1	ENL	Selects which LRCK edge starts a new frame (channel 0 or slot 0).	0: I^2S and LJ mode: Falling LRCLK edge starts a new frame. In TDM modes: Rising LRCLK edge starts a new frame. 1: In I^2S and LJ mode: Rising LRCLK edge starts a new frame. In TDM modes: Falling LRCLK edge starts a new frame.
PCM_TX_EXTRA_HIZ	0	ENL	Select whether DOUT is driven to zero or Hi-Z during extra BCLK cycles.	0: Drive DOUT to zero for extra BCLK cycles 1: Drive DOUT to Hi-Z for extra BCLK cycles

PCM Clock Setup (0x2202)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
Reset	–	–	–	0b0	0x4			
Access Type	–	–	–	Write, Read	Write, Read			
Restriction	–	–	–	Normal	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BCLKEDGE	4	ENL	Selects the active BCLK edge.	0: Input data captured and output data valid on the rising edge of BCLK. 1: Input data captured and output data valid on the falling edge of BCLK.
PCM_BSEL	3:0	ENL	Selects the number of BCLKs per LRCLK expected by the PCM Interface.	0x0: Reserved 0x1: Reserved 0x2: 32 0x3: 48 0x4: 64 0x5: 96 0x6: 128 0x7: 192 0x8: 256 0x9: 384 0xA: 512 0xB: 320

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0xC: 250 0xD: 125 0xE to 0xF: Reserved

PCM Sample Rate Setup 1 (0x2203)

BIT	7	6	5	4	3	2	1	0
Field	IVFB_SR[3:0]				PCM_SR[3:0]			
Reset	0x8				0x8			
Access Type	Write, Read				Write, Read			
Restriction	Normal				Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVFB_SR	7:4	ENL	Sets the sample rate of the I/V Feedback Path.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB: 176.4kHz 0xC: 192KHz 0xD to 0xF: Reserved
PCM_SR	3:0	ENL	Sets the sample rate of the PCM interface. This corresponds to the expected LRCLK frequency.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB: 176.4kHz 0xC: 192KHz 0xD to 0xF: Reserved

PCM TX Control 6 (0x2209)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_THERM_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_THERM_SLOT	5:0	TXEN	Thermal Data (ADC) Output Slot Select. Thermal data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 7 (0x220A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_DHT_ATN_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DHT_ATN_SLOT	5:0	TXEN	DHT attenuation Data Output Slot Select. DHT attenuation data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 8 (0x220B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_STATUS_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_STATUS_SLOT	5:0	TXEN	Device Satus Data Output Slot Select. Device status requires two slots.	0x00: Slot 00/01 0x01: Slot 01/02 0x02 to 0x3D: .... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 9 (0x220C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPA_DSP_MONITOR_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPA_DSP_MONITOR_SLOT	5:0	TXEN	DSP Monitor Data Output Slot Select. DSP Monitor Data requires four slots.	0x0: Slot 00/01/02/03 0x1: Slot 01/02/03/04 0x2: Slot 02/03/04/05 0x3 to 0x3B: .... 0x3C: Slot 60/61/62/63 0x3D: Reserved 0x3E: Reserved 0x3F: Reserved

PCM TX Control 10 (0x220D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPB_DSP_MONITOR_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPB_DSP_MONITOR_SLOT	5:0	TXEN	DSP Monitor Data Output Slot Select. DSP Monitor Data requires four slots.	0x0: Slot 00/01/02/03 0x1: Slot 01/02/03/04 0x2: Slot 02/03/04/05 0x3 to 0x3B: .... 0x3C: Slot 60/61/62/63 0x3D: Reserved 0x3E: Reserved 0x3F: Reserved

PCM TX Control 11 (0x220E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_BPE_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BPE_SLOT	5:0	TXEN	BPE State Output Slot Select. BPE State requires one slot.	0x0: Slot 00 0x1: Slot 01 0x2: Slot 02 0x22 to 0x3D: ... 0x3E: Slot 62 0x3F: Slot 62

PCM TX Control 12 (0x220F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_ICC_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_ICC_SLOT	5:0	TXEN	Selects the data output (DOUT) slots for the ICC output data. In Non-TDM Mode, only Slot 0 and Slot 1 are valid. If IV Feedback is enabled, ICC over DOUT only works when PCM_CHANSZ is set to 32 bits, PCM_TX_INTERLEAVE is enabled, and PCM_ICC_SLOT is set to the same as PCM_AMPX_VFB_SLOT. In TDM mode, ICC needs 3 slots. PCM_CHANSZ has to be greater than 16 bits, and PCM_ICC_SLOT has to be set in a number that is shown below: If PCM_CHANSZ = 24 bits, then PCM_ICC_SLOT is divisible by 3. If PCM_CHANSZ = 32 bits, then PCM_ICC_SLOT is divisible by 4.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 1 (0x2210)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPA_VFB_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPA_VFB_SLOT	5:0	TXEN	Selects the data output (DOUT) slots for the voltage feedback output data. In Non-TDM Mode, only Slot 0 and Slot 1 are Valid. For MAX98415A only.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 2 (0x2211)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPB_VFB_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPB_VFB_SLOT	5:0	TXEN	Selects the data output (DOUT) slots for the Amp B voltage feedback output data. In Non-TDM Mode, only Slot 0 and Slot 1 are Valid. For MAX98415A only.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ...

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 3 (0x2212)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPA_IMON_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPA_IMON_SLOT	5:0	TXEN	Amp A IMON Data Output Slot Select. IMON data requires two slots. In Non-TDM Mode, only Slot 0 and Slot 1 are Valid. For MAX98415A only.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 4 (0x2213)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_AMPB_IMON_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_AMPB_IMON_SLOT	5:0	TXEN	Amp B IMON Data Output Slot Select. IMON data requires two slots. In Non-TDM Mode, only Slot 0 and Slot 1 are Valid. For MAX98415A only.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM TX Control 5 (0x2214)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_PVDD_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_PVDD_SLOT	5:0	TXEN	PVDD Data (ADC) Output Slot Select. PVDD data requires two slots.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM Tx HiZ Control 1 (0x2220)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[63:56]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM data output slots to transmit either Hi-Z or 0.	Value: Decode 0: Output 0 on idle slots from 63 to 56 1: Output Hi-Z on slots from 63 to 56

PCM Tx HiZ Control 2 (0x2221)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[55:48]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them to Hi-Z or 0.	0: Output 0 on idle slots from 55 to 48 1: Output Hi-Z on slots from 55 to 48

PCM Tx HiZ Control 3 (0x2222)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[47:40]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 47 to 40 1: Output Hi-Z on slots from 47 to 40

PCM Tx HiZ Control 4 (0x2223)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[39:32]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 39 to 32 1: Output Hi-Z on slots from 39 to 32

PCM Tx HiZ Control 5 (0x2224)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[31:24]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on slots from 31 to 24 1: Output Hi-Z on idle slots from 31 to 24

PCM Tx HiZ Control6 (0x2225)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[23:16]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 23 to 16 1: Output Hi-Z on slots from 23 to 16

PCM Tx HiZ Control 7 (0x2226)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[15:8]							
Reset	0xFF							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on slots from 15 to 8 1: Output Hi-Z on idle slots from 15 to 8

PCM Tx HiZ Control 8 (0x2227)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[7:0]							
Reset	0xFF							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	TXEN	Configures the unused PCM Slots to set them all to Hi-Z or 0.	0: Output 0 on idle slots from 7 to 0 1: Output Hi-Z on slots from 7 to 0

PCM RX Source 1 (0x2229)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Restriction	–	–	–	–	–	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DMMIX_CFG	1:0	PCM	Determines the behavior of the mono mixer circuit.	0x0: The output of the mono mixer is Channel 0 for AmpA and Channel 1 for AmpB. 0x1: The output of the mono mixer is Channel 1 for AmpA and Channel 0 for AmpB. 0x2: The output of the monomixer is (Channel 0 + Channel1)/2 for AmpA and AmpB. 0x3: Reserved.

PCM RX Source 2 (0x222A)

BIT	7	6	5	4	3	2	1	0
Field	PCM_DMMIX_CH1_SOURCE[3:0]				PCM_DMMIX_CH0_SOURCE[3:0]			
Reset	0x1				0x0			
Access Type	Write, Read				Write, Read			
Restriction	Normal				Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DMMIX_CH1_SOURCE	7:4	PCM	Selects the PCM data input channel that is routed to the channel 1 of the digital mono mixer.	0x0: PCM Input Channel 0. 0x1: PCM Input Channel 1. 0x2: PCM Input Channel 2. ...: ... 0xE: PCM Input Channel 14. 0xF: PCM Input Channel 15.
PCM_DMMIX_CH0_SOURCE	3:0	PCM	Selects the PCM data input channel that is routed to the channel 0 of the digital mono mixer.	0x0: PCM Input Channel 0. 0x1: PCM Input Channel 1. 0x2: PCM Input Channel 2. ...: ... 0xE: PCM Input Channel 14. 0xF: PCM Input Channel 15.

PCM Bypass Source (0x222B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PCM_BYPASS_SOURCE[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BYPASS_SOURCE	3:0	PCM	Selects the PCM data input channel that is routed to the speaker audio processing bypass path.	0x0: PCM Input Channel 0. 0x1: PCM Input Channel 1. 0x2: PCM Input Channel 2. ...: ... 0xE: PCM Input Channel 14. 0xF: PCM Input Channel 15.

PCM TX Source Enables 1 (0x222C)

BIT	7	6	5	4	3	2	1	0
Field	PCM_BPE_EN	PCM_STATUS_EN	PCM_DHT_ATN_EN	PCM_THERM_EN	PCM_PVDD_EN	PCM_DSPMONITOR_EN	PCM_IMON_AMPA_EN	PCM_VFB_AMPA_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BPE_EN	7	TXEN	Enables transmit of the BPE (Brownout Prevention Engine) state on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable the BPE state transmit. 1: Enable the BPE state transmit.
PCM_STATUS_EN	6	TXEN	Enables transmit of the device status on the assigned data output (DOUT) slots. This output data can be transmitted only in TDM mode.	0: Disable the device status transmit. 1: Enable the device status transmit.
PCM_DHT_ATN_EN	5	TXEN	Enables transmit of the applied DHT attenuation on the assigned data output	0: Disable the DHT attenuation data transmit. 1: Enable the DHT attenuation data transmit.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			(DOUT) slot. This output data can be transmitted only in TDM mode.	
PCM_THERM_EN	4	TXEN	Enables transmit of the measured temperature on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable the temperature data transmit. 1: Enable the temperature data transmit.
PCM_PVDD_EN	3	TXEN	Enables transmit of the measured PVDD supply voltage on the assigned data output (DOUT) slot. This output data can be transmitted only in TDM mode.	0: Disable the PVDD supply voltage data transmit. 1: Enable the PVDD supply voltage data transmit.
PCM_DSPMONITOR_EN	2	TXEN	Enables transmit of the Amp A and Amp B playback path DSP output data on the assigned data output (DOUT) slot.	0: Disable the playback path data transmit. 1: Enable the playback path data transmit.
PCM_IMON_AMPA_EN	1	TXEN	Enables transmit of the Amp A current sense output data on the assigned data output (DOUT) slot. For MAX98415A only.	0: Disable the current sense data transmit. 1: Enable the current sense data transmit.
PCM_VFB_AMPA_EN	0	TXEN	Enables transmit of the Amp A voltage feedback output data on the assigned data output (DOUT) slot. For MAX98415A only.	0: Disable the voltage feedback data transmit. 1: Enable the voltage feedback data transmit.

PCM TX Source Enables 2 (0x222D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_IMON_AMPB_EN	PCM_VFB_AMPB_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_IMON_AMPB_EN	1	TXEN	Enables transmit of the Amp B current sense output data on the assigned data output (DOUT) slot. For MAX98415A only.	0: Disable the current sense data transmit. 1: Enable the current sense data transmit.
PCM_VFB_AMPB_EN	0	TXEN	Enables transmit of the Amp B voltage feedback output data on the assigned data output (DOUT) slot. For MAX98415A only.	0: Disable the voltage feedback data transmit. 1: Enable the voltage feedback data transmit.

PCM Rx Enables (0x222E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_BYP_EN	PCM_RX_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BYP_EN	1	–	Enables the PCM data input to speaker amplifier via bypass path. This path bypasses the speaker playback path audio processing	0x0: Audio processing bypass path disabled. 0x1: Audio processing bypass path enabled.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			features like - volume control, gains, DHT, BPE and Thermal Foldback.	
PCM_RX_EN	0	–	Enables the speaker amplifier playback path for both Amp A and Amp B.	0: PCM data input disabled 1: PCM data input enabled

PCM Tx Enables (0x222F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_TX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_EN	0	TXEN	Enables the data output (DOUT) of the PCM interface.	0: PCM data output disabled 1: PCM data output enabled

ICC Rx Enables A (0x2270)

BIT	7	6	5	4	3	2	1	0
Field	ICC_RX_CH7_EN	ICC_RX_CH6_EN	ICC_RX_CH5_EN	ICC_RX_CH4_EN	ICC_RX_CH3_EN	ICC_RX_CH2_EN	ICC_RX_CH1_EN	ICC_RX_CH0_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ICC_RX_CH7_EN	7	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 7 is disabled 1: ICC receive channel 7 is enabled
ICC_RX_CH6_EN	6	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 6 is disabled 1: ICC receive channel 6 is enabled
ICC_RX_CH5_EN	5	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 5 is disabled 1: ICC receive channel 5 is enabled
ICC_RX_CH4_EN	4	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 4 is disabled 1: ICC receive channel 4 is enabled
ICC_RX_CH3_EN	3	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 3 is disabled 1: ICC receive channel 3 is enabled
ICC_RX_CH2_EN	2	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 2 is disabled 1: ICC receive channel 2 is enabled
ICC_RX_CH1_EN	1	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 1 is disabled 1: ICC receive channel 1 is enabled
ICC_RX_CH0_EN	0	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 0 is disabled 1: ICC receive channel 0 is enabled

ICC Rx Enables B (0x2271)

BIT	7	6	5	4	3	2	1	0
Field	ICC_RX_CH15_EN	ICC_RX_CH14_EN	ICC_RX_CH13_EN	ICC_RX_CH12_EN	ICC_RX_CH11_EN	ICC_RX_CH10_EN	ICC_RX_CH9_EN	ICC_RX_CH8_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	Normal	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ICC_RX_CH15_EN	7	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 15 is disabled 1: ICC receive channel 15 is enabled
ICC_RX_CH14_EN	6	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 14 is disabled 1: ICC receive channel 14 is enabled
ICC_RX_CH13_EN	5	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 13 is disabled 1: ICC receive channel 13 is enabled
ICC_RX_CH12_EN	4	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 12 is disabled 1: ICC receive channel 12 is enabled
ICC_RX_CH11_EN	3	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 11 is disabled 1: ICC receive channel 11 is enabled
ICC_RX_CH10_EN	2	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 10 is disabled 1: ICC receive channel 10 is enabled
ICC_RX_CH9_EN	1	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 9 is disabled 1: ICC receive channel 9 is enabled
ICC_RX_CH8_EN	0	ICC	Configures whether or not the ICC interface accepts data from this channel.	0: ICC receive channel 8 is disabled 1: ICC receive channel 8 is enabled

ICC Tx Control (0x2272)

BIT	7	6	5	4	3	2	1	0
Field	–	ICC_INTERLEAVE_MODE	ICC_DATA_SEL	ICC_TX_EXTRA_HIZ	ICC_TX_DEST[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			
Restriction	–	Normal	Normal	Normal	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ICC_INTERLEAVE_MODE	6	ICC	Select whether the ICC pin transmits DHT and Thermal Foldback data in interleaving fashion when PCM data word size (data width) is only 16-bits. This has no effect when the data word size is 24- or 32- bits.	0: ICC transmits either DHT or Thermal data based on ICC_DATA_SEL. 1: ICC transmits in interleaved mode which DHT and Thermal data are sent alternatively.
ICC_DATA_SEL	5	ICC	Select whether the ICC pin transmits DHT or Thermal Foldback data when PCM data word size (data width) is only 16-bits. This has no effect when the data word size is 24- or 32-bits.	0: ICC transmits the DHT data + BPE state. 1: ICC transmits the Thermal Foldback data + BPE state.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ICC_TX_EXTRA_HIZ	4	ICC	Selects whether ICC is driven to zero or Hi-Z for extra BCLK cycles.	0: Drive ICC to zero for extra BCLK cycles 1: Drive ICC to Hi-Z for extra BCLK cycles
ICC_TX_DEST	3:0	ICC	Selects the device transmit channel for ICC data.	0x0: ICC Channel 0 0x1: ICC Channel 1 ...: ... 0xE: ICC Channel 14 0xF: ICC Channel 15

ICC Enables (0x227F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ICC_OVER_DOUT_EN	ICC_LINK_EN	ICC_TX_EN
Reset	–	–	–	–	–	0b0	0b0	0b0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read
Restriction	–	–	–	–	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ICC_OVER_DOUT_EN	2	–	Enables ICC link data sent over PCM DOUT pin.	0: ICC link over DOUT disabled 1: ICC link over DOUT enabled
ICC_LINK_EN	1	–	Enables ICC link between devices.	0: ICC link disabled 1: ICC link enabled
ICC_TX_EN	0	–	Select whether the ICC pin transmitter is enabled/disabled.	0: ICC transmit disabled 1: ICC transmit enabled

Tone Generator and DC Config (0x2283)

BIT	7	6	5	4	3	2	1	0
Field	–	–	TONE_AMPLITUDE[1:0]		TONE_CONFIG[3:0]			
Reset	–	–	0b00		0x4			
Access Type	–	–	Write, Read		Write, Read			
Restriction	–	–	Normal		Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
TONE_AMPLITUDE	5:4	EN	Sets the sine wave amplitude. This register is not used when programming the Tone generator to output DC signals.	0x0: -6dBFS. 0x1: -4.8dBFS. 0x2: 0dBFS. 0x3: Reserved.
TONE_CONFIG	3:0	EN	Configures the output of the tone generator. For signal outputs the frequency is a division of the sample rate (f_S).	0x0: DC value programmed by TONE_DC[23:0] 0x1: DC = 0x0000 = 0 0x2: DC = +FullScale/2 0x3: DC = -FullScale/2 0x4: 1 KHz tone at all sample rates 0x5: fs/4 0x6: fs/6 0x7 to 0xF: Reserved

Tone Generator DC Level 1 (0x2284)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[23:16]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
TONE_DC	7:0	EN	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator DC Level 2 (0x2285)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[15:8]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
TONE_DC	7:0	EN	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator DC Level 3 (0x2286)

BIT	7	6	5	4	3	2	1	0
Field	TONE_DC[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
TONE_DC	7:0	EN	Sets the tone generator DC output level as a signed binary relative to full-scale.

Tone Generator Enable (0x228F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PINK_NOISE_EN	TONE_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PINK_NOISE_EN	1	ENL	Enables Pink Noise data output to the speaker amplifier path.	0: Pink Noise disabled. 1: Pink Noise enabled.
TONE_EN	0	ENL	Enables the tone generator. When enabled it replaces the PCM interface as the input to the speaker amplifier path.	0: Tone generator disabled. 1: Tone generate enabled.

Noise Gate/Idle Mode Control (0x22E0)

BIT	7	6	5	4	3	2	1	0
Field	NG_UNMUTE_THRESH[3:0]				NG_MUTE_THRESH[3:0]			
Reset	0x3				0x2			
Access Type	Write, Read				Write, Read			
Restriction	Normal				Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
NG_UNMUTE_THRESH	7:4	NG	Sets the threshold (number of LSBs toggling) at which the noise gate/idle mode deactivates.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9: 10 LSBs 0xA to 0xF: Reserved
NG_MUTE_THRESH	3:0	NG	Sets the threshold (number of LSBs toggling) at which the noise gate/Idle mode is activated.	0x0: 1 LSB 0x1: 2 LSBs 0x2: 3 LSBs 0x3: 4 LSBs 0x4: 5 LSBs 0x5: 6 LSBs 0x6: 7 LSBs 0x7: 8 LSBs 0x8: 9 LSBs 0x9: 10 LSBs 0xA to 0xF: Reserved

Noise Gate/Idle Mode Enables (0x22E3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IDLE_MODE_EN	NOISEGATE_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IDLE_MODE_EN	1	ENL	Enables the amplifier Idle Mode. Idle mode cannot be enabled when the noise gate function is also enabled.	0: Idle Mode disabled. 1: Idle Mode enabled.
NOISEGATE_EN	0	–	Enables the noise gate.	0: Noise Gate disabled. 1: Noise Gate enabled.

AMP A Volume Level Control (0x22F0)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_SPK_VOL[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_VOL	7:0	–	Sets the digital volume level of the speaker Amp A path in a single channel and Stereo modes. The AMPA_VOL_UPDATE must be set to apply the volume for the speaker Amp A path.	0x00: 0dB 0x01: -0.5dB 0x02: -1.0dB ...: (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63dB ...: -0.5dB steps) 0xB4: -90dB 0xB5 - 0xFE: Reserved 0xFF: Mute

AMP B Volume Level Control (0x22F1)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_SPK_VOL[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_VOL	7:0	–	Sets the digital volume level of the speaker Amp B path. The AMPB_VOL_UPDATE must be set to apply the volume for speaker Amp B path in single channel, and Stereo modes.	0x00: 0dB 0x01: -0.5dB 0x02: -1.0dB ...: (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63dB ...: -0.5dB steps) 0xB4: -90dB 0xB5 - 0xFE: Reserved 0xFF: Mute

Amplifier Volume Update Control (0x22FF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMPB_VOL_UPDATE	AMPA_VOL_UPDATE
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write Only	Write Only
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_VOL_UPDATE	1	–	This bit applies the volume level set in the AMPB_SPK_VOL to the Playback path.	0: No action 1: Triggers a software reset event
AMPA_VOL_UPDATE	0	–	This bit applies the volume level set in AMPA_SPK_VOL to the Playback path.	0: No action 1: Triggers a software reset event

AMP A Volume Ramp Control (0x2300)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPA_SPK_VOL_RMP_RATE[1:0]		–	–	AMPA_SPK_VOL_RMPDN_BYPASS	AMPA_SPK_VOL_RMPUP_BYPASS
Reset	–	–	0b00		–	–	0b0	0b0
Access Type	–	–	Write, Read		–	–	Write, Read	Write, Read
Restriction	–	–	Normal		–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_VOL_RMP_RATE	5:4	SPK_A	Sets the speaker amplifier path volume ramp rate for Amplifier A during volume changes. The register settings are ignored if volume ramping is bypassed.	0x0: 64 x tVOL_COEFF 0x1: 128 x t_{VOL_COEFF} 0x2: 256 x t_{VOL_COEFF} 0x3: 512 x t_{VOL_COEFF}
AMPA_SPK_VOL_RMPDN_BYPASS	1	SPK_A	Controls whether the speaker amplifier path volume is internally ramped down during volume changes.	0: Volume ramp enabled 1: Volume ramp bypassed
AMPA_SPK_VOL_RMPUP_BYPASS	0	SPK_A	Controls whether the speaker amplifier path volume is internally ramped up during volume changes.	0: Volume ramp enabled 1: Volume ramp bypassed

AMP A Path Gain (0x2302)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	AMPA_SPK_GAIN_MAX[4:0]				
Reset	–	–	–	0b10010				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_GAIN_MAX	4:0	SPK_A	Sets the maximum peak output voltage level (V_{MPO}) for the Amp A speaker path (no-load). Values in dB are relative to the baseline speaker path DAC full-scale output level of 0.39dBV.	0x00: 2.98V_P (6dB) 0x01: 3.35V_P (7dB) 0x02: 3.76V_P (8dB) 0x03: 4.22V_P (9dB) 0x04: 4.73V_P (10dB) 0x05: 5.31V_P (11dB) 0x06: 5.96V_P (12dB) 0x07: 6.68V_P (13dB) 0x08: 7.50V_P (14dB) 0x09: 8.41V_P (15dB) 0x0A: 9.44V_P (16dB) 0x0B: 10.59V_P (17dB) 0x0C: 11.88V_P (18dB) 0x0D: 13.33V_P (19dB) 0x0E: 14.96V_P (20dB) 0x0F: 16.79V_P (21dB) 0x10: 18.83V_P (22dB) 0x11: 21.13V_P (23dB) 0x12: 23.71V_P (24dB) 0x13-0x1F: Reserved

AMP A DSP Config (0x2303)

BIT	7	6	5	4	3	2	1	0
Field	–	AMPA_SPK_WBAND_FILT_EN	AMPA_SPK_SAFE_EN	AMPA_SPK_INVERT	AMPA_SPK_DITH_EN	AMPA_SPK_IVF_DCBLK_CFG[1:0]		AMPA_SPK_DCBLK_EN
Reset	–	0b0	0b1	0b0	0b1	0b00		0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read
Restriction	–	Normal	Normal	Normal	Normal	Normal		Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_WBAND_FILT_EN	6	SPK_A	Enables the wideband filters in the Amp A speaker amplifier path with increased passband for sample rates higher than 50kHz.	0: Higher passband filters are disabled. 1: Higher passband filters are enabled.
AMPA_SPK_SAFE_EN	5	SPK_A	The Safe Mode bit protects any speaker connected to the Amp A playback path on power up. When this setting is enabled the SPK_VOL, SPK_GAIN_MAX settings are ignored and the amplifier output is set to -18dBFS.	0: Speaker safe mode is disabled. 1: Speaker safe mode is enabled.
AMPA_SPK_INVERT	4	–	Inverts the Amp A speaker amplifier path output.	0: Output is normal. 1: Output is inverted.
AMPA_SPK_DITH_EN	3	SPK_A	Selects whether or not dither is applied data in the Amp A speaker amplifier path.	0: Dither is disabled. 1: Dither is enabled.
AMPA_SPK_IVF_DCBLK_CFG	2:1	–	Sets the cutoff frequency of the DC Blocker High Pass Filter for Amp A speaker, current sense, and voltage feedback paths.	0: f_C = 1.872Hz. 1: f_C = 0.936Hz. 2: f_C = 0.468Hz. 3: f_C = 0.234Hz.
AMPA_SPK_DCBLK_EN	0	SPK_A	Controls the DC blocking filter in the Amp A speaker amplifier path.	0: DC blocking filter is disabled. 1: DC blocking filter is enabled.

AMP A SPK Path Wideband Only Enable (0x230B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AMPA_SPK_WIDEBAND_ONLY_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_WIDEBAND_ONLY_EN	0	SPK_A	Enable bit to improve inband noise performance when only an ultrasound signal is sent on the path. When enabled, only a wideband signal is sent to the Amp A.	0x0: Ultrasound Signal Mode Disable 0x1: Ultrasound Signal Mode Enable

AMP A Clip Gain (0x230E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPA_SPK_CLIP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_CLIP	3:0	SPK_A	Sets the digital clip gain level of the Amp A speaker amplifier path.	0x00: 0dB 0x01: 0.5dB 0x02: 1.0dB 0x03: 1.5dB 0x04: 2.0dB 0x05: 2.5dB 0x06: 3.0dB 0x07: 3.5dB 0x08: 4.0dB 0x9: 5.0dB 0xA: 6.0dB 0xB-0xF: 0 dB

AMP B Volume Ramp Control (0x2320)

BIT	7	6	5	4	3	2	1	0
Field	–	–	AMPB_SPK_VOL_RMP_RATE[1:0]		–	–	AMPB_SPK_VOL_RMPDN_BYPASS	AMPB_SPK_VOL_RMPUP_BYPASS
Reset	–	–	0b00		–	–	0b0	0b0
Access Type	–	–	Write, Read		–	–	Write, Read	Write, Read
Restriction	–	–	Normal		–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_VOL_RMP_RATE	5:4	SPK_B	Sets the Amp B speaker amplifier path volume ramp rate settings during volume changes. The register settings are ignored if volume ramping is bypassed.	0x0: 64 x t_{ON} 0x1: 128 x t_{ON} 0x2: 256 x t_{ON} 0x3: 512 x t_{ON}
AMPB_SPK_VOL_RMPDN_BYPASS	1	SPK_B	Controls whether the speaker amplifier path volume is internally ramped down during volume changes.	0: Volume ramp enabled 1: Volume ramp bypassed
AMPB_SPK_VOL_RMPUP_BYPASS	0	SPK_B	Controls whether the speaker amplifier path volume is internally ramped up during volume changes.	0: Volume ramp enabled 1: Volume ramp bypassed

AMP B Path Gain (0x2322)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	AMPB_SPK_GAIN_MAX[4:0]				
Reset	–	–	–	0b10010				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_GAIN_MAX	4:0	SPK_B	Sets the maximum peak output voltage level (V_{MPO}) for the Amp B speaker path (no-load). Values in dB are relative to the baseline speaker path DAC full-scale output level of 0.39dBV.	0x00: 2.98V_P (6dB) 0x01: 3.35V_P (7dB) 0x02: 3.76V_P (8dB) 0x03: 4.22V_P (9dB) 0x04: 4.73V_P (10dB) 0x05: 5.31V_P (11dB) 0x06: 5.96V_P (12dB) 0x07: 6.68V_P (13dB) 0x08: 7.50V_P (14dB) 0x09: 8.41V_P (15dB) 0x0A: 9.44V_P (16dB) 0x0B: 10.59V_P (17dB) 0x0C: 11.88V_P (18dB) 0x0D: 13.33V_P (19dB) 0x0E: 14.96V_P (20dB) 0x0F: 16.79V_P (21dB) 0x10: 18.83V_P (22dB) 0x11: 21.13V_P (23dB) 0x12: 23.71V_P (24dB) 0x13-0x1F: Reserved

AMP B DSP Config (0x2323)

BIT	7	6	5	4	3	2	1	0
Field	–	AMPB_SPK_WBAND_FILT_EN	AMPB_SPK_SAFE_EN	AMPB_SPK_INVERT	AMPB_SPK_DITH_EN	AMPB_SPK_IVF_DCBLK_CFG[1:0]		AMPB_SPK_DCBLK_EN
Reset	–	0b0	0b1	0b0	0b1	0b00		0b0

BIT	7	6	5	4	3	2	1	0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read
Restriction	–	Normal	Normal	Normal	Normal	Normal		Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_WBAND_FILT_EN	6	SPK_B	Enables the wideband filters in the Amp B speaker amplifier path with increased passband for sample rates higher than 50kHz.	0: Higher passband filters are disabled. 1: Higher passband filters are enabled.
AMPB_SPK_SAFE_EN	5	SPK_B	The Safe Mode bit protects any speaker connected to the Amp B playback path on power up. When this setting is enabled the SPK_VOL, SPK_GAIN_MAX settings are ignored and the amplifier output is set to -18dBFS.	0: Speaker safe mode is disabled 1: Speaker safe mode is enabled
AMPB_SPK_INVERT	4	–	Inverts the Amp B speaker amplifier path output.	0: Output is normal. 1: Output is inverted.
AMPB_SPK_DITH_EN	3	SPK_B	Selects whether or not dither is applied data in the Amp B speaker amplifier path.	0: Dither disabled. 1: Dither enabled.
AMPB_SPK_IVF_DCBLK_CFG	2:1	–	Sets the cutoff frequency of the DC Blocker High Pass Filter for Amp B speaker, current sense, and voltage feedback paths.	0: f_C = 1.872Hz 1: f_C = 0.936Hz 2: f_C = 0.468Hz 3: f_C = 0.234Hz
AMPB_SPK_DCBLK_EN	0	SPK_B	Controls the DC blocking filter in the Amp B speaker amplifier path.	0: DC blocking filter is disabled. 1: DC blocking filter is enabled.

AMP B SPK Path Wideband Only Enable (0x232B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AMPB_SPK_WIDEBAND_ONLY_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_WIDEBAND_ONLY_EN	0	SPK_B	Enable bit to improve inband noise performance when only an ultrasound signal is sent on the path. When enabled, only a wideband signal is sent to the Amp B.	0x0: Ultrasound Signal Mode Disable. 0x1: Ultrasound Signal Mode Enable.

AMP B Clip Gain (0x232E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_SPK_CLIP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_CLIP	3:0	–	Sets the digital clip gain level of the Amp B speaker amplifier path.	0x00: 0dB 0x01: 0.5dB 0x02: 1.0dB 0x03: 1.5dB 0x04: 2.0dB 0x05: 2.5dB 0x06: 3.0dB 0x07: 3.5dB 0x08: 4.0dB 0x9: 5.0dB 0xA: 6.0dB 0xB-0xF: 0 dB

SSM Configuration (0x23D3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPK_TRI_SSM_EN	–	SPK_TRI_SSM_MOD[1:0]	
Reset	–	–	–	–	0b1	–	0b00	
Access Type	–	–	–	–	Write, Read	–	Write, Read	
Restriction	–	–	–	–	Normal	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_TRI_SSM_EN	3	–	Enables Spread-Spectrum Clocking in the triangle wave generator for both Amp A and Amp B.	0: Spread-Spectrum Clocking is disabled. 1: Spread-Spectrum Clocking is enabled.
SPK_TRI_SSM_MOD	1:0	–	Selects the modulation index for the Class D amplifier's triangle wave spread-spectrum clock. This controls the modulation index for both Amp A and Amp B.	0x0: ±1.5% variation 0x1: ±3.0% variation 0x2: ±4.5% variation 0x3: ±6.0% variation

SPK Switching Frequency (0x23DA)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SPK_TRI_FSW2X_MODE	–	–
Reset	–	–	–	–	–	0b0	–	–
Access Type	–	–	–	–	–	Write, Read	–	–
Restriction	–	–	–	–	–	Normal	–	–

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_TRI_FSW2X_MODE	2	–	Controls the nominal Class-D switching frequency of Amp A and Amp B outputs.	0: Normal tri-wave oscillation frequency. 1: 2X triwave oscillation frequency.

SPK Edge Control 1 (0x23DD)

BIT	7	6	5	4	3	2	1	0
Field	SPK_SL_RATE_LS[3:0]				SPK_SL_RATE_HS[3:0]			

BIT	7	6	5	4	3	2	1	0
Reset	0xA				0xA			
Access Type	Write, Read				Write, Read			
Restriction	Normal				Normal			

BITFIELD	BITS	RES	DESCRIPTION
SPK_SL_RATE_LS	7:4	–	These bits control the on/off time of the low-side power FET. This, in effect, strongly controls fall time at the OUTx node and weakly controls rise time at OUTx nodes. Rise times are strongly controlled by SPK_SL_RATE_HS. **SPK_SL_RATE_LS<3:0>** / **OUTx Fall Time** 0000 – Slowest Fall time. 0101 – Slower fall time than default. 1010 – Default fall time. 1111 – Faster fall time than default.
SPK_SL_RATE_HS	3:0	–	These bits control the on/off time of high-side power FET connected to the PVDD supply pin. This, in effect, controls the rise time at OUTx nodes and weakly controls the fall time of OUTx nodes. Fall time is strongly controlled by SPK_SL_RATE_LS. **SPK_SL_RATE_HS<3:0>** / **OUTx Rise Time** 0000 – Slowest rise time. 0101 – Slower rise time than default. 1010 – Default rise time. 1111 – Faster rise time than default.

Bypass Path Config (0x23E0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	BYP_WBAND_FILT_EN	BYP_INVERT
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BYP_WBAND_FILT_EN	1	SPK	Enables the wideband filters with increased passband for sample rates higher than 50kHz in the amplifier audio processing bypass path.	0x0: Higher passband filters are disabled. 0x1: Higher passband filters are enabled.
BYP_INVERT	0	–	Inverts the bypass amplifier path output.	0: Output is normal. 1: Output is inverted.

Bypass Path Routing Config (0x23E1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	BYP_PATH_AMP_SEL[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	
Restriction	–	–	–	–	–	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BYP_PATH_AMP_SEL	1:0	–	Routes bypass channel to appropriate Amplifier playback path.	0: Output is routed to Amp A. 1: Output is routed to Amp B. 2: Output is routed to Amp A. and Amp B 3: Reserved.

AMP output mode select (0x23F0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	AMP_MODE
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMP_MODE	0	TXEN	Enables the speaker amplifier path.	0: Stereo Mode 1: RESERVED

AMP enables (0x23FF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_SPK_FB_EN	AMPA_SPK_FB_EN	AMPB_SPK_EN	AMPA_SPK_EN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_SPK_FB_EN	3	TXEN	Enables PCM data output from the end of the speaker amplifier path DSP.	0: Speaker amplifier path DSP feedback is disabled. 1: Speaker amplifier path DSP feedback is enabled.
AMPA_SPK_FB_EN	2	TXEN	Enables PCM data output from the end of the speaker amplifier path DSP.	0: Speaker amplifier path DSP feedback is disabled. 1: Speaker amplifier path DSP feedback is enabled.
AMPB_SPK_EN	1	TXEN	Enables the Amp B speaker amplifier path.	0: Speaker amplifier is disabled 1: Speaker amplifier is enabled

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_SPK_EN	0	TXEN	Enables the Amp A speaker amplifier path.	0: Speaker amplifier is disabled 1: Speaker amplifier is enabled

I_V Sense Path Config (0x2400)

BIT	7	6	5	4	3	2	1	0
Field	IVF_WBAND_FILT_EN	VFB_DITH_EN	IMON_DITH_EN	–	AMPB_IVF_I_DCBLK_EN	AMPB_IVF_V_DCBLK_EN	AMPA_IVF_I_DCBLK_EN	AMPA_IVF_V_DCBLK_EN
Reset	0b0	0b1	0b0	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	Normal	Normal	Normal	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVF_WBAND_FILT_EN	7	IVS	Enables the wideband filters with increased passband for sample rates higher than 50kHz in the IV Feedback path. For MAX98415A only.	0x0: Higher passband filters are disabled. 0x1: Higher passband filters are enabled.
VFB_DITH_EN	6	IVS	Select whether or not dither is applied to the $V_{FEEDBACK}$ path. For MAX98415A only.	0: Dither Off. 1: Dither On.
IMON_DITH_EN	5	–	Select whether or not dither is applied to the I_{SENSE} path. For MAX98415A only.	0x0: Dither Off. 0x1: Dither On.
AMPB_IVF_I_DCBLK_EN	3	IVS_B	Enables the DC blocking filter in the current sense ADC path. For MAX98415A only.	0: DC blocker is disabled. 1: DC blocker is enabled.
AMPB_IVF_V_DCBLK_EN	2	IVS_B	Enables the DC blocking filter in the voltage feedback path. For MAX98415A only.	0: DC blocker is disabled. 1: DC blocker is enabled.
AMPA_IVF_I_DCBLK_EN	1	IVS_A	Enables the DC blocking filter in the current sense ADC path. For MAX98415A only.	0: DC blocker is disabled. 1: DC blocker is enabled.
AMPA_IVF_V_DCBLK_EN	0	IVS_A	Enables the DC blocking filter in the voltage feedback path. For MAX98415A only.	0: DC blocker is disabled. 1: DC blocker is enabled.

I_V Sense Path Enables (0x2404)

BIT	7	6	5	4	3	2	1	0
Field	–	IVF_AMPB_IM_EN	IVF_AMPB_I_EN	IVF_AMPB_V_EN	–	IVF_AMPA_IM_EN	IVF_AMPA_I_EN	IVF_AMPA_V_EN
Reset	–	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read
Restriction	–	Normal	Normal	Normal	–	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVF_AMPB_IM_EN	6	–	Enables the speaker's current sense ADC path. When this bit is set to 1, the current sense ADC path is powered up if the device is in the active state (EN = 1) during Idle Mode. For MAX98415A only.	0: The speaker's current sense ADC path is disabled during Idle Mode. 1: The speaker's current sense ADC path is enabled during Idle Mode.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVF_AMPB_I_EN	5	–	Enables the speaker's current sense ADC path. When this bit is set to 1, the current sense ADC path is powered up if the device is in the active state (EN = 1). For MAX98415A only.	0: Speaker current sense ADC path disabled. 1: Speaker current sense ADC path enabled.
IVF_AMPB_V_EN	4	–	Enables the speaker voltage sense ADC path. When this bit is set to 1, the voltage sense ADC path is powered up if the device is in the active state (EN = 1). For MAX98415A only.	0: The speaker voltage sense ADC path is disabled. 1: The speaker voltage sense ADC path is enabled.
IVF_AMPA_IM_EN	2	–	Enables the speaker current sense ADC path. When this bit is set to 1, the current sense ADC path is powered up if the device is in the active state (EN = 1) during Idle Mode. For MAX98415A only.	0: The speaker's current sense ADC path is disabled during Idle Mode. 1: The speaker's current sense ADC path is enabled during Idle Mode.
IVF_AMPA_I_EN	1	–	Enables the speaker current sense ADC path. When this bit is set to 1, the current sense ADC path is powered up if the device is in the active state (EN = 1). For MAX98415A only.	0: The speaker's current sense ADC path is disabled. 1: The speaker's current sense ADC path is enabled.
IVF_AMPA_V_EN	0	–	Enables the speaker voltage sense ADC path. When this bit is set to 1, the voltage sense ADC path is powered up if the device is in the active state (EN = 1). For MAX98415A only.	0: The speaker's voltage sense ADC path is disabled. 1: The speaker's voltage sense ADC path is enabled.

Meas ADC Sample Rate (0x2700)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_AMPB_TEMP_SR[1:0]		MEAS_ADC_AMPA_TEMP_SR[1:0]		–	–	MEAS_ADC_PVDD_SR[1:0]	
Reset	0b11		0b00		–	–	0b00	
Access Type	Write, Read		Write, Read		–	–	Write, Read	
Restriction	Normal		Normal		–	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_AMPB_TEMP_SR	7:6	EN	Configures the sample rate of the Amp B thermal channel of the measurement ADC.	0x0: 300kHz 0x1: 150kHz 0x2: 75kHz 0x3: 37.5kHz
MEAS_ADC_AMPA_TEMP_SR	5:4	EN	Configures the sample rate of the Amp A thermal channel of the measurement ADC.	00: 300kHz 01: 150kHz 10: 75kHz 11: 37.5kHz
MEAS_ADC_PVDD_SR	1:0	EN	Configures the sample rate of the PVDD channel of the measurement ADC.	0x0: 300kHz 0x1: 150kHz 0x2: 75kHz 0x3: 37.5kHz

Meas ADC Optimal Mode (0x2702)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEAS_ADC_OPT_AVE_SEL[1:0]		MEAS_ADC_OPT_MODE[1:0]	
Reset	–	–	–	–	0b01		0b00	

BIT	7	6	5	4	3	2	1	0
Access Type	–	–	–	–	Write, Read		Write, Read	
Restriction	–	–	–	–	Normal		Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_OPT_AVE_SEL	3:2	–	When MEAS_ADC_OPT_MODE is enabled, the optimized channel's moving averager can be set by this register.	0x0: Bypass 0x1: 2 samples 0x2: 4 samples 0x3: Reserved
MEAS_ADC_OPT_MODE	1:0	–	Enables the measurement of ADC optimal mode. When it is set, the PVDD channel runs at the highest rate, and the thermal channels run at a lower rate. The MEAS_ADC_xxx_SR has no effect in optimal mode.	0x0: Measurement ADC runs at regular mode. 0x1: Measurement ADC runs at optimal mode 1, BPE power source at 850KHz, and both Thermal channels at 75KHz. 0x2: Measurement ADC runs at optimal mode 1, BPE power source at 925KHz, and both Thermal channels at 37.5KHz. 0x3: Reserved.

Meas ADC Readback Control 1 (0x2704)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEAS_ADC_AMPB_TEMP_RD_MODE	MEAS_ADC_AMPA_TEMP_RD_MODE	–	MEAS_ADC_PVDD_RD_MODE
Reset	–	–	–	–	0b0	0b0	–	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	–	Write, Read
Restriction	–	–	–	–	Normal	Normal	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_AMPB_TEMP_RD_MODE	3	–	Controls whether the AMPB thermal ADC channel output readback is updated automatically or manually after each conversion is completed.	0: Measurement ADC channel readback data is automatically updated. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_AMPA_TEMP_RD_MODE	2	–	Controls whether the AMPA thermal ADC channel output readback is updated automatically or manually after each conversion is completed.	0: Measurement ADC channel readback data is automatically updated. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_MODE	0	–	Controls whether the PVDD ADC channel output readback is updated automatically or manually after each conversion is completed.	0: Measurement ADC channel readback data is automatically updated. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC Readback Control 2 (0x2705)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	MEAS_ADC_AMPB_TEMP_RD_UPD	MEAS_ADC_AMPA_TEMP_RD_UPD	–	MEAS_ADC_PVDD_RD_UPD
Reset	–	–	–	–	0b0	0b0	–	0b0
Access Type	–	–	–	–	Write Only	Write Only	–	Write Only
Restriction	–	–	–	–	Normal	Normal	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_AMPB_TEMP_RD_UPD	3	–	Write 1 to initiate a measurement and lock the result into the measurement ADC AMPB thermal channel readback register.	0: No effect. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_AMPA_TEMP_RD_UPD	2	–	Write 1 to initiate a measurement and lock the result into the measurement ADC AMPA thermal channel readback register.	0: No effect. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.
MEAS_ADC_PVDD_RD_UPD	0	–	Write 1 to initiate a measurement and lock the result into the measurement ADC PVDD channel readback register.	0: No effect. 1: Initiates a measurement and locks the result into the measurement ADC channel readback register.

Meas ADC PVDD Config (0x2710)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_PVDD_FILT_EN	MEAS_ADC_PVDD_FILT_COEFF[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Write, Read	Write, Read			
Restriction	–	–	–	Normal	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_PVDD_FILT_EN	4	EN	Controls whether filtering is applied to the PVDD channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_PVDD_FILT_COEFF	3:0	EN	Sets the PVDD channel lowpass filter bandwidth.	Value: Decode 0x0: 0.4khz (Across all sample rates). 0x1: 2.5kHz (Across all sample rates). 0x2: 7.5kHz (Across all sample rates). 0x3: 50kHz (only 150kHz & 300kHz sample rate). 0x4: 150kHz (only 300kHz sample rate). 0x5 to 0xF: Reserved.

Meas ADC AMPA Thermal Config (0x2712)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_AMPA_TEMP_FILT_EN	MEAS_ADC_AMPA_TEMP_FILT_COEFF[3:0]			

BIT	7	6	5	4	3	2	1	0
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Write, Read	Write, Read			
Restriction	–	–	–	Normal	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_AMPA_TEMP_FILT_EN	4	EN	Controls whether filtering is applied to the Amp A Temperature channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_AMPA_TEMP_FILT_COEFF	3:0	EN	Sets the Amp A Temperature channel lowpass filter bandwidth.	Value: Decode 0x0: 0.4khz (Across all sample rates). 0x1: 2.5kHz (Across all sample rates). 0x2: 7.5kHz (Across all sample rates). 0x3: 50kHz (only 150kHz & 300kHz sample rate). 0x4: 150kHz (only 300kHz sample rate). 0x5 to 0xF: Reserved.

Meas ADC AMPB Thermal Config (0x2713)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	MEAS_ADC_AMPB_TEMP_FILT_EN	MEAS_ADC_AMPB_TEMP_FILT_COEFF[3:0]			
Reset	–	–	–	0b0	0x0			
Access Type	–	–	–	Write, Read	Write, Read			
Restriction	–	–	–	Normal	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC_AMPB_TEMP_FILT_EN	4	EN	Controls whether filtering is applied to Amp B Temperature channel output.	0: Filter is bypassed 1: Filter is applied
MEAS_ADC_AMPB_TEMP_FILT_COEFF	3:0	EN	Sets the Amp B Temperature channel lowpass filter bandwidth.	Value: Decode 0x0: 0.4khz (Across all sample rates). 0x1: 2.5kHz (Across all sample rates). 0x2: 7.5kHz (Across all sample rates). 0x3: 50kHz (only 150kHz & 300kHz sample rate). 0x4: 150kHz (only 300kHz sample rate). 0x5 to 0xF: Reserved.

Meas ADC PVDD Readback MSB (0x2720)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_PVDD_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_PVDD_DATA	7:0	–	Provides the measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = **MEAS_ADC_PVDD_DATA[8:0] x 0.04399V.**

Meas ADC PVDD Readback LSB (0x2721)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_PVDD_DATA[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_PVDD_DATA	0	–	Provides the measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = MEAS_ADC_PVDD_DATA[8:0] x 0.04399V.

Meas ADC AMPA Thermal Readback MSB (0x2724)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_AMPA_THERM_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_AMPA_THERM_DATA	7:0	–	Provides the measured Thermal value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPA Thermal Readback LSB (0x2725)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_AMPA_THERM_DATA[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_AMPA_THERM_DATA	0	–	Provides the measured temperature value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPB Thermal Readback MSB (0x2726)

BIT	7	6	5	4	3	2	1	0
Field	MEAS_ADC_AMPB_THERM_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_AMPB_THERM_DATA	7:0	–	Provides the measured temperature value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPB Thermal Readback LSB (0x2727)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_AMPB_THERM_DATA[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read Only
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
MEAS_ADC_AMPB_THERM_DATA	0	–	Provides the measured temperature value. To convert the 9-bit code into a real temperature, use the following: Measured Temperature (°C) = (MEAS_ADC_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC Lowest PVDD Readback MSB (0x2730)

BIT	7	6	5	4	3	2	1	0
Field	LOWEST_PVDD_DATA[8:1]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
LOWEST_PVDD_DATA	7:0	–	Provides the lowest measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = MEAS_ADC_PVDD_DATA[8:0] x 0.04399V.

Meas ADC Lowest PVDD Readback LSB (0x2731)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOWEST_PVDD_DATA[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read, Ext
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
LOWEST_PVDD_DATA	0	–	Provides the lowest measured PVDD value. To convert the 9-bit code into a real voltage, use the following: Measured V_{PVDD} (V) = MEAS_ADC_PVDD_DATA[8:0] x 0.04399V.

Meas ADC AMPA Highest Thermal Readback MSB (0x2732)

BIT	7	6	5	4	3	2	1	0
Field	HIGHEST_AMPA_THERMAL_DATA_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
HIGHEST_AMPA_THERMAL_DATA_MSB	7:0	–	Provides the highest measured Thermal value. To convert the 9-bit code into a real temperature, use the following: Highest Measured Temperature (°C) = (HIGHEST_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPA Highest Thermal Readback LSB (0x2733)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HIGHEST_AMPA_THERMAL_DATA_LSB
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read, Ext
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
HIGHEST_AMPA_THERMAL_DATA_LSB	0	–	Provides the highest measured Thermal value. To convert the 9-bit code into a real temperature, use the following: Highest Measured Temperature (°C) = (HIGHEST_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPB Highest Thermal Readback MSB (0x2734)

BIT	7	6	5	4	3	2	1	0
Field	HIGHEST_AMPB_THERMAL_DATA_MSB[7:0]							
Reset	0x00							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
HIGHEST_AMPB_THERMAL_DATA_MSB	7:0	–	Provides the highest measured Thermal value. To convert the 9-bit code into a real temperature, use the following: Highest Measured Temperature (°C) = (HIGHEST_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC AMPB Highest Thermal Readback LSB (0x2735)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	HIGHEST_AMPB_THERMAL_DATA_LSB
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Read, Ext
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
HIGHEST_AMPB_THERMAL_DATA_LSB	0	–	Provides the highest measured Thermal value. To convert the 9-bit code into a real temperature, use the following: Highest Measured Temperature (°C) = (HIGHEST_THERM_DATA[8:0] x 1.0°C) - 252°C.

Meas ADC Config (0x273F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MEAS_ADC_PVDD_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
MEAS_ADC _PVDD_EN	0	–	Manually enables the measurement ADC PVDD channel.	0: Do not manually enable the measurement ADC channel (may be automatically enabled) 1: Manually force the measurement ADC channel to be enabled anytime the device is in the active state

Thermal Warning Threshhold (0x2750)

BIT	7	6	5	4	3	2	1	0
Field	–	THERMWARN1_THRESH[6:0]						
Reset	–	0b1000110						
Access Type	–	Write, Read						
Restriction	–	Normal						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMWAR N1_THRESH	6:0	EN	Sets the first thermal warning threshold temperature.	0x00: 50°C 0x01: 51°C 0x02: 52°C ...: ... 0x62: 148°C 0x63: 149°C 0x64-0x7F: 150°C

Warning Threshold 2 Amp 1 (0x2754)

BIT	7	6	5	4	3	2	1	0
Field	–	THERMWARN2_THRESH[6:0]						
Reset	–	0b1000110						
Access Type	–	Write, Read						
Restriction	–	Normal						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMWAR N2_THRESH	6:0	EN	Sets the second thermal warning threshold temperature.	0x00: 50°C 0x01: 51°C 0x02: 52°C ...: ... 0x62: 148°C 0x63: 149°C 0x64-0x7F: 150°C

Thermal Shutdown Threshold (0x2758)

BIT	7	6	5	4	3	2	1	0
Field	–	THERMSHDN_THRESH[6:0]						
Reset	–	0b1100100						
Access Type	–	Write, Read						
Restriction	–	Normal						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMSHDN_THRESH	6:0	EN	Sets the thermal shutdown threshold temperature.	0x00: 50°C 0x01: 51°C 0x02: 52°C .... 0x30: 98°C 0x31: 99°C 0x64 to 0x7F: 150°C

Thermal Hysteresis (0x275C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	THERM_HYST[1:0]	
Reset	–	–	–	–	–	–	0b10	
Access Type	–	–	–	–	–	–	Write, Read	
Restriction	–	–	–	–	–	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERM_HYST	1:0	EN	Controls the amount hysteresis applied to the thermal threshold measurements.	0x0: 2°C 0x1: 5°C 0x2: 7°C 0x3: 10°C

Thermal Foldback Settings (0x275F)

BIT	7	6	5	4	3	2	1	0
Field	THERMFB_HOLD[1:0]		THERMFB_RLS[1:0]		THERMFB_SLOPE2[1:0]		THERMFB_SLOPE1[1:0]	
Reset	0b11		0b00		0b01		0b01	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	
Restriction	Normal		Normal		Normal		Normal	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMFB_HOLD	7:6	TFB	The thermal foldback hold time controls how long the device temperature must remain below the configured thermal threshold hysteresis before thermal foldback release begins.	0x0: 0ms 0x1: 20ms 0x2: 40ms 0x3: 80ms
THERMFB_RLS	5:4	TFB	This sets the release rate of the thermal foldback attenuation.	0x0: 3 ms/dB 0x1: 10 ms/dB 0x2: 100 ms/dB 0x3: 300 ms/dB
THERMFB_SLOPE2	3:2	TFB	This sets the slope of the thermal foldback attenuation when die temperature exceeds THERMWARN2_THRESH.	0x0: 0.25 dB/°C 0x1: 0.5 dB/°C 0x2: 1.0 dB/°C 0x3: 2.0 dB/°C
THERMFB_SLOPE1	1:0	TFB	This sets the slope of the thermal foldback attenuation when the die temperature exceeds	0x0: 0.25 dB/°C 0x1: 0.5 dB/°C

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			the thermal-warning1 threshold (THERMWARN1_THRESH) but is lower than the thermal-warning2 threshold (THERMWARN2_THRESH).	0x2: 1.0 dB/°C 0x3: 2.0 dB/°C

Thermal Foldback Enable (0x276F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	THERMFB_EN
Reset	–	–	–	–	–	–	–	0b1
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMFB_EN	0	–	Enables Thermal Foldback.	0: Thermal Foldback is Disabled. 1: Thermal Foldback is Enabled.

BPE State (0x2800)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BPE_STATE[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read Only		
Restriction	–	–	–	–	–	Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_STATE	2:0	–	Current level of Brownout Controller. Reads back 000 when EN = 0.	000: Brownout inactive - normal operation 001: Level 3 010: Level 2 011: Level 1 100: Level 0 101 to 111: Reserved

BPE L3 Threshold MSB (0x2801)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L3_VTHRESH[8:1]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
BPE_L3_VTHRESH	7:0	BPE	BPE_Ln_VTHRESH[8:0] Sets the trigger level for each threshold in the Brownout Controller. See the Measurement ADC CH0 (PVDD) Result register to set these levels.

BITFIELD	BITS	RES	DESCRIPTION
			A value of 0000 0000 (all zeros) means that the state is not used and is entirely bypassed.

BPE L3 Threshold LSB (0x2802)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BPE_L3_VTHRESH[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
BPE_L3_VTHRESH	0	BPE	

BPE L2 Threshold MSB (0x2803)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L2_VTHRESH[8:1]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
BPE_L2_VTHRESH	7:0	BPE	BPE_Ln_VTHRESH[8:0] Sets the trigger level for each threshold in the Brownout Controller. See the Measurement ADC CH0 (PVDD) Result register to set these levels. A value of 0000 0000 (all zeros) means that the state is not used and is entirely bypassed.

BPE L2 Threshold LSB (0x2804)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BPE_L2_VTHRESH[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
BPE_L2_VTHRESH	0	BPE	

BPE L1 Threshold MSB (0x2805)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L1_VTHRESH[8:1]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
BPE_L1_VTHRESH	7:0	BPE	BPE_Ln_VTHRESH[8:0] Sets the trigger level for each threshold in the Brownout Controller. See the Measurement ADC CH0 (PVDD) Result register to set these levels. A value of 0000 0000 (all zeros) means that the state is not used and is entirely bypassed.

BPE L1 Threshold LSB (0x2806)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BPE_L1_VTHRESH[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
BPE_L1_VTHRESH	0	BPE	

BPE L0 Threshold MSB (0x2807)

BIT	7	6	5	4	3	2	1	0
Field	BPE_L0_VTHRESH[8:1]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
BPE_L0_VTHRESH	7:0	BPE	BPE_Ln_VTHRESH[7:0] Sets the trigger level for each threshold in the Brownout Controller. See the Measurement ADC CH0 (PVDD) Result register to set these levels. BA value of 0000 0000 (all zeros) means that the state is not used and is entirely bypassed (no hold times). Level 0 cannot be bypassed by writing all zeros.

BPE L0 Threshold LSB (0x2808)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BPE_L0_VTHRESH[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
BPE_L0_VTHRESH	0	BPE	

BPE L3 Dwell and Hold Time (0x2809)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L3_DWELL[2:0]			BPE_L3_HOLD[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_DWELL	5:3	BPE	Sets the BPE level 3 gain attenuation dwell time.	0x0: 0µs 0x1: 100µs 0x2: 250µs 0x3: 500µs 0x4: 1000µs 0x5: 2000µs 0x6: 4000µs 0x7: 8000µs
BPE_L3_HOLD	2:0	BPE	Sets the BPE level 3 gain attenuation hold time.	0x0: 0ms 0x1: 10ms 0x2: 100ms 0x3: 250ms 0x4: 500ms 0x5: 1000ms 0x6: 1000ms 0x7: Infinite

BPE L2 Dwell and Hold Time (0x280A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L2_DWELL[2:0]			BPE_L2_HOLD[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L2_DWELL	5:3	BPE	Sets the BPE level 2 gain attenuation dwell time.	0x0: 0µs 0x1: 100µs

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x2: 250µs 0x3: 500µs 0x4: 1000µs 0x5: 2000µs 0x6: 4000µs 0x7: 8000µs
BPE_L2_HOLD	2:0	BPE	Sets the BPE level 2 gain attenuation hold time.	0x0: 0ms 0x1: 10ms 0x2: 100ms 0x3: 250ms 0x4: 500ms 0x5: 1000ms 0x6: 1000ms 0x7: Infinite

BPE L1 Dwell and Hold Time (0x280B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L1_DWELL[2:0]			BPE_L1_HOLD[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_DWELL	5:3	BPE	Sets the BPE level 1 gain attenuation dwell time.	0x0: 0µs 0x1: 100µs 0x2: 250µs 0x3: 500µs 0x4: 1000µs 0x5: 2000µs 0x6: 4000µs 0x7: 8000µs
BPE_L1_HOLD	2:0	BPE	Sets the BPE level 1 gain attenuation hold time.	0x0: 0ms 0x1: 10ms 0x2: 100ms 0x3: 250ms 0x4: 500ms 0x5: 1000ms 0x6: 1000ms 0x7: Infinite

BPE L0 Hold Time (0x280C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BPE_L0_HOLD[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		
Restriction	–	–	–	–	–	Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_HOLD	2:0	BPE	Sets the BPE level 0 gain attenuation hold time.	0x0: 0ms 0x1: 10ms 0x2: 100ms

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x3: 250ms 0x4: 500ms 0x5: 1000ms 0x6: 1000ms 0x7: Infinite

BPE L3 Attack and Release Step (0x280D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L3_STEP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_STEP	3:0	BPE	Sets the BPE level 3 gain attenuation step size.	0x0: 0.0625dB 0x1: 0.125dB 0x2: 0.1875dB 0x3: 0.25dB 0x4: 0.375dB 0x5: 0.5dB 0x6: 0.75dB 0x7: 1.0dB 0x8: 1.5dB 0x9: 2.0dB 0xA: 2.5dB 0xB: 3.0dB 0xC: 4.0dB 0xD: 5.0dB 0xE: 5.5dB 0xF: 6.0dB

BPE L2 Attack and Release Step (0x280E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L2_STEP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L2_STEP	3:0	BPE	Sets the BPE level 2 gain attenuation step size.	0x0: 0.0625dB 0x1: 0.125dB 0x2: 0.1875dB 0x3: 0.25dB 0x4: 0.375dB 0x5: 0.5dB 0x6: 0.75dB 0x7: 1.0dB 0x8: 1.5dB 0x9: 2.0dB 0xA: 2.5dB 0xB: 3.0dB 0xC: 4.0dB 0xD: 5.0dB

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0xE: 5.5dB 0xF: 6.0dB

BPE L1 Attack and Release Step (0x280F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L1_STEP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_STEP	3:0	BPE	Sets the BPE level 1 gain attenuation step size.	0x0: 0.0625dB 0x1: 0.125dB 0x2: 0.1875dB 0x3: 0.25dB 0x4: 0.375dB 0x5: 0.5dB 0x6: 0.75dB 0x7: 1.0dB 0x8: 1.5dB 0x9: 2.0dB 0xA: 2.5dB 0xB: 3.0dB 0xC: 4.0dB 0xD: 5.0dB 0xE: 5.5dB 0xF: 6.0dB

BPE L0 Attack and Release Step (0x2810)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L0_STEP[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_STEP	3:0	BPE	Sets the BPE level 0 gain attenuation step size.	Value: Decode 0x0: 0.0625dB 0x1: 0.125dB 0x2: 0.1875dB 0x3: 0.25dB 0x4: 0.375dB 0x5: 0.5dB 0x6: 0.75dB 0x7: 1.0dB 0x8: 1.5dB 0x9: 2.0dB 0xA: 2.5dB 0xB: 3.0dB 0xC: 4.0dB 0xD: 5.0dB 0xE: 5.5dB 0xF: 6.0dB

BPE L3 Max Gain Attn (0x2811)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BPE_L3_MAXATTN[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_MAXATTN	4:0	BPE	Sets the BPE level 3 maximum gain attenuation.	0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4.. 0x1D: ...(-1dB steps) 0x1E: -30dB 0x1F: -31dB

BPE L2 Max Gain Attn (0x2812)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BPE_L2_MAXATTN[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L2_MAXATTN	4:0	BPE	Sets the BPE level 2 maximum gain attenuation.	0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4.. 0x1D: ...(-1dB steps) 0x1E: -30dB 0x1F: -31dB

BPE L1 Max Gain Attn (0x2813)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BPE_L1_MAXATTN[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_MAXATTN	4:0	BPE	Sets the BPE level 1 maximum gain attenuation.	0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4..

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x1D: ...(-1dB steps) 0x1E: -30dB 0x1F: -31dB

BPE L0 Max Gain Attn (0x2814)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	BPE_L0_MAXATTN[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_MAXATTN	4:0	BPE	Sets the BPE level 0 maximum gain attenuation.	0x0: 0dB 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4.. 0x1D: ...(-1dB steps) 0x1E: -30dB 0x1F: -31dB

BPE L3 Gain Attack and Rls Rates (0x2815)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L3_GAIN_RLS[2:0]			BPE_L3_GAIN_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_GAIN_RLS	5:3	BPE	Sets the BPE level 3 gain attenuation release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L3_GAIN_ATK	2:0	BPE	Sets the BPE level 3 gain attenuation attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L2 Gain Attack and Rls Rates (0x2816)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L2_GAIN_RLS[2:0]			BPE_L2_GAIN_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L2_GAIN_RLS	5:3	BPE	Sets the BPE level 2 gain attenuation release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L2_GAIN_ATK	2:0	BPE	Sets the BPE level 2 gain attenuation attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L1 Gain Attack and Rls Rates (0x2817)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L1_GAIN_RLS[2:0]			BPE_L1_GAIN_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_GAIN_RLS	5:3	BPE	Sets the BPE level 1 gain attenuation release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L1_GAIN_ATK	2:0	BPE	Sets the BPE level 1 gain attenuation attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L0 Gain Attack and Rls Rates (0x2818)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L0_GAIN_RLS[2:0]			BPE_L0_GAIN_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_GAIN_RLS	5:3	BPE	Sets the BPE level 0 gain attenuation release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L0_GAIN_ATK	2:0	BPE	Sets the BPE level 0 gain attenuation attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L3 Limiter Config (0x2819)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L3_LIM[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_LIM	3:0	BPE	Sets the limiter threshold for BPE level 3.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -7dBFS 0x8: -8dBFS 0x9: -9dBFS 0xA: -10dBFS 0xB: -11dBFS 0xC: -12dBFS 0xD: -13dBFS 0xE: -14dBFS 0xF: -15dBFS

BPE L2 Limiter Config (0x281A)

BIT	7	6	5	4	3	
Field	–	–	–	–		
Reset	–	–	–	–		
Access Type	–	–	–	–		
Restriction	–	–	–	–		

BITFIELD	BITS	RES	DESCRIPTION	
BPE_L2_LIM	3:0	BPE	Sets the limiter threshold for BPE level 2.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -7dBFS 0x8: -8dBFS 0x9: -9dBFS 0xA: -10dBFS 0xB: -11dBFS 0xC: -12dBFS 0xD: -13dBFS 0xE: -14dBFS 0xF: -15dBFS

BPE L1 Limiter Config (0x281B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L1_LIM[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_LIM	3:0	BPE	Sets the limiter threshold for BPE level 1.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -7dBFS 0x8: -8dBFS 0x9: -9dBFS 0xA: -10dBFS 0xB: -11dBFS 0xC: -12dBFS 0xD: -13dBFS 0xE: -14dBFS 0xF: -15dBFS

BPE L0 Limiter Config (0x281C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BPE_L0_LIM[3:0]			

BIT	7	6	5	4	3	2	1	0
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_LIM	3:0	BPE	Sets the limiter threshold for BPE level 0.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -7dBFS 0x8: -8dBFS 0x9: -9dBFS 0xA: -10dBFS 0xB: -11dBFS 0xC: -12dBFS 0xD: -13dBFS 0xE: -14dBFS 0xF: -15dBFS

BPE L3 Limiter Attack and Release Rates (0x281D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L3_LIM_RLS[2:0]			BPE_L3_LIM_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L3_LIM_RLS	5:3	BPE	Sets the BPE level 3 limiter release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L3_LIM_ATK	2:0	BPE	Sets the BPE level 3 limiter attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L2 Limiter Attack and Release Rates (0x281E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L2_LIM_RLS[2:0]			BPE_L2_LIM_ATK[2:0]		
Reset	–	–	0b000			0b000		

BIT	7	6	5	4	3	2	1	0
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L2_LIM_RLS	5:3	BPE	Sets the BPE level 2 limiter release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L2_LIM_ATK	2:0	BPE	Sets the BPE level 2 limiter attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L1 Limiter Attack and Release Rates (0x281F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L1_LIM_RLS[2:0]			BPE_L1_LIM_ATK[2:0]		
Reset	–	–	0b000			0b000		
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L1_LIM_RLS	5:3	BPE	Sets the BPE level 1 limiter release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L1_LIM_ATK	2:0	BPE	Sets the BPE level 1 limiter attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE L0 Limiter Attack and Release Rates (0x2820)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BPE_L0_LIM_RLS[2:0]			BPE_L0_LIM_ATK[2:0]		
Reset	–	–	0b000			0b000		

BIT	7	6	5	4	3	2	1	0
Access Type	–	–	Write, Read			Write, Read		
Restriction	–	–	Normal			Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_L0_LIM_RLS	5:3	BPE	Sets the BPE level 0 limiter release rate.	0x0: 5ms/step 0x1: 10ms/step 0x2: 25ms/step 0x3: 50ms/step 0x4: 100ms/step 0x5: 250ms/step 0x6: 500ms/step 0x7: 1000ms/step
BPE_L0_LIM_ATK	2:0	BPE	Sets the BPE level 0 limiter attack rate.	0x0: 2.5µs/step 0x1: 5µs/step 0x2: 10µs/step 0x3: 25µs/step 0x4: 50µs/step 0x5: 100µs/step 0x6: 250µs/step 0x7: 500µs/step

BPE Threshold Hysteresis (0x2821)

BIT	7	6	5	4	3	2	1	0
Field	BPE_VTHRESH_HYST[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_VTHRESH_HYST	7:0	BPE	Sets the hysteresis to move up to the next level in the Brownout Controller. See the Measurement ADC PVDD channel result register to set these levels.	00000000: No hysteresis 00000001: 1 LSB of hysteresis 00000010: 2 LSBs of hysteresis ...: 1 LSB steps 11111101: 253 LSBs of hysteresis 11111110: 254 LSBs of hysteresis 11111111: 255 LSBs of hysteresis

BPE Infinite Hold Clear (0x2822)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BPE_HLD_RLS
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_HLD_RLS	0	BPE	Manually releases the BPE controller when infinite hold is enabled.	0x0: Writing 0 has no effect. 0x1: Release the Brownout-Protection Engine Controller from Infinite Hold.

BPE Lowest State (0x2824)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	BPE_LOWEST[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Read, Ext		
Restriction	–	–	–	–	–	Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_LOWEST	2:0	–	Returns the lowest level the Brownout-Protection Engine has transitioned to. Upon reading the register it is updated to show the current level of the brownout controller.	000: Brownout inactive - normal operation 001: Level 3 010: Level 2 011: Level 1 100: Level 0 101 to 111: Reserved

BPE Lowest Gain (0x2825)

BIT	7	6	5	4	3	2	1	0
Field	BPE_LOWEST_GAIN[7:0]							
Reset	0x00							
Access Type	Read, Ext							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_LOWEST_GAIN	7:0	–	Returns the lowest gain (highest gain attenuation) of the Brownout-Protection Engine. Upon reading the register, it is updated to show the current gain attenuation applied by the BPE. Gain format: 5-bit integer and 3-bit fraction. The integer part is 1 dB per step, while fractional part is 1/8 dB per step.	000: Brownout inactive - normal operation 001: Level 3 010: Level 2 011: Level 1 100: Level 0 101 to 111: Reserved

BPE Lowest Limiter (0x2826)

BIT	7	6	5	4	3	2	1	0
Field	BPE_LOWEST_LIMIT[7:0]							
Reset	0x00							
Access Type	Read, Ext							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_LOWEST_LIMIT	7:0	–	Return the lowest limiter setting applied by the Brownout-Protection Engine. Upon reading the register it is updated to show the current limiter setting of the BPE. Limiter format: 4-bit integer and 4-bit fraction. The integer part is 1 dB per step, while the fractional part is 1/16 dB per step.	000: Brownout inactive - normal operation 001: Level 3 010: Level 2 011: Level 1 100: Level 0 101 to 111: Reserved

BPE Enable (0x283F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	BPE_LIM_EN	BPE_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BPE_LIM_EN	1	EN	Enables the BPE Limiter function.	0x0: The BPE Limiter is Disabled. 0x1: The BPE Limiter is Enabled.
BPE_EN	0	–	Enables the BPE function.	0x0: BPE is Disabled. 0x1: BPE is Enabled.

DHT Configuration 1 (0x2840)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_VROT_PNT[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_VROT_PNT	3:0	DHT	Sets the DRC Rotation Point.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -8dBFS 0x8: -10dBFS 0x9: -12dBFS 0xA: -15dBFS 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

Limiter Configuration 1 (0x2841)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_HR[4:0]				
Reset	–	–	–	0b01000				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_HR	4:0	–	Selects the DHT supply headroom for the DRC and Limiter functions.	0x0: -20% 0x1: -17.5% 0x2: -15% 0x3: -12.5% 0x4: -10% 0x5: -7.5% 0x6: -5.0% 0x7: -2.5% 0x8: 0% 0x9: +2.5% 0xA: +5.0% 0xB: +7.5% 0xC: +10% 0xD: +12.5% 0xE: +15% 0xF: +17.5% 010: +20%

Limiter Configuration 2 (0x2842)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DHT_LIM_THRESH[4:0]					DHT_LIM_MODE
Reset	–	–	0b00000					0b0
Access Type	–	–	Write, Read					Write, Read
Restriction	–	–	Normal					Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_LIM_THRESH	5:1	DHT	Selects the fixed threshold level for signal level limiter mode (SLL). Has no effect in signal distortion limiter mode (SDL).	00000: 0dBFS 00001: -1dBFS 00010: -2dBFS ...: (-1dBFS steps) 01110: -14dBFS 01111: -15dBFS 10000 to 11111: Reserved
DHT_LIM_MODE	0	DHT	Selects whether the DHT limiter is in signal distortion or signal level limiter mode.	0: Signal Distortion Limiter mode where limiter threshold tracks supply 1: Signal Level Limiter mode where limiter uses fixed thresholds

DHT Configuration 2 (0x2843)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	DHT_MAX_ATN[4:0]				
Reset	–	–	–	0b10100				
Access Type	–	–	–	Write, Read				
Restriction	–	–	–	Normal				

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_MAX_ATN	4:0	DHT	Selects the maximum attenuation that can be applied to the audio signal by the DHT.	0x0: Reserved 0x1: -1dB 0x2: -2dB 0x3: -3dB 0x4: -4dB

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x5: -5dB 0x6: -6dB 0x7: -7dB 0x8: -8dB 0x9: -9dB 0xA: -10dB 0xB: -11dB 0xC: -12dB 0xD: -13dB 0xE: -14dB 0xF: -15dB 0x10: -16dB 0x11: -17dB 0x12: -18dB 0x13: -19dB 0x14: -20dB 0x15-0x1F: Reserved

DHT Configuration 3 (0x2844)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_ATK_RATE[3:0]			
Reset	–	–	–	–	0x2			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_ATK_RATE	3:0	–	Selects the DHT attack rate.	0x0: 20µs/dB 0x1: 40µs/dB 0x2: 80µs/dB 0x3: 160µs/dB 0x4: 320µs/dB 0x5: 640µs/dB 0x6: 1.28ms/dB 0x7: 2.56ms/dB 0x8: 5.12ms/dB 0x9: 10.24ms/dB 0xA: 20.48ms/dB 0xB: 40.96ms/dB 0xC: 81.92ms/dB 0xD: 163.84ms/dB 0xE: Reserved 0xF: Reserved

DHT Configuration 4 (0x2845)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_RLS_RATE[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_RLS_RATE	3:0	–	Selects the DHT release rate. For release due to signal level change, settings 0x0-0x2 have a	0x0: 2ms/dB 0x1: 4ms/dB

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			release rate of 15ms/dB. For release due to PVDD level change, settings 0x0-0x2 follow the table below.	0x2: 7ms/dB 0x3: 14ms/dB 0x4: 28ms/dB 0x5: 54ms/dB 0x6: 108ms/dB 0x7: 216ms/dB 0x8: 432ms/dB 0x9: 864ms/dB 0xA: 1.728s/dB 0xB: 3.456s/dB 0xC: 6.912s/dB 0xD: 13.824s/dB 0xE: Reserved 0xF: Reserved

DHT Supply Hysteresis Configuration (0x2846)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	DHT_SUPPLY_HYST[2:0]			DHT_SUPPLY_HYST_EN
Reset	–	–	–	–	0b011			0b1
Access Type	–	–	–	–	Write, Read			Write, Read
Restriction	–	–	–	–	Normal			Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_SUPPLY_HYST	3:1	DHT	Selects the supply hysteresis for DHT attenuation release when supply increases.	0x0: 1 LSB 0x1: 2 LSB 0x2: 3 LSB 0x3: 4 LSB 0x4: 6 LSB 0x5: 8 LSB 0x6: 10 LSB 0x7: 12 LSB 0x8: RSVD
DHT_SUPPLY_HYST_EN	0	DHT	Select whether PVDD DHT hysteresis is enabled or disabled.	0: DHT is disabled 1: DHT is enabled

DHT Enable (0x284F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DHT_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DHT_EN	0	SPK	Select whether DHT is enabled or disabled.	0: DHT is disabled 1: DHT is enabled

ET Levels (0x2860)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ET_LEVEL_SEL[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ET_LEVEL_SEL	3:0	–	Configures the number of levels of the ET algorithm.	0x0: Reserved 0x1: 2 Levels 0x2: 3 Levels 0x3: 4 Levels ... 0xF: 16 Levels

ET Level Step Size MSB (0x2861)

BIT	7	6	5	4	3	2	1	0
Field	ET_LVL_STEPSIZE[8:1]							
Reset	0x0F							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
ET_LVL_STEPSIZE	7:0	–	ET_LVL_STEPSIZE[8:0] Sets the step size for each level in the ET algorithm Decode: (DUTY_CYCLE_STEPSIZE(%)/100)*2^10

ET Level Step Size LSB (0x2862)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ET_LVL_STEPSIZE[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
ET_LVL_STEPSIZE	0	–	

ET Level PVDD Step Size MSB (0x2863)

BIT	7	6	5	4	3	2	1	0
Field	ET_PVDD_STEPSIZE[8:1]							
Reset	0x64							

BIT	7	6	5	4	3	2	1	0
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
ET_PVDD_STEPSIZE	7:0	–	ET_PVDD_STEPSIZE[8:0] Sets the voltage step size for each level in the ET algorithm Decode: PVDD_STEP*0.025

ET Level PVDD Step Size LSB (0x2864)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ET_PVDD_STEPSIZE[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
ET_PVDD_STEPSIZE	0	–	

Maximum Duty Cycle MSB (0x2866)

BIT	7	6	5	4	3	2	1	0
Field	ET_MAXDUTY_CYC[9:2]							
Reset	0xF3							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
ET_MAXDUTY_CYC	7:0	–	ET_MAXDUTYCYC[9:0] Sets the maximum duty cycle for Envelope Tracking Algorithm Decode: (MAX_DUTY%/100)*2^{10}

Maximum Duty Cycle LSB (0x2867)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ET_MAXDUTY_CYC[1:0]	
Reset	–	–	–	–	–	–	0b01	
Access Type	–	–	–	–	–	–	Write, Read	
Restriction	–	–	–	–	–	–	Normal	

BITFIELD	BITS	RES	DESCRIPTION
ET_MAXDUTY_CYC	1:0	–	

Minimum PVDD Level MSB (0x2868)

BIT	7	6	5	4	3	2	1	0
Field	MIN_PVDD_LVL[8:1]							
Reset	0x64							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION
MIN_PVDD_LVL	7:0	–	Min_PVDD_Lvl[8:0] Sets the minimum voltage for the ET algorithm Decode: MIN_PVDDV*0.025

Minimum PVDD Level LSB (0x2869)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	MIN_PVDD_LVL[0]
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION
MIN_PVDD_LVL	0	–	

ET PVDD headroom (0x286A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ET_PVDD_HDRM[5:0]					
Reset	–	–	0b100000					
Access Type	–	–	Write, Read					
Restriction	–	–	Normal					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ET_PVDD_HDRM	5:0	–	Headroom for the envelope tracking operation in 0.046875dB steps (The 1st step counts as 2 steps) Note settings below -1.5dB introduces a risk of clipping.	0x0: 0dB headroom 0x1: -0.09375dB 0x2: -0.140625dB 0x3 ... 0x20: -1.5dB ... 0x3D 0x3E: -2.953125dB 0x3F: -3dB

ET Delay Time (0x286C)

BIT	7	6	5	4	3	2	1	0
Field	–	ET_PB_DELAY_TIME[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						
Restriction	–	Normal						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ET_PB_DELAY_TIME	6:0	–	Sets the playback delay time from Audio data input to Speaker output. The step size, maximum programmable delay setting and the resultant maximum programmable delay time are determined by PCM sample rate (PCM_SR) configuration. See Envelope Tracking Output section to see the decode table based on each sample rate setting.	0x00: RESERVED

ET Level Hold Time (0x286E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ET_HOLD_TIME[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read		
Restriction	–	–	–	–	–	Normal		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ET_HOLD_TIME	2:0	–	Sets the hold time before the envelope tracker starts boost output voltage decrease.	000: 10 ms 001: 50 ms 010: 100 ms 011: 250 ms 100: 500 ms 101: 750 ms 110: 1000 ms 111: 1500 ms

AMP A Limiter Threshold 1 (0x2890)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_RMS_LIM_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_RMS_LIM_THRESH	7:0	RMS_EN	Sets the RMS Limiter Threshold for Amplifier A. See RMS Limiter section for decode of actual RMS threshold and input referred thresholds for DC and sinewave input signals.	0x0-0x18: From 0dBFs, in 0.25dBFs steps 0x19: -6.25dBFs 0x1A: -6.5dBFs 0x1B: -6.75dBFs 0x1C: -7dBFs

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			For the DC input signal, the input-referred threshold value is given as: Decode (dBFS) = 20 x $\log_{10}(\sqrt{(10^{(-\text{Value(In Decimal)} \times 0.25)/20)})}$ For the sinewave input signal, the input-referred threshold value is given as: Decode (dBFS) = 20 x $\log_{10}(\sqrt{(2 \times 10^{(-\text{Value(In Decimal)} \times 0.25)/20)})}$	0x1D: -7.25dBFs ..: .. 0x20: -8dBFs ..: .. 0x28: -10dBFs ..: .. 0x30: -12dBFs ..: .. 0x40: -16dBFs ..: .. 0xB8: -46dBFs ..: .. 0xE4: -57dBFs 0xE5-0xFF: RESERVED

AMP A Limiter Time Constant MSB (0x2893)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPA_RMS_LIM_TIME_CONST[19:16]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_RMS_LIM_TIME_CONST	3:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier A. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz.	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

AMP A Limiter Time Constant MSB (0x2894)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_RMS_LIM_TIME_CONST[15:8]							
Reset	0x02							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_RMS_LIM_TIME_CONST	7:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier A. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz.	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

AMP A Limiter Time Constant LSB (0x2895)

BIT	7	6	5	4	3	2	1	0
Field	AMPA_RMS_LIM_TIME_CONST[7:0]							

BIT	7	6	5	4	3	2	1	0
Reset	0xBB							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPA_RMS_LIM_TIME_CONST	7:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier A. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz.	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

AMP B Limiter Threshold 1 (0x2898)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_RMS_LIM_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_THRESH	7:0	RMS_EN	Sets the RMS Limiter Threshold for Amplifier B. See RMS Limiter section for decode of actual RMS threshold and input referred thresholds for DC and sinewave input signals. For the DC input signal, the input-referred threshold value is given as: Decode (dBFS) = $20 \times \log_{10}(\sqrt{(10^{(-\text{Value(InDecimal)} \times 0.25)/20)})}$ For the sinewave input signal, the input-referred threshold value is given as: Decode (dBFS) = $20 \times \log_{10}(\sqrt{(2 \times 10^{(-\text{Value(In Decimal)} \times 0.25)/20)})}$	0x0-0x18: From 0dBFs, in 0.25dBFs steps 0x19: -6.25dBFs 0x1A: -6.5dBFs 0x1B: -6.75dBFs 0x1C: -7dBFs 0x1D: -7.25dBFs ..: .. 0x20: -8dBFs ..: .. 0x28: -10dBFs ..: .. 0x30: -12dBFs ..: .. 0x40: -16dBFs ..: .. 0xB8: -46dBFs ..: .. 0xE4: -57dBFs 0xE5-0xFF: RESERVED

AMP B Limiter Time Constant MSB (0x289B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	AMPB_RMS_LIM_TIME_CONST[19:16]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			
Restriction	–	–	–	–	Normal			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_TIME_CONST	3:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier B. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz.	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

AMP B Limiter Time Constant MSB (0x289C)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_RMS_LIM_TIME_CONST[15:8]							
Reset	0x02							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_TIME_CONST	7:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier B. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

AMP B Limiter Time Constant LSB (0x289D)

BIT	7	6	5	4	3	2	1	0
Field	AMPB_RMS_LIM_TIME_CONST[7:0]							
Reset	0xBB							
Access Type	Write, Read							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_TIME_CONST	7:0	RMS_EN	Sets the time constant for the RMS Limiter function for Amplifier B. Time Constant (decimal) = $2^{25}/(RMS_{TC} \times Fs+1)$ where RMS_{TC} is in seconds (used for both attack and release) and F_S is in Hz	0x23 - 0x6522C: Valid Values for RMS_{TC} from 0.01s to 5s 0x80000 - 0xFFFFF: RESERVED

RMS Limiter Enable (0x28AF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	AMPB_RMS_LIM_EN	AMPA_RMS_LIM_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BIT	7	6	5	4	3	2	1	0
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
AMPB_RMS_LIM_EN	1	EN	Enables RMS Limiter for Amplifier B.	0x0: The RMS Limiter for Amplifier B is Disabled. 0x1: The RMS Limiter for Amplifier B is Enabled.
AMPA_RMS_LIM_EN	0	EN	Enables RMS Limiter for Amplifier A.	0x0: The RMS Limiter for Amplifier A is Disabled. 0x1: The RMS Limiter for Amplifier A is Enabled.

Group Write Address Ctrl (0x29F1)

BIT	7	6	5	4	3	2	1	0
Field	GRP_WR_ADDR[6:0]							GRP_WR_EN
Reset	0b0001000							0b0
Access Type	Write, Read							Write, Read
Restriction	Normal							Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
GRP_WR_ADDR	7:1	–	7-bit Group Write Address for the I^2C Device, only active when GRP_WR_EN is 1.	0x00 to 0x07: Reserved per I^2C bus specification. 0x08-0x7B: Valid 7-bit Group Write Addresses. 0x7C-0x7F: Reserved per I^2C bus specification.
GRP_WR_EN	0	–	Group Write Function Enable.	0x0: Group Write Function is Disabled. 0x1: Group Write Function Is Enabled.

Device Ramp Control (0x29FD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SHTDWN_RMPDN_BYPASS	STARTUP_RMPUP_BYPASS
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read
Restriction	–	–	–	–	–	–	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SHTDWN_RMPDN_BYPASS	1	EN	Controls whether the speaker amplifier path volume is internally ramped up during the startup and during volume changes.	0: Ramp enabled. 1: Ramp disabled - volume will change instantaneously.
STARTUP_RMPUP_BYPASS	0	EN	Controls whether the speaker amplifier path volume is internally ramped up during the startup and during volume changes.	0: Ramp enabled. 1: Ramp disabled - volume will change instantaneously.

Auto-Restart Behavior (0x29FE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OVC_AUTORESTART_EN	THERM_AUTORESTART_EN	VBAT_AUTORESTART_EN	PVDD_AUTORESTART_EN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read
Restriction	–	–	–	–	Normal	Normal	Normal	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
OVC_AUTORESTART_EN	3	EN	Controls whether or not the speaker amplifier is automatically reenabled after an overcurrent fault condition.	0: Overcurrent recovery is in manual mode 1: Overcurrent recovery is in auto mode
THERM_AUTORESTART_EN	2	EN	Controls whether or not the device automatically returns to the active state when the die temperature recovers from thermal shutdown.	0: Thermal Shutdown recovery is in manual mode. 1: Thermal shutdown recovery is in auto mode.
VBAT_AUTORESTART_EN	1	EN	Controls whether or not the device automatically returns to the active state when VBAT recovers from the UVLO event.	0: VBAT UVLO recovery is in manual mode. 1: VBAT UVLO recovery is in auto mode.
PVDD_AUTORESTART_EN	0	EN	Controls whether or not the device automatically returns to the active state when PVDD recovers from the UVLO event.	0: PVDD UVLO recovery is in manual mode. 1: PVDD UVLO recovery is in auto mode.

Global Enable (0x29FF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext
Restriction	–	–	–	–	–	–	–	Normal

BITFIELD	BITS	RES	DESCRIPTION	DECODE
EN	0	–	Disable or enable all blocks and reset all logic except the I^2C interface and control registers.	0: Device powered down. 1: Device enabled.

Device ID MSB (0x3FFD)

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID_MSB[7:0]							
Reset	0x84							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DEVICE_ID_MSB	7:0	–	ID of the device.	0x8425: Readback for MAX98425A 0x8415: Readback for MAX98415A

Device ID LSB (0x3FFE)

BIT	7	6	5	4	3	2	1	0
Field	DEVICE_ID_LSB[7:0]							
Reset	0x25							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
DEVICE_ID_LSB	7:0	–	ID of the device.	0x8425: Readback for MAX98425A. 0x8415: Readback for MAX98415A.

Revision ID (0x3FFF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x42							
Access Type	Read Only							
Restriction	Normal							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REV_ID	7:0	–	Revision of the device. Updated at every device revision.	0x42: Device Revision.

Applications Information

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Use at least four PCB layers and add thermal vias to the ground/power plane close to the device to ensure good thermal performance and high-end output power. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal. Ground the power signals and the analog signals of the IC separately at the system ground plane, to prevent switching interference from corrupting sensitive analog signals. Place the recommended supply decoupling capacitors as close as possible to the IC. The PVDD to PGND connection must be kept short and should have minimum trace length and loop area to ensure optimal Noise, THD+N, and EMI performance. Use wide, low-resistance output, supply, and ground traces. As load impedance decreases, the current drawn from the device outputs increases. At higher currents, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through a 100mΩ trace, 50mW is consumed in the trace. If power is delivered through a 10mΩ trace, only 5mW is consumed in the trace. Wide output, supply, and ground traces also improve the power dissipation of the device. The device is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on the top and bottom PCB planes. It is advisable to follow the layout of the MAX98415A/MAX98425A EV kit as closely as possible in the application. Thermal and performance measurements shown in the data sheet are measured with a 6-layer board (θ_{JA} = 28°C/W). As a result, the EV kit performance is likely better than what can be achieved with a JEDEC standard board.

Recommended External Components

Table 16 shows the recommended external components. See the *Typical Application Circuits* for more details.

Table 16. Component List

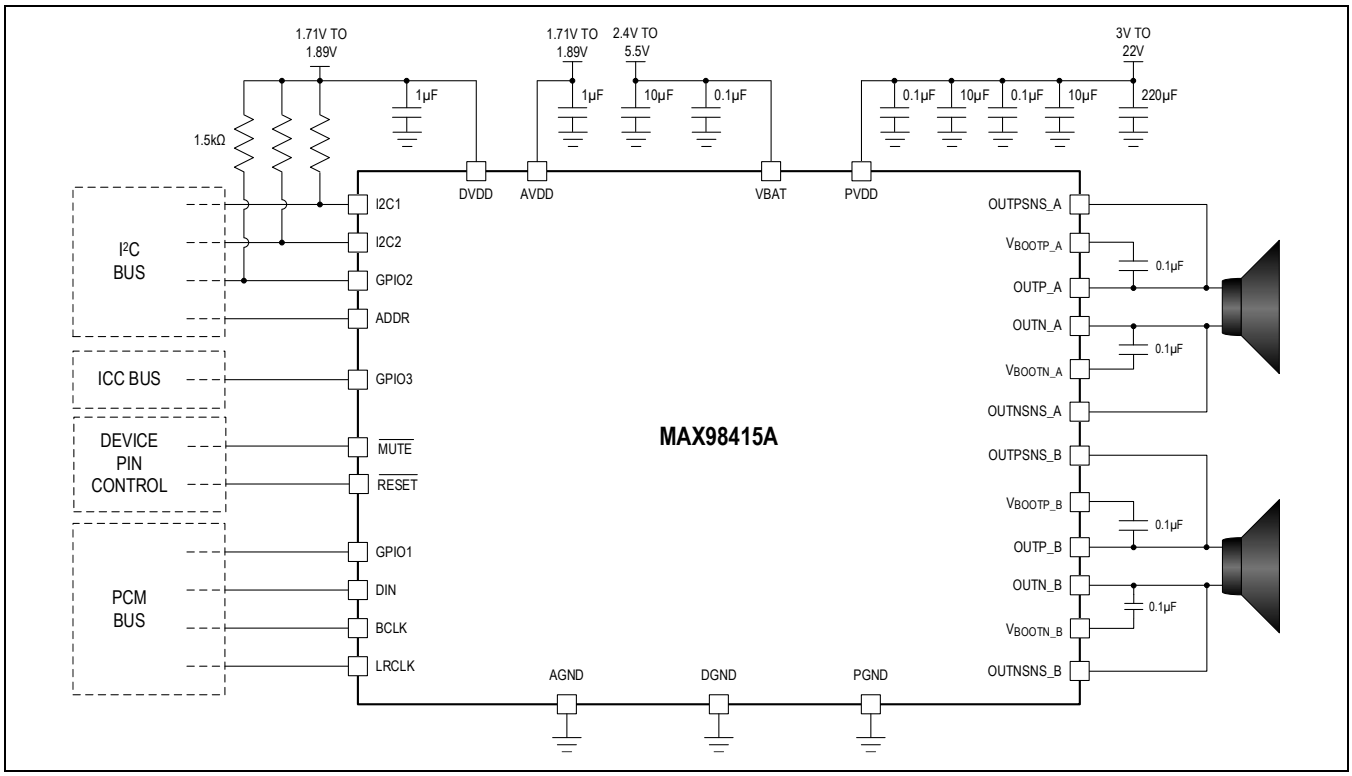
BUMP	VALUE	SIZE	VOLTAGE RATING (V)	DI-ELECTRIC
PVDD	220µF ± 20%	—	50	Alum-Elec
PVDD	10µF ± 10%	1206	50	X5R
PVDD	1µF ± 10%	0603	50	X5R
PVDD	0.1µF ± 10%	0402	50	X7R
VBAT	1µF ± 10%	0402	16	X5R
VBAT	10µF ± 10%	0603	16	X5R
DVDD	1µF ± 20%	0201	6.3	X5R
AVDD	1µF ± 20%	0201	6.3	X5R
V_{BOOTPX}	0.1µF ± 10%	0201	50	X7R
V_{BOOTNX}	0.1µF ± 10%	0201	50	X7R

Bootstrap Capacitors

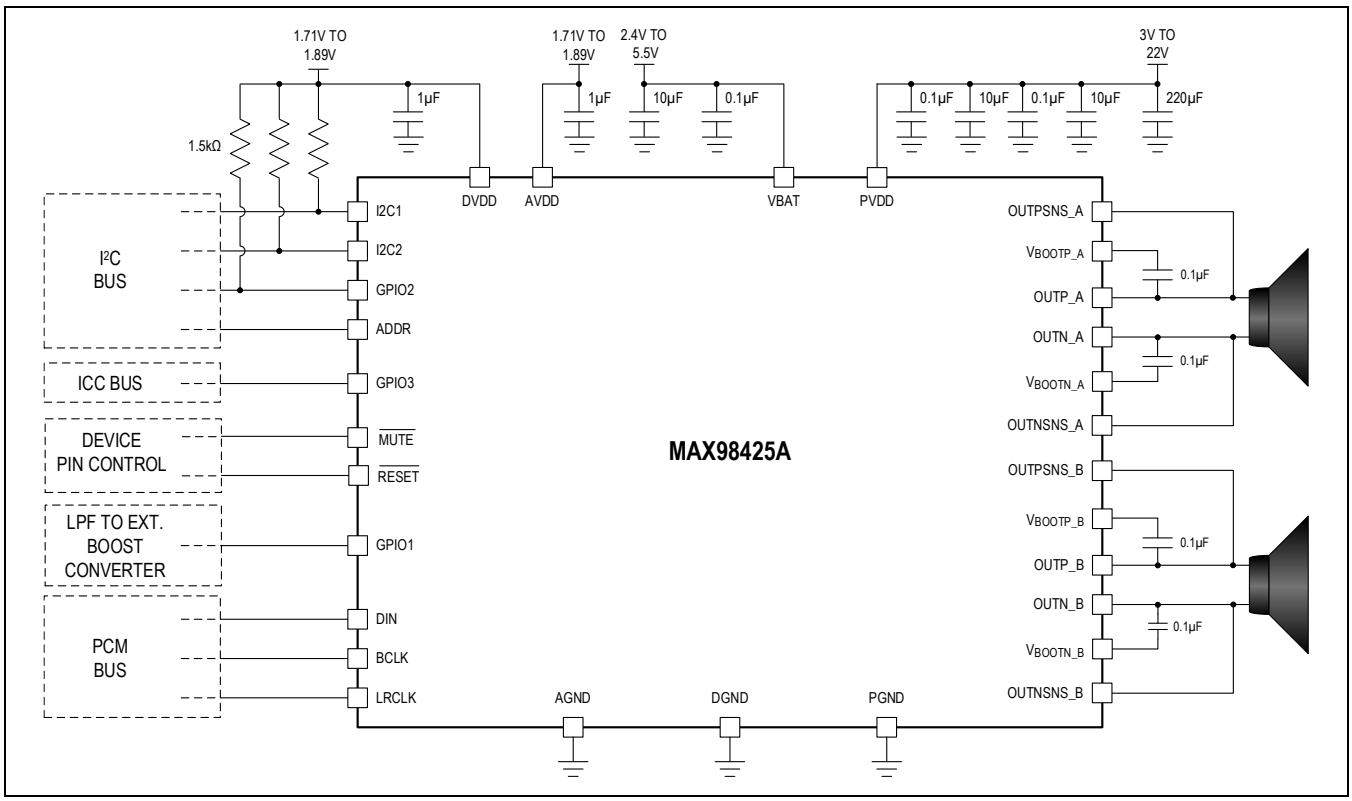
The output stage of the MAX98415A/MAX98425A uses NMOS power FETs as high-side drivers to provide high output power with high efficiency in a small package. A bootstrap capacitor connected between the OUTx pin and V_{BOOTx} pin acts as a floating power supply for the gate driver of the high-side nMOS power FET of the corresponding OUTx pin. During normal operation, the bootstrap capacitor gets charged when the PWM output forces the OUTx pin low i.e., the low-side nMOS power FET of the corresponding OUTx pin is on. As the high-side power FET of the OUTx pin turns on, OUTx and the corresponding V_{BOOTx} pin voltages rise due to capacitive action, thus providing the required high-side driver voltage. The necessary charge to turn on the high-side power FET comes from the bootstrap capacitor, and hence, every time the high-side power FET turns on, it loses charge, which needs to be replenished during the next low-side turn-on. Thus, it is important to choose a bootstrap capacitor value that can sustain this switching action i.e., large enough to not lose too much charge during high-side turn-on, and any other supervisory circuit biased from the bootstrap capacitor supply. However, there is an upper limit to how large the bootstrap capacitor can be, apart from being too large on the PCB. During hard-clipping at the output of the Class-D amplifier, the high-side power FET of the OUTx pin can remain on for hundreds of microseconds. This causes the bootstrap capacitor to continue to lose charge due to charge consumption by internal circuitry and capacitance leakage. When the bootstrap capacitor voltage becomes too low, it forces a small cycle of low-side turn-on to replenish the charge on the bootstrap capacitor. This is called a refresh cycle, and care must be taken to ensure that a large capacitor value does not force a refresh cycle at a rate that affects the audio band. It is recommended to use a 0.1µF, 16V capacitor as a bootstrap capacitor with the MAX98415A/MAX98425A and to place the capacitor as close to the pins as possible to minimize the loop between the OUTx and V_{BOOTx} pins.

Typical Application Circuits

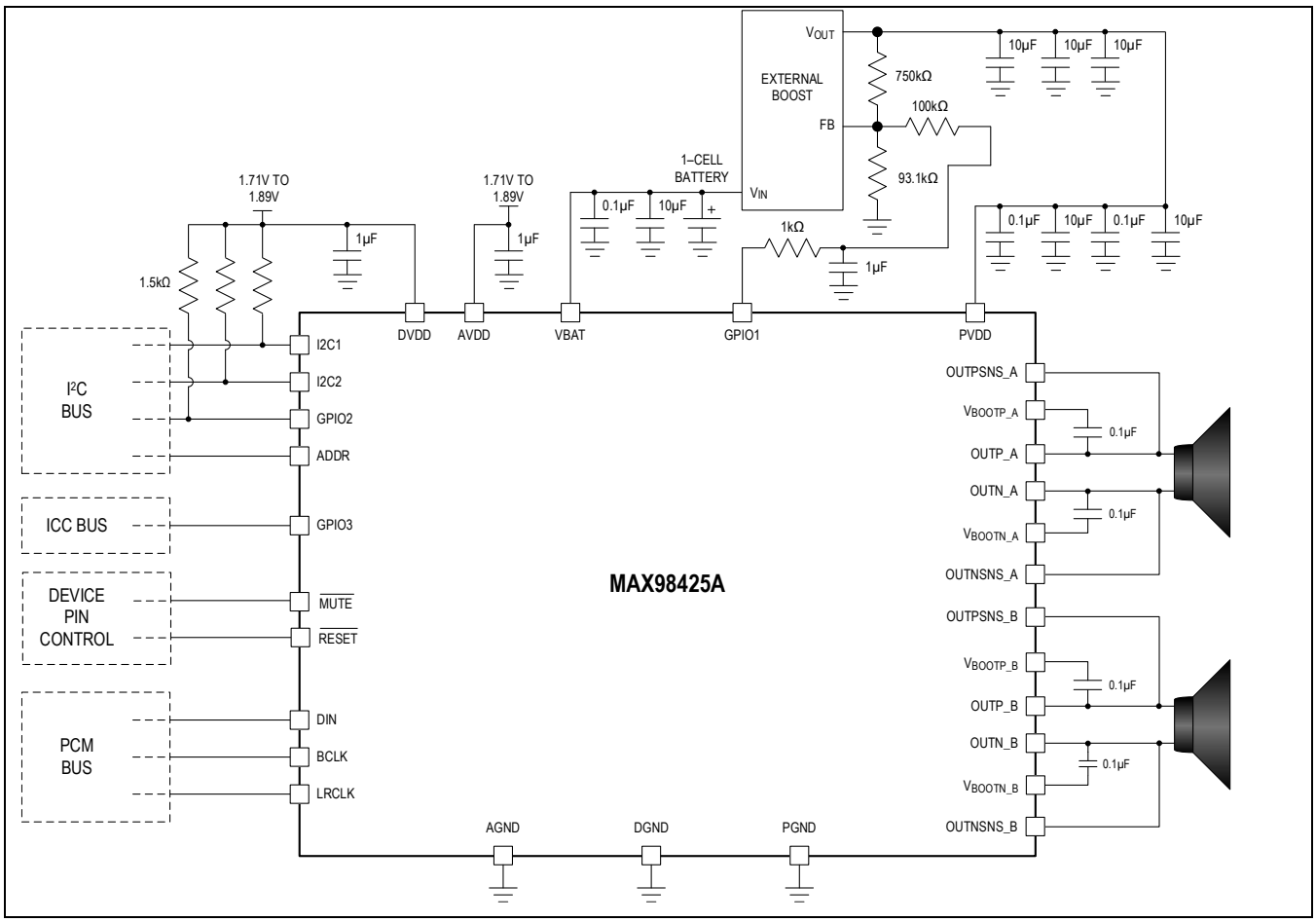
Typical Application Circuit for MAX98415A in Stereo Mode



Typical Application Circuit for MAX98425A in Stereo Mode



Typical Application Circuit for MAX98425A with External Boost Converter



Ordering Information

PART NUMBER	TEMP RANGE	PIN PACKAGE
MAX98415AEWL+	-40°C to +85°C	40 WLP
MAX98415AEWL+T	-40°C to +85°C	40 WLP
MAX98425AEWL+	-40°C to +85°C	40 WLP
MAX98425AEWL+T	-40°C to +85°C	40 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/25	Initial Release	—