16V Input, 4.6A Switching Current Low IQ Buck Converter

MAX77505

General Description

The MAX77505 is a low-quiescent current (800nA typ), high-efficiency hysteretic buck converter operating from a 2.5V to 16V input voltage range. The device offers high efficiency over the entire load range. Hence, it is ideal for either a primary battery or four alkaline battery-powered applications, which require long standby/idling time with short working time, such as asset tracking and door-lock devices.

A resistor (R_{SEL}) selects one of thirty preset output voltages between 0.8V and 5.5V. The device has input undervoltage lockout, cycle-by-cycle switch current limit, and thermal shutdown to protect the system and the device itself. The device is available in a 10-lead FC2QFN package (2.0mm x 2.0mm x 0.55mm).

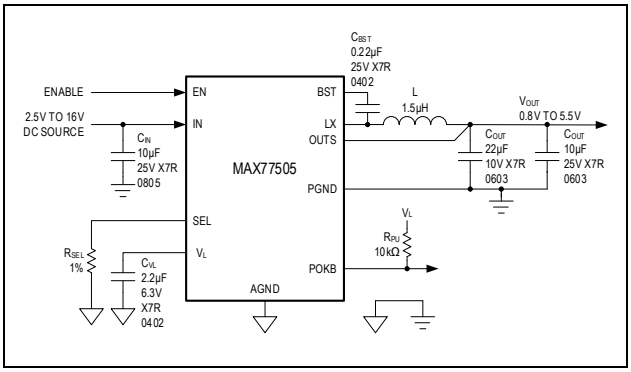
Applications

- 2-3 Cell Li+ Battery Applications
- 4-Cell Alkaline Battery Applications
- IoT, Wearable Devices
- Smart Meter, Door Locks, Asset Trackers, etc.

Benefits and Features

- Input Voltage: 2.5V to 16V
- Output Voltage: 0.8V to 5.5V
- Long Battery Life
  - 70nA Shutdown Current
  - 800nA Ultra-Low Quiescent Current (I_Q)
  - 86% Efficiency at 100µA Load at 7.6V_{IN}, 3.3V_{OUT}
  - 95% Peak Efficiency at 7.6V_{IN}, 3.3V_{OUT}
- POKB Output (Open-Drain)
- SEL Pin for Output Voltage Selection
- Protections Features
  - Cycle-by-Cycle Inductor Peak Current Limit
  - Short Circuit, Undervoltage Lockout (UVLO), and Thermal Protection
- FC2QFN-10 Package (2.0mm x 2.0mm x 0.55mm)

Simplified Application Diagram



***Ordering Information* appears at end of data sheet.**

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19-101751; Rev 0; 10/23

Absolute Maximum Ratings

IN, LX to PGND ..... -0.3V to +17.6V

LX to PGND (less than 10ns) (Note 1) .. (V_{IN} – 22)V to +22.0V

BST to LX ..... -0.3V to +2.0V

V_L, POKB, SEL to AGND ..... -0.3V to +2.0V

EN to AGND ..... -0.3V to +17.6V

OUTS to AGND ..... -0.3V to +6.0V

PGND to AGND ..... -0.3V to +0.3V

Continuous Power Dissipation at T_A = 70ºC (Derate 12.05mW/°C above +70°C) (Note 2) 963.70mW

Maximum Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (Reflow) ..... +260°C

Note 1: LX has internal clamp diodes to its corresponding PGND and IN. Applications that forward bias these diodes should not exceed the ICs package power dissipation limits.

Note 2: Package thermal measurements were obtained using the method described in JEDEC specification JESD51-7, using a FR-4, four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

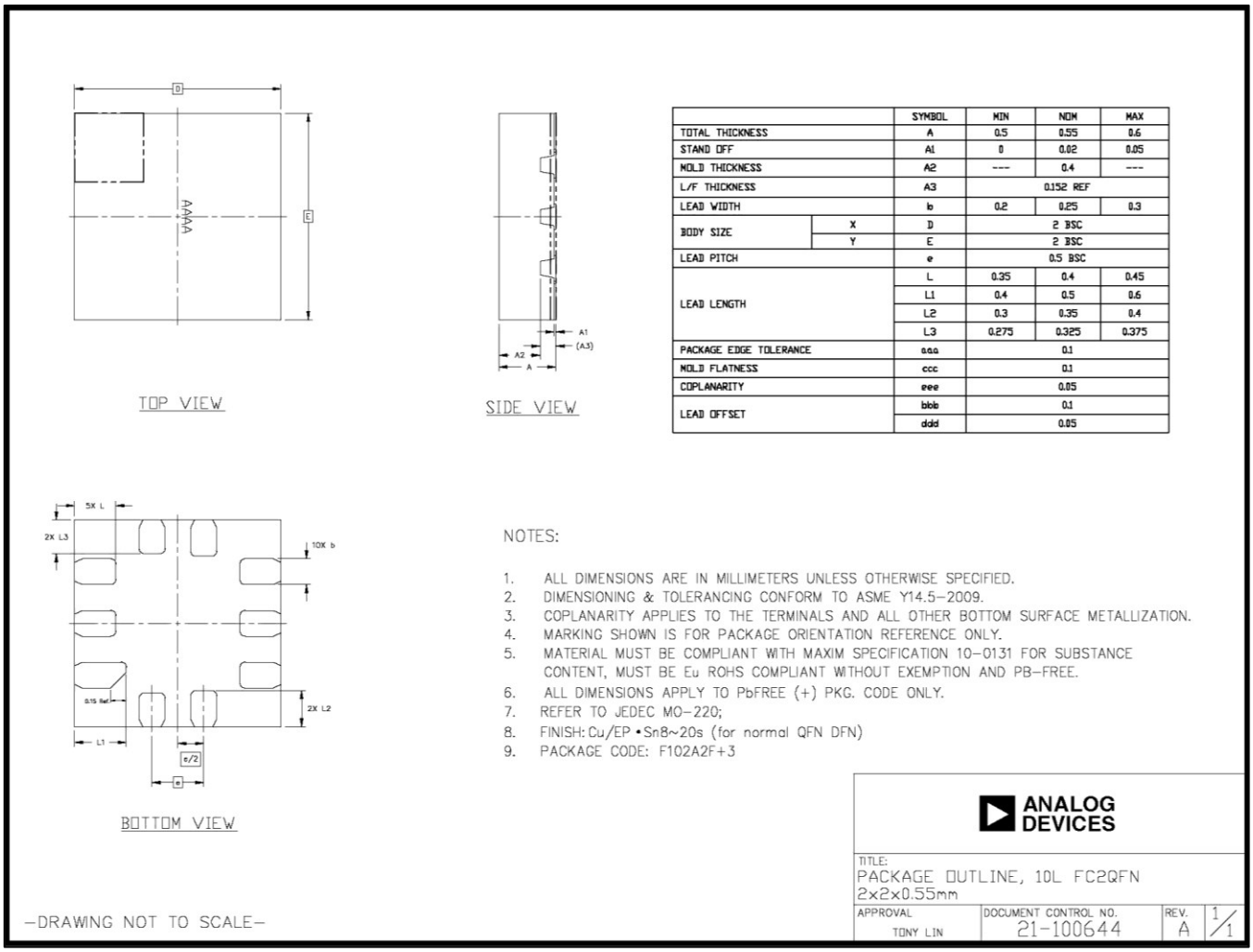
Recommended Operating Conditions

PARAMETERS	SYMBOL	CONDITIONS	TYPICAL RANGE
Input Voltage Range	V_{IN}		2.5V to 16V
Output Current Range	I_{OUT}		0A to 3A
Junction Temperature Range	T_J		-40°C to +125°C

Package Information

10 FC2QFN

Package Code	F102A2F+3
Outline Number	*21-100644*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	83.01°C/W
Junction-to-Case (BOT) Thermal Resistance (θ_{JC})	38.24°C/W



Electrical Characteristics

($T_A \approx T_J$, V_{IN} = 7.6V, V_{OUT} = 3.3V, Typicals are at $T_A \approx T_J$ = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77505 is tested under pulsed load conditions such that $T_A \approx T_J$. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods. (Note 3))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Operating Voltage Range	V_{IN}			2.5		16	V
Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{IN} rising		2.400	2.450	2.500	V
	V_{UVLO_F}	V_{IN} falling		2.325	2.375	2.425	
Shutdown Current	I_{SHDN}	EN = Low, V_{IN} < 13V, T_J = +25°C			70	300	nA
Quiescent Current	I_Q	EN = High, no load, T_J = +25°C			800		nA
OUTPUT VOLTAGE ACCURACY							
Output Voltage Range	V_{OUT}			0.8		5.5	V
Output Voltage Accuracy	V_{OUT_ACC}	V_{IN} = 2 x V_{OUT}	In CCM operation	-2		+2	%
Low-Power Mode Over-Regulation Hysteresis (Skip Lower Limit)	V_{OUT_HYS}	Measured as a percentage of target output voltage	0.8V ≤ V_{OUT} ≤ 2.3V	+2.75	+4.5	+6	%
			2.5V ≤ V_{OUT} ≤ 5.5V	+1.2	+2.75	+4	
OUTPUT VOLTAGE REGULATION							
Line Regulation	$\Delta V/V_{IN}$	(*Note 4*)	V_{IN} = 2.5V to 16V, I_{OUT} = 0.8A	-0.1		+0.1	%/V
Load Regulation	$\Delta V/I_{OUT}$	(*Note 4*)	In CCM operation		0.35		%/A
POWER STAGE							
High-Side MOSFET Peak Current Limit	I_{LIM}			4000	4600	5200	mA
High-Side MOSFET On-Resistance	R_{DSON_HS}	I_{LX} = -300mA			50		mΩ
Low-Side MOSFET On-Resistance	R_{DSON_LS}	I_{LX} = 300mA			45		mΩ
Switching Frequency	f_{SW}	In CCM operation			2.0		MHz
Output Voltage Active Discharge Resistance	R_{ADIS}				120		Ω
Minimum Effective Output Capacitance	$C_{EFF(MIN)}$	0.8V ≤ V_{OUT} < 1.5V			20		µF
		V_{OUT} ≥ 1.5V			10		
TIMING							
Turn-On Delay Time	t_{DLY_EN}	From EN = High to POKB = Low, T_J = -10°C to +125°C			3	32	ms
LOGIC THRESHOLD							
Input High Level	V_{IH}			1.2			V
Input Low Level	V_{IL}					0.4	V
Output Low Level	V_{OL}	I_{POKB} = -1mA				0.3	V
Inverted Power-OK (POKB) Threshold	V_{POKB_F}	V_{OUT} rising, expressed as a percentage of target V_{OUT}		90	93		%
	V_{POKB_R}	V_{OUT} falling, expressed as a percentage of target V_{OUT}			85	88	
THERMAL PROTECTION							

($T_A \approx T_J$, V_{IN} = 7.6V, V_{OUT} = 3.3V, Typicals are at $T_A \approx T_J$ = +25°C. Limits are 100% production tested at T_J = +25°C. The MAX77505 is tested under pulsed load conditions such that $T_A \approx T_J$. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant voltage range are guaranteed by design and characterization using statistical process control methods. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Threshold	T_{SHDN}	T_J rising		150		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			20		°C

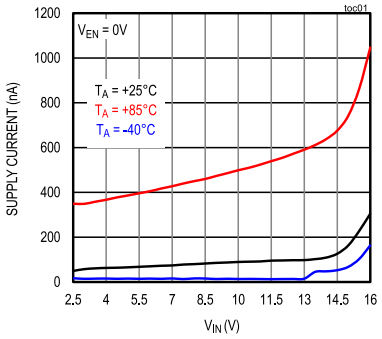
Note 3: The maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

Note 4: Not production tested. Design guidance only.

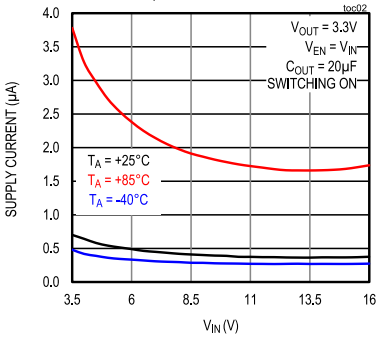
Typical Operating Characteristics

(V_{IN} = 7.6V, V_{OUT} = 3.3V, L = 1.5µH (Sumida 0420CDMCCDS-1R5MC), C_{OUT} = 3x10µF, T_A = +25°C, unless otherwise noted.)

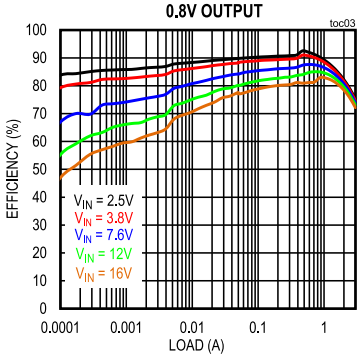
SHUTDOWN CURRENT



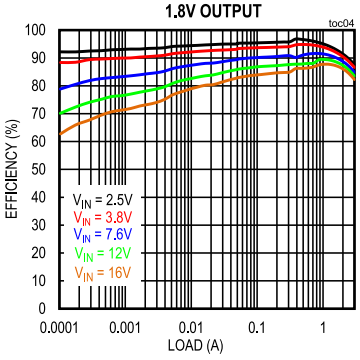
QUIESCENT CURRENT



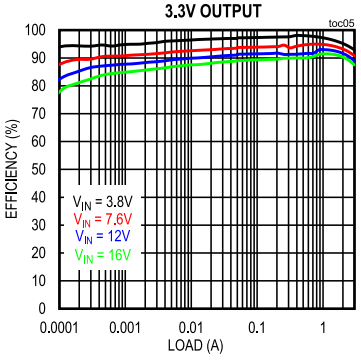
EFFICIENCY vs. LOAD 0.8V OUTPUT



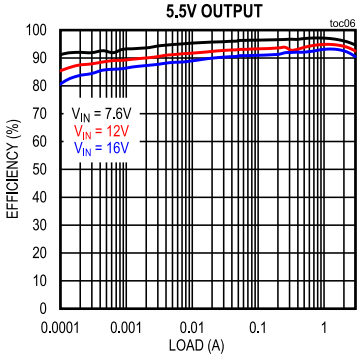
EFFICIENCY vs. LOAD 1.8V OUTPUT



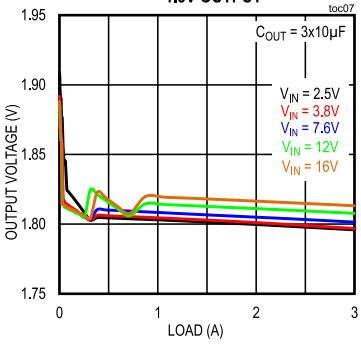
EFFICIENCY vs. LOAD 3.3V OUTPUT



EFFICIENCY vs. LOAD 5.5V OUTPUT



LOAD REGULATION 1.8V OUTPUT



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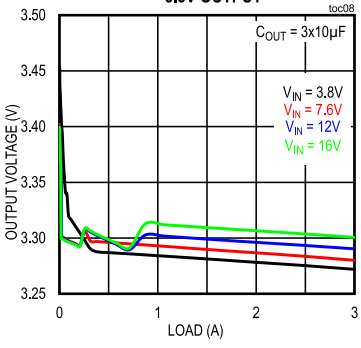

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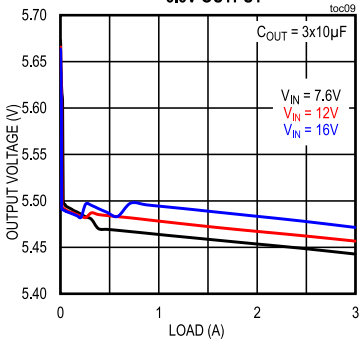
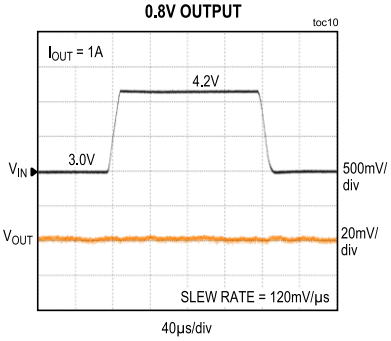


(V_{IN} = 7.6V, V_{OUT} = 3.3V, L = 1.5µH (Sumida 0420CDMCCDS-1R5MC), C_{OUT} = 3x10µF, T_A = +25°C, unless otherwise noted.)

LINE TRANSIENT RESPONSE 0.8V OUTPUT



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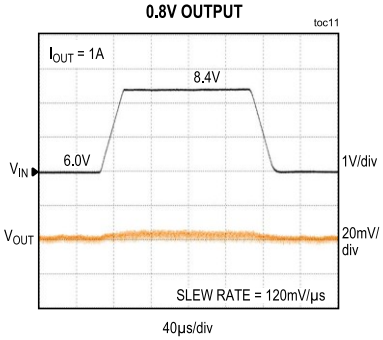
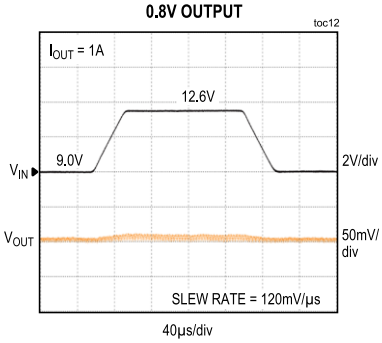
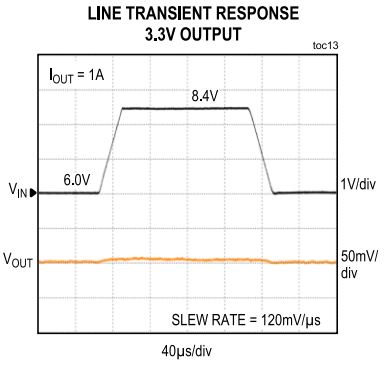


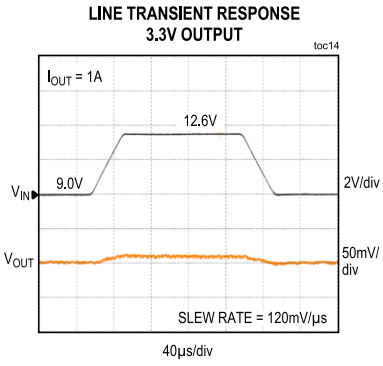
LINE TRANSIENT RESPONSE 0.8V OUTPUT



LINE TRANSIENT RESPONSE 3.3V OUTPUT



LINE TRANSIENT RESPONSE 3.3V OUTPUT



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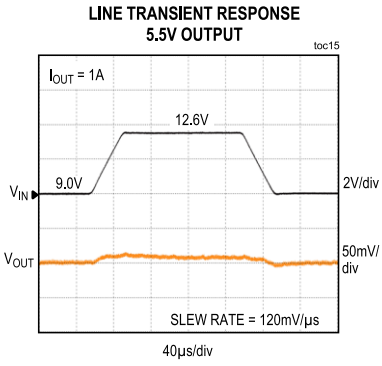

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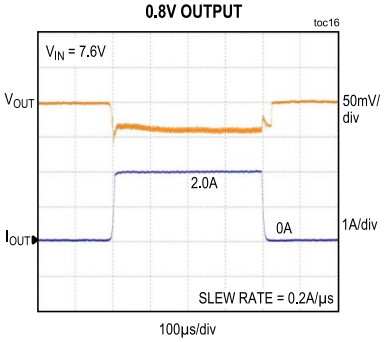

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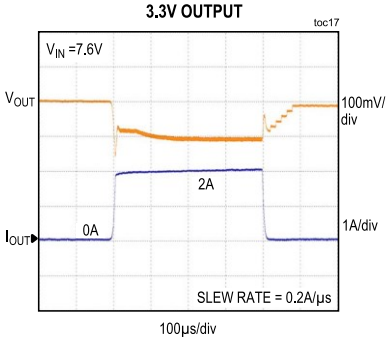

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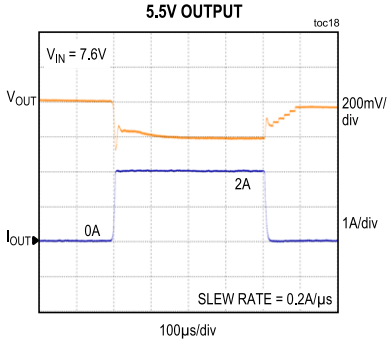

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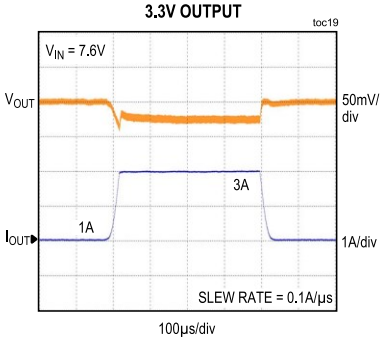
LOAD TRANSIENT RESPONSE 3.3V OUTPUT



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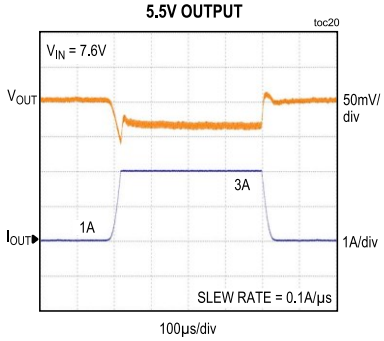
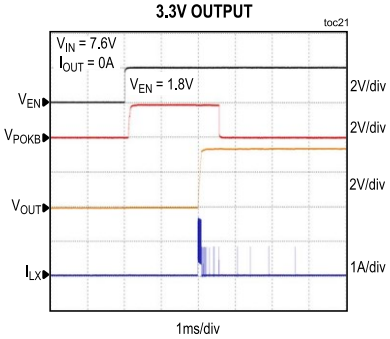
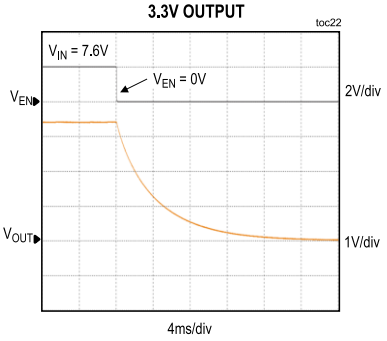


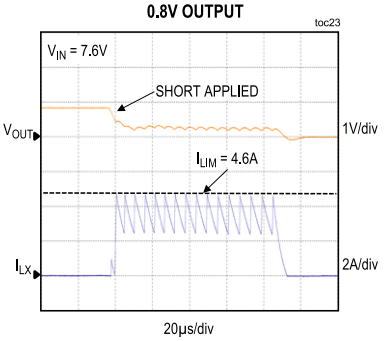
ENABLE STARTUP WAVEFORM 3.3V OUTPUT



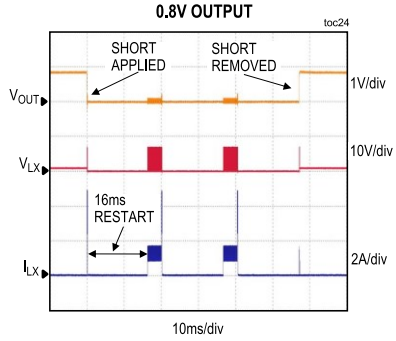
ENABLE SHUTDOWN WAVEFORM 3.3V OUTPUT



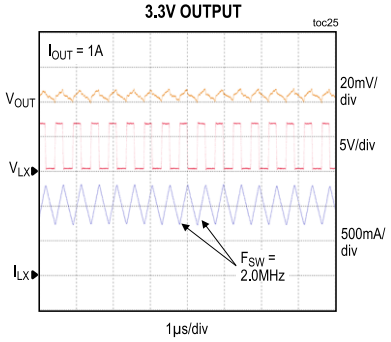
SHORT-CIRCUIT RESPONSE 0.8V OUTPUT



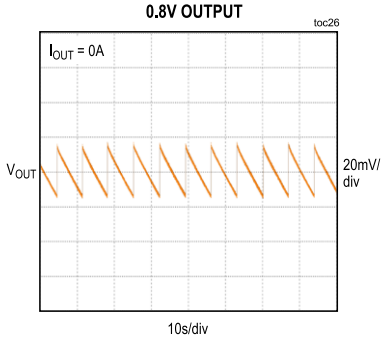
HICCUP MODE AND RECOVERY 0.8V OUTPUT



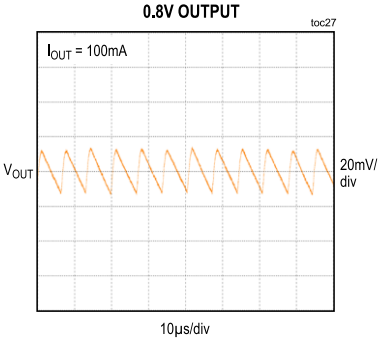
SWITCHING WAVEFORM 3.3V OUTPUT



OUTPUT RIPPLE IN SKIP MODE 0.8V OUTPUT



OUTPUT RIPPLE IN SKIP MODE 0.8V OUTPUT



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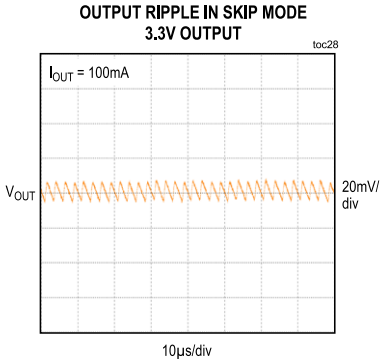
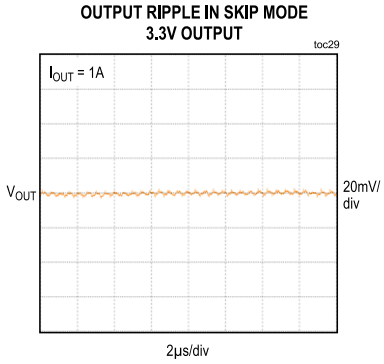
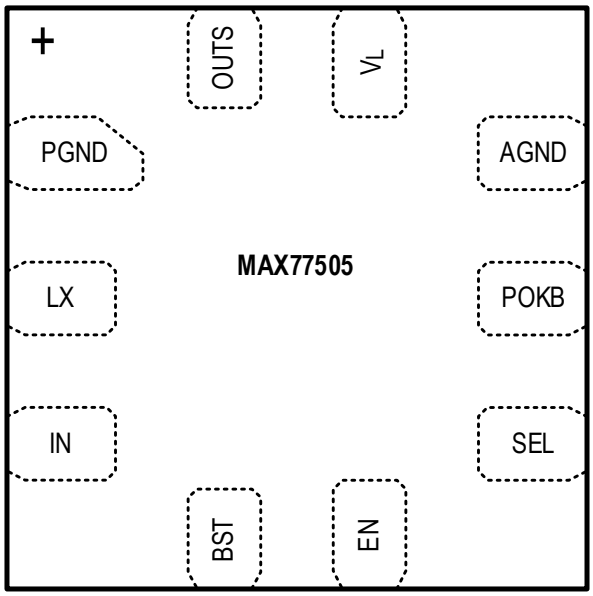




Pin Configurations

10 FC2QFN

TOP VIEW
(LEAD-SIDE DOWN)

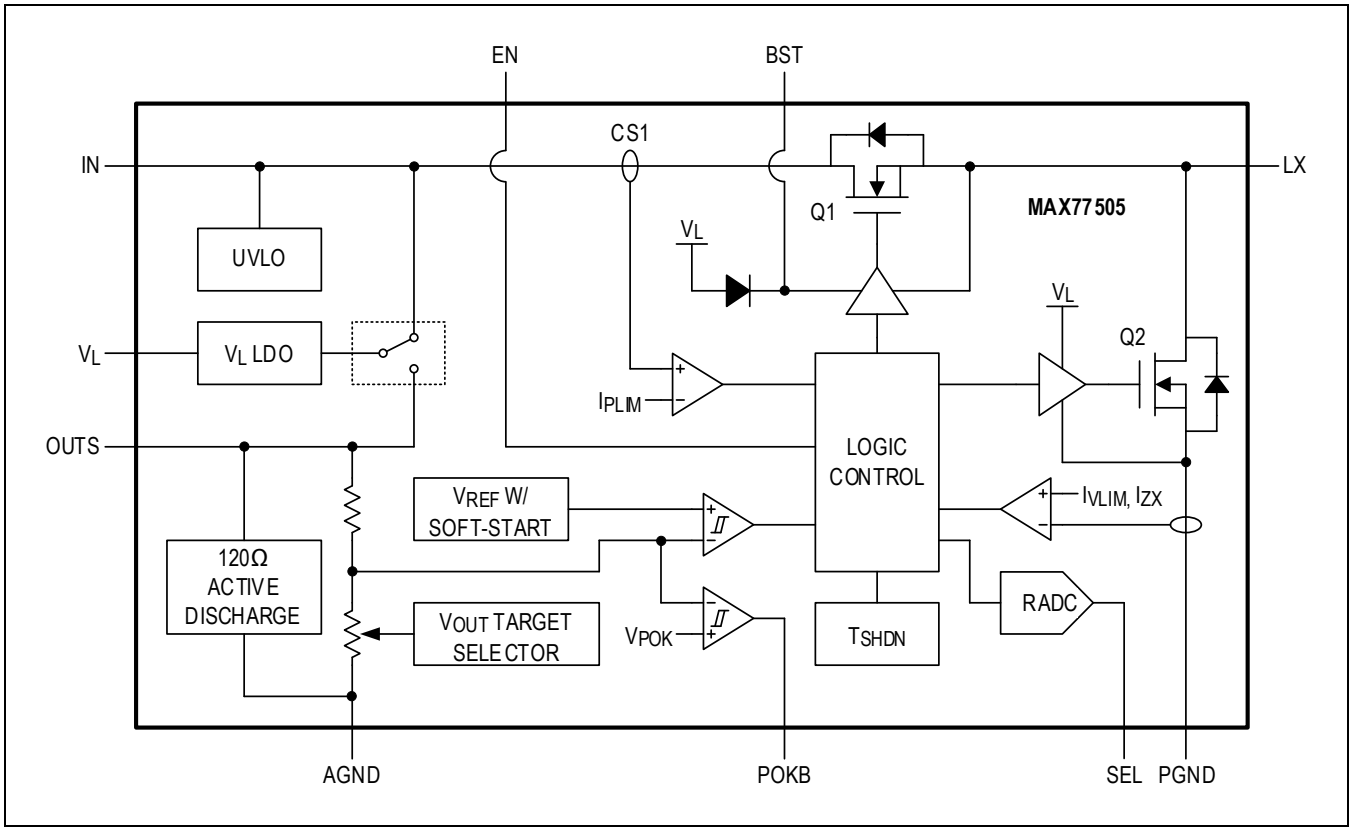


(2mm x 2mm x 0.55mm, 0.5mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION	Type
1	PGND	Power Ground	Power Ground
2	LX	Buck Converter Switch Node	Power
3	IN	Buck Converter Power Input. Bypass to PGND with a 10µF X7R ceramic capacitor.	Power Input
4	BST	Buck Converter Bootstrap Input. Connect a 0.22µF X7R ceramic capacitor between BST and LX.	Power
5	EN	Buck Converter Enable Input	Input
6	SEL	Output Voltage Selection Input. Connect a resistor between SEL and AGND to preset output voltage.	Analog
7	POKB	Inverted Power-OK Output (Open-Drain). A 10kΩ pullup resistor is required.	Digital Output
8	AGND	Analog Ground	Analog Ground
9	V_L	Internal LDO Bypass Output. Bypass to AGND with a 2.2µF X7R ceramic capacitor.	Analog
10	OUTS	Buck Output Voltage Sensing Input	Analog Input

Block Diagram



Detail Descriptions

The MAX77505 is a small, high-efficiency nanoPower step-down (buck) DC-DC converter. The step-down converter uses synchronous rectification and internal current mode compensation. The buck operates on a supply voltage between 2.5V and 16V. The output voltage is configurable through a single resistor (R_{SEL}) from the SEL pin to ground. The buck utilizes Analog Devices nanoPower Technology™ to achieve ultra-low sub-microampere quiescent current (I_Q), which maintains high efficiency at light loads.

Buck Regulator Control Scheme

The MAX77505 buck converter uses a current-control hysteretic topology. The buck converter senses the inductor current to implement a pseudo-fixed inductor ripple current, which gives approximately 2MHz switching frequency in CCM operation under typical operating conditions (V_{IN} = 7.6V, V_{OUT} = 3.3V with a 1.5µH inductor). To accommodate the pseudo-fixed inductor current ripple, the switching frequency varies over operating conditions.

In DCM operation, the buck converter turns on the high side MOSFET (Q1) until the inductor current reaches $I_{LIM}/6$. The buck converter then turns on the low side MOSFET (Q2) to deliver the energy stored in the inductor until the inductor current falls below I_{ZX} (zero crossing). When zero crossing is no longer detected due to an increased load current, the buck controller increases the peak current limit from $I_{LIM}/6$ to $I_{LIM}/3$ and repeats the process. When zero crossing is no longer detected after $I_{LIM} = I_{LIM}/3$, the part transitions into CCM. See *Figure 1* and *Table 1* for more information.

Once the sensed output voltage at the OUTS pin reaches the low-power mode over-regulation hysteresis (V_{OUT_HYS}), the buck converter goes into low-power mode by turning off control circuits whenever the inductor current zero-crossing is detected. In low-power mode, the controller wakes up every 20ms to check if the output voltage is still higher than V_{OUT_HYS}. If the output voltage hits V_{OUT_HYS} while the buck controller is awake, it initiates an LX switching. In case the output voltage drops below V_{OUT_HYS} by 10mV, the buck controller exits low-power mode immediately.

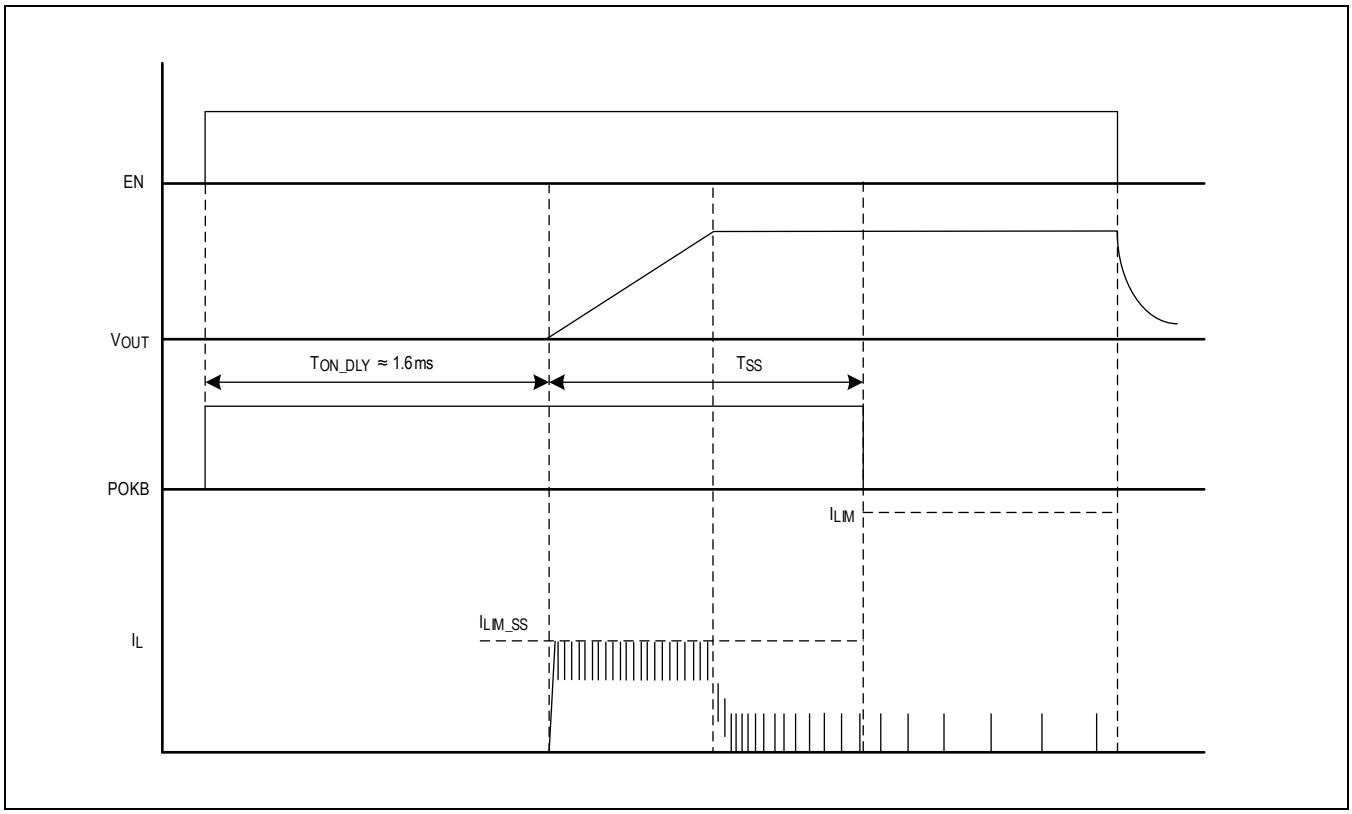


Figure 1. MAX77505 Startup Operation

Output Enable Control

The MAX77505 includes an EN pin that can be used to turn on the 16V input low quiescent current hysteretic buck converter. It can be connected to a separate supply as well as pulled up to IN. When the EN pin is pulled HIGH, the MAX77505 goes through the soft-start process to start the buck converter to the output voltage selected by the R_{SEL} which can be seen in *Table 1*. See the *Startup* section and *Output Voltage Selection* section for more details.

When the EN pin goes low, the MAX77505 stops switching immediately and turns off the output voltage active discharge circuit which is described in the *Output Voltage Active Discharge* section.

Startup

When the EN pin goes logic high, the internal reference circuit and the bias circuits start up and then the resistance value at the SEL pin is latched. With about 1.6ms of startup delay time, the MAX77505 initiates the soft-start.

The soft-start function is to prevent the MAX77505 from drawing too much current from the input source (due to an inrush current to the output capacitors) by ramping up the internal reference voltage from zero to the target value with a controlled slew rate. During startup, the MAX77505 also reduces the switch current limit to 25% of its normal value until the POKB comparator triggers.

Power Down

When the EN pin is pulled logic low threshold, the MAX77505 stops switching and turns on the output voltage discharge resistor until the output is discharged.

Output Voltage Selection with R_{SEL}

Whenever the MAX77505 is enabled, it reads the resistance (R_{SEL}) between the SEL and AGND and programs the output voltage according to *Table 1*. Ensure that R_{SEL} resistors have 1% or better tolerances.

Table 1. R_{SEL} Selection Table

R_{SEL} (Ω)	V_{OUT} (V)	R_{SEL} (Ω)	V_{OUT} (V)
≤ 95.3	3.3	3.74k	3.0
200	0.8	8.06k	3.2
309	0.9	12.4k	3.4
422	1.0	16.9k	3.6
536	1.1	21.5k	3.7
649	1.2	26.1k	3.8
768	1.3	30.9k	4.0
909	1.5	36.5k	4.2
1.05k	1.8	42.2k	4.3
1.21k	1.9	48.7k	4.5
1.40k	2.2	56.2k	5.0
1.62k	2.3	64.9k	5.2
1.87k	2.5	75.0k	5.3
2.15k	2.7	86.6k	5.5
2.49k	2.8	100k	3.1
2.87k	2.9	≥ 115k	4.8

Switch Current Limit

The MAX77505 provides a cycle-by-cycle switch current limit (I_{LIM}) at the high-side MOSFET. When the peak current limit is triggered, the MAX77505 turns off the high-side MOSFET immediately and the low-side MOSFET starts to discharge the inductor current and the high-side MOSFET stays off until the inductor current reaches 50% of the I_{LIM}. In case the MAX77505 detects peak current limit events more than 16 times consecutively, the MAX77505 enters hiccup mode and keeps both high-side and low-side MOSFETs off for about 15ms before attempting startup again.

When the zero crossing is detected at the low-side MOSFET, both the high-side and the low-side MOSFETs are turned off (Hi-Z state of LX node) until the voltage at the OUTS pin falls below its target output voltage.

Output Voltage Active Discharge

When the MAX77505 is disabled by the EN pin or the UVLO fault event, the active discharge circuit is engaged to discharge the energy stored at the output capacitor. When the active discharge circuit is activated, a 120Ω (typ) resistor is connected between the OUTS pin and AGND.

Undervoltage Lockout

When the input voltage falls below the UVLO falling threshold (V_{UVLO_F}, 2.375V, typ) during the operation, the MAX77505 disables the buck output immediately. If the EN pin is kept high, the MAX77505 automatically reinitiates the startup procedure when the input voltage rises above the UVLO rising threshold (V_{UVLO_R}, 2.450V typ).

Thermal Shutdown

When the junction temperature exceeds 150ºC (typ), the buck converter output is latched off and is not allowed to restart until the junction temperature drops below the thermal shutdown hysteresis level (130ºC, typ). Once the junction temperature cools down, either power cycling of the input voltage or toggling the EN pin is required to restart the buck converter from the latch-off state.

Applications Information

Inductor Selection

Choose an inductor with a saturation current that is greater than or equal to the maximum peak current limit setting (I_{LIM}). Inductors with lower saturation current and higher DCR ratings tend to be physically small. Higher values of DCR reduce buck efficiency. Choose the RMS current rating of the inductor (the current at which temperature rises appreciably) based on the system's expected load current.

The chosen inductor value should ensure that the peak inductor ripple current (I_{PEAK}) is below the high-side MOSFET peak current limit (I_{LIM}) so that the buck can maintain voltage regulation overload. A 1.5µH value inductor is recommended through the operation range of the device.

Input Capacitor selection

Choose the input capacitor (C_{IN}) to be a 10µF nominal capacitor that maintains 2µF effective capacitance at its working voltage. Larger values improve the decoupling of the buck converter but increase inrush current from the voltage supply when connected. C_{IN} reduces the current peaks drawn from the input power source during buck operation and filters the switching noise in the system.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the buck. Choose the effective C_{OUT} to be 20µF minimum for output voltage ranges between 0.8V to 1.5V and 10µF for output ranges above 1.5V.

Effective C_{OUT} is the actual capacitance value seen by the buck output during operation. Choose effective C_{OUT} carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information.

Larger values of C_{OUT} (above the required effective minimum) improve load transient performance but increase the input surge currents during soft-start and output voltage changes. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor’s ESR dominates the output voltage ripple in continuous conduction mode.

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, small case size capacitors derate heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet.

Bootstrap Capacitor

Sufficient bootstrap capacitance is required to ensure that the internal gate drive for the switch MOSFETs is properly biased. Select a bootstrap capacitor C_{BST} value of 0.22µF. Ensure that the voltage rating of the bootstrap capacitor is a minimum of 2V.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. *Figure 2* shows an example of a PCB top-metal layout for the device.

Follow these guidelines when designing the PCB:

- Place the input capacitors immediately next to the IN pin of the device. Since the device can operate up to 2.0MHz switching frequency, this placement is critical for the effective decoupling of high-frequency noise from the IN pin.
- Place the inductor and output capacitor close to the device and keep the loop area of the switching current small.
- Make the trace between LX and the inductor short and wide. Do not take up an excessive amount of area. The voltage on this node switches quickly and additional area creates additional radiated emissions.
- Connect AGND and PGND on the PCB. Connect them through a low-impedance inner PCB ground layer close to the IC.
- Keep the power traces and load connections short and wide. Use both top and inner PCB copper planes to reduce the trace impedance. This practice is essential for high-efficiency performance.
- Place the V_L capacitor close to the V_L pin and next to the AGND pin.

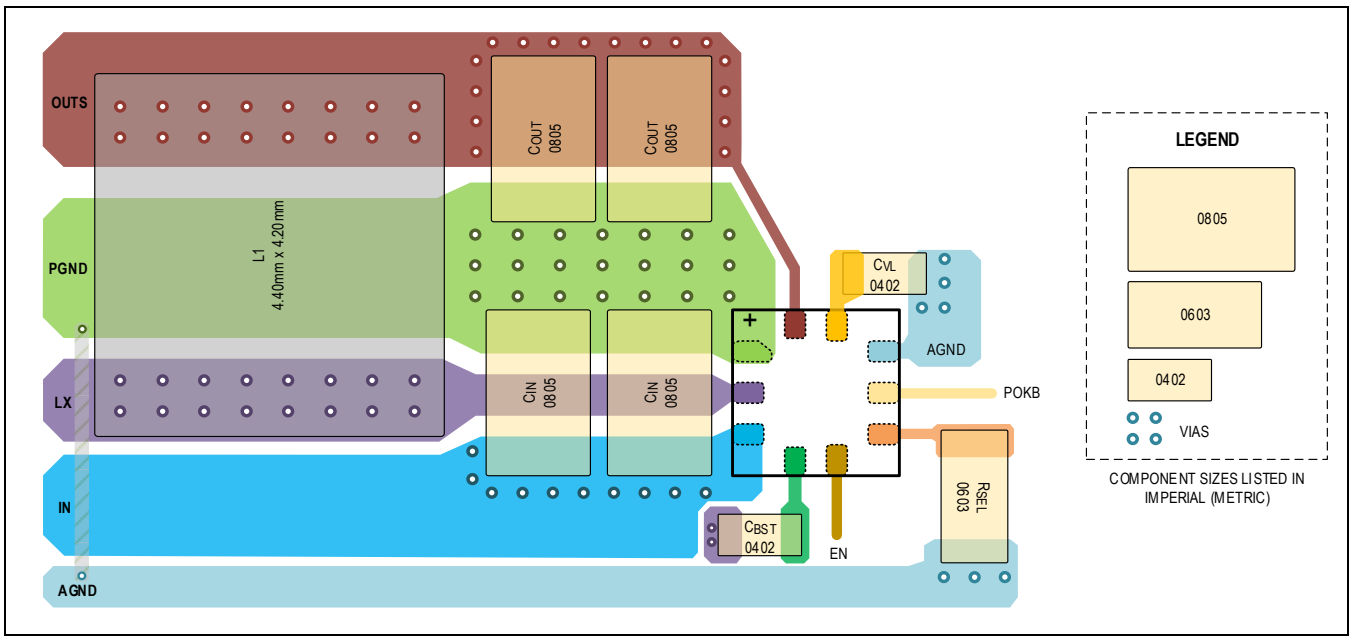
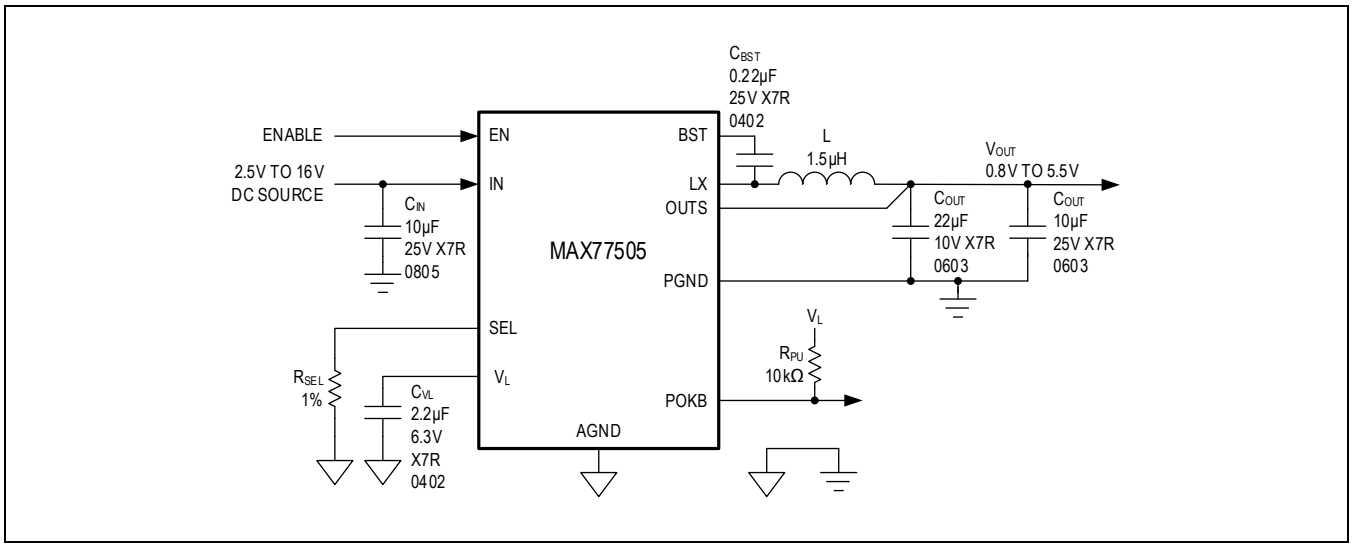


Figure 2. PCB Layout Example (FC2QFN)

Typical Application Circuit



Ordering Information

PART NUMBER	I_{LIM} (TYP)	PIN-PACKAGE
MAX77505AEFB+	4.6A	10-FC2QFN
MAX77505AEFB+T	4.6A	10-FC2QFN

+Denotes a lead(Pb)-free/ROHS-compliant package.
T = Tape and reel.
Note: *Contact Analog Devices for a list of future products.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/23	Initial release	—