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Digital Temperature Sensor and Thermal Watchdog with Bus Lockup Protection

MAX7500

General Description

The MAX7500 temperature sensor accurately measures temperature and provides an overtemperature alarm/interrupt/shutdown output. This device converts the temperature measurements to digital form using a high-resolution, sigma-delta, analog-to-digital converter (ADC). Communication is through an I²C-compatible 2-wire serial interface. The MAX7500 integrates a timeout feature that offers protection against I²C bus lockups.

The 2-wire serial interface accepts standard write byte, read byte, send byte, and receive byte commands to read the temperature data and configure the behavior of the open-drain overtemperature shutdown output.

The MAX7500 features three address select lines. The MAX7500's 3.0V to 5.5V supply voltage range, low 250µA supply current, and a lockup-protected I²C-compatible interface make it ideal for a wide range of applications, including personal computers (PCs), electronic test equipment, and office electronics.

The MAX7500 is available in an 8-pin µMAX® package and operates over the -40°C to +125°C temperature range.

Applications

- PCs
- Servers
- Office Electronics
- Electronic Test Equipment
- Industrial Process Control

Benefits and Features

- Timeout Prevents Bus Lockup
- I²C Bus Interface
- 3.0V to 5.5V Supply Voltage Range
- 250µA (typ) Operating Supply Current
- 3µA (typ) Shutdown Supply Current
- +3.5°C (max) Temperature Accuracy (-40°C to +85°C, 3-σ)
- µMAX and SO Packages Save Space
- Separate Open-Drain OS Output Operates as Interrupt or Comparator/Thermostat Input
- Register Readback Capability
- Improved LM75 Second Source
- Automotive AEC-Q100 Qualified

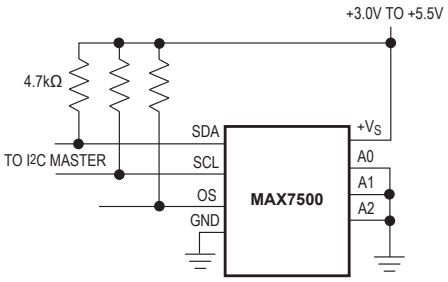
Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	TIMEOUT
MAX7500AUA/V+	-40°C to +125°C	8 µMAX	X
MAX7500ASA/V+	-40°C to +125°C	8 SO	X

+Denotes a lead(Pb)-free/RoHS-compliant package.

***Pin Configuration* appears at end of data sheet.**

Typical Application Circuit



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Analog Devices is in the process of updating documentation to provide culturally appropriate terminology and language. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.

19-100176; Rev 2; 2/24

Absolute Maximum Ratings

(Note 1)
$+V_S$ to GND.....-0.3V to +6V
OS, SDA, SCL to GND.....-0.3V to +6.0V
All Other Pins to GND.....-0.3V to ($+V_S$ + 0.3V)
Input Current at Any Pin (Note 2).....+5mA
Package Input Current (Note 2).....+20mA
ESD Protection (all pins, Human Body Model, Note 3)..±2000V
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 4.8mW/°C above +70°C).....390mW
8-Pin SO (derate 7.60mW/oC) above +70°C.....606.1mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing lead(Pb).....+240°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: When the input voltage (V_I) at any pin exceeds the power supplies ($V_I < V_{GND}$ or $V_I > + V_S$), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to 4.

Note 3: Human Body Model, 100pF discharged through a 1.5kΩ resistor.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8-pin µMAX

Package Code	U8+4
Outline Number	21-0036
Land Pattern Numer	90-0092
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	206°C/W
Junction to Ambient (θ_{JC})	42°C/W

8-pin SO

Package Code	S8+22
Outline Number	21-0041
Land Pattern Numer	90-0096
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	132°C/W
Junction to Ambient (θ_{JC})	38°C/W

For the latest package outline information and land patterns (footprints), go to Packaging Index | Analog Devices. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.

Electrical Characteristics

(+V_S = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +V_S = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy, 6-σ		-40°C ≤ T_A ≤ +85°C	-3.0		+5.0	°C
		-40°C ≤ T_A ≤ +125°C	-7.0		+5.0	
Accuracy, 3-σ (Note 5)		-40°C ≤ T_A ≤ +85°C	-1.5		+3.5	°C
		-40°C ≤ T_A ≤ +125°C	-4.5		+3.5	
Resolution				9		bits
Conversion Time		(Note 6)		100		ms
Quiescent Supply Current		I^2C inactive		0.25	0.5	mA
		Shutdown mode, +V_S = 3V		3		µA
		Shutdown mode, +V_S = 5V		5		
+V_S Supply Voltage Range			3.0		5.5	V
OS Output Saturation Voltage		I_{OUT} = 4.0mA (Note 7)			0.8	V
OS Delay		(Note 8)	1		6	Conversions
T_{OS} Default Temperature		(Note 9)		80		°C
T_{HYST} Default Temperature		(Note 9)		75		°C
LOGIC (SDA, SCL, A0, A1, A2)						
Input High Voltage	V_{IH}		+V_S x 0.7			V
Input Low Voltage	V_{IL}				+V_S x 0.3	V
Input High Current	I_{IH}	V_{IN} = 5V		0.005	1.0	µA
Input Low Current	I_{IL}	V_{IN} = 0V		0.005	1.0	µA
Input Capacitance		All digital inputs		5		pF
Output High Current		V_{IN} = 5V			1	µA
Output Low Voltage		I_{OL} = 3mA			0.4	V
I^2C-COMPATIBLE TIMING (Note 10)						
Serial Clock Frequency	f_{SCL}	Bus timeout inactive	DC		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA	100			ns
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
START Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA	100			ns
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL	100			ns
Data Hold Time	$t_{HD:DAT}$	10% of SCL to 10% of SDA (Note 11)	0		0.9	µs
Maximum Receive SCL/SDA Rise Time	t_R			300		ns
Minimum Receive SCL/SDA Rise Time	t_R	(Note 12)		20 + 0.1 x C_B		ns

Electrical Characteristics (continued)

(+V_S = +3.0V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at +V_S = +3.3V, T_A = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Receive SCL/SDA Fall Time	t_F			300		ns
Minimum Receive SCL/SDA Fall Time	t_F	(Note 12)		20 + 0.1 x C_B		ns
Transmit SDA Fall Time	t_F	(Note 12)	20 + 0.1 x C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}	(Note 13)	0		50	ns
SDA Time Low for Reset of Serial Interface	$t_{TIMEOUT}$	MAX7500 (Note 14)	150		300	ms

Note 4: All parameters are measured at +25°C. Values over the temperature range are guaranteed by design.

Note 5: There are no industry-wide standards for temperature accuracy specifications. These values allow comparison to vendors who use 3-σ limits.

Note 6: This specification indicates how often temperature data is updated. The devices can be read at any time without regard to conversion state, while yielding the last conversion result.

Note 7: For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy due to internal heating.

Note 8: OS delay is user programmable up to six “over-limit” conversions before OS is set to minimize false tripping in noisy environments.

Note 9: Default values set at power-up.

Note 10: All timing specifications are guaranteed by design.

Note 11: A master device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL’s falling edge.

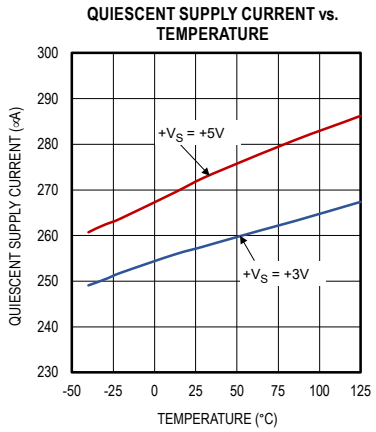
Note 12: C_B = total capacitance of one bus line in pF. Tested with C_B = 400pF.

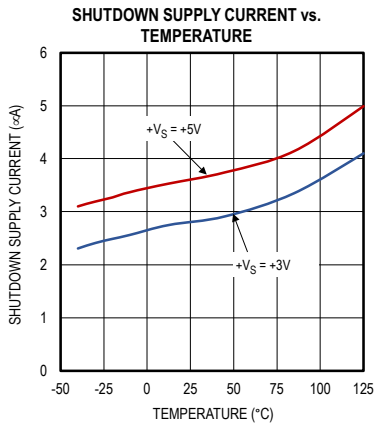
Note 13: Input filters on SDA, SCL, and A_ suppress noise spikes less than 50ns.

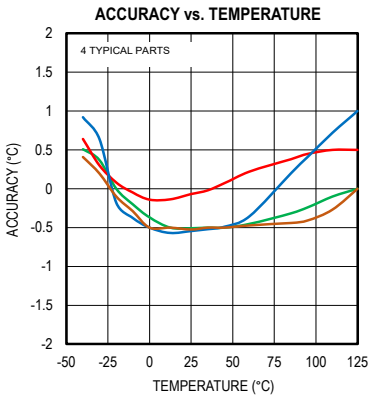
Note 14: Holding the SDA line low for a time greater than $t_{TIMEOUT}$ causes the devices to reset SDA to the IDLE state of the serial bus communication (SDA set high).

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)







Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial Data Input/Output Line. Open-drain. Connect SDA to a pullup resistor.
2	SCL	Serial Data Clock Input. Open drain. Connect SCL to a pullup resistor.
3	OS	Overtemperature Shutdown Output. Open drain. Connect OS to a pullup resistor.
4	GND	Ground
5	A2	2-Wire Interface Address Input. Connect A2 to GND or $+V_S$ to set the desired I²C bus address. Do not leave unconnected (see Table 1).
6	A1	2-Wire Interface Address Input. Connect A1 to GND or $+V_S$ to set the desired I²C bus address. Do not leave unconnected (see Table 1).
7	A0	2-Wire Interface Address Input. Connect A0 to GND or $+V_S$ to set the desired I²C bus address. Do not leave unconnected (see Table 1).
8	$+V_S$	Positive Supply Voltage Input. Bypass to GND with a 0.1µF bypass capacitor.

Detailed Description

The MAX7500 temperature sensor measures temperature, converts the data into digital form using a sigma-delta ADC, and communicates the conversion results through an I²C-compatible 2-wire serial interface. The device accepts standard I²C commands to read the data, sets the overtemperature alarm (OS) trip thresholds, and configures other characteristics. The MAX7500 features three address select lines (A0, A1, A2). The MAX7500 operates from a +3.0V to +5.5V supply voltage and consumes 250µA of supply current.

I²C-Compatible Bus Interface

From a software perspective, the MAX7500 appears as a set of byte-wide registers that contain temperature data, alarm threshold values, and control bits. A standard I²C-compatible 2-wire serial interface reads temperature data and writes control bits and alarm threshold data. Each device responds to its own I²C slave address, which is selected using A0, A1, and A2. See Table 1.

The MAX7500 employs four standard I²C protocols: write byte, read byte, send byte, and receive byte (Figure 1, Figure 2, and Figure 3). The shorter receive byte protocol

Table 1. I²C Slave Addresses

DEVICE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MAX7500	1	0	0	1	A2	A1	A0	RD/$\overline{W}$

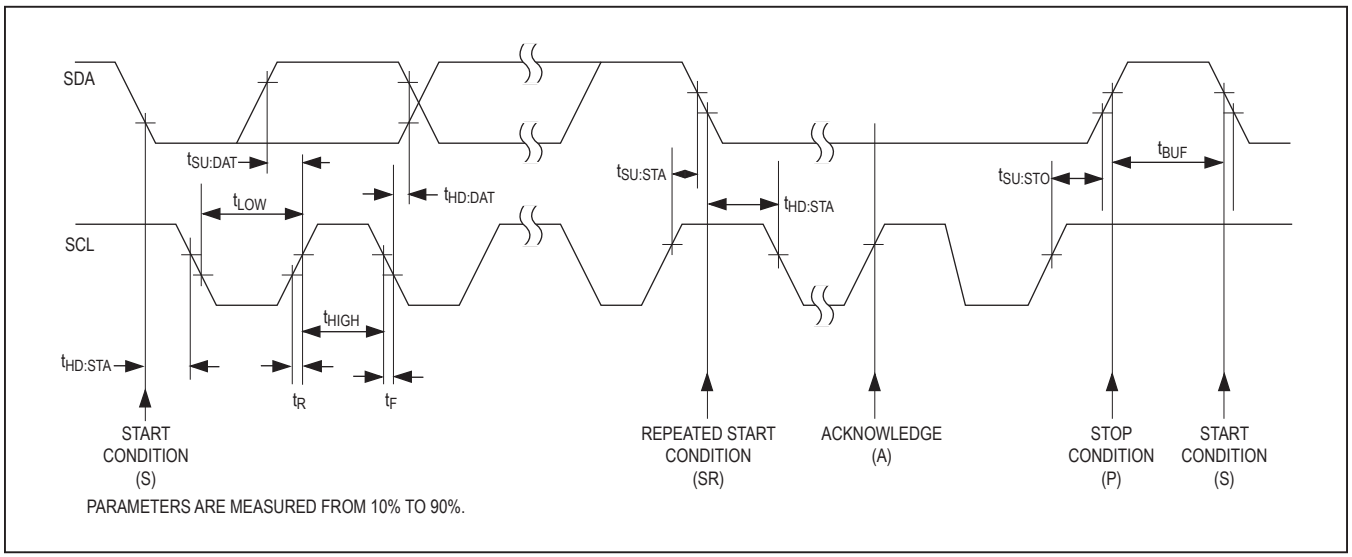


Figure 1. Serial Bus Timing

allows quicker transfers, provided that the correct data register was previously selected by a read-byte instruction. Use caution when using the shorter protocols in multi-master systems, as a second master could overwrite the command byte without informing the first master. The MAX7500 has eight different slave addresses available; therefore, a maximum of eight MAX7500 devices can share the same bus.

Register Descriptions

The MAX7500 has an internal pnp-junctionbased temperature sensor whose analog output is converted to digital form using a 9-bit sigma-delta ADC. The measured temperature and temperature configurations are controlled by the temperature, configuration, T_{HYST}, and T_{OS} registers. See Table 2.

Temperature Register

Read the measured temperature through the temperature register. The temperature data format is 9 bits, two's complement, and the register is read out in 2 bytes: an upper byte and a lower byte. Bit D15 is the sign bit. When bit D15 is 1, the temperature reading is negative. When bit D15 is zero, the temperature reading is positive. Bits D14–D7 contain the temperature data, with the LSB representing 0.5°C and the MSB representing 64°C (see Table 3). The MSB is transmitted first. The last 7 bits of the lower byte, bits D6–D0, are don't cares. When reading the temperature register, bits D6–D0 must be ignored. When the measured temperature is greater than +127.5°C, the value stored in the temperature register is clipped to 7F8h. When the measured temperature is below -64°C, the value in the temperature register is clipped to BF8h.

During the time of reading the temperature register, any changes in temperature are ignored until the read is completed. The temperature register is updated upon completion of the next conversion.

Table 3 lists the temperature register definition.

Configuration Register

The 8-bit configuration register sets the fault queue, OS polarity, shutdown control, and whether the OS output functions in comparator or interrupt mode. When writing to the configuration register, set bits D7, D6, and D5 to zero. See Table 5.

Bits D4 and D3, the fault queue bits, determine the number of faults necessary to trigger an OS condition. See Table 6. The number of faults set in the queue must occur to trip the OS output. The fault queue prevents OS false tripping in noisy environments.

Set bit D2, the OS polarity bit, to zero to force the OS output active low. Set bit D2 to 1 to set the OS output polarity to active high. OS is an open-drain output under all conditions and requires a pullup resistor to output a high voltage. See Figure 4.

Set bit D1, the comparator/interrupt bit to zero to run the overtemperature shutdown block in comparator mode. In comparator mode, OS is asserted when the temperature rises above the T_{OS} value. OS is deasserted when the temperature drops below the T_{HYST} value.

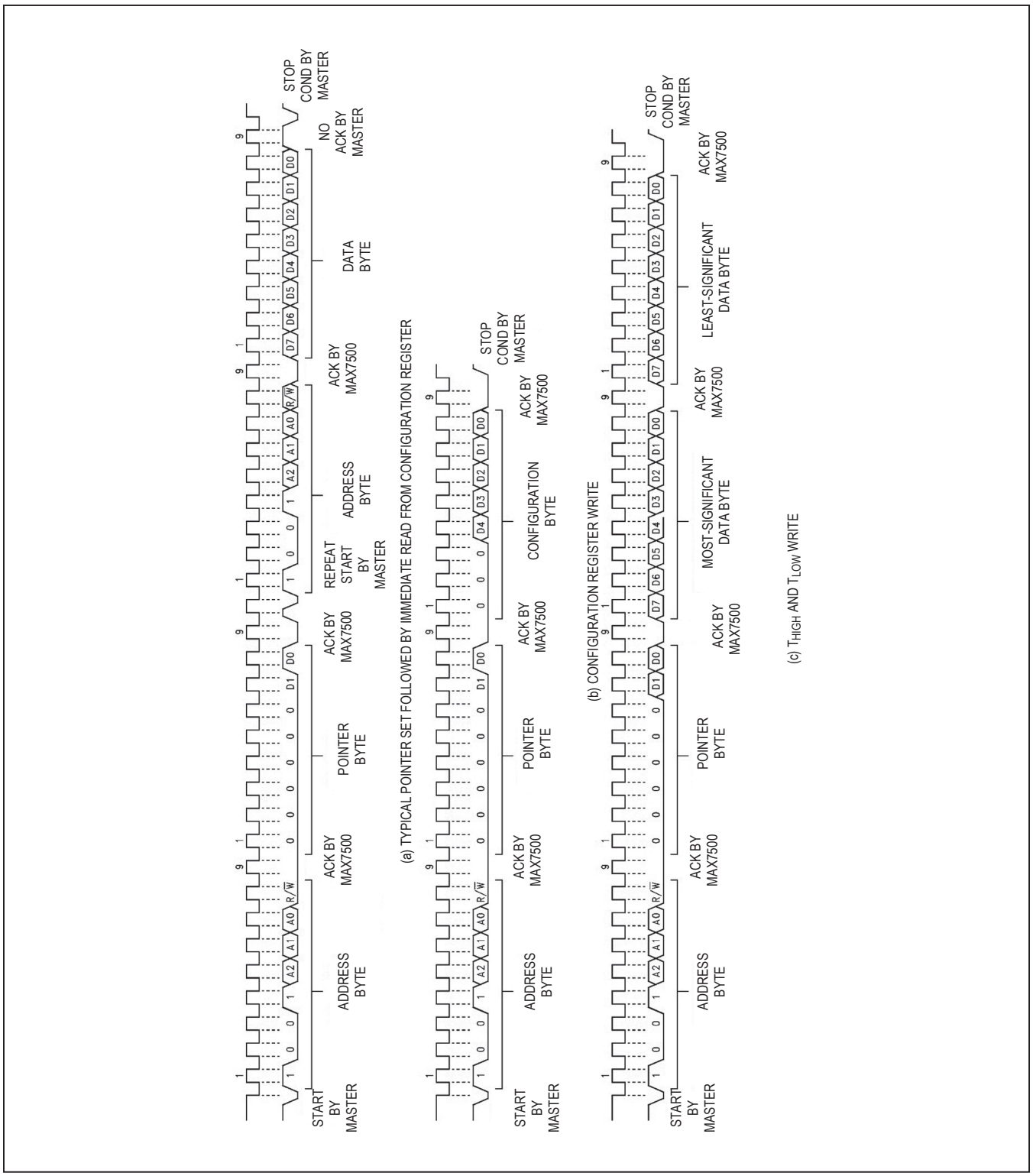


Figure 2. I²C-Compatible Timing Diagram (Write)

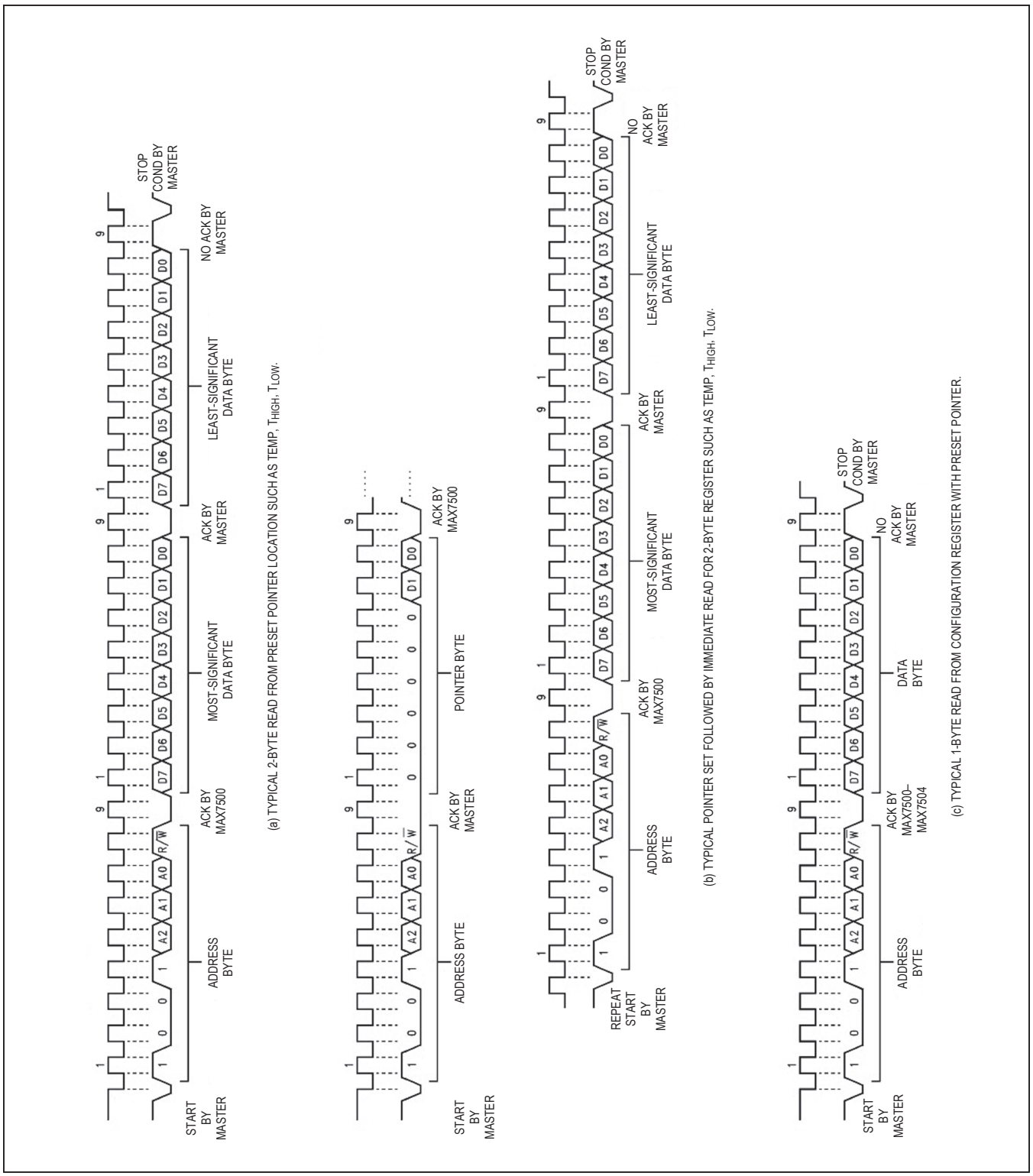


Figure 3. I²C-Compatible Timing Diagram (Read)

Table 2. Register Functions

REGISTER NAME	ADDRESS (HEX)	POR STATE (HEX)	POR STATE (BINARY)	POR STATE (°C)	READ/ WRITE
Temperature	00	—	—	—	Read only
Configuration	01	00	0000 0000	—	R/$\overline{W}$
T_{HYST}	02	4B0	0100 1011 0	75	R/$\overline{W}$
T_{OS}	03	500	0101 0000 0	80	R/$\overline{W}$

Table 3. Temperature Register Definition

UPPER BYTE									LOWER BYTE						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign bit 1= Negative 0 = Positive	MSB 64°C	32°C	16°C	8°C	4°C	2°C	1°C	LSB 0.5°C	X	X	X	X	X	X	X

X = Don't care.

See Figure 4. Set bit D1 to 1 to run the overtemperature shutdown block in interrupt mode. OS is asserted in interrupt mode when the temperature rises above the T_{OS} value or falls below the T_{HYST} value. OS is deasserted only after performing a read operation.

Set bit D0, the shutdown bit, to zero for normal operation. Set bit D0 to 1 to shut down the MAX7500 internal blocks, dropping the supply current to 3µA. The I^2C interface remains active as long as the shutdown bit is set. The T_{OS}, T_{HYST}, and configuration registers can still be written to and read from while in shutdown.

T_{OS} and T_{HYST} Registers

In comparator mode, the OS output behaves like a thermostat. The output asserts when the temperature rises above the limit set in the T_{OS} register. The output de-asserts when the temperature falls below the limit set in the T_{HYST} register. In comparator mode, the OS output can be used to turn on a cooling fan, initiate an emergency shutdown signal, or reduce system clock speed.

Table 4. Temperature Data Output

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	hex
+125	0111 1101 0xxx xxxx	7D0x
+25	0001 1001 0xxx xxxx	190x
+0.5	0000 0000 1xxx xxxx	008x
0	0000 0000 0xxx xxxx	000x
-0.5	1111 1111 1xxx xxxx	FF8x
-25	1110 0111 0xxx xxxx	E70x

In interrupt mode, exceeding T_{OS} also asserts OS. OS remains asserted until a read operation is performed on any of the registers. Once OS has asserted due to crossing above T_{OS} and is then reset, it is asserted again only when the temperature drops below T_{HYST}. The output remains asserted until it is reset by a read. Putting the MAX7500 into shutdown mode also resets OS.

The T_{OS} and T_{HYST} registers are accessed with 2 bytes, with bits D15–D7 containing the data. Bits D6–D0 are don't cares when writing to these two registers and read-back zeros when reading from these registers. The LSB represents 0.5°C while the MSB represents 64°C. See Table 7.

Shutdown

Set bit D0 in the configuration register to 1 to place the MAX7500 in shutdown mode and reduce supply current to 3µA.

Power-Up and Power-Down

The MAX7500 powers up to a known state, as indicated in Table 2. Some of these settings are summarized below:

- Comparator mode
- T_{OS} = +80°C
- T_{HYST} = +75°C
- OS active low
- Pointer = 00

Table 5. Configuration Register Definition

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault queue	Fault queue	OS polarity	Comparator/ interrupt	Shutdown

Table 6. Configuration Register Fault Queue Bits

D4	D3	NO. OF FAULTS
0	0	1 (POR state)
0	1	2
1	0	4
1	1	6

Internal Registers

The MAX7500's pointer register selects between four data registers. See Figure 5. At power-up, the pointer is set to read the temperature register at address 00. The pointer register latches the last location to which it was set. All registers are read and write, except the temperature register, which is read only.

Write to the configuration register by writing an address byte, a data pointer byte, and a data byte. If 2 data bytes are written, the second data byte overrides the first. If more than 2 data bytes are written, only the first 2 bytes are recognized while the remaining bytes are ignored. The T_{OS} and T_{HYST} registers require 1 address byte and 1 pointer byte and 2 data bytes. If only 1 data byte is written, it is saved in bits D15–D8 of the respective register. If more than 2 data bytes are written, only the first 2 bytes are recognized while the remaining bytes are ignored.

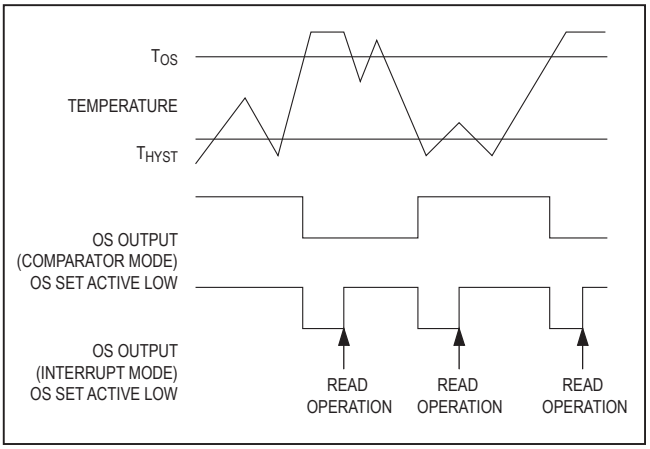


Figure 4. OS Timing Diagram

Read from the MAX7500 in one of two ways. If the location latched in the pointer register is set from the previous read, the new read consists of an address byte, followed by retrieving the corresponding number of data bytes. If the pointer register needs to be set to a new address, perform a read operation by writing an address byte, pointer byte, repeat start, and another address byte.

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the MAX7500 to stop in a state where the SDA line is held low. Ordinarily, this would prevent any further bus communication until the master sends nine additional clock cycles or SDA goes high. At

Table 7. T_{OS} and T_{HYST} Register Definitions

COMMAND	UPPER BYTE								LOWER BYTE							
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Write	Sign bit 1 = negative 0 = positive	MSB 64°C	32°C	16°C	8°C	4°C	2°C	1°C	LSB 0.5°C	X	X	X	X	X	X	X
Read	Sign bit 1 = negative 0 = positive	MSB 64°C	32°C	16°C	8°C	4°C	2°C	1°C	LSB 0.5°C	0	0	0	0	0	0	0

X = Don't care.

that time, a stop condition resets the device. With the MAX7500, if the additional clock cycles are not generated by the master, the bus resets and unlocks after the bus timeout period has elapsed.

Bus Timeout

Communication errors sometimes occur due to noise pickup on the bus. In the worst case, such errors can cause the slave device to hold the data line low, thereby preventing other devices from communicating over the bus. The MAX7500's internal bus timeout circuit resets the bus and releases the data line if the line is low for more than 250ms. When the bus timeout is active, the minimum serial clock frequency is limited to 6Hz.

Applications Information

Digital Noise

The MAX7500 features an integrated low-pass filter on both the SCL and the SDA digital lines to mitigate the effects of bus noise. Although this filtering makes communication robust in noisy environments, good layout practices are always recommended. Minimize noise coupling by keeping digital traces away from switching power supplies. Ensure that digital lines containing high-speed data communications cross at right angles to the SDA and SCL lines.

Excessive noise coupling into the SDA and SCL lines on the MAX7500—specifically noise with amplitude greater than $400mV_{P-P}$ (the typical hysteresis), overshoot greater than 300mV above $+V_S$, and undershoot more than 300mV below GND—may prevent successful serial communication. Serial bus no-acknowledge is the most common symptom, causing unnecessary traffic on the bus.

Care must be taken to ensure proper termination within a system with long PCB traces or multiple parts on the bus. Resistance can be added in series with the SDA and SCL lines to further help filter noise and ringing. If it proves to be necessary, a 5kΩ resistor should be placed in series with the SCL line, placed as close as possible to SCL. This 5kΩ resistor, with the 5pF to 10pF stray capacitance of the MAX7500 provides a 6MHz to 12MHz lowpass filter, which is sufficient filtering in most cases.

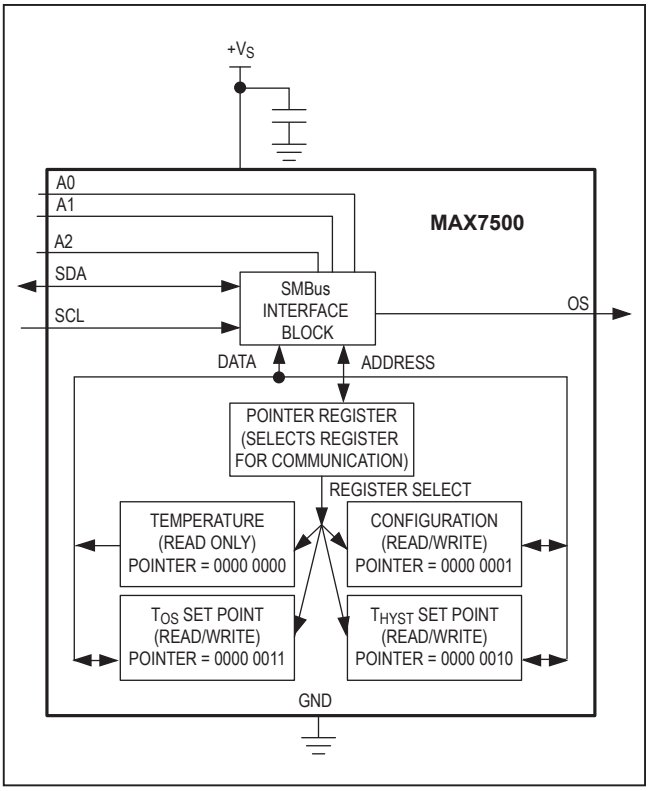
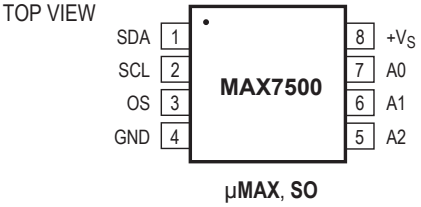


Figure 5. Block Diagram

Pin Configuration



µMAX, SO

Chip Information

PROCESS: CMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/17	Initial release	—
1	1/18	Updated *Benefits and Features*, *Absolute Maximum Ratings*, and *Package Information* sections	1, 2, 11
2	2/24	Updated *Package Information* Table and Disclaimer has been added on Page 1	1, 2