2.5A Battery Backup Power Manager

FEATURES

- **Step-Up Backup Supply and Step-Down Battery Charger**
- **6.5A Switches for 2.5A Backup from 3.2V Battery**
- **Input Current Limit Prioritizes Load Over Charge Current**
- **Input Disconnect Switch Isolates Input During Backup**
- **Automatic Seamless Switch-Over to Backup Mode**
- Input Power Loss Indicator
- System Power Loss Indicator
- Pin Selectable Battery: Li-Ion (3.95V/4.0V/4.05V/4.1V) or $LiFePO_4$ (3.45V/3.5V/3.55V/3.6V)
- Optional OVP Circuitry Protects Device to >60V
- Constant Frequency Operation
- Low Profile (0.75mm) 24-Lead 4mm × 5mm QFN Package

APPLICATIONS

- Fleet and Asset Tracking
- Automotive GPS Data Loggers
- Automotive Telematics Systems
- Toll Collection Systems
- Security Systems
- USB Powered Devices

DESCRIPTION

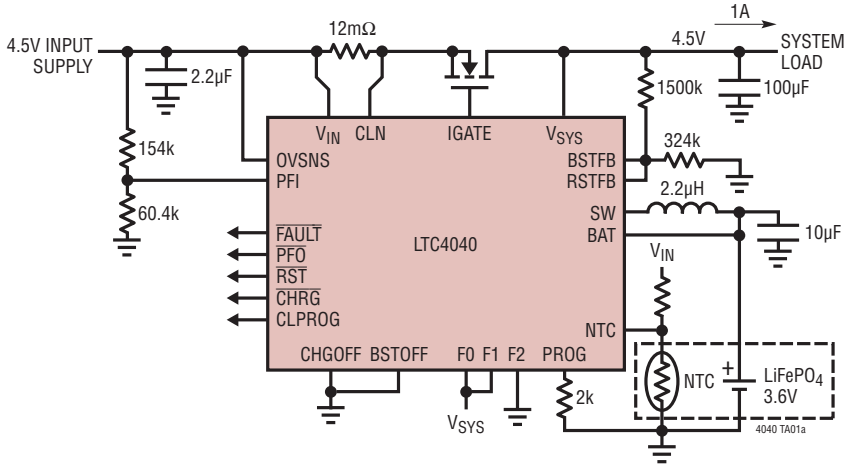
The LTC®4040 is a complete 3.5V to 5.5V supply rail battery backup system. It contains a high current step-up DC/DC regulator to back up the supply from a single-cell Li-Ion or $LiFePO_4$ battery. When external power is available, the step-up regulator operates in reverse as a step-down battery charger.

The LTC4040's adjustable input current limit function reduces charge current to protect the main supply from overload while an external disconnect switch isolates the external supply during backup. When the input supply drops below the adjustable PFI threshold, the 2.5A boost regulator delivers power from the battery to the system output.

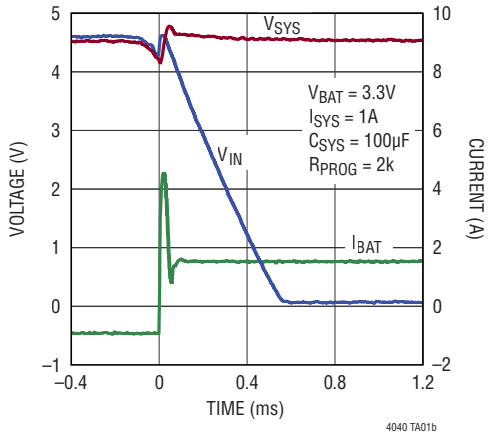
An optional input overvoltage protection (OVP) circuit protects the LTC4040 from high voltage damage at the V_{IN} pin. One logic input selects either the Li-Ion or the $LiFePO_4$ battery option, and two other logic inputs program the battery charge voltage to one of four levels suitable for backup applications. The LTC4040 is available in a low profile (0.75mm) 24-Lead 4mm × 5mm QFN package.

TYPICAL APPLICATION

4.5V Backup Application with 4.22V PFI Threshold (Charge Current Setting: 1A, Input Current Limit Setting: 2A)



Normal to Backup Mode Transition Waveform

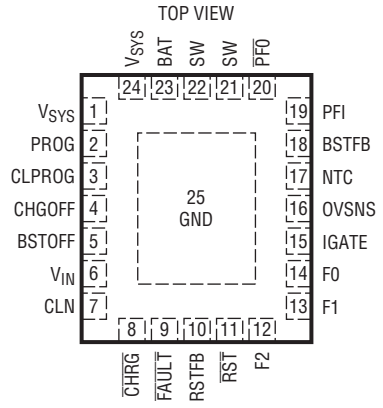


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN} (Transient) t < 1ms, Duty Cycle < 1% ....–0.3V to 7V
V_{IN} (Steady State), BAT, CLN, V_{SYS}, BSTFB, NTC, OVSNS, $\overline{CHRG}$, $\overline{PFO}$, $\overline{RST}$, $\overline{FAULT}$ .....–0.3V to 6V
F0, F1, F2, BSTOFF, RSTFB, PFI, CHGOFF .....–0.3V to Max (V_{IN}, V_{BAT}, V_{SYS}) + 0.3V
I_{OVSNS} ..... ±10mA
$I_{\overline{CHRG}}$, $I_{\overline{PFO}}$, $I_{\overline{RST}}$, $I_{\overline{FAULT}}$ 10mA
I_{PROG}, I_{CLPROG}..... 1.1mA
Operating Junction Temperature Range (Note 3).....–40 to 125°C
Storage Temperature Range .....–65 to 125°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC4040#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4040EUFD#PBF	LTC4040EUFD#TRPBF	4040	24-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C to 125°C
LTC4040IUFD#PBF	LTC4040IUFD#TRPBF	4040	24-Lead (4mm × 5mm × 0.75mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = 5V, V_{BAT} = 3.6V, R_{PROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	3.5		5.5	V
V_{BAT}	Battery Voltage Range (Backup Boost Input)			2.7		5	V
I_{INQ}	V_{IN} Quiescent Current	Normal Mode (V_{PFI} = 2V), Battery Charger Timed Out Shutdown (BSTOFF = CHGOFF=1)			570 3.5	 7	µA µA
I_{BATQ}	BAT Quiescent Current	Normal Mode (V_{PFI} = 2V), Battery Charger Timed Out Backup Mode (V_{IN} = V_{PFI} = 0V), No System Load Shutdown (BSTOFF = CHGOFF = 1)	 ● 		45 40 1.5	 70 3	µA µA µA
Battery Charger							
V_{CHG}	BAT Regulated Output Voltage for $LiFePO_4$ Option (F2 = 0)	F2 = 0, F1 = 0, F0 = 0 F2 = 0, F1 = 0, F0 = 1 F2 = 0, F1 = 1, F0 = 0 F2 = 0, F1 = 1, F0 = 1	● ● ● ●	3.42 3.47 3.52 3.57	3.45 3.50 3.55 3.60	3.48 3.53 3.58 3.63	V V V V
	BAT Regulated Output Voltage for Li-Ion Option (F2 = 1)	F2 = 1, F1 = 0, F0 = 0 F2 = 1, F1 = 0, F0 = 1 F2 = 1, F1 = 1, F0 = 0 F2 = 1, F1 = 1, F0 = 1	● ● ● ●	3.92 3.97 4.02 4.07	3.95 4.00 4.05 4.10	3.98 4.03 4.08 4.13	V V V V
I_{CHG}	Regulated Battery Charge Current	R_{PROG} = 2k		950	1000	1050	mA
	V_{SYS}-to-V_{BAT} Differential Undervoltage Lockout Threshold (Falling)			40	50	60	mV
	V_{SYS}-to-BAT Differential Undervoltage Lockout Threshold (Rising)			125	145	165	mV
V_{PROG}	PROG Pin Servo Voltage				800		mV
h_{PROG}	Ratio of Battery Current to PROG Pin Current				2500		mA/mA
I_{TRKL}	Trickle Charge Current	V_{BAT} = 2.5V, R_{PROG} = 2k			125		mA
	PROG Pin Servo Voltage at Trickle Charge	V_{BAT} = 2.5V, R_{PROG} = 2k			100		mV
	Input Current Limit Threshold Voltage	$V_{IN} - V_{CLN}$	●	23.5	25	26.5	mV
A_{CLPROG}	Input Current Limit Amplifier Gain	Ratio of CLPROG Voltage to ($V_{IN} - V_{CLN}$)			32		V/V
	CLN Input Bias Current	V_{CLN} = V_{IN}				300	nA
V_{RECHG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{CHG} if F2 = 0 and F1 = 1 Threshold Voltage Relative to V_{CHG} All Other Cases		94.2 96.7	95 97.5	95.8 98.3	% %
$t_{TERMINATE}$	Safety Timer Termination Period	Timer Starts When V_{BAT} = V_{CHG} F2 = 1 (Li-Ion) F2 = 0 ($LiFePO_4$)		 3.7 1.85	 4.25 2.13	 5 2.5	 Hours Hours
V_{LOWBAT}	Low Battery Threshold Voltage for Trickle Charge	V_{BAT} Rising		2.75	2.85	2.95	V
ΔV_{LOWBAT}	Low Battery Hysteresis				150		mV
t_{BADBAT}	Bad-Battery Termination Time	$V_{BAT} < (V_{LOWBAT} - \Delta V_{LOWBAT})$		0.47	0.54	0.64	Hours
$V_{C/8}$	End-of-Charge Indication	PROG Pin Average Voltage		90	100	110	mV
$f_{OSC(BUCK)}$	Step-Down (Buck) Converter Switching Frequency	Normal Mode (V_{PFI} > 1.21V)		1.96	2.25	2.65	MHz
$R_{P(BUCK)}$	High Side Switch On-Resistance	Normal Mode (V_{PFI} > 1.21V)			130		mΩ
$R_{N(BUCK)}$	Low Side Switch On-Resistance	Normal Mode (V_{PFI} > 1.21V)			120		mΩ
$I_{LIM(BUCK)}$	PMOS Switch Current Limit			3	4.3		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = 5V, V_{BAT} = 3.6V, R_{PROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Voltage Threshold Hysteresis		75.0	76.5 1.5	78	$\%V_{IN}$ $\%V_{IN}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Voltage Threshold Hysteresis		33.4	34.9 1.73	36.4	$\%V_{IN}$ $\%V_{IN}$
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.7	1.7 50	2.7	$\%V_{IN}$ mV
I_{NTC}	NTC Leakage Current			–20		20	nA
Backup Mode Boost Switching Regulator							
V_{BSTFB}	BSTFB Reference Voltage		●	0.78	0.8	0.82	V
I_{BSTFB}	BSTFB Input Bias Current			–20		20	nA
V_{SYS}	Step-up (Boost) Converter Output Voltage Range			3.5		5	V
f_{OSCBST}	Step-Up Converter Switching Frequency	Backup Mode (V_{PFI} < 1.17V)		0.98	1.125	1.33	MHz
I_{LIMBST}	NMOS Switch Current Limit			5.5	6.5	7.5	A
R_{PBST}	Boost High Side Switch On-Resistance				75		mΩ
R_{NBST}	Boost Low Side Switch On-Resistance				70		mΩ
V_{OVSD}	V_{SYS} Overvoltage Shutdown Threshold	V_{SYS} Rising		5.3	5.5	5.7	V
	Overvoltage Shutdown Hysteresis				100		mV
V_{UVLO}	BAT Pin Undervoltage Lockout	V_{BAT} Falling			2.45	2.6	V
	BAT Pin Undervoltage Lockout Hysteresis				150		mV
D_{MAX}	Maximum Boost Duty Cycle				88	93	%
	NMOS Switch Leakage	BSTOFF = 1, CHGOFF = 1			1		µA
	PMOS Switch Leakage	BSTOFF = 1, CHGOFF = 1			1		µA
Reset Comparator							
	RSTFB Threshold (Falling)		●	0.72	0.74	0.76	V
	RSTFB Hysteresis				20		mV
	RSTFB Pin Leakage Current	V_{RSTFB} = 0.9V		–50		50	nA
	$\overline{RST}$ Delay (RSTFB Rising)				232		ms
Power-Fail Comparator							
	PFI Input Threshold (Falling Edge)	Initiates Backup Mode	●	1.17	1.19	1.21	V
	PFI Input Hysteresis				30		mV
	PFI Pin Leakage Current	V_{PFI} = 1.3V		–100		100	nA
	PFI Delay to $\overline{PFO}$	PFI Falling			0.5		µs
	$\overline{PFO}$ Pin Leakage Current	$V_{\overline{PFO}}$ = 5V			10		µA
	$\overline{PFO}$ Pin Output Low Voltage	$I_{\overline{PFO}}$ = 5mA			65		mV
Logic Input (CHGOFF, BSTOFF, F0, F1, F2)							
V_{IL}	Logic Low Input Voltage		●			0.4	V
V_{IH}	Logic High Input Voltage		●	1.2			V
I_{IL}	Logic Low Input Leakage			–1		1	µA
I_{IH}	Logic High Input Leakage			–1		1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 3) V_{IN} = 5V, V_{BAT} = 3.6V, R_{PROG} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Open-Drain Output ($\overline{CHRG}$, $\overline{RST}$, $\overline{FAULT}$)							
	Pin Leakage Current	V = 5V				1	µA
	Pin Output Low Voltage	I = 5mA			65		mV
Overvoltage Protection							
$V_{OV(CUTOFF)}$	Overvoltage Protection Threshold	Rising Threshold, R_{OVSNS} = 6.2k		6.1	6.4	6.7	V
V_{OVGT}	IGATE Output Voltage Active	Input Voltage < $V_{OV(CUTOFF)}$			1.88 • V_{OVSNS}	12	V
$V_{OVGT(LOAD)}$	IGATE Voltage Under Load	5V Through 6.2k Into OVSNS, I_{IGATE} = 1µA		8	8.6		V
I_{OVSNSQ}	OVSNS Quiescent Current	V_{OVSNS} = 5V			40		µA
	OVSNS Quiescent Current at Shutdown	BSTOFF = H, CHGOFF = H			25		µA
	IGATE Time to Reach Regulation	C_{IGATE} = 2.2nF			3.5		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTC4040E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4040E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process control. The LTC4040I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

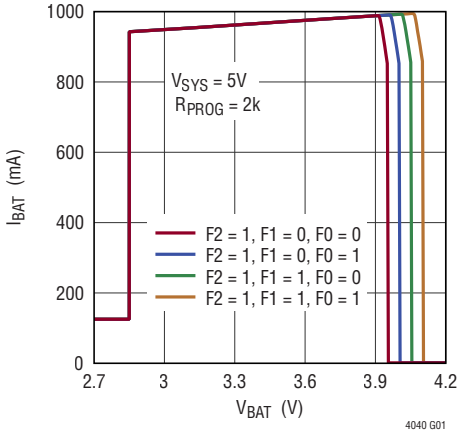
$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where the package thermal impedance θ_{JA} = 43°C/W.

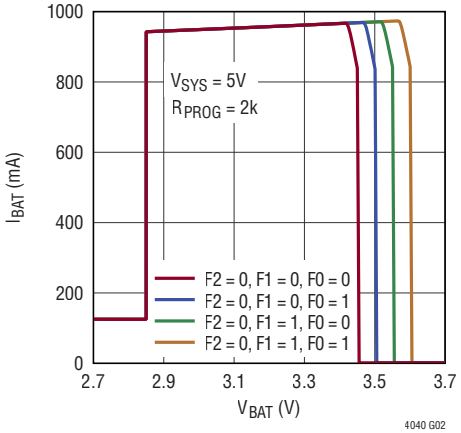
Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

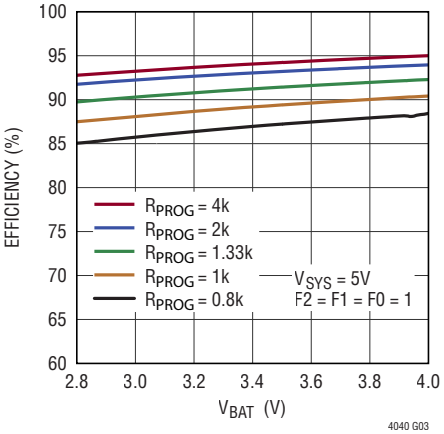
I_{BAT} vs V_{BAT} (Li-Ion) with Different Charge Voltage Settings



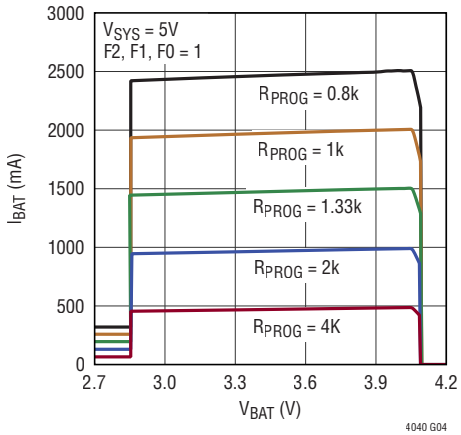
I_{BAT} vs V_{BAT} ($LiFePO_4$) with Different Charge Voltage Settings



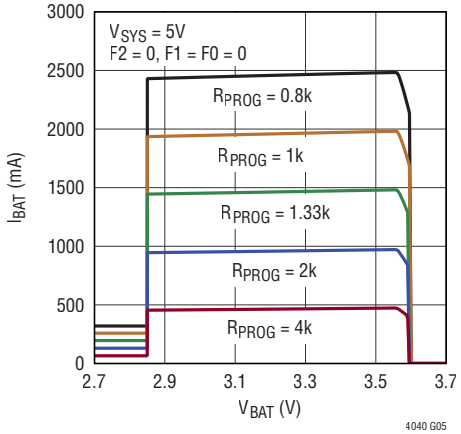
Step-Down Charger Efficiency vs V_{BAT}



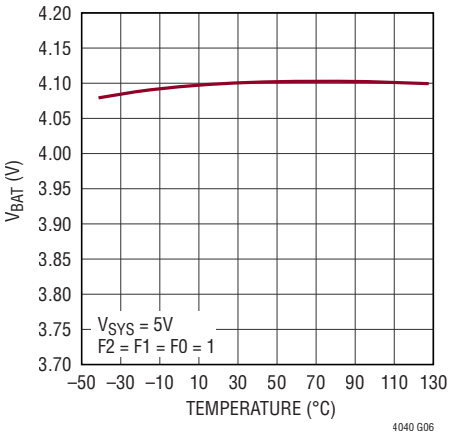
I_{BAT} vs V_{BAT} (Li-Ion) with Different PROG Resistor Values



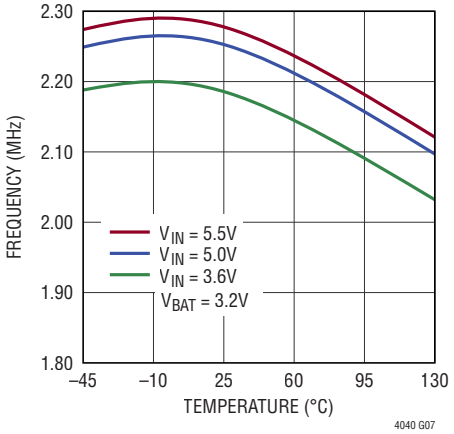
I_{BAT} vs V_{BAT} ($LiFePO_4$) with Different PROG Resistor Values



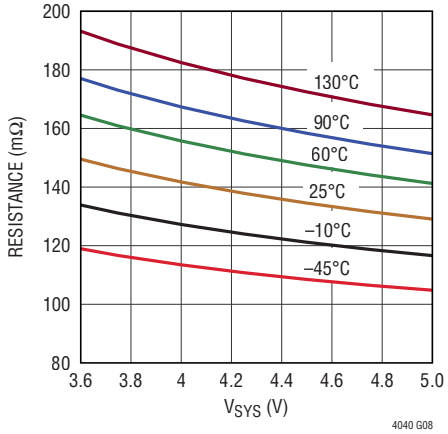
Battery Charge Voltage (Li-Ion) vs Temperature



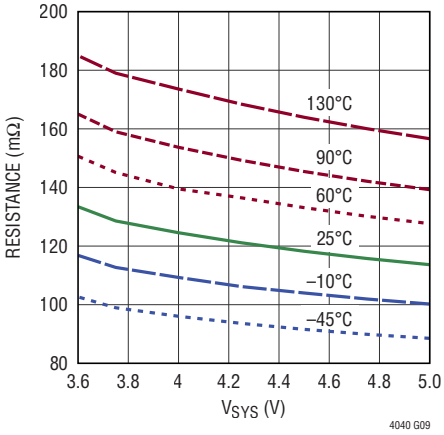
Step-Down Charger Oscillator Frequency vs Temperature



Step-Down Charger PMOS On-Resistance vs V_{SYS} over Temperature

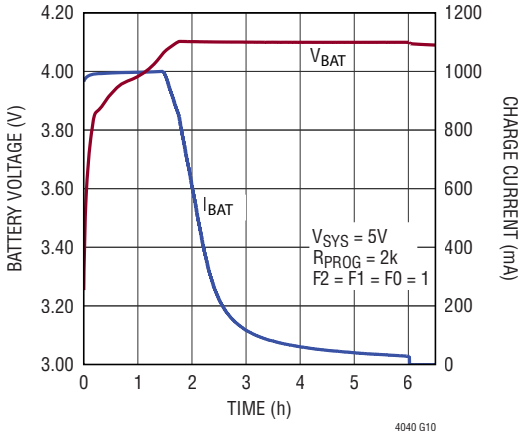


Step-Down Charger NMOS On-Resistance vs V_{SYS} over Temperature

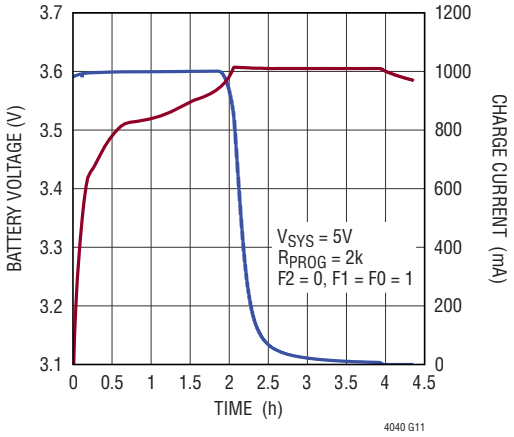


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

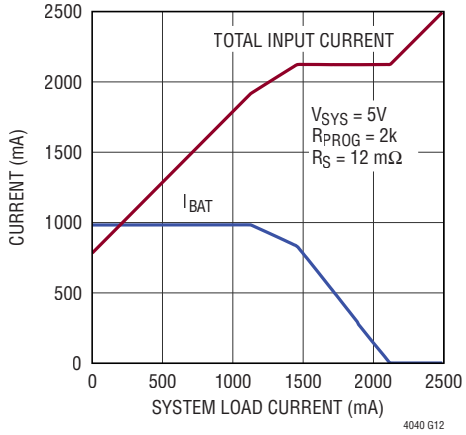
Li-Ion Battery Charging Profile



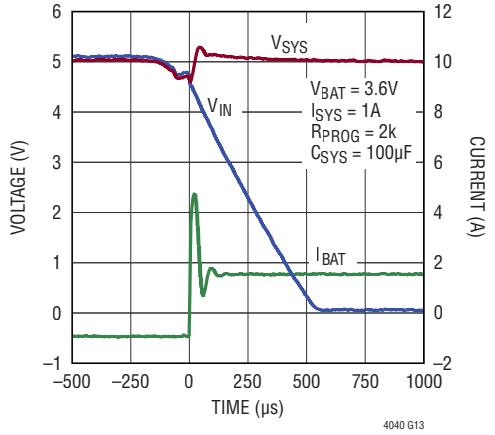
$LiFePO_4$ Battery Charging Profile



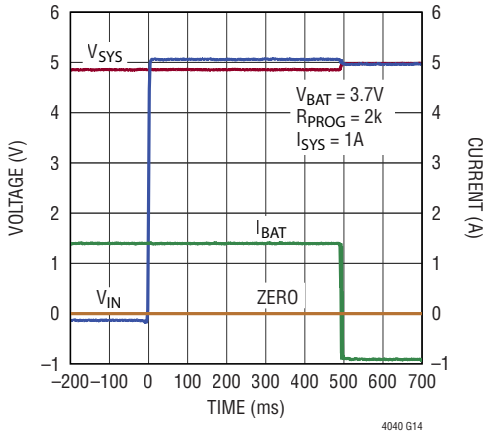
Charge Current Reduction Due to Input Current Limit Set by R_S



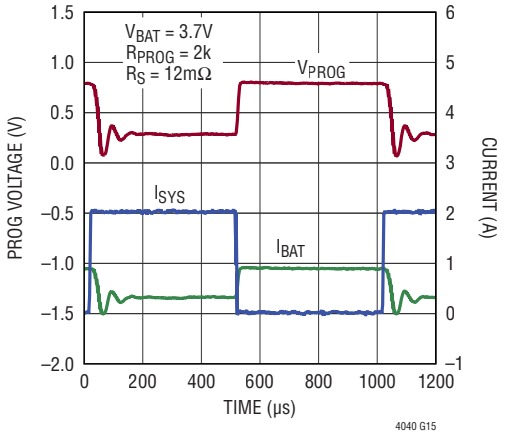
Normal to Backup Mode Transition Waveform (Li-Ion)



Backup to Normal Mode Transition Waveform

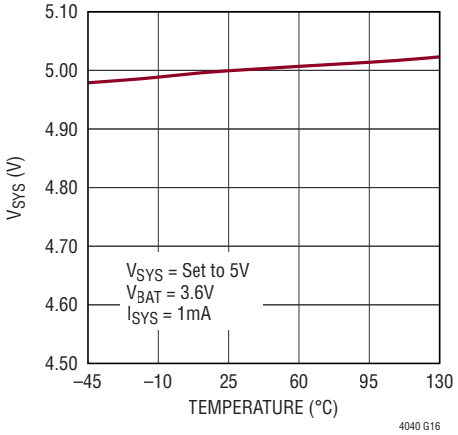


PROG Voltage Transient Response by System Step Load

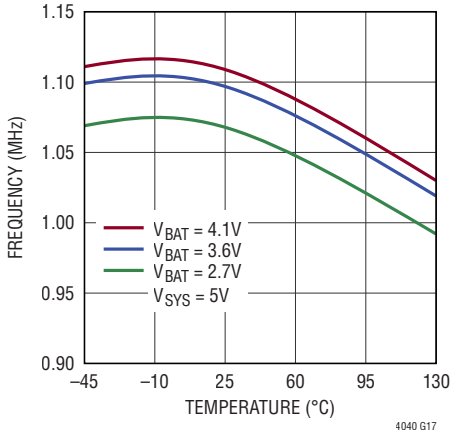


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

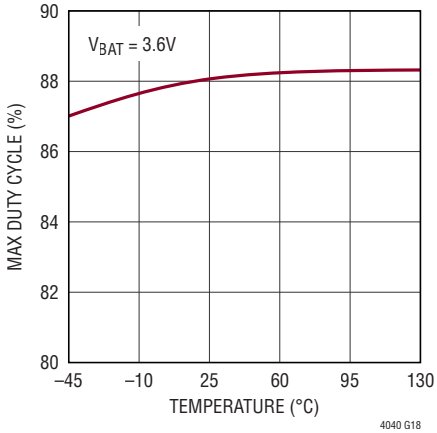
Back-Up Boost Output Voltage (V_{SYS}) vs Temperature



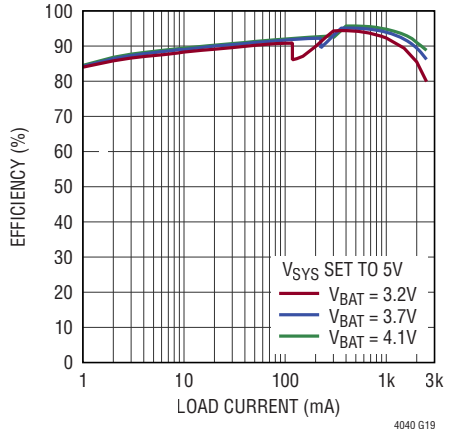
Backup Boost Oscillator Frequency vs Temperature



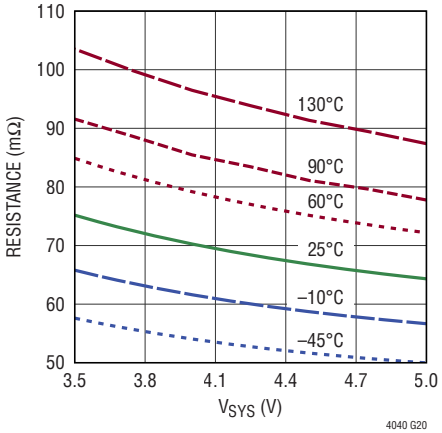
Backup Boost Maximum Duty Cycle vs Temperature



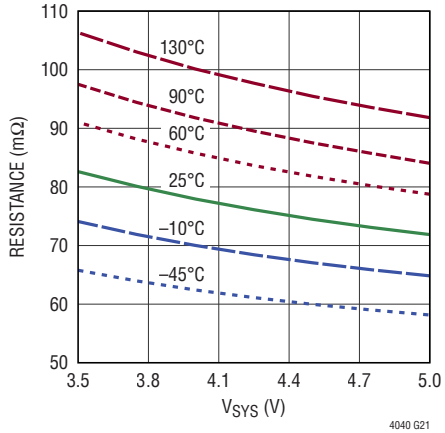
Backup Boost Efficiency vs Load Current



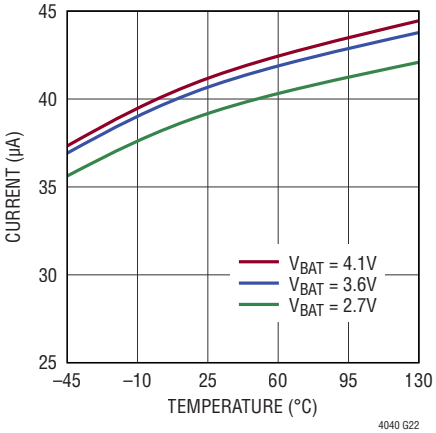
Backup Boost NMOS On-Resistance vs V_{SYS} over Temperature



Backup Boost PMOS On-Resistance vs V_{SYS} over Temperature

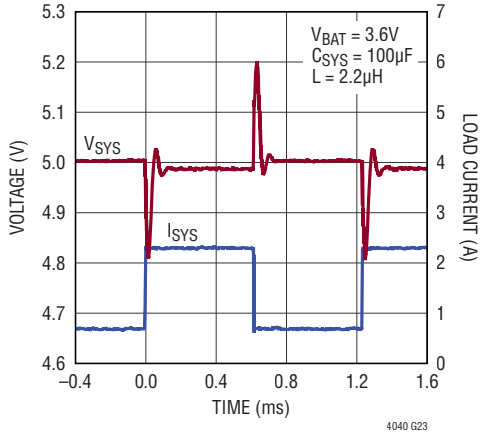


SLEEP Mode (Backup) I_{BATQ} vs Temperature

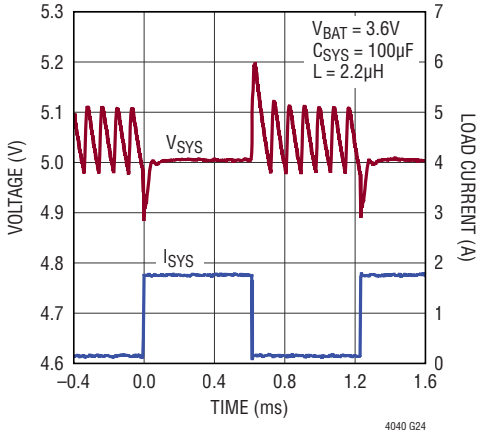


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

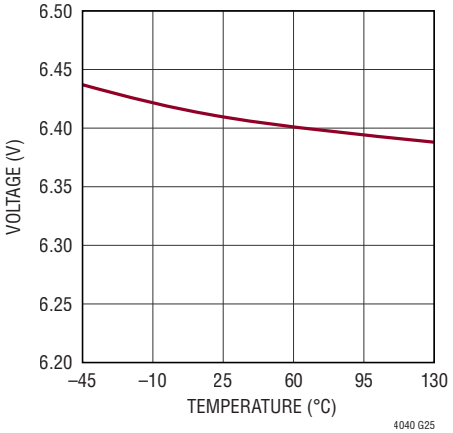
Backup Boost Transient Response to Load Step



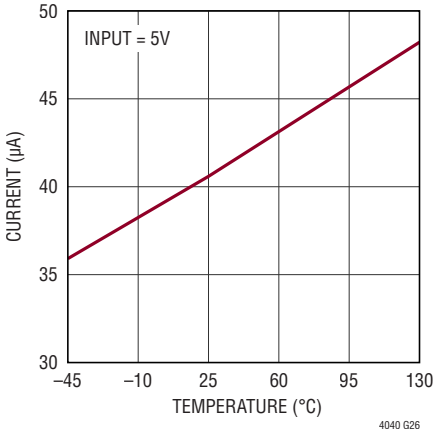
Burst Mode to Constant Frequency Mode Transition Waveform



OVP Module Shutdown Voltage (Through 6.2k) vs Temperature



OVSNS Pin Quiescent Current vs Temperature



PIN FUNCTIONS

V_{SYS} (Pins 1, 24): System Voltage Output Pin. This pin is used to provide power to an external load from either the primary input supply or the backup battery if the primary input supply is not available. In addition to supplying power to the load, this pin provides power to charge the battery when input power is available. V_{SYS} should be bypassed with a low ESR ceramic capacitor of at least 100µF to GND.

PROG (Pin 2): Charge Current Program Pin. An external resistor from the PROG pin to ground programs the full-scale charge current. At full scale, the PROG pin servos to 0.8V. The ratio of BAT pin current to PROG pin current is internally set to 2500.

CLPROG (Pin 3): V_{SYS} Current Monitoring Pin. The ratio between the CLPROG pin voltage and the differential voltage between V_{IN} and CLN is internally set to 32. Charge current is reduced when the CLPROG pin voltage reaches 0.8V.

CHGOFF (Pin 4): Disable Pin for the Battery Charger. Tie this pin to GND to enable the charger or to a voltage above 1.2V to disable it. Do not leave this pin unconnected.

BSTOFF (Pin 5): Disable Pin for the Backup Boost Converter. Tie this pin to GND to enable the boost backup or to a voltage above 1.2V to disable backup. Do not leave this pin unconnected.

V_{IN} (Pin 6): Input Pin. Power can be applied directly to this pin if the optional overvoltage protection (OVP) feature is not used. For applications where the OVP feature is required, connect an external N-channel FET between the power supply output V_{PWR} and this pin.

CLN (Pin 7): Negative terminal pin for an external current limit sense resistor connected between V_{IN} and this pin. This resistor is used to monitor the current from V_{IN} to V_{SYS}. The LT4040 reduces charge current in order to maintain 25mV across this sense resistor. However, it does not limit the system current if the drop exceeds 25mV.

$\overline{CHRG}$ (Pin 8): Open-Drain Charge Status Output; typically pulled up through a resistor to a reference voltage. During a battery charging cycle, $\overline{CHRG}$ is pulled low until the charge current drops below C/8 when the $\overline{CHRG}$ pin becomes high impedance.

$\overline{FAULT}$ (Pin 9): Open-Drain Fault Status Output; typically pulled up through a resistor to a reference voltage. This pin indicates charge cycle fault conditions during a battery charging cycle. A temperature fault or a bad-battery fault causes this pin to be pulled low. If no fault conditions exist, the $\overline{FAULT}$ pin remains high impedance.

RSTFB (Pin 10): Reset Comparator Input. High Impedance input to an accurate comparator with a 0.74V falling threshold and 20mV hysteresis. This pin controls the state of the $\overline{RST}$ output pin. An external resistor divider is used between V_{SYS}, RSTFB and GND. It can be the same resistor divider as the BSTFB divider to monitor the system output voltage V_{SYS}. See the Applications Information section.

$\overline{RST}$ (Pin 11): Open-Drain Status Output of the Reset Comparator. This pin is pulled to ground by an internal N-channel MOSFET whenever the RSTFB pin falls below 0.74V. Once the RSTFB pin voltage recovers, the pin becomes high impedance after a 232ms delay.

F2 (Pin 12): Logic Input to Select Battery Chemistry. A logic high on this pin selects Li-Ion and a logic low selects $LiFePO_4$. Do not leave this pin unconnected.

F1, F0 (Pins 13, 14): Logic inputs to select one of the four possible charge voltage settings for each battery chemistry. Do not leave these pins unconnected.

F0	F1	F2 = 1: Li-Ion (V)	F2 = 0: $LiFePO_4$ (V)
0	0	3.95	3.45
1	0	4.00	3.50
0	1	4.05	3.55
1	1	4.10	3.60

PIN FUNCTIONS

IGATE (Pin 15): Gate Pin for the External N-Channel FETs. This pin is driven by an internal charge pump to develop sufficient overdrive to fully enhance the pass transistors. The first pass transistor is connected between the supply output V_{PWR} and V_{IN} and is part of the optional overvoltage protection module. The second pass transistor, connected between V_{IN} and V_{SYS}, is mandatory and is used to disconnect the system from the input supply during backup mode.

OVSNS (Pin 16): Overvoltage Protection Sense Input. If the overvoltage feature is used, the OVSNS pin should be connected through a 6.2k resistor to an input power connector and the drain of an N-channel MOS pass transistor. If not, this pin should be shorted to V_{IN}. When voltage is detected on OVSNS, it draws a small amount of current to power a charge pump which then provides gate drive to IGATE to energize the external transistor. When the voltage on this pin exceeds typically 6V, IGATE is pulled to GND to disable the pass transistor and protect the LTC4040 from high voltage.

NTC (Pin 17): Input to the Thermistor Monitoring Circuits. The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it re-enters the valid range. A low drift bias resistor is required from V_{IN} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

BSTFB (Pin 18): Feedback Input for the Backup Boost Regulator. During steady-state backup operation, voltage on this pin servos to 0.8V.

PFI (Pin 19): Power-Fail Input. High impedance input to an accurate comparator (power-fail) with a 1.19V falling threshold and 30mV hysteresis. PFI controls the state of the $\overline{PFO}$ output pin and sets the input voltage threshold below which the boost backup is initiated. This threshold voltage also represents the minimum voltage above which the step-down battery charger is enabled and the part allows power to flow from the input to the output through the external pass transistors.

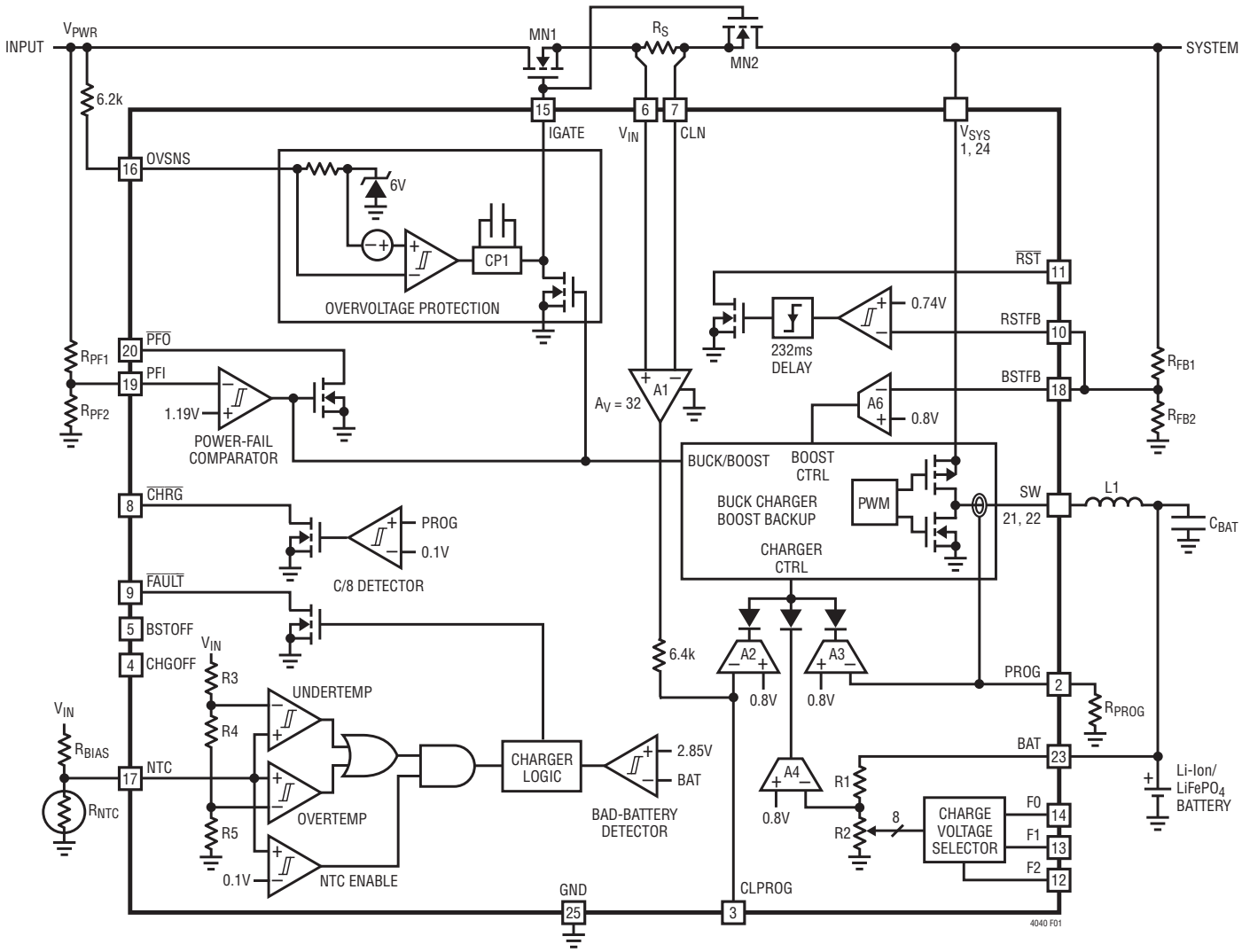
$\overline{PFO}$ (Pin 20): Open-Drain Power-Fail Status Output. This pin is pulled to ground by an internal N-channel MOSFET when the PFI input is below the falling threshold of the power-fail comparator. Once the PFI input rises above the rising threshold, this pin becomes high impedance.

SW (Pins 21, 22): Power Transmission Pin for the Buck Switching Charger and the Boost Switching Backup Converter. A 1µH to 2.2µH inductor should be connected from SW to BAT.

BAT (Pin 23): Single Cell Li-Ion or $LiFePO_4$ Battery Pin. Depending on the availability of input power, the battery will either deliver power to V_{SYS} via the boost converter or be charged from V_{SYS} via the buck charger. BAT should be bypassed with a low ESR ceramic capacitor of at least 10µF to GND.

GND (Exposed Pad Pin 25): The exposed pad must be soldered to the PCB to provide a low electrical and thermal impedance connection to the printed circuit board's ground. A continuous ground plane on the second layer of a multilayer printed circuit board is strongly recommended.

BLOCK DIAGRAM



OPERATION

The LTC4040 is a complete battery backup system manager for a 3.5V to 5.5V supply rail. The system has three principal circuit components: a full-featured step-down (buck) battery charger, a step-up (boost) backup converter with automatic burst feature to deliver power to the system load when external input power is lost and a power-fail comparator to decide which one to activate. The LTC4040 has several other auxiliary components: an input current limit (CLPROG) amplifier, an optional input overvoltage protection (OVP) circuit and a reset comparator.

The LTC4040 has three modes of operation: normal, backup and shutdown. If the input supply is above an externally programmable PFI threshold voltage, the part is considered to be in normal mode in which power flows from input to output (V_{SYS}) while the step-down switching regulator charges the battery to one of eight charge voltage settings programmed by the F0, F1, and F2 digital inputs. Please refer to the Block Diagram. The total system load is monitored by the CLPROG amplifier via an external series resistor, R_S, connected between the V_{IN} and CLN pins. This amplifier can reduce the charge current from its programmed value (set by the PROG pin external resistor R_{PROG}) if the external load demand increases beyond a programmable level set by R_S. When the input supply falls below the PFI threshold, backup mode disconnects the switches (MN1 and MN2) to isolate the system (V_{SYS}) from the input while the boost converter powers the system load from the battery using the same external inductor, L1.

THE BATTERY CHARGER

The LTC4040 includes a full-featured constant-current (CC)/constant-voltage (CV) battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad-battery detection and thermistor sensor input for out-of-temperature charge pausing. The battery charger is a high efficiency buck switching converter used to transfer charge from V_{SYS} to BAT via the SW pin. The charger can be disabled by pulling the CHGOFF pin above 1.2V.

Buck Switching Charger

The LTC4040 battery charger is a constant frequency (2.25MHz) synchronous buck converter capable of directly charging the battery to its charge voltage with an externally programmable charge current up to 2.5A from an input supply as high as 5.5V. A zero current comparator monitors the inductor current and shuts off the NMOS synchronous rectifier once the current reduces to approximately 250mA. This prevents the inductor current from reversing and improves efficiency for low charging current.

Battery Preconditioning (Trickle Charge) and Bad-Battery Fault

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{LOWBAT}, typically 2.85V, an automatic trickle charge feature sets the charge current to 1/8th or 12.5% of the programmed value. To improve charge current accuracy at this low level, the buck switching charger is turned off and a secondary linear charger is used to deliver charge to the battery. If the low voltage persists for more than half an hour, the battery charger automatically terminates and indicates, via the $\overline{CHRG}$ and $\overline{FAULT}$ pins, that the battery is in bad-battery fault.

Constant-Current Mode Charging

Once the battery voltage is above V_{LOWBAT}, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 2000V/R_{PROG}. Depending on the external load condition, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The battery charger will charge at the full programmed rate only if the sum of the external load and the charger input current is less than or equal to the input current limit set by R_S.

OPERATION

Charge Termination

The battery charger has a built-in safety timer. Once the voltage on the battery reaches the charge voltage set by the F0, F1 and F2 pins, the charger will regulate the battery voltage there and the charge current will decrease naturally. The safety timer (approximately 4-hour for Li-Ion and approximately 2-hour for $LiFePO_4$ batteries) starts once the charger detects that the battery has reached the charge voltage. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered unless the battery voltage falls below the automatic recharge threshold.

Automatic Recharge

Once the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the product remains in this state long enough, the battery will eventually self-discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG}. In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, it will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHG} for more than 2.4ms.

Charge Status Indication via the $\overline{CHRG}$ and $\overline{FAULT}$ Pins

The status of the battery charger is indicated via the $\overline{CHRG}$ and $\overline{FAULT}$ pins according to the fallowing table:

Table 1. Charge Status Indication

$\overline{CHRG}$	$\overline{FAULT}$	STATUS
0	0	NTC Fault and C/8 Not Reached
0	1	Charging (No Fault)
1	0	Bad Battery Fault
1	1	Charging Nearly Complete – C/8 Reached

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charging cycle. When charge current drops to 1/8th the value programmed by R_{PROG}, the $\overline{CHRG}$ pin is released (Hi-Z). The $\overline{CHRG}$ pin does not respond to the C/8 threshold if the LTC4040 is in input current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for more than 1/2 hour), the $\overline{CHRG}$ pin will be released and the $\overline{FAULT}$ pin will be pulled low, indicating that the charging has been terminated. However, if there is a fault due to NTC, only the $\overline{FAULT}$ pin is pulled low while the $\overline{CHRG}$ pin remains low, indicating a pause in charging.

Battery Thermal Protection with NTC Thermistor

The LTC4040 monitors the battery temperature during the charging cycle by using a negative temperature coefficient (NTC) thermistor, placed close to the battery pack. If the battery temperature moves outside a safe charging range, the IC suspends charging and signals a fault condition until the temperature returns to the safe charging range. The safe charging range is determined by two comparators that monitor the voltage at the NTC pin as shown in the Block Diagram. To use this feature, connect the thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{BIAS}, from V_{IN} to NTC. R_{BIAS} should be a 1% resistor with a value equal to the value of the chosen thermistor at 25°C (R25).

Thermistor manufacturers usually include either a temperature lookup table identified with a characteristic curve number, or a formula relating temperature to the resistor value. Each thermistor is also typically designated by a thermistor gain value ß25/85.

The LTC4040 will pause charging when the resistance of the thermistor increases to 325% of the R_{BIAS} resistor as the temperature drops. For a Vishay Curve 2 thermistor with ß25/85 = 3490K and 25°C resistance of 10k, this corresponds to a temperature of about 0°C. The LTC4040 also pauses charging if the thermistor resistance decreases to 53.6% of the R_{BIAS} resistor. For the same Vishay Curve 2 thermistor, this corresponds to approximately 40°C. If the battery charger is in constant-voltage mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. The hot and cold comparators each have approximately 2°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

OPERATION

Differential Undervoltage Lockout

An undervoltage lockout circuit monitors the differential voltage between V_{SYS} and BAT and shuts off the charger if the BAT voltage reaches within 50mV of the V_{SYS} voltage. Charging does not resume until this difference increases to 145mV.

BACKUP BOOST CONVERTER

To supply the system load from the battery in backup mode, the LTC4040 contains a 1.125MHz constant-frequency current-mode synchronous boost switching regulator with output disconnect and automatic Burst Mode features. The regulator can provide a maximum load of 2.5A from a battery as low as 3.2V and the system output voltage (V_{SYS}) can be programmed up to a maximum of 5V via the BSTFB pin. See the Applications Information section for details. The converter can be disabled by pulling the BSTOFF pin high. The boost regulator includes safety features like short-circuit current protection, input undervoltage lockout, and output overvoltage protection.

Zero Current Comparator

The LTC4040 boost converter includes a zero current comparator which monitors the inductor current and shuts off the PMOS synchronous rectifier once the current drops to approximately 250mA. This prevents the inductor current from reversing in polarity thereby improving efficiency at light loads.

PMOS Synchronous Rectifier

To prevent the inductor current from running away, the PMOS synchronous rectifier is only enabled when $V_{SYS} > (V_{BAT} – 200mV)$. Additionally, if the current through the synchronous FET (PMOS) ever exceeds 8A, the converter skips the next two clock cycles so that the inductor current has a chance to discharge safely below this level.

Short-Circuit Protection

The output disconnect feature enables the LTC4040 boost converter to survive a short circuit at its output. It incorporates internal features such as current limit foldback and thermal shutdown for protection from excessive power dissipation during short circuit.

V_{BAT} Undervoltage Lockout

To prevent the battery from discharging too deeply, the LTC4040 incorporates an undervoltage lockout circuit which shuts down the boost regulator when V_{BAT} drops below 2.45V.

Boost Overvoltage Protection

If the BSTFB node were inadvertently shorted to ground, then the boost converter output would increase indefinitely with the maximum current that could be sourced from BAT. The LTC4040 protects against this by shutting off both switches if the output voltage exceeds 5.5V.

Burst Mode Operation

To improve battery life during backup, the LTC4040 boost converter provides automatic Burst Mode operation which increases the efficiency of power conversion at very light loads. Burst Mode operation is initiated if the output load current falls below an internally set threshold. Once Burst Mode operation is initiated, only the circuitry required to monitor the output is kept alive. This is referred to as the sleep state in which the backup boost consumes only 40µA from the battery. When the V_{SYS} pin voltage drops by about 1% from its nominal value, the part wakes up and commences normal PWM operation. The output capacitor recharges and causes the part to re-enter the sleep state if the output load remains less than the Burst Mode threshold. The frequency of this intermittent PWM or Burst Mode operation depends on the load current; that is, as the load current drops further below the burst threshold, the boost converter turns on less frequently. When the load current increases above the burst threshold, the converter seamlessly resumes continuous PWM operation. Thus, Burst Mode operation maximizes the efficiency at very light loads by minimizing switching and quiescent losses. However, the output ripple typically increases to about 2% peak-to-peak. Burst Mode ripple can be reduced, in some circumstances, by placing a small phase-lead capacitor (C_{PL}) between the V_{SYS} and BSTFB pins. However, this may adversely affect the efficiency and the quiescent current at light loads. Typical values of C_{PL} range from 15pF to 100pF.

OPERATION

$V_{BAT} > V_{SYS}$ Operation

The LTC4040 boost converter will maintain voltage regulation even if its input voltage is above the output voltage. This is achieved by terminating the switching of the synchronous PMOS and applying V_{BAT} voltage statically on its gate. This ensures that the slope of the inductor current will reverse during the time current is flowing to the output. Since the PMOS no longer acts as a low impedance switch in this mode, there will be more power dissipation within the IC. This will cause a sharp drop in the efficiency. The maximum output current should be limited in order to maintain an acceptable junction temperature.

INPUT CURRENT LIMIT AND CLPROG MONITOR

The LTC4040 contains an input current limit circuit which monitors the total system current (the external load plus the charger input current) via an external series resistor, R_S, connected between the pins V_{IN} and CLN. The part does not actually limit the external load but as the external load demand increases, it reduces charge current, if necessary, in an attempt to maintain a maximum of 25mV across the V_{IN} and CLN pins. Please refer to Programming the Input Current Limit and CLPROG Monitor section in Applications Information. However, if the external load demand exceeds the limit set by R_S, the part does not reduce the load current but the charge current will drop to zero. In all scenarios, the voltage on the CLPROG pin will correctly represent the total system current. 800mV on the CLPROG pin represents the full-scale current set by the external series resistor, R_S.

POWER-FAIL COMPARATOR AND MODE SWITCHING

The LTC4040 contains a fast power-fail comparator which switches the part from normal to backup mode in the event the input supply voltage falls below an externally programmed threshold voltage. This threshold voltage is programmed by an external resistor divider via the PFI pin. See the Applications Information section for details of how to choose values for the resistor divider. The output of the power-fail comparator also directly drives the gate of an open-drain NMOS to report the status of the availability of input power via the $\overline{PFO}$ pin. If input power is available, the $\overline{PFO}$ pin is high impedance; otherwise, the pin is pulled down to ground.

At the onset of backup mode, the battery charger shuts off, the external NMOS pass transistors (MN1 and MN2 in Block Diagram) are quickly turned off by discharging IGATE to ground thereby disconnecting the system output V_{SYS} from the input and the backup boost converter activates promptly to deliver load from the battery. Although the power-fail comparator has a hysteresis of approximately 30mV, it may not be able to overcome the input voltage spike resulting from the sudden collapse of the forward current from the input to V_{SYS}. To prevent repeated unwanted mode switching, once activated, the backup boost stays on for at least half a second. During this time, the power-fail comparator output is ignored and an internal switch of approximately 270Ω pulls down the OVSNS pin to help discharge the input. After the half-second timer expires, if the power-fail comparator output indicates that power is still not available, the backup boost continues to deliver the load but the pull-down on the OVSNS pin is released. When the power-fail comparator detects that input power is available, the OVP charge pump starts to charge up the IGATE pin but the backup boost converter continues to deliver system load until IGATE is approximately 8V. This ensures that the forward conduction path through the external NFET pass transistors has been established. At this point, the backup boost gets deactivated and the charger turns back on to charge the battery while the system load gets delivered directly from the input to V_{SYS} through the pass transistors.

RESET COMPARATOR

The LTC4040 contains a reset comparator which monitors V_{SYS} under all operating modes via the RSTFB pin and reports the status via an open-drain NMOS transistor on the $\overline{RST}$ pin. At any time, if V_{SYS} falls 7.5% from its programmed value, the $\overline{RST}$ pin pulls low almost instantaneously. However, the comparator waits approximately 232ms after V_{SYS} rises above the threshold before making the $\overline{RST}$ pin high impedance. Please refer to Programming the Reset Comparator Threshold section in Applications Information.

OPERATION

OPTIONAL INPUT OVERVOLTAGE PROTECTION (OVP)

The LTC4040 can protect itself from the inadvertent application of excessive voltage with just two external components: an N-channel FET (MN1) and a 6.2k resistor as shown in the Block Diagram. The maximum safe overvoltage magnitude will be determined by the choice of external NMOS and its associated drain breakdown voltage.

The optional overvoltage protection (OVP) module consists of two pins. The first, OVSNS, is used to measure the applied voltage through an external resistor. The second, IGATE, is an output used to drive the gate pins of two external N-channel FETs, MN1 and MN2 (Block Diagram). The voltage at the OVSNS pin will be lower than the OVP input voltage by about 250mV due to the OVP circuit's quiescent current flowing through the OVSNS resistor. When OVSNS is below 6V, an internal charge pump will drive IGATE to approximately 1.88 • V_{OVSNS}. This will enhance the N-channel FETs and provide a low impedance connection to V_{SYS} and power the chip. If OVSNS should rise above 6V due to a fault, IGATE will be pulled down to ground, disabling the external FETs to protect downstream circuitry. At the same time, the backup boost converter will be activated to supply the system load from the battery. When the voltage drops below 6V again, the external FETs will be re-enabled. If the OVP feature is not desired, remove MN1, short OVSNS to V_{IN} and apply external power directly to V_{IN}.

SHUTDOWN MODE OPERATION

The LTC4040 can be shutdown almost entirely by pulling both CHGOFF and BSTOFF pin above 1.2V. In this mode, the internal charge pump is shutdown and IGATE is pulled to ground disconnecting the forward path from input to output via the external FETs. Only the internal OVP shunt regulator remains active to monitor the input supply for any possible overvoltage condition and consumes about 25µA via the OVSNS pin. Total current draw from the BAT pin drops to below 3µA during shutdown.

APPLICATIONS INFORMATION

CHOOSING A CHARGE VOLTAGE FOR THE BATTERY:

The LTC4040 offers 4 different charge voltage options for each of the two battery chemistries (Li-Ion and $LiFePO_4$) and these levels are selected by the digital inputs F0, F1 and F2. Choosing a higher charge voltage increases the battery capacity to provide a longer product run-time but reduces the battery lifetime, usually measured by the number of charge/ discharge cycles. Battery manufacturers usually consider the end of life for a battery to be when the battery capacity drops to 80% of the rated capacity. The curves in Figure 1 show the relationship between cell capacity and cycle life for a typical Li-Ion battery cell. Using 4.2V as the charge voltage, a typical Li-Ion battery is considered at 100% initial capacity but delivers about 500 charge/ discharge cycles before the capacity drops to 80%. However, if the same battery uses 4.1V as the charge voltage, it is at 85% initial capacity but the number of charge/discharge cycles can be almost doubled to 1000 before the capacity drops to 80%. Lowering the charge voltage even further to 4.0V can increase the battery lifetime more than three times to 1800 charge/ discharge cycles. Since LTC4040 is a backup product, the battery is likely to spend the majority of its lifetime fully charged. This makes it even more critical to charge at a lower charge voltage to maximize battery lifetime since battery capacity degrades even faster when batteries remain fully charged. Because of the different Li-Ion battery chemistries and other conditions that can affect battery lifetime, the curves shown here are only estimates of the number of charge cycles and battery-capacity levels.

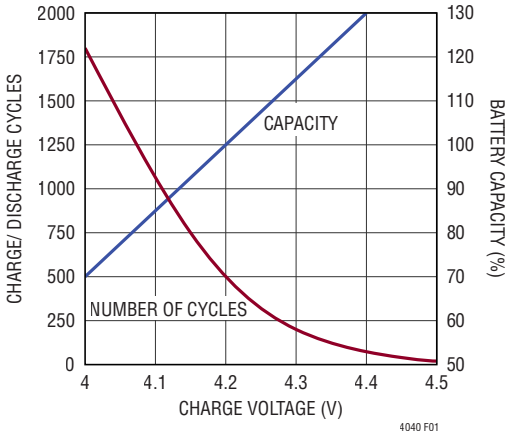


Figure 1. Battery Cycle Life and Capacity as a Function of Charge Voltage

PROGRAMMING THE INPUT VOLTAGE THRESHOLD FOR THE POWER-FAIL COMPARATOR

The input voltage threshold below which the power-fail status pin $\overline{PFO}$ indicates a power-fail condition and the LTC4040 activates the backup boost operation can be programmed by using a resistor divider from the supply to GND via the PFI pin such that:

$$V_{SUPP(PFO)} = V_{PFI} \bullet \left(1+\frac{R_{PF1}}{R_{PF2}}\right) = 1.19V \bullet \left(1+\frac{R_{PF1}}{R_{PF2}}\right)$$

V_{PFI} is approximately 1.19V. See Block Diagram. The PFI threshold voltage should be set to a level between 200mV to 300mV below the nominal input supply voltage so that the supply transients do not trip the comparator. On the other hand, it should be set high enough so that the V_{SYS} voltage does not drop too much to trip the reset comparator during the transition to backup mode.

PROGRAMMING THE BATTERY CHARGE CURRENT

Battery charge current is programmed using a single resistor from the PROG pin to ground. To set a charge current of I_{CHG}, the PROG pin resistor value can be determined using the following equation:

$$R_{PROG} = 2500 \bullet \frac{0.8V}{I_{CHG}} = \frac{2000V}{I_{CHG}}$$

For example, to set the charge current to 1A, the value of the PROG pin resistor should be 2k. The minimum recommended charge current is 500mA, below which the accuracy of the charge current suffers. This corresponds to a maximum R_{PROG} resistor of 4k.

APPLICATIONS INFORMATION

PROGRAMMING THE INPUT CURRENT LIMIT AND CLPROG MONITOR

The input current limit is programmed by connecting a series resistor between the V_{IN} and CLN pins. To limit the total system current to I_{SYSLIM}, the value of the required resistor can be calculated using the following equation:

$$R_S = \frac{25mV}{I_{SYSLIM}}$$

For example, to set the current limit to 2A, the series resistor should be 12.5mΩ. As discussed in the Operations section, the part does not limit the system current but reduces the charge current to zero in case the system load exceeds this limit.

The voltage on the CLPROG pin always represents the total system current I_{SYS} through the external series resistance, R_S. 800mV on CLPROG represents the full-scale current set by R_S. The system current can be calculated from the CLPROG pin voltage by using the following equation:

$$I_{SYS} = \frac{V_{CLPROG}}{32 \bullet R_S}$$

For example, if the CLPROG pin voltage is 600mV and R_S is 12.5mΩ, then the total system current is 1.5A. As shown in the block diagram, the CLPROG pin is not buffered internally. So it is important to isolate this pin before connecting to an ADC or any other monitoring device. Failure to do so would degrade the accuracy of this circuit.

PROGRAMMING THE BOOST OUTPUT VOLTAGE

The boost converter output voltage in backup mode can be programmed for any voltage from 3.5V to 5V by using a resistor divider from the V_{SYS} pin to GND via the BSTFB pin such that:

$$V_{SYS} = V_{BSTFB} \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) = 0.8V \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

V_{BSTFB} is 0.8V. See the Block Diagram. Typical values for R_{FB1} and R_{FB2} are in the range of 40k to 2M. Too small a resistor will result in a large quiescent current whereas too large a resistor coupled with any parasitic BSTFB pin capacitance will create an additional pole and may cause loop instability.

PROGRAMMING THE RESET COMPARATOR THRESHOLD

The threshold for the reset comparator can be programmed by using a resistor divider from the V_{SYS} pin to GND via the RSTFB pin such that:

$$V_{SYS(RST)} = V_{RSTFB} \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) = 0.74V \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

V_{RSTFB} is 0.74V. See the Block Diagram. Typical values for R_{FB1} and R_{FB2} are in the range of 40k to 2M. In most applications, the BSTFB and RSTFB pins can be shorted together and only one resistor divider between V_{SYS} and GND is needed to set the V_{SYS} voltage during backup mode and the reset threshold 7.5% below the V_{SYS} programmed voltage.

CHOOSING THE EXTERNAL RESISTOR FOR THE OVERVOLTAGE PROTECTION (OVP) MODULE

In an overvoltage condition, the OVSNS pin will be clamped at 6V. The external 6.2k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/8W 6.2k resistor can have at most $\sqrt{P_{MAX} \bullet 6.2k\Omega} = 28V$ applied across its terminals. With the 6V at OVSNS, the maximum overvoltage magnitude that this resistor can withstand is 34V. A 1/4W 6.2k resistor raises the value to 45V. The OVSNS pin's absolute maximum current rating of 10mA imposes an upper limit of 68V protection.

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CHOOSING THE EXTERNAL TRANSISTORS (MN1 AND MN2) FOR THE OVP MODULE AND THE INPUT-TO-OUTPUT DISCONNECT SWITCH

The LTC4040 uses a weak internal charge pump to pump IGATE above the input voltage so that N-channel external FETs can be used as pass transistors. However, these transistors should be carefully chosen so that they are fully enhanced with a VGS of 3V. Since one of these pass transistors is the OVP FET, its breakdown voltage (BV_{DSS}) determines the maximum voltage the LTC4040 can withstand at its input. Also, care must be taken to avoid any leakage on the IGATE pin, as it may adversely affect the FET operation. See Table 2 for a list of recommended transistors.

Table 2. Recommended NMOS FETs for Overvoltage Protection and Disconnect Switch

NMOS FET	BV_{DSS}	R_{ON}
SIR424DP (Vishay)	20V	7.4mΩ
SiS488DN (Vishay)	40V	7.5mΩ
SiS424DN (Vishay)	20V	8.9mΩ

CHOOSING THE INDUCTOR FOR THE SWITCHING REGULATORS

Since the same inductor is used to charge the battery in normal mode and to deliver the system load in backup mode, its inductance should be low enough so that the inductor current can reverse quickly as soon as the backup mode is initiated. On the other hand, the inductance should not be so low that the inductor current is discontinuous at the lowest charge current setting since charge current accuracy suffers greatly if the inductor current is discontinuous. Inductor current ripple (ΔI_L) can be computed using the following equation:

$$\Delta I_L = V_{BAT} \bullet \left(1 - \frac{V_{BAT}}{V_{SYS}}\right) \bullet \frac{1}{L \bullet f_{OSC}}$$

Since the lowest recommended charge current setting is 500mA, inductor current will be discontinuous if the ripple is more than twice that amount, i.e, 1A. For V_{SYS} = 5V, V_{BAT} = 3.2V, f_{OSC} = 2.25MHz (buck mode), and ΔI_L = 1A, the theoretical minimum inductor size to avoid discontinuous operation can be computed by using the above equation to be 0.5µH. To account for inaccuracies in the system and component values, the practical low limit should be 1µH. Since the backup boost operates at half the frequency (1.125MHz), the inductor current ripple with a 1µH inductor using the same equation will be approximately 1A in backup mode. If this seems excessive, inductors up to 2.2µH can be used to lower the inductor current ripple.

The other considerations when choosing an inductor is the maximum DC current (IDC) and the maximum DC resistance (DCR) rating as shown in Table 3 below. The chosen inductor should have a max IDC rating which is greater than the current limit specification of the part in order to prevent an inductor current runaway situation. For the LTC4040, the maximum current that the inductor can experience is approximately 8A in backup mode. It is also important to keep the max DCR as low as possible in order to minimize conduction loss and help improve the converter's efficiency.

Table 3. Recommended Inductors for the LTC4040

INDUCTOR TYPE	L (µH)	MAX IDC (A)	MAX DCR (MΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL-5020-122	1.2	8.3	20.5	5.68 × 5.68 × 2	Coilcraft www.coilcraft.com
XAL-6030-122	1.2	10.8	7.5	6.76 × 6.76 × 3.1	Coilcraft www.coilcraft.com
XAL-6020-132	1.3	9	15.4	6.76 × 6.76 × 2.1	Coilcraft www.coilcraft.com
XAL-6030-182	1.8	14	10.52	6.76 × 6.76 × 3.1	Coilcraft www.coilcraft.com
XAL-5030-222	2.2	9.2	14.5	5.3 × 5.5 × 3.1	Coilcraft www.coilcraft.com
XAL-6030-222	2.2	15.9	13.97	6.38 × 6.58 × 3.1	Coilcraft www.coilcraft.com

CHOOSING V_{SYS} CAPACITOR

The worst-case delay for the backup boost converter to meet the system load demand can happen if the PFI input falls below the externally set threshold at a time when the buck charger is charging at the highest setting of 2.5A

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and the system load is also very high, e.g., 2.5A. Under this scenario, as soon as the part initiates the backup mode, the inductor current will have to reverse from 2.5A (from SW to BAT) to as high as the boost current limit of approximately 6.5A (from BAT to SW). That is a 9A current change in the inductor with a slope of V_{BAT}/L. At a low battery voltage of 3.2V, this might take almost 3µs even with a 1µH inductor. During this transition, C_{SYS}, the capacitor on the V_{SYS} pin, will have to deliver the shortfall until the inductor current is caught up with the system load demand, and the capacitor will deplete according to the following equation:

$$C_{SYS} = I_{LOAD} \bullet \frac{\Delta t}{\Delta V}$$

The size of the capacitor should be big enough to hold the system voltage, V_{SYS}, up above the reset threshold during this transition. For a system load I_{LOAD} = 2.5A, transition time Δt = 3µs, if the maximum droop ΔV allowed in the system output is 100mV, the required capacitance at the V_{SYS} pin should be at least 75µF.

The other consideration for choosing V_{SYS} capacitor size is the maximum acceptable output voltage ripple during steady-state backup boost operation. For a given duty cycle of D and load of I_{LOAD}, the output ripple V_{RIP} of a boost converter is calculated using the following equation:

$$V_{RIP} = \frac{I_{LOAD}}{C_{SYS}} \bullet D \bullet \frac{1}{f_{OSC}}$$

If the maximum allowable ripple is 20mV under 2.5A steady-state load while boosting from 3.2V to 5V (D = 36%), the required capacitance at V_{SYS} is calculated to be at least 40µF using the above equation. Please refer to Table 4 for recommended ceramic capacitor manufacturers.

Table 4. Recommended Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

BATTERY CHARGER STABILITY CONSIDERATIONS

The LTC4040's switching battery charger contains three control loops: constant-voltage, constant-current, and input current limit loop, all of which are internally compensated. However, various external conditions like load and component values may interfere with the internal compensation and cause instability. For example, the constant-voltage loop may become unstable due to reduced phase margin if more than 100µF capacitance is added in parallel with the actual battery at the BAT pin.

In constant-current mode, the PROG pin is in the feedback loop rather than the BAT pin. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. For the constant-current loop to be stable, the pole frequency at the PROG pin should be kept above 1MHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 1MHz \bullet C_{PROG}}$$

Alternatively, for R_{PROG} = 4k (500mA setting), the maximum allowable capacitance on the PROG pin is 40pF. If any measuring device is attached to the PROG pin for monitoring the charge current, a 1M isolation resistor should be inserted between the PROG pin and the device.

BACKUP BOOST STABILITY CONSIDERATIONS

The LTC4040's backup boost converter is internally compensated. However, system capacitance less than 100µF or over 1000µF will adversely affect the phase margin and hence the stability of the converter.

Also, if the right-half-plane (RHP) zero moves down in frequency due to external load conditions and the choice of the inductor value, that may also reduce the phase margin and cause instability. If the output power is P_{OUT}, inductor value is L, efficiency is η and the input to the

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boost converter is V_{BAT}, the RHP zero frequency can be expressed as follows:

$$f_{RHP} = \frac{(V_{BAT})^2}{2 \bullet \pi \bullet L \bullet P_{OUT}} \bullet \eta$$

For the LTC4040's backup boost to be able to supply 12.5W of output power (2.5A at 5V) from a 3.2V battery, the maximum inductor size should not exceed 2.2µH because of the RHP zero consideration. Also, too much lead resistance between the battery and the BAT pin can lower the effective input voltage of the boost converter causing the RHP zero to shift downward and cause instability. This is why it is important to minimize the lead resistance and place the battery as close to the BAT pin as possible.

ALTERNATE NTC THERMISTORS AND BIASING

The hot and cold trip points may be adjusted using a different type of thermistor, or a different R_{BIAS} resistor, or by adding a desensitizing resistor R_{ADJ} as shown in Figure 2, or by a combination of these measures. For example, by increasing R_{BIAS} to 12.4k from the default value of 10k, with the same Vishay Curve 2 thermistor, the cold trip point moves down to –5°C, and the hot trip point moves down to 34°C. If a Vishay Curve 1 thermistor with ß25/85 = 3950K and resistor of 100k at 25°C is used, a 1% R_{BIAS} resistor of 118k and a 1% R_{ADJ} resistor of 12.1k results in a cold trip point of 0°C, and a hot trip point of 39°C.

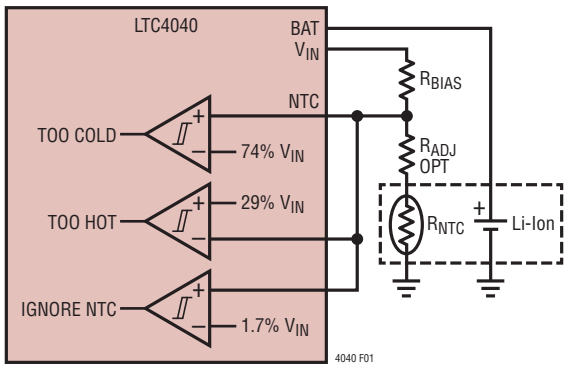

Figure 2. NTC Connections

PCB LAYOUT CONSIDERATIONS

Since the LTC4040 includes a high-current high-frequency switching converter, the following guidelines should be used during printed circuit board (PCB) layout in order to achieve optimum performance and minimum electromagnetic interference (EMI).

1. Even though the converter can operate in both step-down (buck) and step-up (boost) mode, there is only one hot-loop containing high-frequency switching currents. The simplified diagram in Figure 3 can be used to explain the hot-loop in the LTC4040 switching converter. Current follows the blue loop when switch S2 (NMOS) is closed and the red loop when switch S1 (PMOS) is closed. So it is evident that the current in the C_{BAT} capacitor is continuous whereas the C_{SYS} current is discontinuous forming a hot loop with V_{SYS} pins and GND as indicated by the green loop. Since the amount of EMI is directly proportional to the area of this loop, the V_{SYS} capacitor, prioritized over all else, should be placed as close to the V_{SYS} pins as possible and the ground side of the capacitor should return to the ground plane through an array of vias.

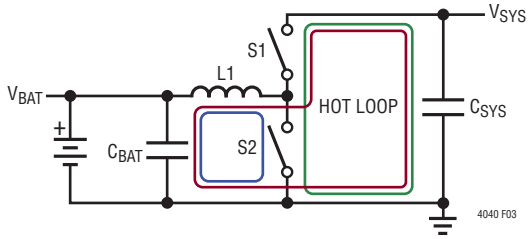

Figure 3. Hot-Loop Illustration for the LTC4040 Switching Converter

2. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (Layer 2). High frequency currents in the hot loop tend to flow along a mirror path on the ground plane which is directly beneath the incident path on the top plane of the board as illustrated in Figure 4. If there are slits or cuts or drill-holes in this mirror path on the ground plane due to other traces, the current will be forced to go around the slits. When high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will

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build up and radiated emissions will occur. So every effort should be made to keep the hot-loop current path as unbroken as possible.

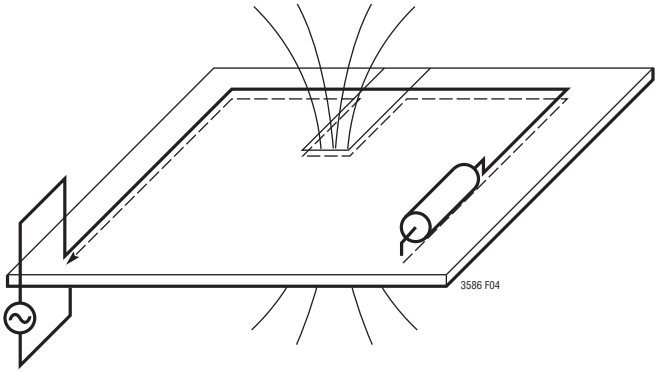
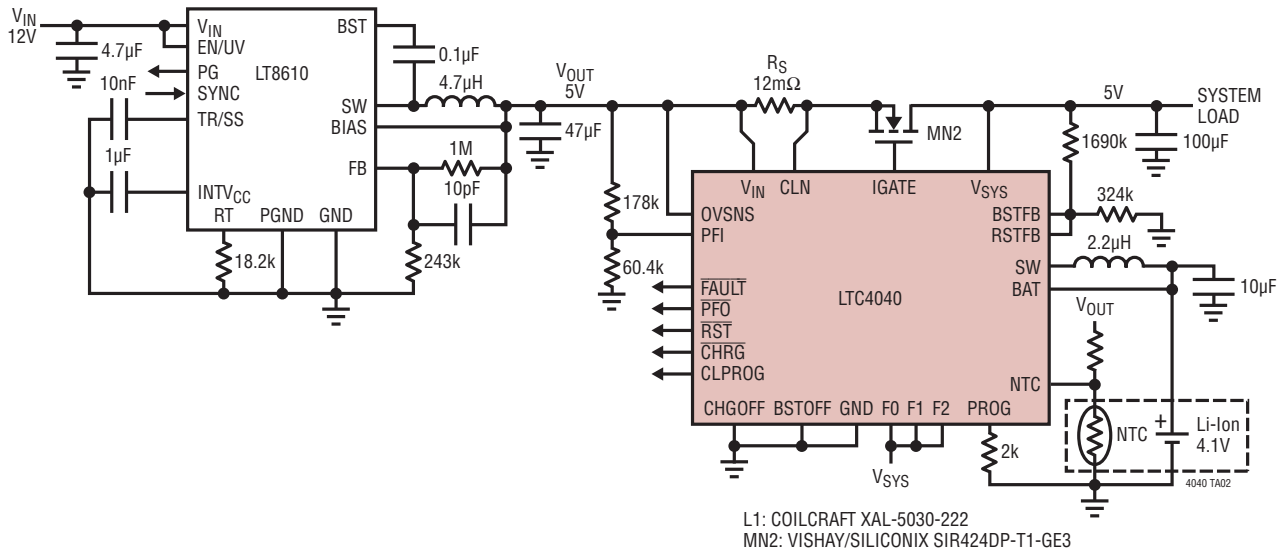


Figure 4. High Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased EMI

3. The other important components that need to be placed close to the pins are the C_{BAT} capacitor and the inductor L1. Even though the current through these components is continuous, they can change very abruptly due to a sudden change in load demand. Also, their traces should be wide enough to handle currents as high as the NMOS current limit (typ. 6.5A) in backup boost mode.
4. Locate the V_{SYS} dividers for BSTFB and RSTFB near the part but away from the switching components. Kelvin the top of the resistor dividers to the positive terminal of C_{SYS}. The bottom of the resistor dividers should return to the ground plane away from the hot-loop current path. The same is true for the PFI divider.
5. The exposed pad on the backside of the LTC4040 package must be securely soldered to the PC board ground and also must have a group of vias connecting it to the ground plane for optimum thermal performance. Also this is the only ground pin in the package, and it serves as the return path for both the control circuitry and the switching converter.
6. The IGATE pin for controlling the gates of the external pass transistors has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{SYS} connected metal.

TYPICAL APPLICATION

5V Backup System with 12V Buck for Automotive Application (Charge Current Setting: 1A, Input Current Limit Setting: 2A)

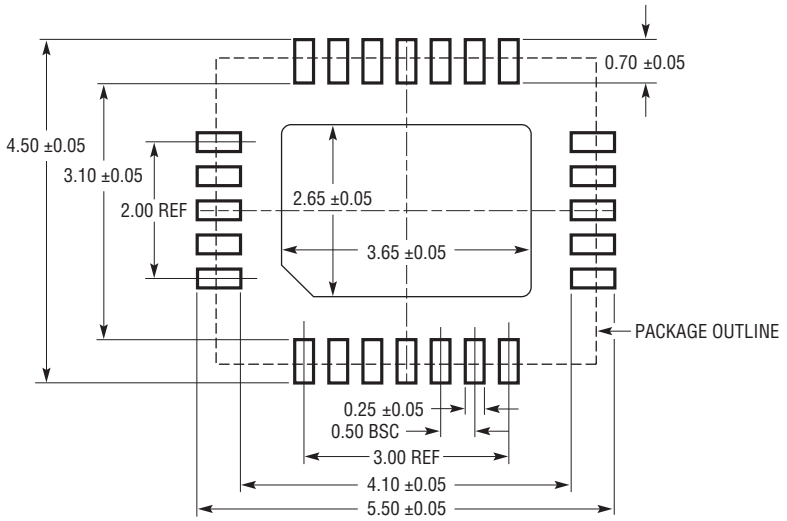


L1: COILCRAFT XAL-5030-222
MN2: VISHAY/SILICONIX SIR424DP-T1-GE3

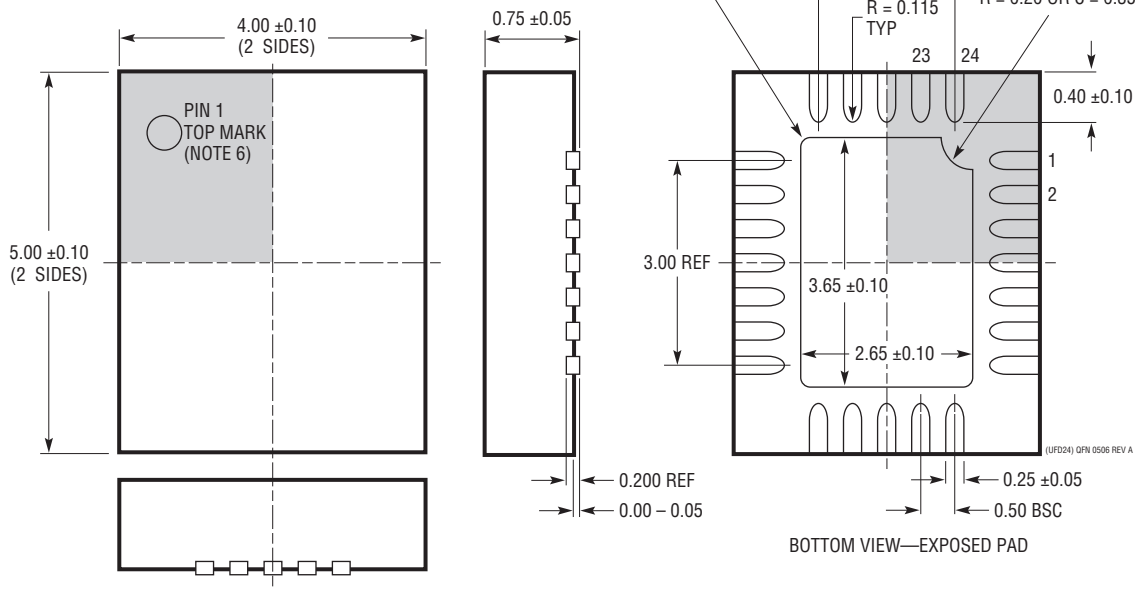
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC4040#packaging for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

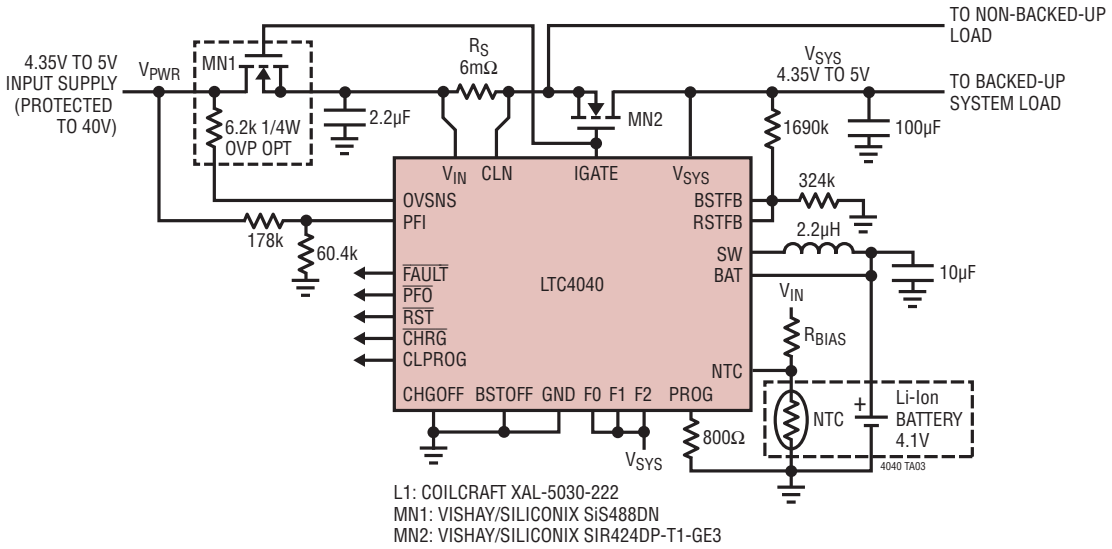
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/15	Added new Applications section, Charge Voltage	18
		Modified Figure 2	22
		Re-assigned new figure numbers	22 – 23
B	08/17	Changed Maximum Boost Duty Cycle maximum limit.	4

TYPICAL APPLICATION

5V Backup Application with OVP Protection and Non-Backed Up Load Option (Charge Current Setting: 2.5A, Input Current Limit Setting: 4A)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3226	2-Cell Supercapacitor Charger with Backup PowerPath™ Controller	1x/2x Multimode Charge Pump Supercapacitor Charger, Internal 2A LDO Backup Supply
LTC3350	High Current Supercapacitor Backup Controller and System Monitor	High Efficiency Synchronous Step-Down CC-CV Charging of 1-4 Series Supercapacitors
LTC3355	20V 1A Buck DC/DC with Integrated SCAP Charger and Backup Regulator	1A Main Buck Regulator, 5A Boost Backup Regulator
LTC4089	USB Power Manager with High Voltage Switching Charger	1.2A Charger for Li-Ion from 6V to 86V Supply
LTC4090	USB Power Manager with 2A High Voltage Bat-Track Buck Regulator	2A Charger with Bat-Track for Li-Ion Batteries
LTC4110	Battery Backup System Manager	Complete Manager for Li-Ion/Polymer, Lead Acid, NiMH/NiCd Batteries and Supercapacitors
LTC4155/LTC4156	Dual Input Power Manager/3.5A Li-Ion Battery Charger with I^2C Control and USB OTG	3.5A Charge Current for Li-Ion/Polymer, LTC4156 for $LiFePO_4$ Batteries
LTC4160	Switching Power Manager with USB On-The-Go and Overvoltage Protection	1.2A Charge Current

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