Data Sheet

LT83205

18V, 5A Step-Down Silent Switcher 3 with Ultra-Low Noise Reference

FEATURES

- **Silent Switcher® 3 Architecture**
  - **Ultra-Low RMS Noise (10Hz to 100kHz): 4µV_{RMS}**
  - **Ultra-Low Spot Noise: 4nV/√Hz at 10kHz**
  - **Ultra-Low EMI Emissions**
- **Ultra-Fast Transient Response**
  - **<1µs Transient Recovery Time**
- **High Efficiency at High Frequency**
  - **Up to 93% Efficiency at 2MHz, 12V_{IN} to 3.3V_{OUT}**
  - **Up to 90% Efficiency at 4MHz, 12V_{IN} to 3.3V_{OUT}**
- **Input Voltage Range: 2.8V to 18V**
- **Output Voltage Range: 0V to (V_{IN} – 0.5V)**
  - **Unity Gain Configuration up to 13V Output**
- **Maximum Continuous Output Current**
  - **LT83203: 3A**
  - **LT83205: 5A**
- **Fast Minimum Switch On-Time: 15ns**
- **Adjustable and Synchronizable: 300kHz to 6MHz**
- **Precision Reference: ±0.7% Over Temperature with Remote Sense**
- Supports *Dynamic Output Voltage Control*
- Pin Selectable Forced Continuous Mode or Pulse-Skipping Mode
- Programmable Power Good
- *Tiny 15-Lead 3mm × 2mm LFCSP* Package
- Pin-to-Pin Compatible Family: LT83201 (1A), LT83203 (3A), LT83205 (5A)

GENERAL DESCRIPTION

The **LT®83203/LT®83205** synchronous step-down regulator is uniquely designed to combine an ultra-low noise reference with Silent Switcher architecture to achieve both high efficiency and excellent wideband noise performance.

The innovative ultra-low noise architecture provides exceptional low-frequency (0.1Hz to 100kHz) output noise performance in a switching regulator. The output voltage can be programmed with a single resistor, resulting in virtually constant output noise independent of output voltage.

Silent Switcher architecture minimizes EMI emissions while delivering high efficiency at high switching frequencies.

The LT83203/LT83205 is ideal for high-current, noise-sensitive applications that benefit from the high efficiency of a synchronous switching regulator.

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision ADCs/DACs
- Low Noise Instrumentation
- General Purpose Power Supply

TYPICAL APPLICATION

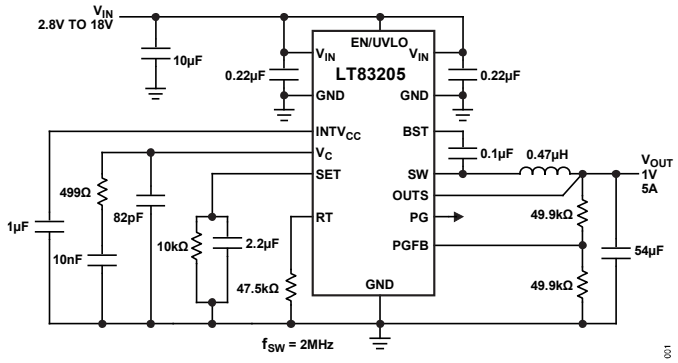

Figure 1. LT83203/LT83205 Application Diagram

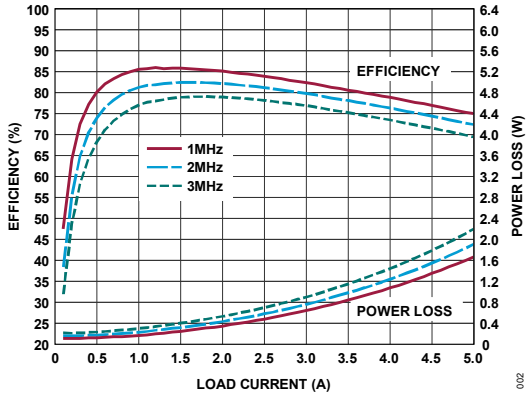

Figure 2. 12V to 1V Efficiency

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REVISION HISTORY

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0	2/25	Initial release	—
A	6/25	Updated the Electrical Characteristics table Updated Pin Descriptions Updated the Related Parts table	4, 5 9 43

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Minimum V_{IN}	V_{IN}	V_{SET} = 1V		2.5	2.8	V
SET Pin Current (I_{SET})	I_{SET}	V_{SET} = V_{OUTS} = 1V, T_A = +25°C	99.85	100	99.15	µA
		V_{SET} = V_{OUTS} = 1V	99.3	100	100.7	
Fast Start-Up Set Pin Current	$I_{FAST\_STARTUP}$	V_{IN} = 12V, V_{SET} = 1V, T_A = +25°C	2.0	2.7	3.2	mA
Start-Up Time Without Fast Start-Up[1, 2]	$t_{STARTUP}$	V_{OUT} = 1V, C_{SET} = 1µF, V_{IN} = 12V, V_{PGFB} = 0.5V		25		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, V_{IN} = 12V, V_{PGFB} = 0.5V		120		
Start-Up Time With Fast Start-Up[1, 2]	$t_{STARTUP}$	V_{OUT} = 1V, C_{SET} = 1µF, V_{IN} = 12V, $R_{PGFB(TOP)}$ = 49.9kΩ, $R_{PGFB(BOT)}$ = 49.9kΩ		1		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, V_{IN} = 12V, $R_{PGFB(TOP)}$ = 49.9kΩ, $R_{PGFB(BOT)}$ = 49.9kΩ		2.5		
Output Noise Spectral Density (10kHz)[1, 3, 4]	$V_{O,NSD(10kHz)}$	V_{IN} = 12V, V_{OUT} = 3.3V, C_{OUT} = 130.4µF, L = 0.47µH, R_{SET} = 33.2kΩ, C_{SET} = 4.7µF, f_{SW} = 6MHz, R_C = 2.7kΩ, C_C = 1nF		4		nV/√Hz
Output RMS Noise (10Hz to 100kHz)[1, 3, 4]	$V_{O,RMS}$	V_{IN} = 12V, V_{OUT} = 3.3V, BW = 10Hz to 100kHz, C_{OUT} = 130.4µF, L = 0.47µH, R_{SET} = 33.2kΩ, C_{SET} = 4.7µF, f_{SW} = 6MHz, R_C = 3.01kΩ, C_C = 560pF		1.93		$µV_{RMS}$
V_{IN} Quiescent Current	I_Q	$V_{EN/UVLO}$ = 2V, Not Switching, T_A = +25°C		2.7	3.6	mA
		$V_{EN/UVLO}$ = 0.2V, Shutdown, T_A = +25°C		40	70	µA
Oscillator Frequency	f_{SW}	R_T = 392kΩ	270	300	330	kHz
		R_T = 47.5kΩ	1.93	2	2.07	MHz
		R_T = 9.76kΩ	5.4	6	6.6	
PGFB Upper Threshold	V_{PGH}	V_{PGFB} Rising	529	537.5	546	mV
PGFB Upper Threshold Hysteresis	V_{PGH_HYS}			10		mV
PGFB Lower Threshold	V_{PGL}	V_{PGFB} Falling	455	462.5	470	mV
PGFB Lower Threshold Hysteresis	V_{PGL_HYS}			10		mV
PGFB Lower Threshold (Start-Up only)	$V_{PGL\_STARTUP}$	V_{PGFB} Rising	479	486.5	495	mV
PGFB Pin Current	I_{PGFB}	$V_{EN/UVLO}$ = 3V, V_{PGFB} = 0.5V		25		nA
PG Leakage	I_{PG_LKG}	V_{PG} = 3.3V, T_A = +25°C	–35		35	nA

(T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PG Pull-Down Resistance	R_{PG}	V_{PG} = 0.5V		380	1200	Ω
SYNC/MODE Threshold	V_{IL}	SYNC/MODE DC and Clock Low Level Voltage	0.7			V
	V_{IH}	SYNC/MODE DC and Clock High Level Voltage			1.5	
OUTS Pin Output Current	I_{OUTS}	V_{OUTS} = 1V, T_A = +25°C	80	160	240	nA
Output Voltage Line Regulation[5]	$\Delta_{VOUT(LINE)}$	V_{IN} = 4V to 18V, T_A = +25°C		0.001	0.01	%/V
Error Amp Offset[5, 6]	$V_{EA, OFFSET}$	V_C = 1.2V, V_{SET} = 3V, V_{IN} = 12V, PNP-Based Input Pair	–2		2	mV
		V_C = 1.2V, V_{SET} = 5V, V_{IN} = 5.7V, NPN-Based Input Pair	–2		2	
Error Amp Transconductance[6]	$g_{m(EA)}$	V_C = 1.2V, V_{SET} = 3V, V_{IN} = 12V, PNP-Based Input Pair, T_A = +25°C	9.5	12	14.5	mS
	$g_{m(EA)}$	V_C = 1.2V, V_{SET} = 5V, V_{IN} = 5.7V, NPN-Based Input Pair, T_A = +25°C	8.3	10.5	12.7	
Error Amp Gain	A_V	V_C = 1.2V, V_{SET} = 1V, V_{IN} = 6V		2800		V/V
V_C Source Current[6]	I_{VC-SRC}	V_C = 1.2V, V_{SET} = 1V, V_{IN} = 12V, PNP-Based Input Pair		330		µA
		V_C = 1.2V, V_{SET} = 5V, V_{IN} = 6V, NPN-Based Input Pair		330		
V_C Sink Current[6]	I_{VC-SNK}	V_C = 1.2V, V_{SET} = 1V, V_{IN} = 12V, PNP-Based Input Pair		330		µA
		V_C = 1.2V, V_{SET} = 5V, V_{IN} = 6V, NPN-Based Input Pair		330		
V_C Pin to Switch Current Gain	G_M	LT83203		5.2		A/V
		LT83205		7.2		
V_C Clamp Voltage	V_{C_CLAMP}			2.2		V
Minimum On-Time	$t_{ON(MIN)}$	I_{LOAD} = 1A		15	20	ns
Minimum Off-Time	$t_{OFF(MIN)}$	I_{LOAD} = 1A		70	90	ns
Top Power N-Channel MOSFET Current Limit	$I_{PEAK-LIMIT}$	LT83203	5.4	6	6.6	A
		LT83205	8.5	10	11	
Bottom Power N-Channel MOSFET Current Limit	$I_{VALLEY-LIMIT}$	LT83203	3.6	4.5	5.4	A
		LT83205	6	7.5	9	
SW Leakage Current	I_{SW_LKG}	V_{IN} = 18V, V_{SW} = 0V, 18V, T_A = +25°C	–10		10	µA
Power MOSFET On-Resistance Main Switch (Top)	R_{DS-ONH}			108		mΩ

(T_J = –40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Power MOSFET On-Resistance Synchronous Switch (Bottom)	R_{DS-ONL}			32		mΩ
Hiccup Timer	t_{HICC}	T_A = +25°C		1.7		ms
SET Pull-Down Resistance	$R_{SET-PULLDOWN}$	V_{SET} = 0.5V		520	850	Ω
EN/UVLO Threshold	V_{ENR}	EN/UVLO Rising	0.70	0.75	0.80	V
EN/UVLO Hysteresis	V_{EN_HYS}			50		mV
EN Delay Timer[9]	t_{EN_DELAY}	V_{IN} = 12V, C_{VCC} = 1µF, R_C = 499, C_C = 10nF, C_{SET} = 2.2µF		1.36		ms
EN/UVLO Input Current	I_{EN}	$V_{EN/UVLO}$ = 2V, T_A = +25°C	–40		40	nA

1 Not subject to production test.

2 The start-up time is defined as the time it takes from the EN/UVLO pin rising above the EN/UVLO threshold to when V_{OUT} has reached 90% of final value.

3 OUTS ties directly to $V_{OUT.}$

4 Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. Use of a SET pin bypass capacitor also increases start-up time.

5 The LT83203/LT83205 is tested in a feedback loop that servos V_C to a specified voltage and measures the resultant V_{OUTS}.

6 The PNP-based input pair is active for the error amplifier as long as V_{IN} is at least 1.4V above V_{SET}. As V_{IN} drops to less than 1.4V above V_{SET}, the part gradually transitions to operating with the NPN-based input pair active.

7 Thermal Resistance (θ) values determined per JEDEC 51-7, 51-12. For information on improving the thermal resistance and for actual temperature measurements of a demo board in typical operating conditions, see the *Applications Information* section.

8 This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature reduces lifetime.

9 EN Delay Timer is the time from EN/UVLO high to the first switching cycle.

ABSOLUTE MAXIMUM RATINGS

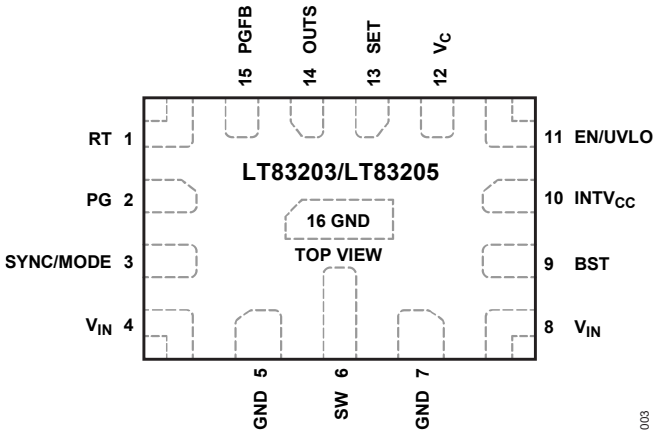
T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, EN/UVLO, PG	–0.3V to 18V
OUTS, SET	–0.3V to 13V
SYNC, PGFB	–0.3V to 6V
Operating Junction Temperature	–40°C to 150°C
Storage Temperature Range	–65°C to 150°C
Peak Package Body Temperature	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



LFCSP PACKAGE
15-Lead (3mm × 2mm × 0.75mm)
JEDEC BOARD θ_{JA} = 50°C/W, $\theta_{JC(TOP)}$ = 67.1°C/W, $\theta_{JC(PAD)}$ = 10.4°C/W
DEMO BOARD θ_{JA} = 33°C/W, Ψ_{JT} = 1.7°C/W
EXPOSED PAD IS GND AND SHOULD BE SOLDERED TO PCB

Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	RT	A resistor is connected between the RT and ground to set the switching frequency.
2	PG	The PG pin is the open-drain output of an internal comparator. PG is pulled low until the PGFB pin is within ±7.5% of 0.5V, and there are no fault conditions. PG is pulled low when EN/UVLO is below 0.75V, $INTV_{CC}$ has fallen too low, or during thermal shutdown. PG is valid when V_{IN} is above 2.7V.
3	SYNC/MODE	For the LT83203/LT83205, this pin programs three different operating modes: 1) Pulse-Skipping Mode: Connect this pin to GND for pulse-skipping mode for improved efficiency at light loads. 2) Forced Continuous Mode (FCM): This mode offers fast transient response and full frequency operation over a wide load range. Connect this pin high to $INTV_{CC}$ (~3.4V) or an external supply >1.5V for FCM. The part also operates in this mode by default if this pin is left floating. 3) Synchronization Mode: Drive this pin with a clock source to synchronize to an external frequency. During synchronization, the part operates in forced continuous mode. The SYNC/MODE pin can be toggled during operation to change the operating mode. Contact the factory for versions of this part that replace the SYNC/MODE pin with a CLKOUT pin. The CLKOUT pin would provide a 50% duty-cycle square wave of the switching frequency, 180° out-of-phase with the internal clock of the part, with a peak-to-peak amplitude of $INTV_{CC}$ to GND.
4, 8	V_{IN}	The V_{IN} pins supply current to the LT83203/LT83205 internal circuitry and to the internal top-side power switch. Two 0402 capacitors of 0.1µF or more should be placed to bypass both V_{IN} pins with the positive terminal of the input capacitor as close as possible to the V_{IN} pins and the negative capacitor terminal as close as possible to the GND pins. V_{IN} pins must also be connected with an additional local bypass capacitor of 4.7µF or more. To provide sufficient headroom for the current reference, V_{IN} must be at least 700mV higher than the required regulation setpoint that is programmed via the SET pin. For example, for the required regulation setpoint of 3.3V, V_{IN} must be at least 3.3V + 700mV = 4V or higher.
5, 7, 16 (Exposed Pad)	GND	Ground. Place the negative terminal of the input capacitor as close to the GND pins as possible. The exposed pads should be soldered to the PCB for good thermal performance. If necessary due to manufacturing limitations, the exposed pad may be left disconnected; however, the performance degrades.
6	SW	The SW pin is the output of the internal power switches. Connect this pin to the inductor. This node must be kept small on the PCB for good performance and low EMI.
9	BST	This pin is used to provide a drive voltage higher than the input voltage to the topside power switch. Place a 0.1µF boost capacitor as close as possible to the IC.
10	$INTV_{CC}$	Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered by this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current is supplied by V_{IN}. Decouple this pin to ground with at least a 1µF low equivalent series resistance (ESR) ceramic capacitor placed close to the IC.
11	EN/UVLO	A voltage at this pin greater than 0.75V enables switching, and a voltage less than 200mV is guaranteed to shut down the internal current bias and sub-regulators. The hysteretic threshold voltage is 0.75V going up and 0.7V going down. Connect to V_{IN} if

		the shutdown feature is not used. An external resistor divider from V_{IN} is used to program a V_{IN} threshold below which the LT83203/LT83205 shuts down.
12	V_C	The V_C pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Connect an RC network from this pin to ground to compensate the control loop.
13	SET	This pin is the non-inverting input of the error amplifier and the regulation setpoint for the LT83203/LT83205. SET sources a precision 100µA current that flows through an external resistor connected between the SET and GND. The LT83203/LT83205's output voltage is determined by $V_{SET} = I_{SET} \times R_{SET}$ when used in the default unity-gain configuration. The SET pin voltage range is from 0V to 13V. For applications with output voltages above 13V, see the *Output Voltages Above 13V* section. A capacitor should be added from SET to GND for the best noise performance. Increasing this capacitance further improves noise at the expense of increased start-up time. See the *SET Pin Capacitor: Noise and Soft-Start* section for important information on how to select this capacitor. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. This pin is pulled to ground with a 520Ω MOSFET ($R_{SET-PULLDOWN}$) during shutdown and fault conditions.
14	OUTS	Output Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load.
15	PGFB	Power Good Feedback. The PG pin pulls low if PGFB increases above 537.5mV or decreases below 462.5mV. Connecting an external resistor divider between V_{OUT}, PGFB, and GND sets the programmable power good threshold with the following transfer function: 0.5V (±7.5%) × (1 + $R_{PGFB(TOP)}/R_{PGFB(BOT)}$). As discussed in the *Applications Information* section, PGFB also activates the fast start-up circuitry. The PGFB pin must be connected to $INTV_{CC}$ or 0.5V if power good and fast start-up functionalities are not needed.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

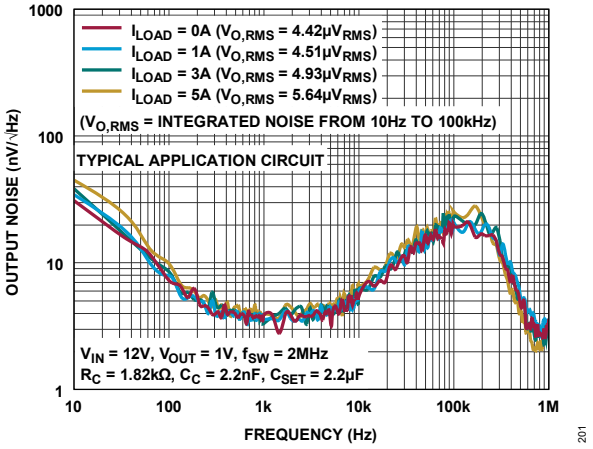


Figure 4. Noise Spectral Density vs. Load

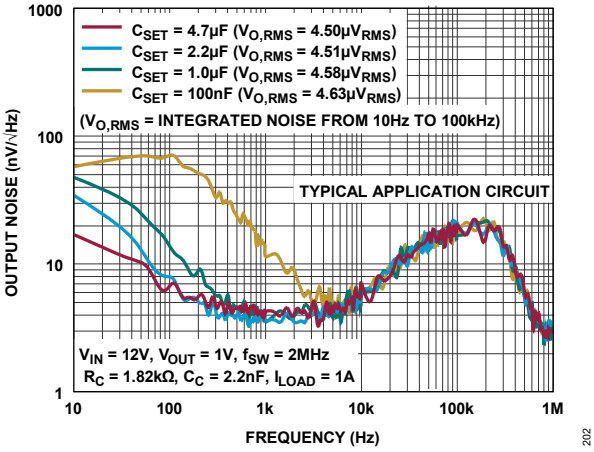


Figure 5. Noise Spectral Density vs. C_{SET}

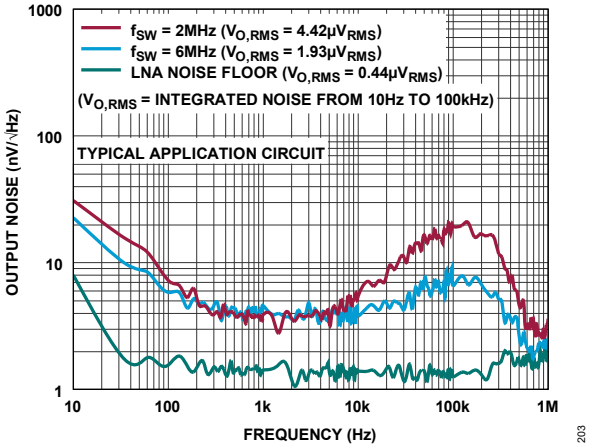


Figure 6. Noise Spectral Density vs. Switching Frequency

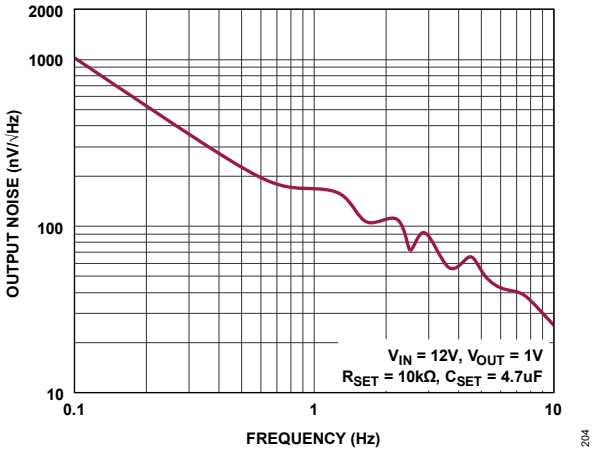


Figure 7. Noise Spectral Density (0.1Hz to 10Hz)

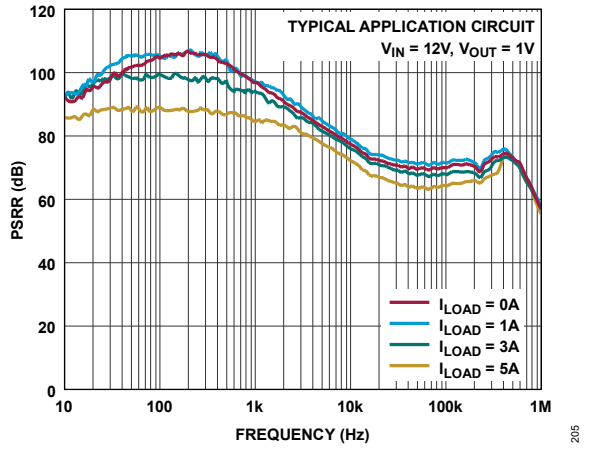


Figure 8. Power-Supply Ripple Rejection

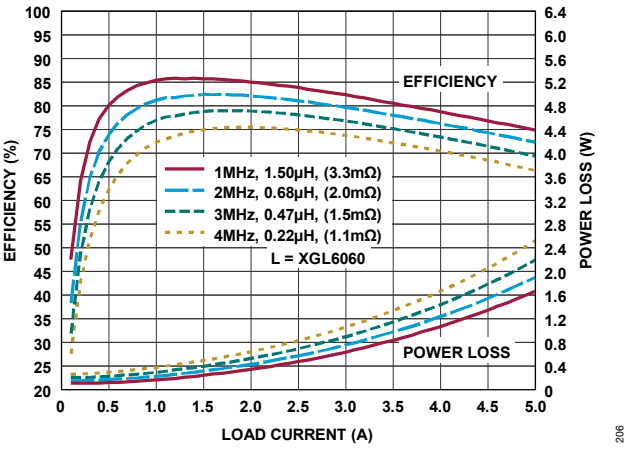


Figure 9. 12V_{IN} to 1V_{OUT} Efficiency

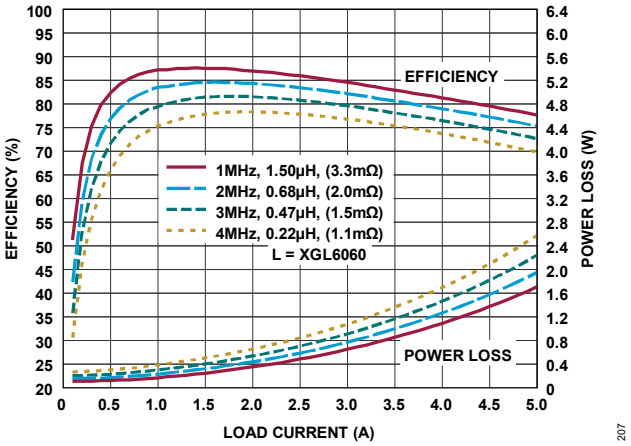


Figure 10. $12V_{IN}$ to $1.2V_{OUT}$ Efficiency

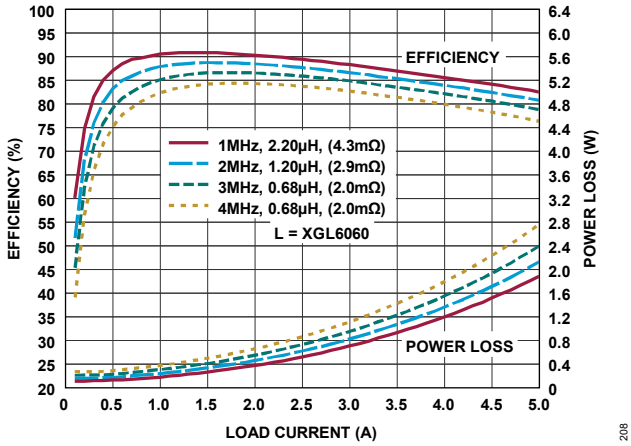


Figure 11. $12V_{IN}$ to $1.8V_{OUT}$ Efficiency

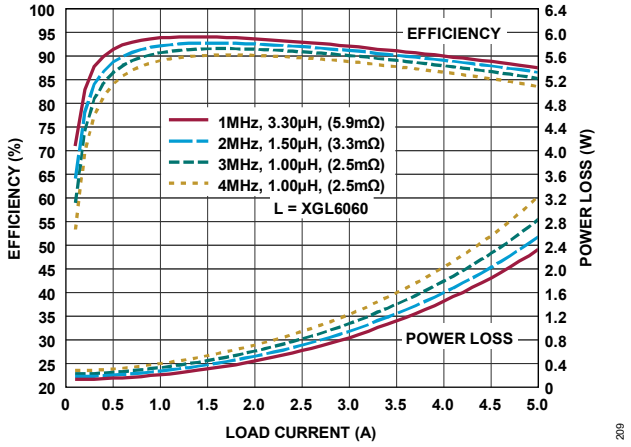


Figure 12. $12V_{IN}$ to $3.3V_{OUT}$ Efficiency

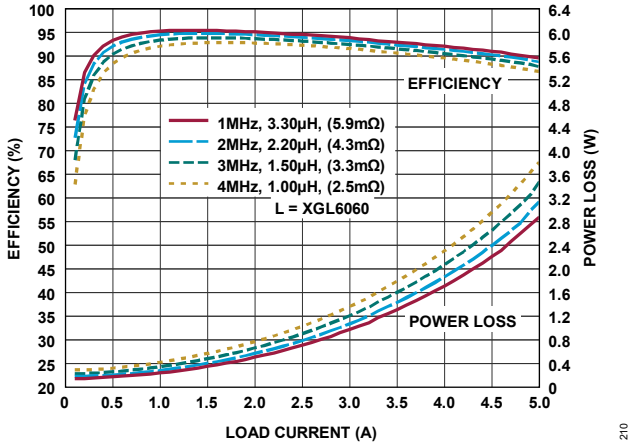


Figure 13. $12V_{IN}$ to $5V_{OUT}$ Efficiency

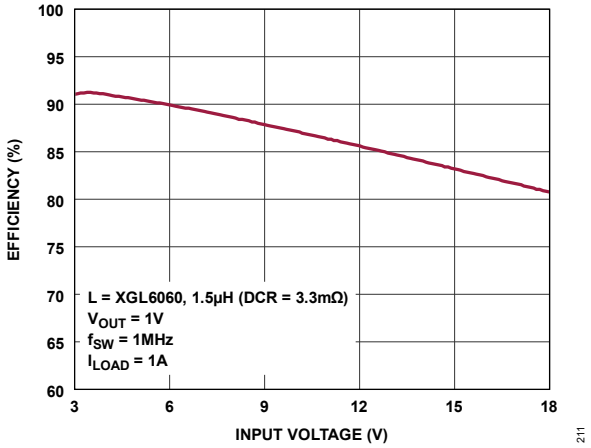


Figure 14. Efficiency vs. V_{IN}

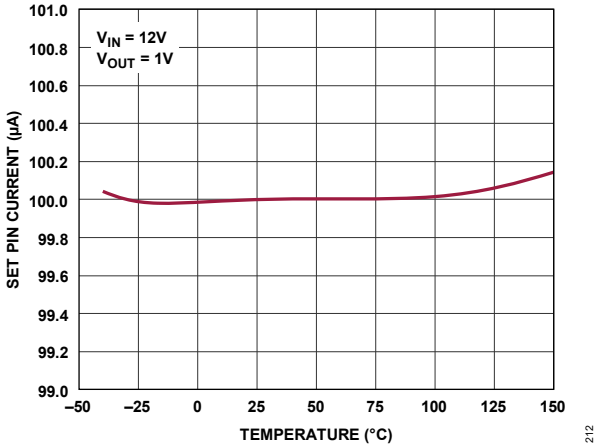


Figure 15. SET Pin Current vs. Temperature

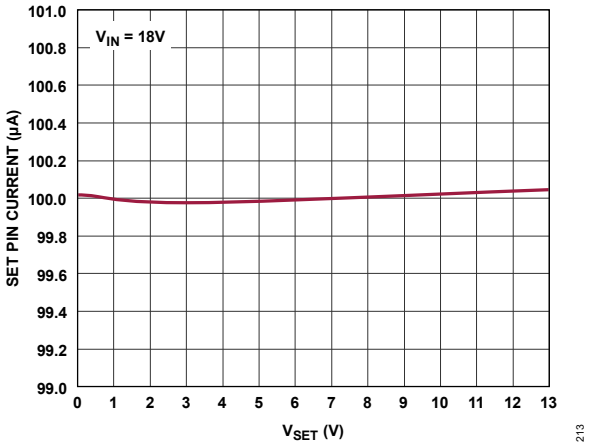


Figure 16. SET Pin Current vs. V_{SET}

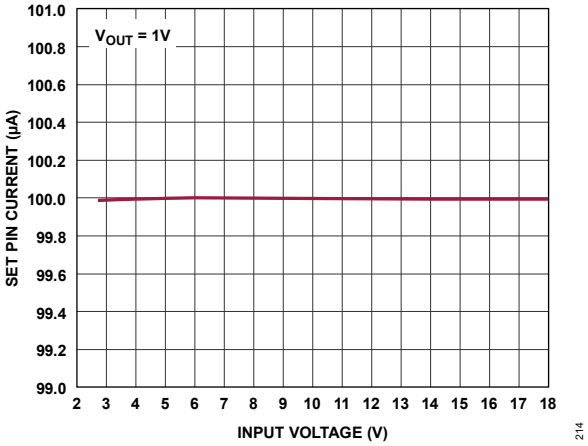


Figure 17. SET Pin Current vs. Input Voltage

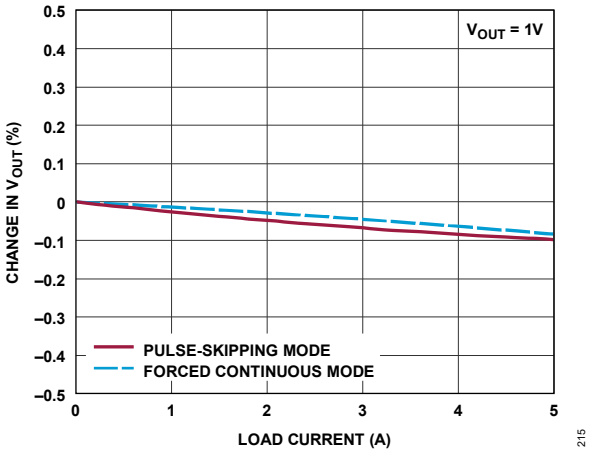


Figure 18. Load Regulation

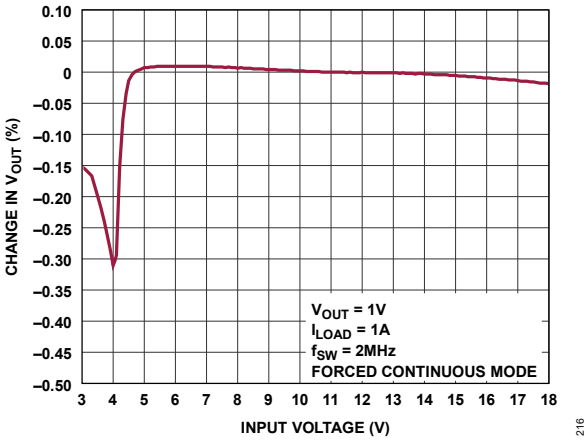


Figure 19. Line Regulation

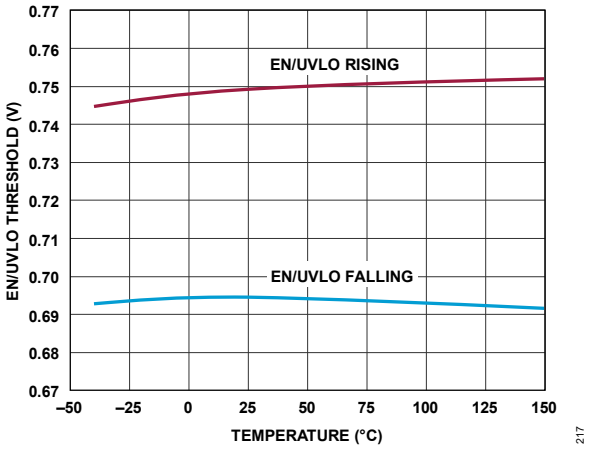


Figure 20. EN/UVLO Pin Thresholds

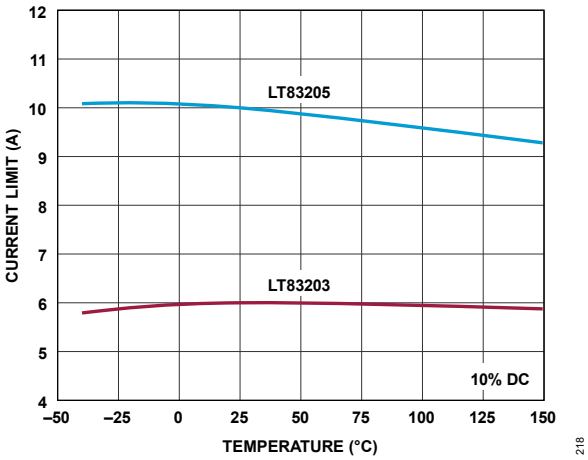


Figure 21. Top MOSFET Current Limit

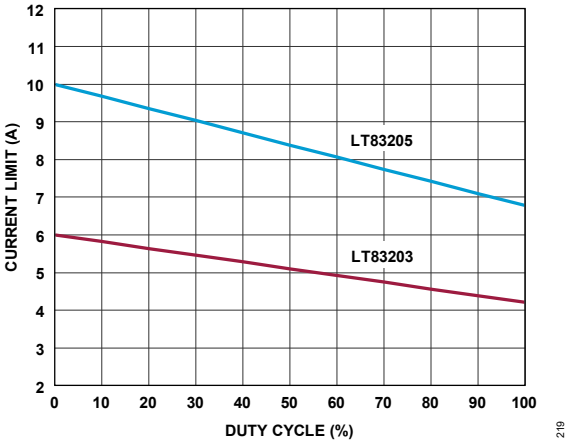


Figure 22. Top MOSFET Current Limit vs. Duty Cycle

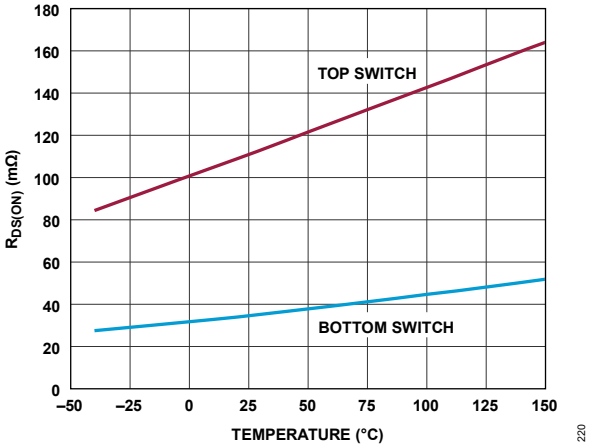


Figure 23. Switch $R_{DS(ON)}$ vs. Temperature

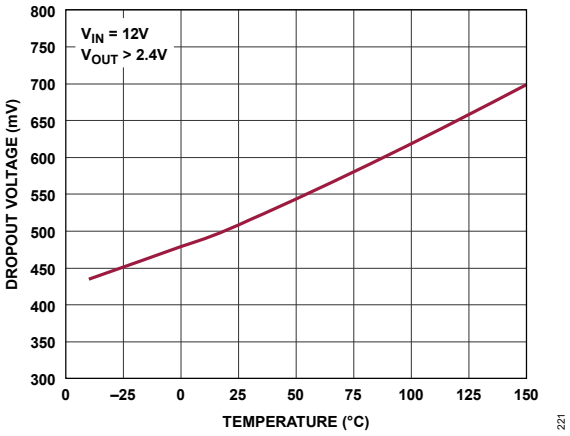


Figure 24. Dropout Voltage vs. Temperature

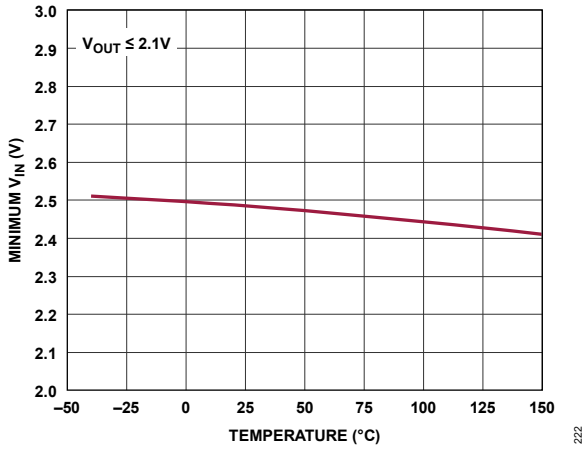


Figure 25. Minimum V_{IN} vs. Temperature

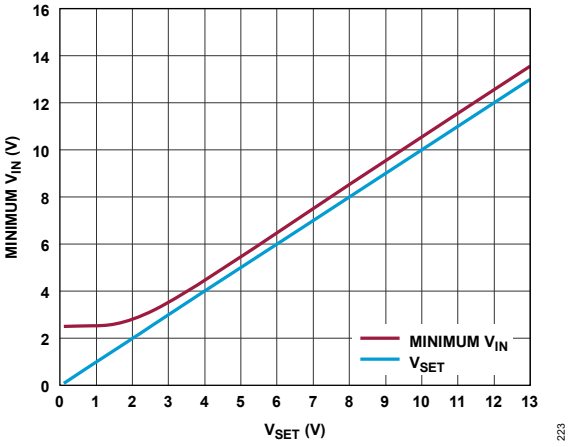


Figure 26. Minimum V_{IN} as a Function of V_{SET}

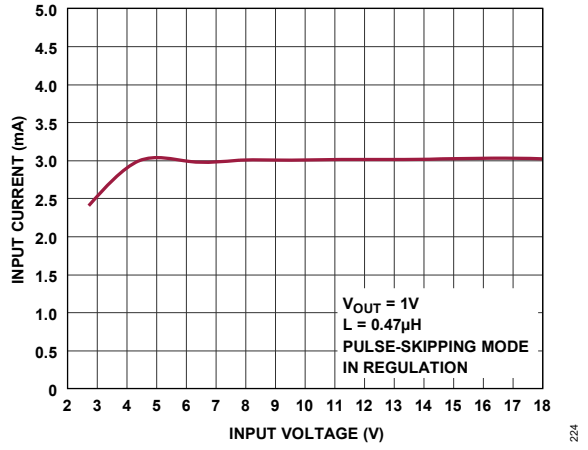


Figure 27. No-Load Supply Current

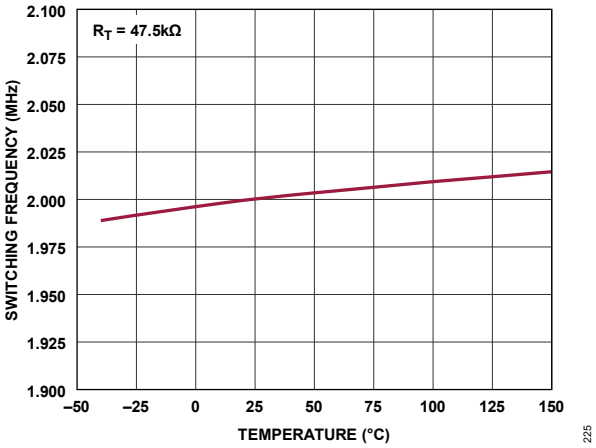


Figure 28. Switching Frequency vs. Temperature

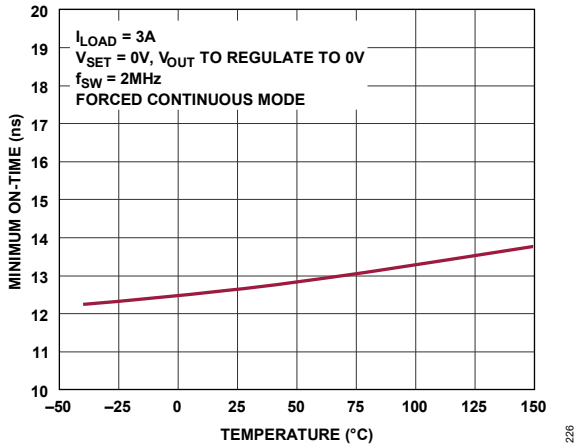


Figure 29. Minimum On-Time vs. Temperature

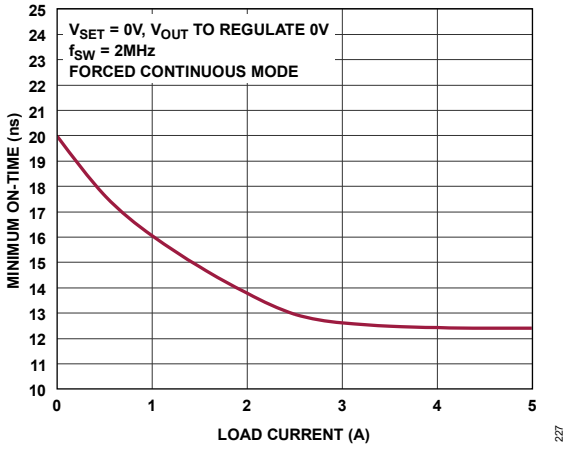


Figure 30. Minimum On-Time vs. Load

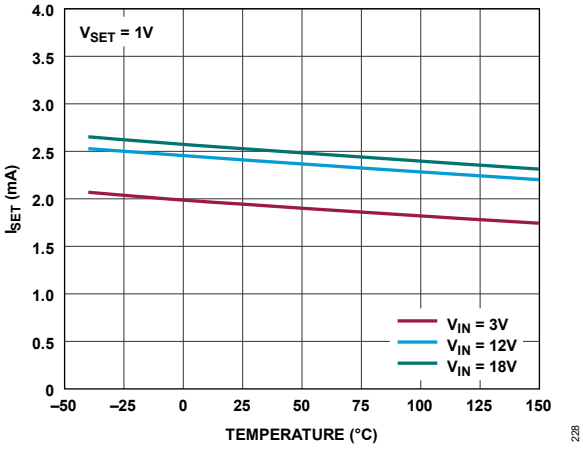


Figure 31. I_{SET} During Start-Up with Fast Start-Up Enabled (vs. Temperature)

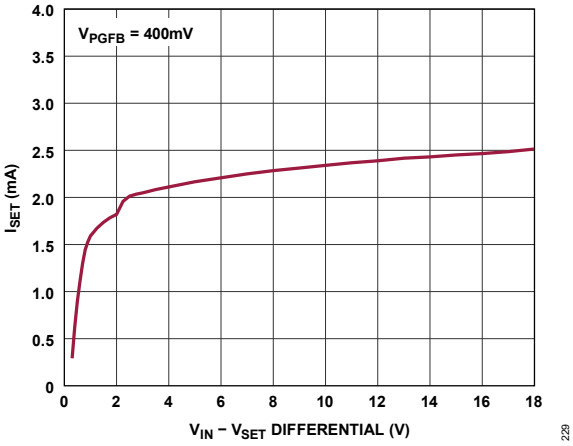


Figure 32. I_{SET} During Start-Up with Fast Start-Up Enabled (vs. V_{IN} – V_{SET} Differential)

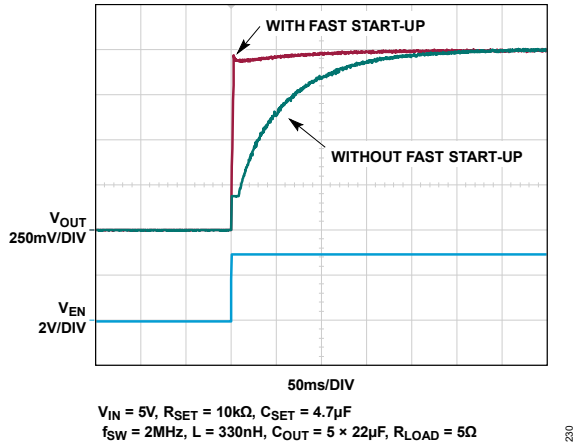


Figure 33. Start-Up Time with and without Fast Start-Up Circuitry for Large C_{SET}

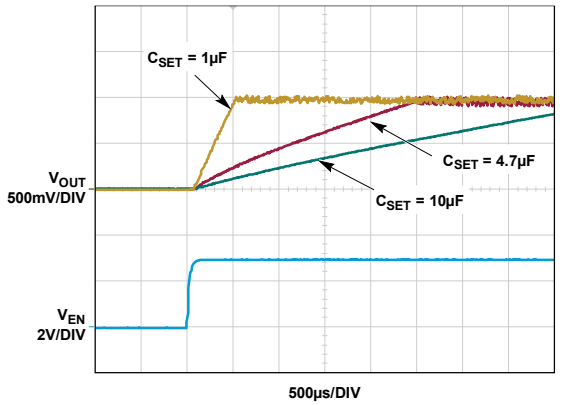


Figure 34. Soft-Start Waveforms

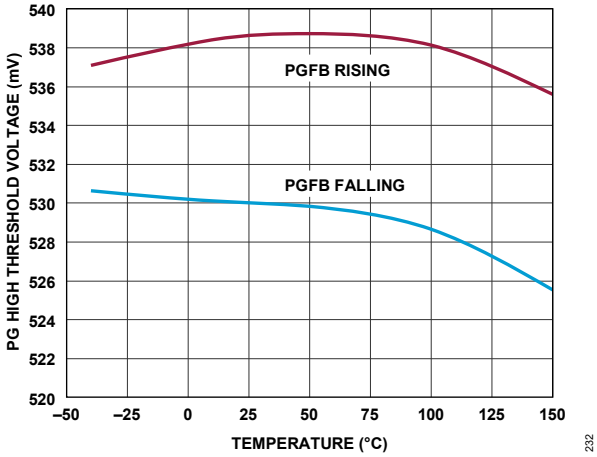


Figure 35. Power-Good High Thresholds

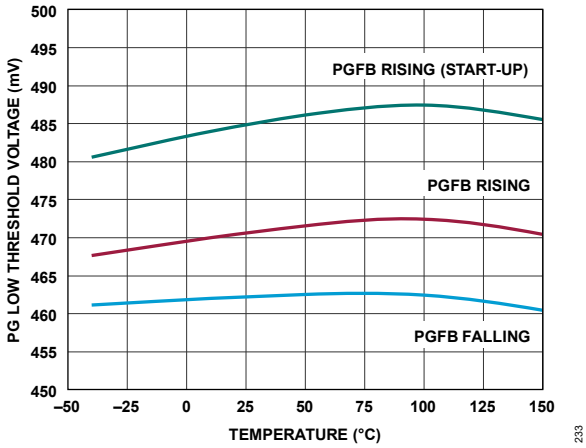


Figure 36. Power-Good Low Thresholds

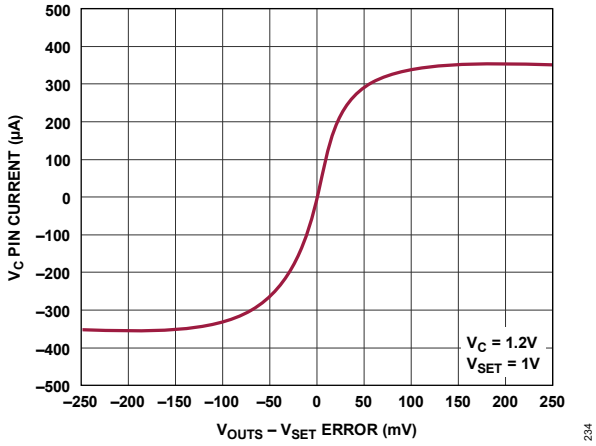


Figure 37. Error Amp Output Current

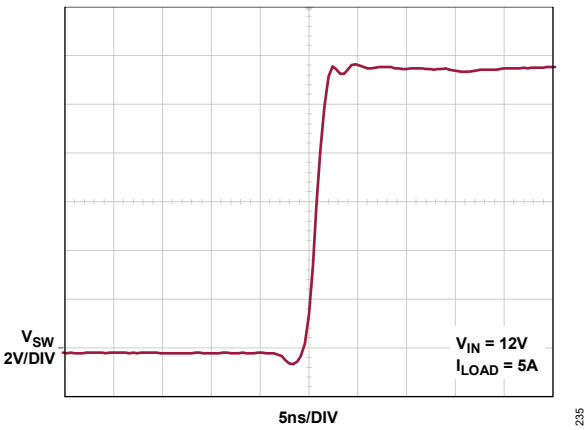


Figure 38. Switch Rising Edge

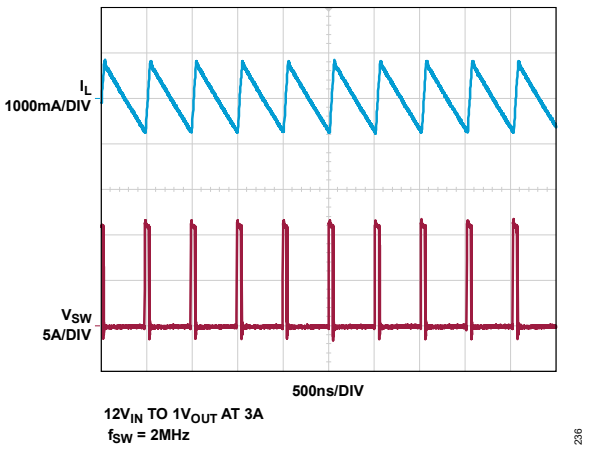


Figure 39. Switching Waveforms, Full Frequency Continuous Operation

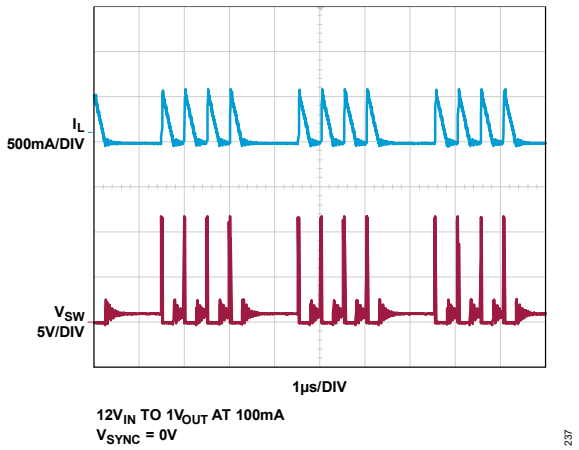


Figure 40. Switching Waveforms, Pulse-Skipping Operation

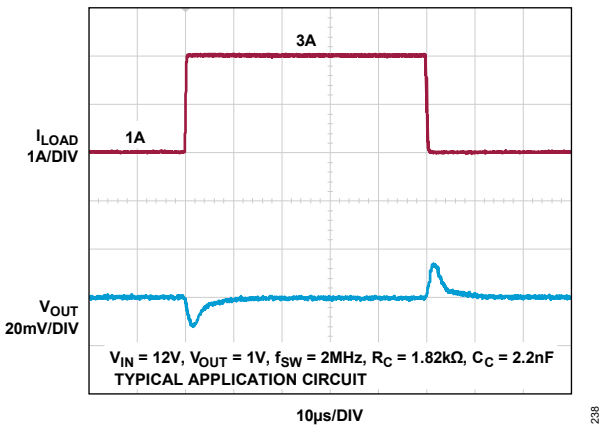


Figure 41. Transient Response: Load Current Stepped from 1A to 3A

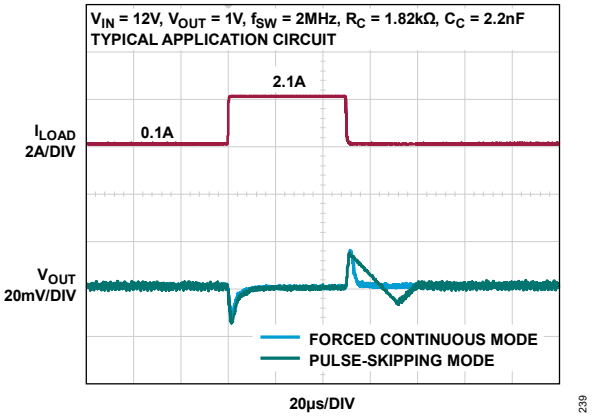


Figure 42. Transient Response: Load Current Stepped from 0.1A to 2.1A

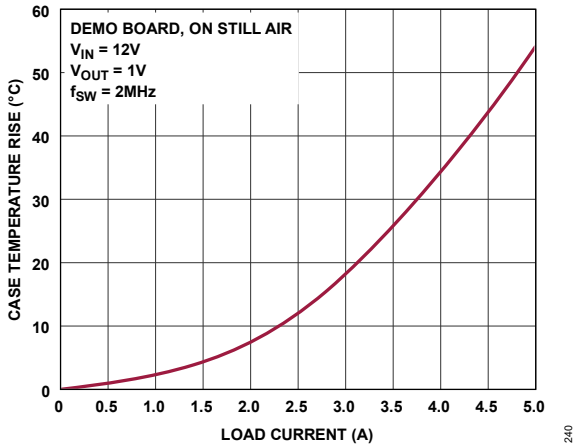


Figure 43. LT83203/LT83205 Case Temperature Rise

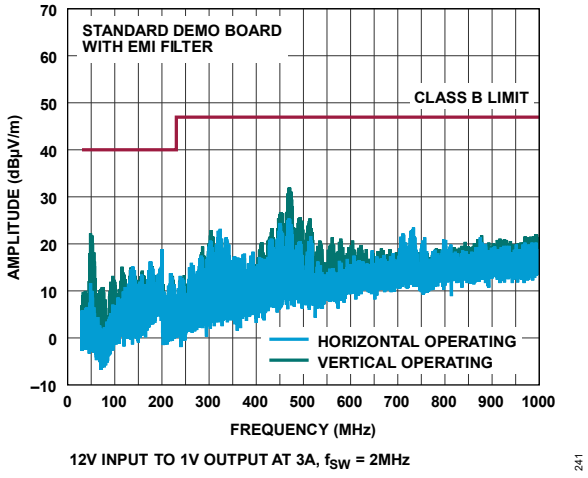


Figure 44. LT83203 Radiated EMI Performance (CISPR32 Radiated Emission Test with Class B Limits)

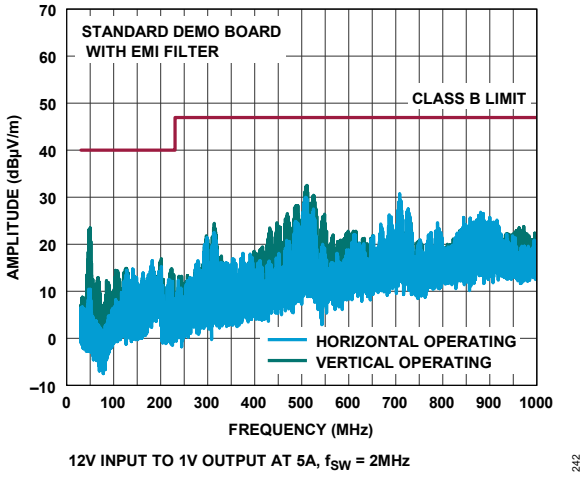


Figure 45. LT83205 Radiated EMI Performance (CISPR32 Radiated Emission Test with Class B Limits)

BLOCK DIAGRAM

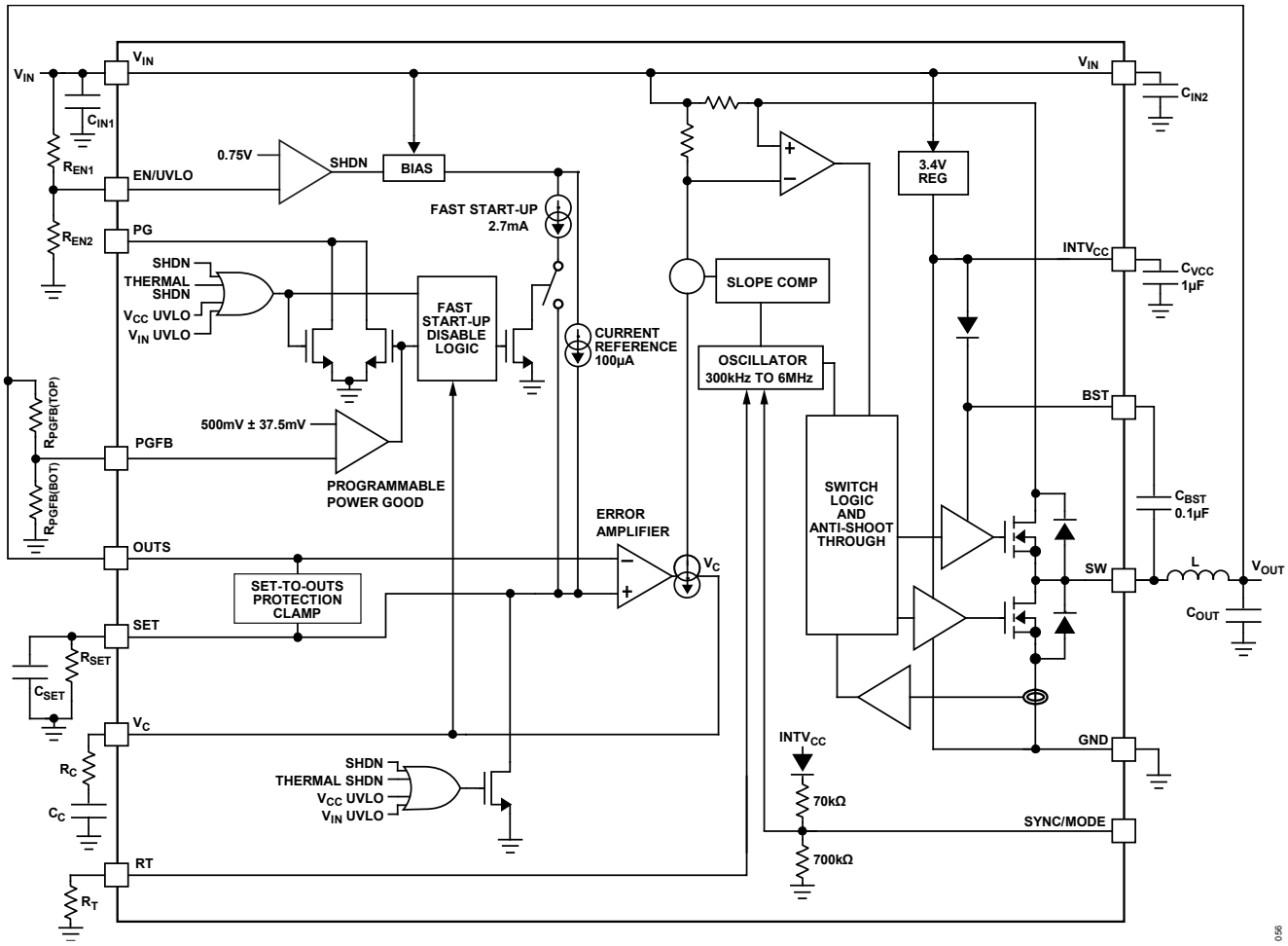


Figure 46. Block Diagram

THEORY OF OPERATION

The LT83203/LT83205 is a constant-frequency, current-mode, monolithic step-down regulator, operating using a current reference-based architecture to allow the employment of unity gain to minimize output noise across all output voltages. An oscillator, with the frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. The current in the inductor increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the V_C pin. The error amplifier servos the V_C node by comparing the voltage on the OUTS pin to the reference voltage on the SET pin, which is set by the user with a resistor from the SET pin to the ground. When the load current increases, it causes a reduction in the OUTS voltage relative to the reference, leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or the inductor current falls to zero (only in the pulse-skipping mode). If overload conditions result in more than 4.5A (LT83203)/7.5A (LT83205) flowing through the bottom switch, the next clock cycle is delayed until the switch current returns to a safe level. If an overload condition is detected and persists for longer than 1.7ms (t_{HICC}), the part enters hiccup mode and suspends switching for ~12ms ($7*t_{HICC}$) before soft-start is attempted again.

The LT83203/LT83205 features third-generation Silent Switcher technology, which combines an ultra-low noise current reference with previous generation Silent Switcher technology. The output voltage can be programmed with a single resistor, providing unity-gain operation over the output range, resulting in virtually constant ultra-low output noise independent of the output voltage.

If the EN/UVLO pin is below 0.2V, the LT83203/LT83205 shuts down and draws 40µA from the input. When the EN/UVLO pin rises above 0.75V, the switching regulator becomes active.

To improve efficiency at light loads, the LT83203/LT83205 can operate in pulse-skipping mode in light load situations. The SYNC/MODE pin is connected to ground to use pulse-skipping operation and connected to $INTV_{CC}$ or to a voltage higher than 1.5V or floated to use FCM. If a clock is applied to the SYNC pin, the part synchronizes to an external clock frequency and operates in FCM.

The LT83203/LT83205 can operate in FCM for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed. In this mode, the LT83203/LT83205 can sink current from the output and return this charge to the input, improving load-step transient response.

The V_C pin allows the loop compensation of the switching regulator to be optimized based on the programmed switching frequency, allowing for a fast transient response.

APPLICATIONS INFORMATION

Low Frequency Output Noise

The LT83203/LT83205 offers many advantages with respect to noise performance in the low-frequency range (<100kHz). Conventional step-down regulators have several sources of low frequency noise. The most critical noise sources for a conventional regulator are its reference, error amplifier, noise from the resistor divider network used for setting output voltage, and the noise gain created by this resistor divider.

Unlike most step-down regulators, the LT83203/LT83205 does not use a voltage reference; instead, it uses a 100µA current reference. One problem that conventional step-down regulators face is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the current reference architecture employed by the LT83203/LT83205 allows unity-gain operation to avoid gaining up the noise from the reference to the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise is independent of the programmed output voltage. The resultant output noise is typically 4nV/√Hz at 10kHz.

With the previously mentioned noise sources operating at such low noise levels, other noise sources become non-negligible contributors to the output noise. Choosing a compensation network that achieves good transient performance with a good phase margin ensures optimal noise performance. The Applications Information section on *Frequency Compensation* provides guidelines on how to choose appropriate compensation.

Filtering Switching Ripple and High Frequency Noise

The LT83203/LT83205 is a switching regulator and also have the typical artifacts of a switching regulator at the output, namely a ripple at the fundamental switching frequency as well as high-frequency spikes associated with the fast switching edges. While the output capacitor absorbs some of these spikes, the capacitor ESL limits its ability to do so at high frequencies. Additional filtering at the output in the form of feedthrough capacitors, ferrite beads, or an additional LC filter stage is recommended to eliminate these high-frequency spikes and significantly reduce switching ripple.

If additional switching ripple reduction is required while retaining fast transient response, ferrite beads, a PCB trace, or feedthrough capacitors may be used. For feedthrough capacitors, ensure sufficient feedthrough capacitors are paralleled to carry the required load current. *Figure 47* shows an example where two 3A-rated feedthrough capacitors are used for additional switching ripple suppression to deliver up to 6A at the output. In practice, this is limited to 3A for the LT83203 and 5A for the LT83205.

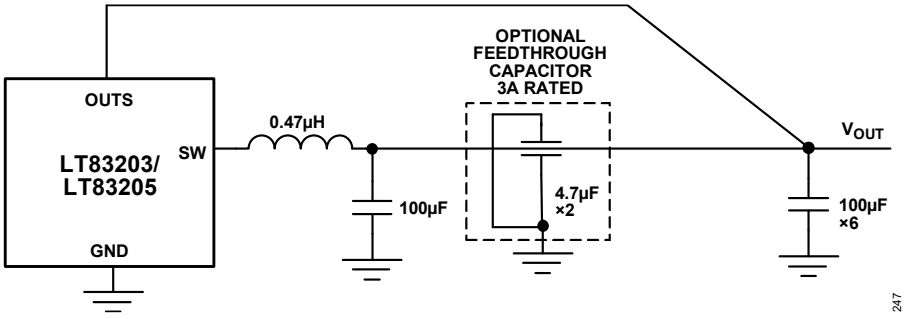


Figure 47. Additional Output Ripple Filtering Using Feedthrough Capacitors

If transient performance is not critical, other passive filter solutions can be realized using a physical inductor as a larger second L and additional output capacitance for the second C, as shown in *Figure 48*.

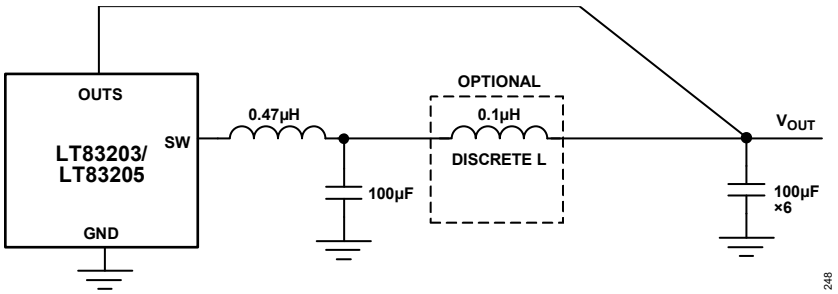


Figure 48. Additional Output Ripple Filtering Using a Second LC Filter

When designing an additional filter for further attenuation of the switching ripple, it is highly recommended to design with LTpowerCAD® to ensure that the design is stable with a good phase margin and provides sufficient attenuation at the switching frequency of interest.

The Silent Switcher 3 architecture makes it possible to achieve excellent noise performance from low to high frequencies at the output of the LT83203/LT83205 while utilizing only passive filtering.

PCB Layout Recommendations

The LT83203/LT83205 is specifically designed to minimize low-frequency (10Hz to 100kHz) noise and EMI emissions and maximize efficiency when switching at high frequencies. For optimal performance, the LT83203/LT83205 can use multiple V_{IN} bypass capacitors.

Two small capacitors are placed as close as possible to the LT83203/LT83205 V_{IN} pins, and the third capacitor with a larger value, 4.7µF or higher, should be placed near one of these two capacitors. For a recommended PCB layout, see *Figure 49*.

For more details and PCB design files, refer to the LT83203/LT83205 demo board manual. Note that large, switched currents flow in the LT83203/LT83205 V_{IN} and GND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and GND pins. Capacitors with small case sizes, such as 0402 or 0603, are optimal due to their low parasitic inductance. Special care must be taken with the input capacitors to ensure they have a low-impedance return path to the IC ground. This is achieved by placing several grounds through the GND side of the input capacitors such that the ground plane is utilized to full advantage. This should be an unbroken ground plane with a solid connection to the exposed pad of the IC, as shown in *Figure 49*.

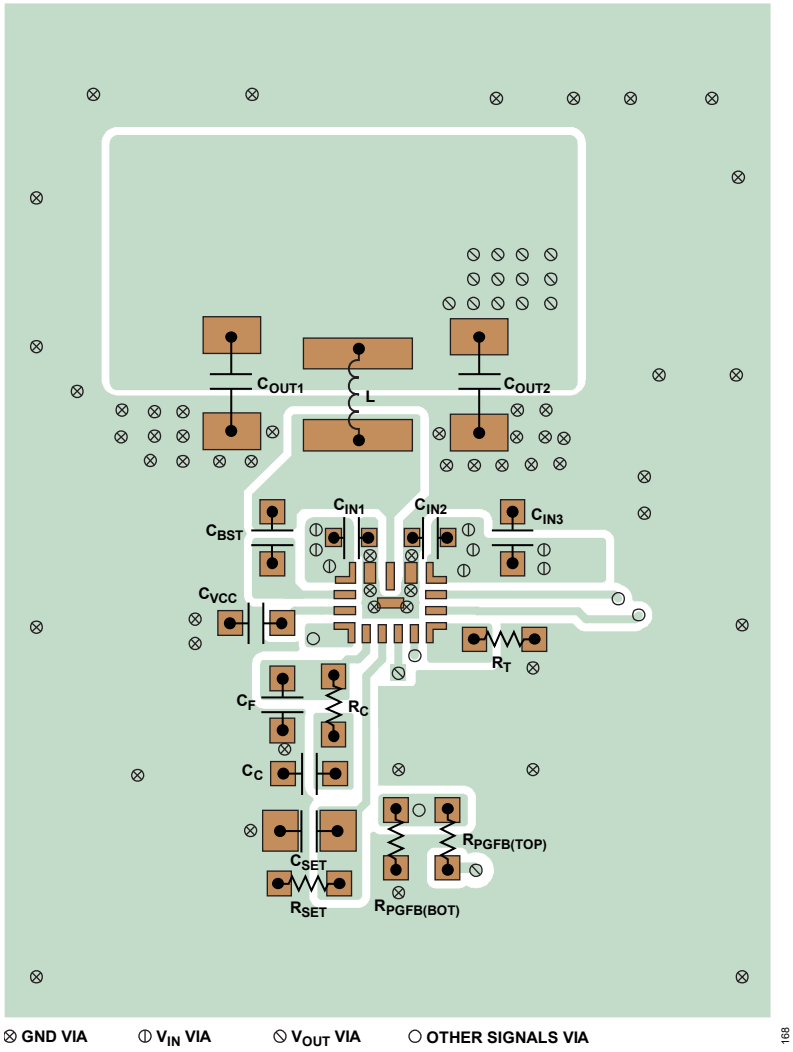


Figure 49. LT83203/LT83205 Suggested Layout

The main inductor and output capacitors should be placed on the same side of the circuit board as the IC, and their connections should be made on that layer. The impedance of the output bulk capacitor's return path to IC ground should also be minimized through the generous use of ground vias. Care with ground layout prevents switching currents from the input capacitors coupling to the output through the ground, which can introduce unintentional perturbations onto the OUTS pin. A small capacitor may also be placed locally to decouple the OUTS pin if needed.

An additional LC filter, if used, can be placed on the other side of the circuit board for optimal EMI performance, though this is not required. Place a local unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BST nodes should be as small as possible. Finally, keep the OUTS, PGFB, and RT nodes small so that the ground traces shield them from the SW and BST nodes. The OUTS, PGFB, and RT traces should not pass underneath the main inductor and should also be kept away from the inductor vias.

The exposed pad on the bottom of the package should be soldered to the PCB to reduce thermal resistance to ambient. To keep thermal resistance low, extend the ground plane from the GND as much as possible and add thermal vias to additional ground planes within the circuit board and on the bottom side.

The current reference architecture of the LT83203/LT83205 allows remote sense of the negative terminals of the load in addition to the positive terminal. Note the via on the ground side of the R_{SET} and C_{SET} going to the ground side of the C_{OUT}, which can be configured for remote sense of the negative terminal of a load placed further away. For more information on implementing remote sense for the LT83203/LT83205, see the *Output Sensing and Stability* section.

Forced Continuous Mode (FCM)

The LT83203/LT83205 can operate in FCM for fast transient response and full-frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is allowed at light loads or under large transient conditions. In this mode, the LT83203/LT83205 can sink current from the output and return this charge to the input, improving load-step transient response (for a comparison of pulse-skipping mode and FCM, see *Figure 50*). At light loads, FCM operation is less efficient than pulse-skipping operation, but it may be useful in applications where it is necessary to keep switching harmonics out of the signal band. FCM must be used if the output is required to sink current. To enable FCM, connect the pin to $INTV_{CC}$ or > 1.5V, or float the pin.

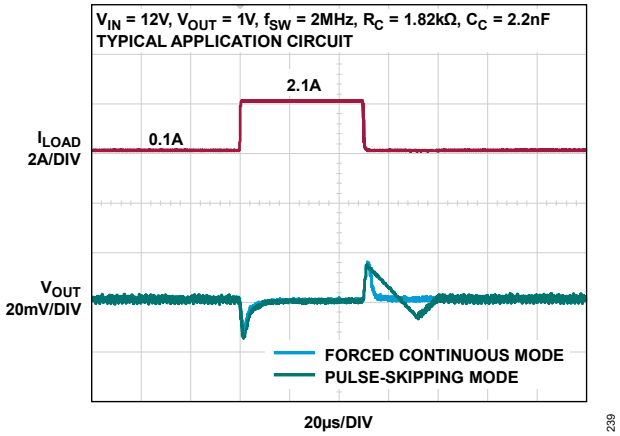


Figure 50. Load Step Transient Response with and without FCM

FCM is disabled under V_{IN} overvoltage conditions (V_{IN} pin is held above 18V), if V_{OUT} is too high (PGFB pin is held greater than 537.5mV) and during start-up until the voltage on V_{OUT} has charged up to ~97.5% of its final value (as indicated when the PGFB pin rises to above 486.5mV). For the latter two conditions, it is assumed the PGFB pin is connected to the output voltage through an appropriate resistor divider. When FCM is disabled in these ways, negative inductor current is not allowed, and the LT83203/LT83205 operates in pulse-skipping mode.

Pulse-Skipping Mode

When not operating in FCM, the LT83203/LT83205 operates in pulse-skipping mode. In this mode, the oscillator operates continuously, and all switching cycles are aligned to the clock. The negative inductor current is not allowed in this mode; therefore, at light loads, the LT83203/LT83205 may be operating in discontinuous mode. Additionally, in pulse-skipping mode, the LT83203/LT83205 may also skip switching cycles at very light loads for improved efficiency or at very high duty cycles to achieve better dropout. To enable pulse-skipping mode, connect the SYNC/MODE pin to GND.

Synchronization

To synchronize the LT83203/LT83205 oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys below 0.7V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

While synchronized to an external clock, the part runs in FCM to maintain regulation. The LT83203/LT83205 may be synchronized over a 300kHz to 6MHz range. The R_T resistor should be chosen to set the LT83203/LT83205 switching frequency to be equal to the synchronization input. The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage.

Setting the Switching Frequency

The LT83203/LT83205 uses a constant-frequency PWM architecture that is programmed to switch from 300kHz to 6MHz by using a resistor connected from the RT pin to GND.

The R_T resistor required for the desired switching frequency is calculated by Equation 1.

$$R_T = \frac{115.8}{f_{SW}} - 10.4 \qquad (1)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz. *Table 4* shows the necessary R_T value for the desired switching frequency.

Table 4. SW Frequency vs. R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47.5
2.5	35.7
3	28.7
3.5	23.2
4	18.0
6	9.76

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high-frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated by Equation 2.

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)} \left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (2)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.38V and ~0.11V, respectively, at maximum load), and $t_{ON(MIN)}$ is the minimum top switch on-time (see the *Electrical Characteristics* table). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 18V regardless of the R_T value; however, the LT83203/LT83205 reduces switching frequency as necessary to maintain control of the inductor current to assure safe operation.

In pulse-skipping mode, the LT83203/LT83205 is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, provided there is sufficient headroom (~0.7V) between V_{IN} and SET for the current reference circuit to function correctly. In this mode, the LT83203/LT83205 skips switch cycles, resulting in a lower switching frequency than programmed by R_T. The LT83203/LT83205 switches as frequently as necessary to keep the boost capacitor refreshed, with a minimum switching frequency of approximately 80kHz. Note that higher switching frequencies increase the minimum input voltage below which cycles are dropped to achieve a higher duty cycle.

In FCM, the LT83203/LT83205 does not skip cycles, and so the maximum duty cycle is limited by the minimum off-time and chosen switching frequency. For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios and thus must operate in FCM, use Equation 3 to set the switching frequency.

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \times t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (3)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.32V/0.54V and ~0.10V/0.16V, respectively, at maximum loads), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time.

Inductor Selection and Maximum Output Current

The LT83203/LT83205 is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions, the LT83203/LT83205 safely tolerates operation with a saturated inductor through the use of a high-speed peak-current mode architecture.

A good starting point for the inductor value is given by Equation 4.

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}}\right) \times 0.8 \quad (4)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.11V/0.16V), and L is the inductor value in µH.

To avoid overheating and poor efficiency, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application.

In addition, the saturation current rating (typically labeled I_{SAT}) of the inductor must be higher than the load current plus ½ of the inductor ripple current. See Equation 5.

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (5)$$

where ΔI_L is the inductor ripple current as calculated in Equation 7 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 3A output should use an inductor with an RMS rating of greater than 3A and an I_{SAT} of greater than 4A. During long-duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 32mΩ, and the core material should be intended for high-frequency applications.

The LT83203/LT83205 limits the peak switch current to protect the switches and the system from overload faults.

The top switch current limit ($I_{PEAK-LIMIT}$) is 6A (LT83203)/10A (LT83205) at low duty cycles and decreases linearly to 4.5A (LT83203)/7.5A (LT83205) at duty cycle = 80%.

The inductor value must be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the top switch current limit ($I_{PEAK-LIMIT}$) and the ripple current (see Equation 6).

$$I_{OUT(MAX)} = I_{PEAK-LIMIT} - \frac{\Delta I_L}{2} \quad (6)$$

The peak-to-peak ripple current in the inductor can be calculated using Equation 7.

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (7)$$

where f_{SW} is the switching frequency of the LT83203/LT83205, and L is the value of the inductor. Therefore, the maximum output current that the LT83203/LT83205 delivers depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger-value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower, and the LT83203/LT83205 may operate with a higher ripple current. This allows the use of a physically smaller inductor or one with a lower DCR, resulting in higher efficiency. Be aware that low inductance may result in discontinuous operation in pulse-skipping mode, which further reduces the maximum load current.

For more information about maximum output current and discontinuous operation, refer to the Application Note 44: *LT1074/LT1076 Design Manual*.

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. For more information, refer to the Application Note 19*: LT1070 Design Manual*. Equation 8 calculates that minimum inductance.

$$L_{MIN} = \frac{V_{IN}(2 \times DC - 1)}{1.1 \times f_{SW}} \quad (8)$$

where DC is the duty cycle ratio (V_{OUT}/V_{IN}), and f_{SW} is the switching frequency.

Overcurrent Protection (OCP) and Hiccup Mode

The LT83203/LT83205 protects against overload and output short-circuit conditions by cycle-by-cycle current limiting both the current through the top and bottom switches.

Current is sensed in the top switch when it is on. The top switch is immediately turned off when the top switch current limit ($I_{PEAK-LIMIT}$) is detected, and the bottom switch is turned on. Current is also sensed in the bottom switch when it is on, and the top switch is not allowed to turn back on unless the current through the bottom switch has dropped below the bottom switch current limit ($I_{VALLEY-LIMIT}$). This effectively stretches the switching period and lowers the frequency for as long as the protection is required, as the top switch will not be allowed to turn on at the oscillator clock edge until the bottom switch current drops below $I_{VALLEY-LIMIT}$. This limits the average current during an output short-circuit condition to the RMS average of $I_{PEAK-LIMIT}$ and $I_{VALLEY-LIMIT}$.

The LT83203/LT83205 recognizes an overcurrent condition when either $I_{PEAK-LIMIT}$ or $I_{VALLEY-LIMIT}$ is triggered, and the V_C voltage rails at its maximum value of V_{C_CLAMP}. Once an overcurrent condition is detected, an internal timer is started. If the overcurrent condition persists for longer than approximately 1.7ms (t_{HICC}), then the part enters hiccup mode and suspends switching for ~12ms ($7*t_{HICC}$) before soft start is attempted again. Hiccup mode ensures low average power dissipation under output short-circuit conditions both within the device and the inductor. During this period of suspended switching in hiccup mode, the V_C pin, PG pin, and SET pin are pulled low internally to ensure the part soft-starts correctly when it next attempts to switch again.

Input Capacitors

The V_{IN} of the LT83203/LT83205 should be bypassed with at least three ceramic capacitors for the best performance. Two small ceramic capacitors can be placed close to the part (C_{OPT1}, C_{OPT2}). These capacitors should be 0402 in size.

Note that a larger input capacitance is required when a lower switching frequency is used. If the input power source has a high impedance or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low-performance electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LT83203/LT83205 is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT83203/LT83205's voltage rating. This situation is easily avoided; for more information, refer to the Application Note 88: *Ceramic Input Capacitors Can Cause Overvoltage Transients*.

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT83203/LT83205 to produce the DC output. In this role, it determines the output ripple; thus, a low impedance at the switching frequency is important. The second function is to store energy to satisfy transient loads and stabilize LT83203/LT83205's control loop. Ceramic capacitors have very low ESR and provide the best ripple performance. For good starting values, see the *Typical Applications* section.

Use X5R or X7R types. This choice provides low output ripple and good transient response. Transient performance can be improved with a higher-value output capacitor. Increasing the output capacitance also decreases the output voltage ripple. A lower value of the output capacitor is used to save space and cost, but transient performance suffers, resulting in loop instability. For the suggested capacitor values, see the *Typical Applications* section.

When choosing a capacitor, special attention should be given to the data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or one with a higher voltage rating may be required.

The LT83203/LT83205 typically operates at a switching frequency of 2MHz. *Table 5* shows some examples of output capacitors with ideal frequency characteristics when operating at switching frequencies around 2MHz. *Figure 51* shows the frequency characteristics of these capacitors; it can be seen that a combination of these capacitors minimizes the impedance at the switching frequency on the output and keeps the impedance low enough to suppress any higher-frequency harmonics near the switching frequency, thus achieving the lowest output ripple.

Table 5. Examples of Output Capacitors with Desirable Frequency Characteristics for 2MHz Operation

PART DESCRIPTION	MANUFACTURER/PART NUMBER
22µF, X7R, 10V, 20% 1206	MURATA, GRM31CR71A226ME15K
10µF, X7R, 25V, 10% 1206	MURATA, GRM31CR71E106KA12
4.7µF, X7S, 16V, 10% 0603	MURATA, GRM188C71C475KE21

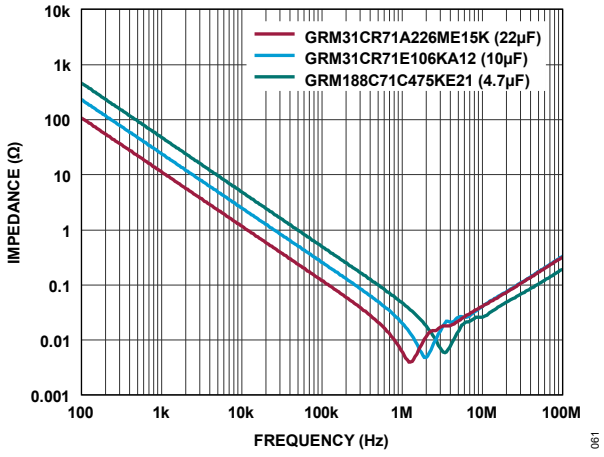


Figure 51. Frequency Characteristics of Example Output Capacitors for 2MHz Operation

Output Voltage

The LT83203/LT83205 incorporates a precision 100µA current source flowing out of the SET pin, which also connects to the error amplifier's non-inverting input. *Figure 52* shows that connecting a resistor from SET to GND generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier's unity-gain configuration produces a low-impedance version of this voltage on its inverting input, the OUTS pin, which is externally connected to the output voltage of the circuit.

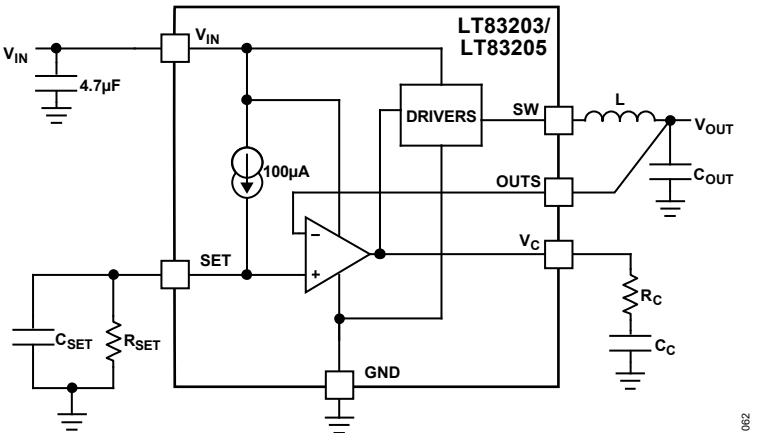


Figure 52. Adjustable Reference for Error Amplifier

The LT83203/LT83205's error amplifier and current reference allow for a wide output voltage range from 0V (using a 0Ω resistor) to 13V. A PNP-based input pair is active from V_{OUT} equals 0V up to V_{IN} minus 1.4V, and an NPN-based input pair is active for output voltages where $V_{IN} - V_{OUT} < 1V$ or less, with a smooth transition between the two input pairs in between these ranges. The PNP-based input pair is designed to offer the best overall performance, as it is active in the vast majority of applications. For more information on offset voltage and SET pin current and output noise, see the *Electrical Characteristics* table. *Table 6* lists many common output voltages and their corresponding 1% R_{SET} resistors. Where the exact resistor value required for the output voltage is not available, two resistors can be paralleled to achieve the desired value. For example, for a 0.8V output voltage, a resistor value of exactly 8kΩ is required. The closest value with a single 1% resistor is 8.06kΩ; with two resistors, 8.25kΩ can be paralleled with 267kΩ to achieve (almost) exactly 8kΩ. 0.1% resistors may be used to achieve higher accuracy.

Table 6. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
0.8	8.06
1	10
1.8	18
2.5	24.9
3.3	33.2
5	49.9
6	60.4
9	90.9
12	120

The benefit of using a current reference compared with a voltage reference, as used in conventional regulators, is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This allows the LT83203/LT83205 to have loop gain, frequency response, and bandwidth independent of the output voltage. Moreover, since none of the error amp gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified.

Since the zero T_C current source is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high-quality insulation (for example, Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High-humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Since the SET pin is a high-impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to GND resolves this issue—100nF is sufficient. This is the minimum recommended capacitance. In general, a larger capacitance is typically preferred; for more information, see the *SET Pin Capacitor: Noise and Soft-Start* section.

For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltage source capable of sinking 100µA. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current SET pin resistor tolerances.

To protect the LT83203/LT83205's low noise error amplifier, a protection clamp exists between the SET and OUTS pins. This SET-to-OUTS protection clamp limits the maximum voltage between SET and OUTS during transient events, with a maximum DC current of 20mA allowed through the clamp. Therefore, in applications where SET is actively driven by a voltage source, the voltage source must be current limited to 20mA or less.

Output Voltages Above 13V

The LT83203/LT83205 can be configured for output voltages above 13V, even though the SET pin voltage is limited to a maximum of 13V, by using a traditional resistor divider from V_{OUT} to OUTS, as shown in *Figure 53*. It is recommended to configure the SET pin voltage to be 12V, in which case the resistor values can be chosen according to Equation 9.

$$R1 = R2 \cdot \left(\frac{V_{OUT} - 12V}{12V + R2 \times I_{OUTS}}\right) \quad (9)$$

The OUTS pin current is 160nA ± 80nA per the *Electrical Characteristics* table. The divider values R1 and R2 can be chosen such that this OUTS pin current variation introduces <0.1% error in output voltage regulation. The thermal noise of the resistors in the resistor divider also adds to the output noise. it is recommended to choose the resistor values such that their impedance as viewed from the SET pin (R1||R2) is less than 5kΩ to keep their noise contribution low compared to the noise contribution of the part itself.

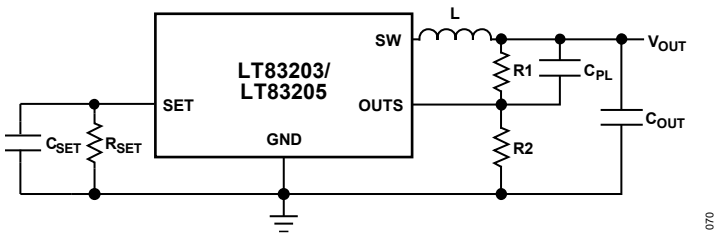


Figure 53. Configuring the LT83203/LT83205 for Output Voltages above 13V

At output voltages above 13V, the low frequency noise has some dependence on the output voltage, the divider gains up the noise. By configuring the SET voltage to be 12V, this dependency is minimized; for example, the noise gain from a 12V reference to $15V_{OUT}$ is 24 times lower than the gain from a conventional 0.5V voltage reference to $15V_{OUT}$.

Output Voltages Below 0.5V

Due to the current reference architecture, the LT83203/LT83205 can be configured for output voltages below 0.5V all the way down to 0V. It should be noted that for output voltages below 0.5V, the Power Good and Fast Start-Up functionalities are not available, and these functionalities must be disabled correctly by tying PGFB to $INTV_{CC}$ or to 0.5V.

Output Sensing and Stability

The LT83203/LT83205's OUTS pin provides a Kelvin sense connection to the output. The SET pin resistor's GND side provides a Kelvin sense connection to the load's GND side.

The LT83203/LT83205's internal error amplifier has a relatively high voltage gain of ~2800. Therefore, it is very important to avoid adding extra impedance (ESR and ESL) to the feedback loop and to minimize the noise coupling onto the OUTS pin, as a combination of excessive parasitics and noise injection can cause instability in the system. To that end, minimize the effects of PCB trace and solder inductance by tying the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}. If this is not possible, for example, due to a design requiring remote sensing, a small local OUTS capacitor of 150pF or less may be added for noise decoupling at the OUTS pin. For more information on the recommended layout that meets these requirements, refer to the LT83203/LT83205 demo board manual.

The LT83203/LT83205 is an externally compensated part, so even if the recommended layout is not followed (sometimes it is not possible due to application-specific limitations), it is possible to choose a more conservative compensation with a lower gain or bandwidth in order to retain stability during operation. However, this is at the

expense of a transient response. A superior layout allows a better tradeoff between transient response, phase margin, and output noise performance when selecting compensation values.

Frequency Compensation

The loop compensation determines the stability and transient performance and is provided by the components connected to the V_C pin. Generally, a capacitor (C_C) and a resistor (R_C) in series to ground are used. Designing the compensation network can be complicated, and the best values depend on the application. A practical approach is to start with one of the circuits in this data sheet that is similar to user's application and tune the compensation network to optimize the performance. LTpowerCAD simulation can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature. The *LT1375* data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 54 shows an equivalent circuit for the LT83203/LT83205 control loop. The error amplifier is a transconductance amplifier with transconductance g_m = 12.5mS, with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier with transconductance G_M = 5.2A/V (LT83203)/7.2A/V (LT83205), generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works as long as the value of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. For more information about the compensation of switching mode power supplies, refer to *Application Note 149: Modeling and Loop Compensation Design of Switching Mode Power Supplies*.

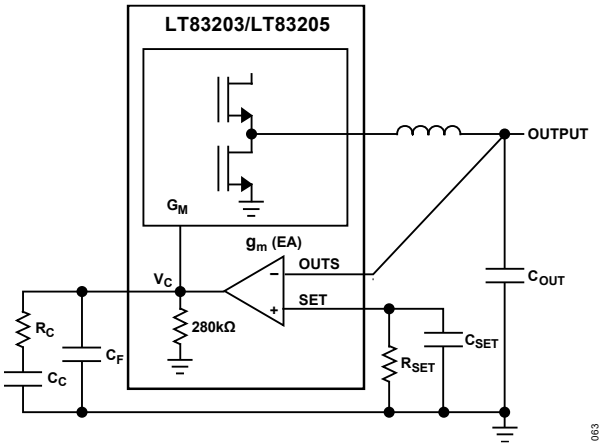


Figure 54. Model for Loop Response

EN/UVLO Pin

The LT83203/LT83205 is in shutdown when the EN/UVLO pin is low and active when the pin is high. The rising threshold of the EN/UVLO comparator is 0.75V, with 50mV of hysteresis. The EN/UVLO pin can be connected to V_{IN} if the shutdown feature is not used or tied to a logic level if shutdown control is required. If connecting the EN/UVLO pin to V_{IN} instead of driving it with a digital signal, it is recommended to connect EN/UVLO to V_{IN} through a resistor divider to set an appropriate UVLO threshold. This ensures correct startup and shutdown behavior in the event of rapid power cycling.

When the enable pin drops below 0.7V, the part stops switching, but internal circuitry continues drawing current as the $INTV_{CC}$ regulator is still awake. Full shutdown is guaranteed when the enable pin drops below 200mV. In full shutdown, the $INTV_{CC}$ regulator is disabled, and the part draws less than 70µA.

Adding a resistor divider from V_{IN} to EN/UVLO programs the LT83203/LT83205 to regulate the output only when V_{IN} is above the required voltage (see the *Block Diagram*). This threshold, $V_{IN(EN)}$, is typically used when the input supply is either current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so the source current increases as the source voltage drops. This looks like a negative resistance load to the source and causes the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values of R_{EN1} and R_{EN2} such that they satisfy Equation 10.

$$V_{IN(EN)} = \left(\frac{R_{EN1}}{R_{EN2}} + 1\right) \times 0.75V \qquad (10)$$

where the LT83203/LT83205 remains off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching does not stop until the input falls slightly below $V_{IN(EN)}$.

$INTV_{cc}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ supplies enough current for the LT83203/LT83205's circuitry. The voltage on $INTV_{CC}$ varies between 2.6V and 3.4V when V_{IN} is between 2.7V and 3.5V. Do not connect an external load to the $INTV_{CC}$ pin.

SET Pin Capacitor: Noise and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor reduces the sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LT83203/LT83205's DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended to use a good quality, low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft-starts the output and limits inrush current. Soft-starting the output prevents a current surge on the input supply. The SET pin capacitor and resistor values set the ramp-up time of the reference voltage, and the output voltage tracks this voltage. The SET pin resistor size is determined by the application's required output voltage; however, the capacitor size may be selected to achieve the desired ramp-up time. It is important to consider that the size of the SET pin capacitor also plays a role in noise performance, which is typically the more important factor in determining the size of this capacitor.

Ceramics are manufactured with a variety of dielectrics, each with a different behavior across temperature and applied voltage. Care should be taken when selecting a ceramic capacitor for bypassing the SET pin, as this is a critical component. An X7R (or better) ceramic capacitor is strongly recommended for its superior stability across temperature and DC voltage bias. Additionally, larger case sizes are recommended for better DC bias and AC voltage characteristics.

As shown in *Figure 55*, capacitor DC bias characteristics tend to improve as component case size increases.

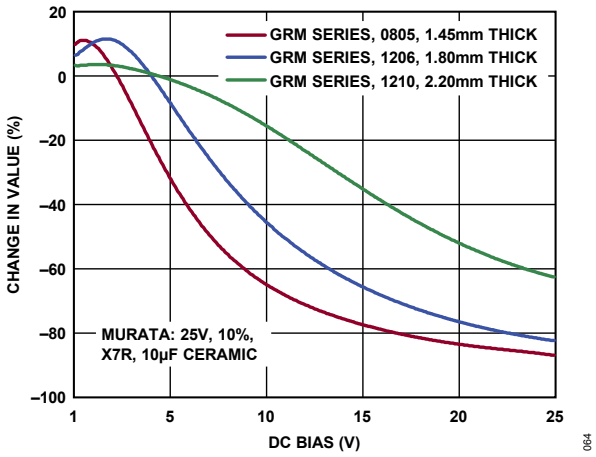


Figure 55. Capacitor Voltage Coefficient for Different Case Sizes

Larger case sizes are also beneficial for improved AC voltage characteristics. Capacitor values are often rated at $1V_{RMS}$ of AC voltage and can drop significantly when operating near $0V_{RMS}$, which is the operating condition of a bypass capacitor.

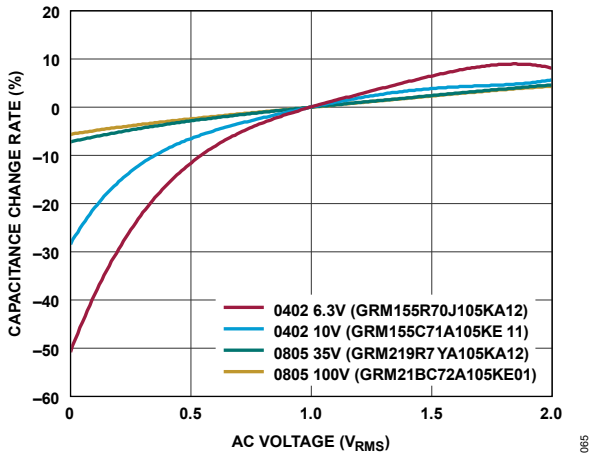
As shown in *Figure 56*, larger case sizes tend to experience a smaller capacitance drop when operating near $0V_{RMS}$. Therefore, an 0805 or larger ceramic capacitor should be used for the SET pin bypass capacitor for best performance. A larger required capacitance value may require larger case sizes; for example, a 4.7µF value should use 1206 or larger.

Table 7 shows some recommended SET pin capacitors.

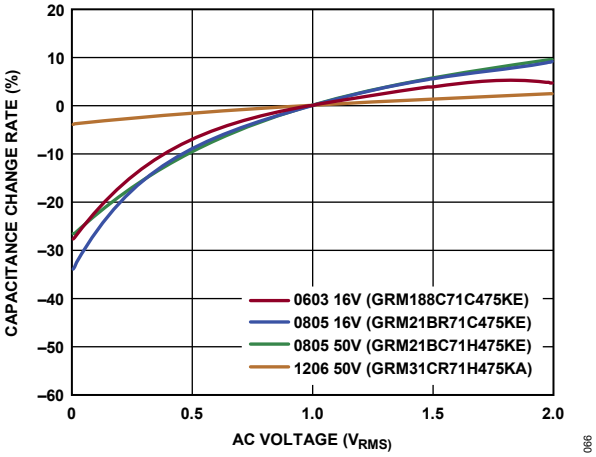
Table 7. Suggested SET Capacitor Part Numbers

PART DESCRIPTION	MANUFACTURER/PART NUMBER
1µF, X7R, 35V, 0805	MURATA, GRM219R7YA105KA12
4.7µF, X7R, 50V, 1206	MURATA, GRM31CR71H475MA12
10µF, X7R, 100V, 1210	MURATA, GRM32EC72A106KE05

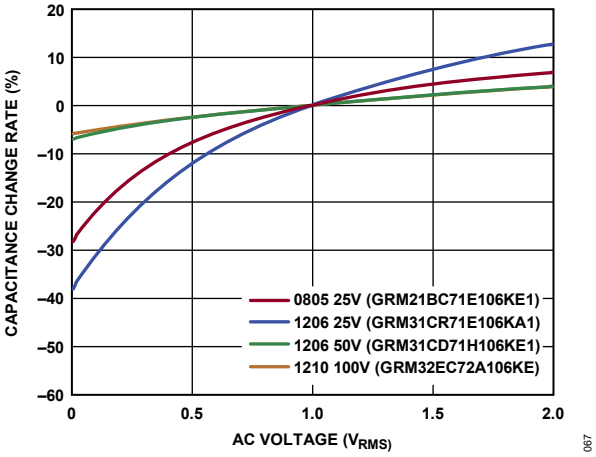
For high-vibration environments, non-piezoelectrically responsive capacitors should be used at the SET pin for optimal performance. A piezoelectric ceramic capacitor generates voltage across its terminals due to mechanical stress upon it, induced by mechanical vibrations or thermal transients. Film capacitors are the preferred option. If a ceramic must be used, soft-termination ceramics are available, which reduce the sensitivity to the piezoelectric effect.



(a) Rated Capacitance = 1µF



(b) Rated Capacitance = 4.7µF



(c) Rated Capacitance = 10µF

Figure 56. AC Voltage Characteristics for Different Capacitor Case Sizes

Without fast start-up enabled, the R_C time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Connect the PGFB pin to $INTV_{CC}$ or to 0.5V to disable fast start-up. The ramp-up rate from 0% to 90% of nominal V_{OUT} is given by Equation 11.

$$t_{START\_NO\_FAST\_START-UP} = 2.3 \times R_{SET} \times C_{SET} \quad (11)$$

With fast-start-up enabled, the start-up time can be significantly reduced, with the ramp-up time from 0% to 90% of the nominal V_{OUT} given by Equation 12. For how the 2.7mA fast start-up current varies with temperature and $V_{IN} - V_{SET}$ differential voltage, see the *Typical Performance Characteristics* section.

$$t_{START\_FAST\_START-UP} = \frac{100\mu A \times R_{SET} \times C_{SET}}{2.7mA} \quad (12)$$

In most applications, fast start-up is enabled, in which case a minimum SET capacitor size of 1µF is recommended for preventing reference voltage overcharge as well as ensuring good noise performance.

The SET pin is pulled to ground with a 520Ω MOSFET ($R_{SET\text{-}PULLDOWN}$) during shutdown, thermal shutdown, V_{CC} UVLO, or V_{IN} UVLO. To ensure a soft start when the part exits any of the above conditions, there must have been sufficient time to allow the SET pin to be pulled to close to ground prior to start-up. This time will be a function of the chosen SET pin capacitance and $R_{SET\text{-}PULLDOWN}$.

Fast Start-Up

For ultra-low noise applications that require low 1/f noise (that is, at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used, but care should be taken regarding leakage. While normally larger capacitors significantly increase the regulator's start-up time, the LT83203/LT83205 incorporates fast start-up circuitry that increases the SET pin current to about 2.7mA during start-up.

Upon start-up, the 2.7mA current source remains engaged while PGFB is below the power good start-up threshold ($V_{PGL\_STARTUP}$) of 486.5mV, unless the regulator is in thermal shutdown, V_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast start-up circuit is permanently disabled once PGFB rises above $V_{PGL\_STARTUP}$ until either the part is powered down or the part is placed into shutdown by pulling the EN/UVLO pin below 0.75V.

There is one more condition under which the 2.7mA current source is disabled during start-up. The purpose of this is to prevent overcharging V_{SET}. Since the part assumes that the PGFB pin is an accurate indication of the voltage on the SET pin, it assumes that V_{OUTS} follows V_{SET} closely. However, this may not always be the case; for example, if the output capacitance is very large or if, for some reason, the output is temporarily shorted to the GND. Therefore, fast charge is disabled whenever V_{OUTS} is lagging V_{SET} by more than 30mV. This prevents incorrect behavior where the 2.7mA current source stays on even when V_{SET} has risen above its intended final value.

If programmable power good and fast start-up capabilities are not required, the PGFB pin must be connected to either $INTV_{CC}$ or to 0.5V.

Programmable Power Good

As shown in the *Block Diagram*, the power good threshold is user programmable using the ratio of two external resistors, $R_{PGFB(BOT)}$ and $R_{PGFB(TOP)}$ (see Equation 13).

$$V_{OUT(PG\_THRESHOLD)} = 0.5V \times \left(1 + \frac{R_{PGFB(TOP)}}{R_{PGFB(BOT)}}\right) + I_{PGFB} \times R_{PGFB(TOP)} \quad (13)$$

If the PGFB pin increases above 537.5mV or decreases below 462.5mV, the open-drain PG pin asserts and becomes low impedance, indicating power is bad. The power good comparator has hysteresis of 10mV. The PGFB pin current

(I_{PGFB}) from the *Electrical Characteristics* table must be considered when determining the resistor divider network. Note that the programmable power good and fast start-up capabilities are disabled when PGFB is tied to 0.5V or when the device is in shutdown.

The PGFB pin current (I_{PGFB}) can be ignored if $R_{PGFB(BOT)}$ is less than 50kΩ. *Table 8* suggests some 1% PGFB resistor divider values for common V_{OUT} configurations.

Table 8. Suggested PGFB Resistor Divider Values

V_{OUT} (V)	$R_{PGFB(TOP)}$ (kΩ)	$R_{PGFB(BOT)}$ (kΩ)
0.8	29.4	48.7
0.9	39.2	48.7
1	49.9	49.9
1.2	69.8	49.9
1.8	130	49.9
3.3	280	49.9
5	453	49.9

Shorted and Reversed Input Protection

The LT83203/LT83205 tolerates a shorted output. The bottom switch current is monitored such that if the inductor current is beyond safe levels, switching on of the top switch is delayed until the inductor current falls to safe levels.

There is another situation to consider in systems where the output is held high when the input to the LT83203/LT83205 is absent. This occurs in battery charging applications or in battery backup systems where a battery or some other supply is diode-ORed with the LT83203/LT83205's output. If the V_{IN} pin is allowed to float and the EN/UVLO pin is held high, then the LT83203/LT83205's internal circuitry pulls its quiescent current through its SW pin. This is acceptable if the system can tolerate current draw in this state. If the EN/UVLO pin is grounded, the SW pin current drops to ~50µA.

However, if the V_{IN} pin is grounded while the output is held high, regardless of EN/UVLO, parasitic body diodes inside the LT83203/LT83205 can pull current from the output through the SW pin and the V_{IN} pin.

Figure 57 shows a connection of the V_{IN} and EN/UVLO pins, which allows the LT83203/LT83205 to run only when the input voltage is present and protects against a shorted or reversed input.

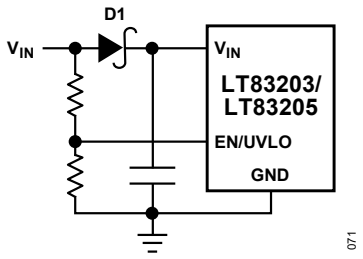


Figure 57. Reverse V_{IN} Protection

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT83203/LT83205. The exposed pad on the bottom of the package should be soldered to a ground plane. This ground should be connected to large copper layers below with thermal vias; these layers spread heat dissipated by the LT83203/LT83205. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT83203/LT83205 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT83203/LT83205 power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT83203/LT83205. If the junction temperature reaches approximately 165°C, the LT83203/LT83205 stops switching and indicates a fault condition until the temperature drops about 5°C cooler.

The temperature rise of the LT83203/LT83205 is at its worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an appropriate level. *Figure 58* shows examples of how case temperature rise can be managed by reducing load.

The LT83203/LT83205's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT83203/LT83205 can deliver for a given application. See curve in *Typical Performance Characteristics*.

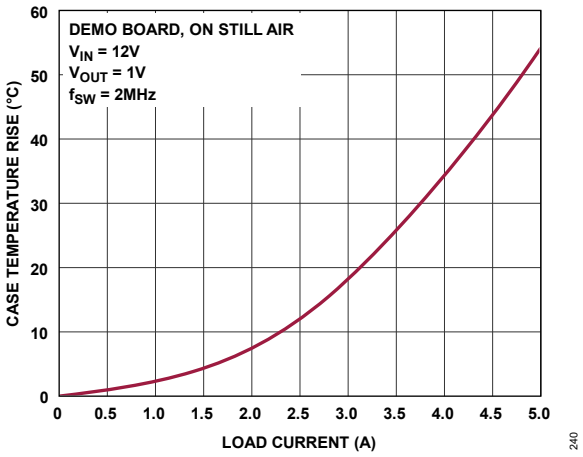


Figure 58. LT83203/LT83205 Case Temperature Rise

TYPICAL APPLICATIONS

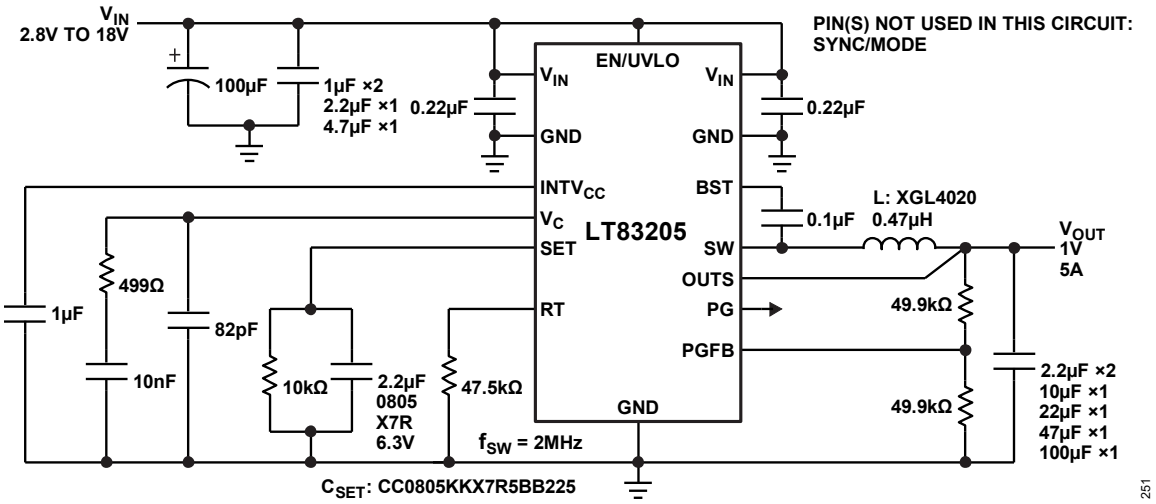


Figure 59. 1V 5A 2MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good

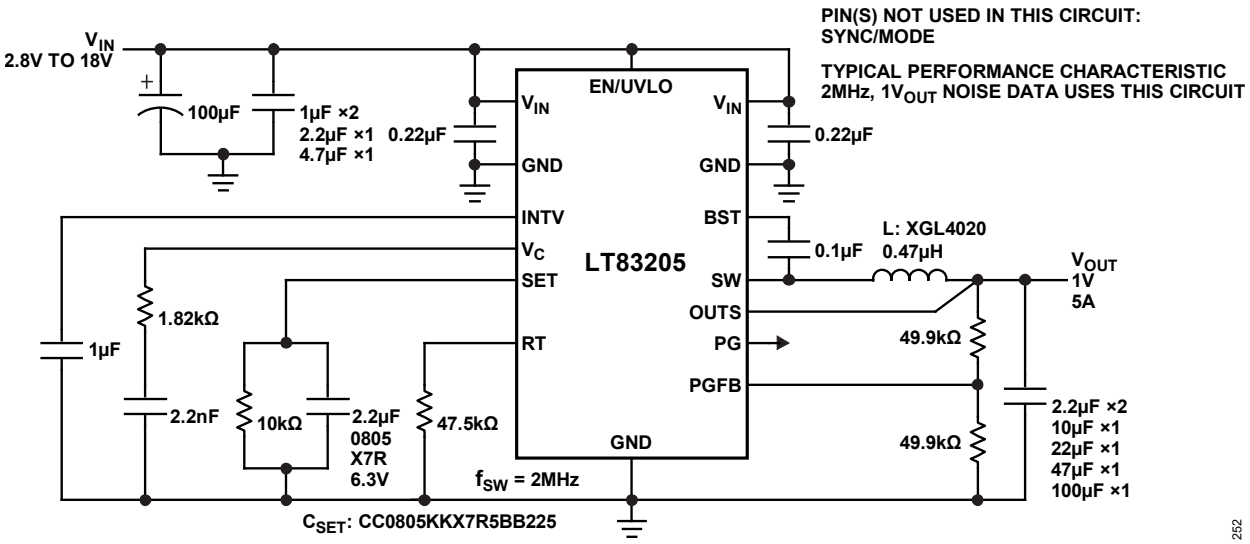


Figure 60. 1V 5A 2MHz Step-Down Converter with High Bandwidth, Soft-Start, Fast Start-Up and Power Good

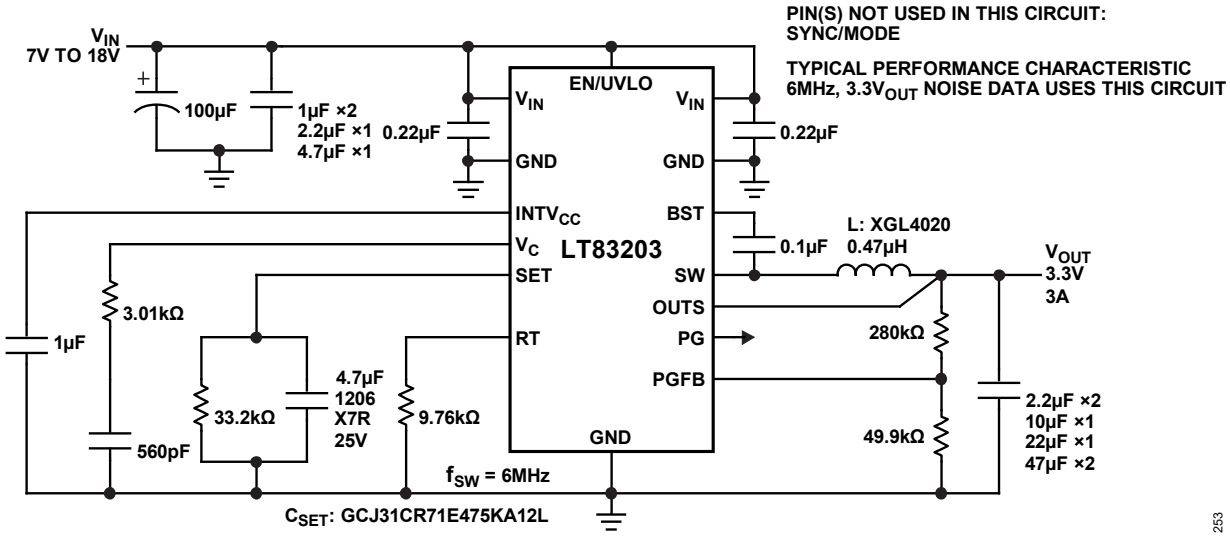
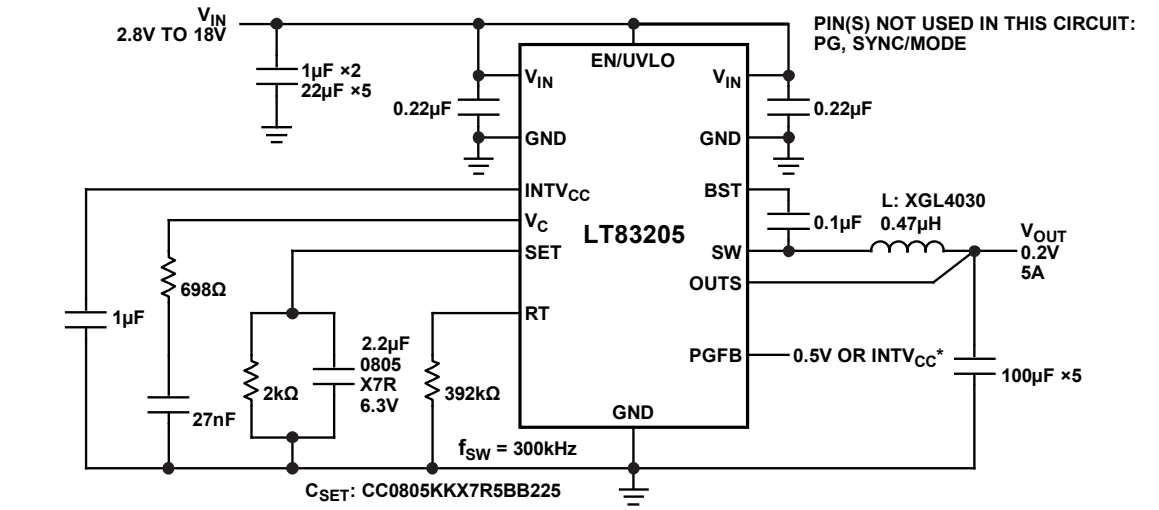


Figure 61. 3.3V 3A 6MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good



*NOTE THAT APPLICATIONS WITH V_{OUT} BELOW 0.5V WILL NOT BE ABLE TO USE THE POWER GOOD AND FAST START-UP FUNCTIONALITIES AND MUST TIE PGFB TO 0.5V TO DISABLE THESE FUNCTIONS CORRECTLY.

Figure 62. 0.2V 5A 300kHz Step-Down Converter with Soft-Start

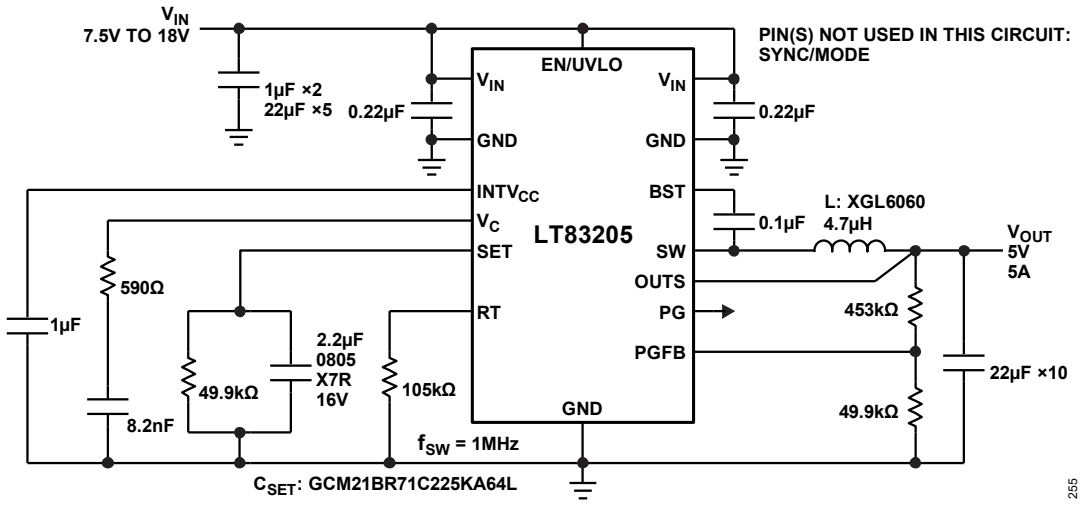


Figure 63. 5V 5A 1MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good

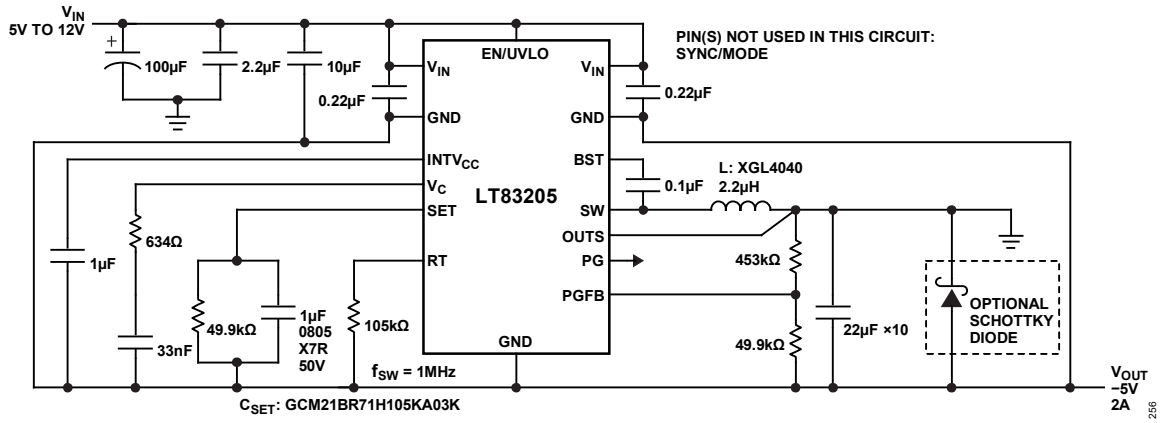


Figure 64. Negative 5V 2A 1MHz Step-Down Converter with Soft-Start, Fast Start-Up and Power Good

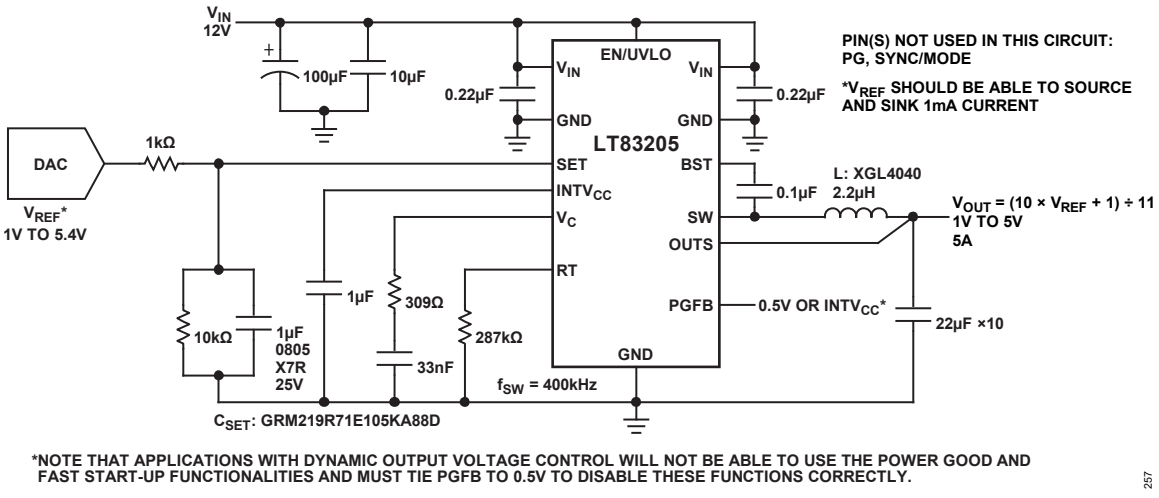
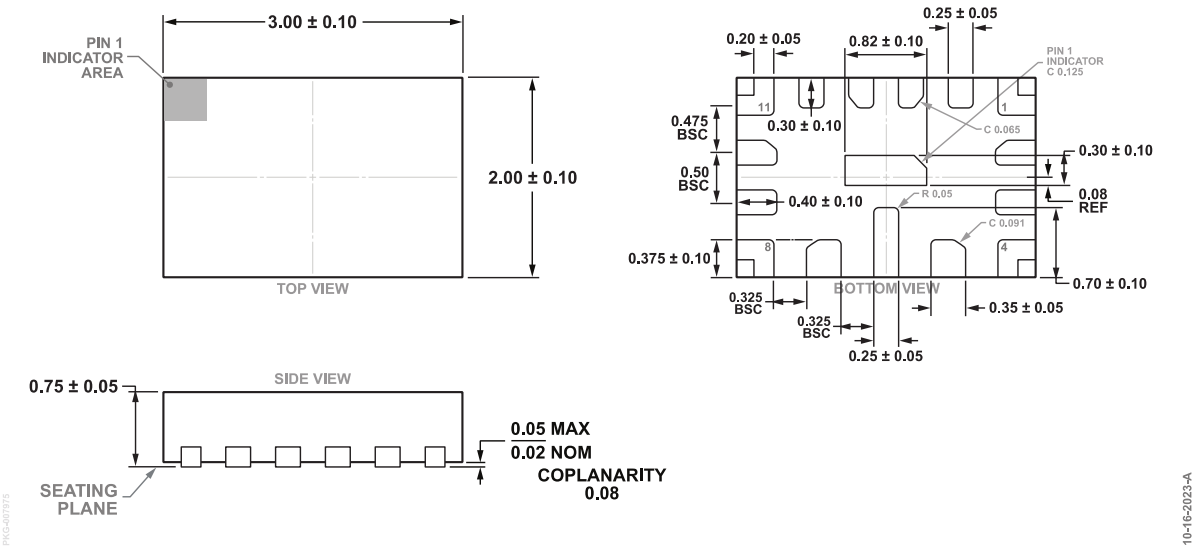


Figure 65. Dynamic Output Voltage Control 1V to 5V 5A 400kHz Step-Down Converter with External DAC

OUTLINE DIMENSIONS

ANALOG DEVICES

15-Lead Lead Frame Chip Scale Package [LFCSP]
3 x 2 mm Body and 0.75 mm Package Height
(CP-15-1)
Dimensions shown in millimeters



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)

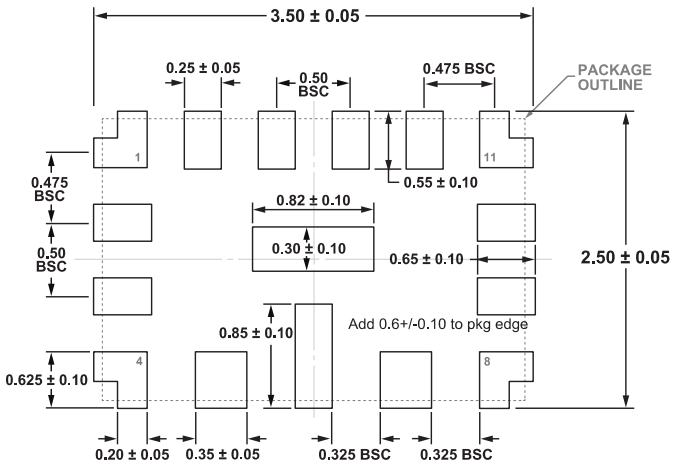


Figure 66. Tiny 15-Lead 3mm × 2mm LFCSP

ORDERING GUIDE

Table 9. Ordering Guide

TAPE AND REEL*	TAPE AND REEL (MINI)**	PAD OR BALL FINISH***	PART MARKING****		PACKAGE TYPE*****	MSL RATING	TEMPERATURE RANGE******
			DEVICE	FINISH CODE			
LT83203RUDB#TRPBF	LT83203RUDB#TRMPBF	Au (RoHS)	LHWJ	e4	LFCSP (Lead Frame Chip Scale Package)	1	–40°C to 150°C
LT83205RUDB#TRPBF	LT83205RUDB#TRMPBF		LHWD				

- *Parts ending with PBF are RoHS and WEEE compliant.
- **Tape and reel specifications. Some packages are available in 500-unit reels through designated sales channels with #TRMPBF suffix.
- ***Pad or ball finish code is per IPC/JEDEC J-STD-609.
- ****The temperature grade is identified by a label on the shipping container.
- *****The LT83203/LT83205 package has the same dimensions as a standard 3mm × 2mm LFCSP package.
- ******The LT83203/LT83205 is specified over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.
- For parts specified with wider operating temperature ranges, contact the factory.
- For recommended LGA and BGA PCB assembly and manufacturing procedures, refer to the *Recommended LGA and BGA PCB Assembly and Manufacturing Procedures*.
- For LGA and BGA package and tray drawings, refer to the *LGA and BGA Package and Tray Drawings*.

RELATED PARTS

Table 10. Related Parts

PART	DESCRIPTION	COMMENTS
LT83201	18V, 1A Synchronous Step-Down Silent Switcher 3 with Ultra-Low Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.8V to 18V, $V_{OUT(MIN)}$ = 0V, 3mm × 2mm LFCSP-15
LT8622S/ LT8624S	18V, 2A/4A Synchronous Step-Down Silent Switcher 3 with Ultra-Low Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.7V to 18V, $V_{OUT(MIN)}$ = 0V, 4mm × 3mm LQFN-20
LT8625S	18V/8A Synchronous Step-Down Silent Switcher 3 with Ultra-Low Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.7V to 18V, $V_{OUT(MIN)}$ = 0V, 4mm × 3mm LQFN-20
LT8625SP/ LT8625SP-1	18V/8A Synchronous Step-Down Silent Switcher 3 with Ultra-Low Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.7V to 18V, $V_{OUT(MIN)}$ = 0V, 4mm × 3mm LQFN-20 or 4mm × 4mm LQFN-24
LT8627SP	18V/16A Synchronous Step-Down Silent Switcher 3 with Ultra-Low Noise Reference	4µV_{RMS} Noise, V_{IN} = 2.8V to 18V, $V_{OUT(MIN)}$ = 0V, 4mm × 4mm LQFN-24
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2 Regulator	96% Efficiency, V_{IN} = 2.8V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 240µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24

PART	DESCRIPTION	COMMENTS
LTC7151S	20V, 15A Synchronous Step-Down Silent Switcher 2 Regulator	92.5% Efficiency, V_{IN} = 3.1V to 20V, $V_{OUT(MIN)}$ = 0.5V, I_Q = 2mA, I_{SD} < 20µA, 4mm × 5mm LQFN-28
LTC7150S	20V, 20A Synchronous Step-Down Silent Switcher 2 Regulator	92% Efficiency, V_{IN} = 3.1V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} ≤ 40µA, Differential Remote Sense, 6mm × 5mm BGA
LT3042	20V, 200mA Ultra-Low Noise Ultra-High PSRR Linear Regulator	0.8µV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm × 3mm DFN and MSOP Packages
LT3045	20V, 500mA Ultra-Low Noise Ultra-High PSRR Linear Regulator	0.8µV_{RMS} Noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV Dropout Voltage, 3mm × 3mm DFN and MSOP Packages
LT8652S	18V, Dual 8.5A, 94% Efficiency, 2.2MHz Synchronous Silent Switcher 2 Step-Down DC/DC Converter with I_Q = 16µA	V_{IN} = 3V to 18V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 16µA, I_{SD} = 6µA, 4mm × 7mm LQFN-36 Package
LTC3636	20V, Dual 6A Synchronous Step-Down Regulator	95% Efficiency, V_{IN} = 3.1V to 17V, $V_{OUT(MIN)}$ = 0.6V, I_Q < 8µA (Both Channels Enabled), I_{SD} < 1µA, 3mm × 5mm QFN-24 Package
LT8640S/ LT8643S	42V, 6A Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 4mm × 4mm LQFN-24
LT8645S/ LT8646S	65V, 8A Synchronous Step-Down Silent Switcher 2 with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3.4V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.97V, I_Q = 2.5µA, I_{SD} < 1µA, 6mm × 4mm LQFN-32
LT8609/ LT8609A	42V, 2A, 94% Efficiency, 2.2MHz Synchronous MicroPower Step-Down DC/DC Converter with I_Q = 2.5µA	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 42V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5µA, I_{SD} < 1µA, MSOP-10E