Data Sheet

LT7153SP

5V, ±25A High Efficiency Silent Switcher®2 Step-Down Regulator

FEATURES

- Silent Switcher®2 Architecture
  - Ultralow EMI
  - Eliminates PCB Layout Sensitivity
  - Internal Bypass Caps Reduce Radiated EMI
- SV_{IN}: 2.7V to 5V; PV_{IN}: 1.5V to 5V
- V_{OUT}: 0.5V to 0.9 · V_{IN}
- Accurate Reference: 0.5V ±0.8% Over Temp
- Integrated N-MOSFETs: 1.8mΩ/0.7mΩ
- 15ns Min On-Time: Low Duty Cycle Operation
- Differential V_{OUT} Remote Sense
- Configurable Fixed Output Options
- Programmable Load Line (3 settings)
- Programmable Current Limit (3 settings)
- Programmable, Synchronizable: 400kHz to 5MHz
- User Selectable Discontinuous Mode® (DCM) or Forced Continuous Mode (FCM) Operation
- Controlled T_{ON}, Current Mode: Excellent Transient
- Power Good status, Output Tracking, Clock-Out
- Supports Spread Spectrum Operation
- PolyPhase Operation: 2, 3, 4, 6, 8 or 12 Phases
- 36-Lead (4mm x 7mm) Exposed Back LQFN Package

APPLICATIONS

- Optical Module Applications
- Distributed Power Systems, Server Power
- Point-of-Load Supply (i.e., ASIC, FPGA, DSP, µP)

TYPICAL APPLICATION

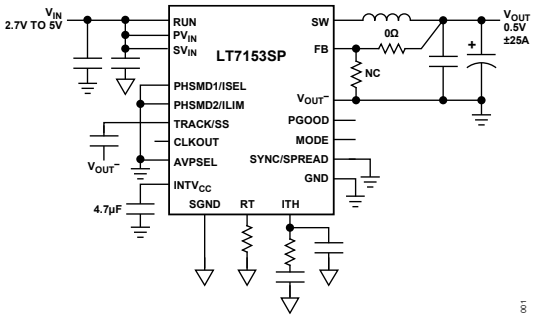

Figure 1. 0.5V, ±25A Buck Regulator

DESCRIPTION

The LT®7153SP is a high efficiency monolithic synchronous, Silent Switcher®2 buck regulator capable of delivering ±25A to the load. The unique constant frequency, controlled on-time, current mode architecture is ideal for high step-down ratio applications that operate at high frequencies while demanding fast transient response. PolyPhase operation allows multiple LT7153SP regulators to run out-of-phase, which reduces the amount of input and output capacitors needed while enables paralleling for higher output currents. The operating supply voltage range is from 2.7V to 5V.

The operating frequency is programmable from 400kHz to 5MHz with an external resistor or sync to an external clock signal. The high frequency capability allows the use of physically smaller inductors and capacitors.

The LT7153SP package features the second-generation Silent Switcher architecture to minimize EMI emissions while delivering high efficiency at high switching frequencies. This includes the integration of bypass capacitors to optimize high frequency current loops and makes it easy to achieve advertised EMI performance by reducing layout sensitivity. It also features an exposed back for heat sink attachment, which can be used to significantly improve thermal performance.

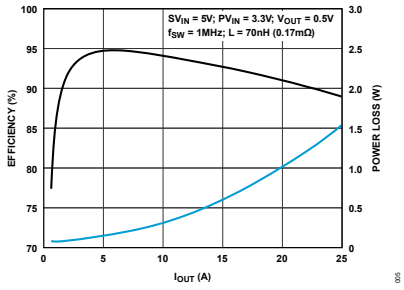

Figure 2. Efficiency and Power Loss (1MHZ)

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	05/25	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Supply Voltage Range	SV_{IN}	-40°C ≤ T_J ≤ 125°C		2.7		5	V
	PV_{IN}			1.5		5	
V_{OUT} Operating Voltage	V_{OUT}	R_{RT} = 100kΩ		0.5		0.9V_{IN}	V
Supply Operating Current[2]	$I_{Q\ (ACT)}$	Active, No-Load R_{RT} = 100kΩ, MODE/SYNC = 0			1.5	3	mA
Supply Shutdown Current[2]	$I_{Q\ (SHDN)}$	V_{RUN} = 0V				5	µA
V_{IN} OV Threshold	V_{IN-OV}	Rising			8.0		V
		Falling			7.5		
RUN Threshold	V_{RUN}	Rising		1.13	1.18	1.23	V
	V_{RUN_Hys}	Hysteresis			80		mV
$INTV_{cc}$ Regulated Voltage	V_{INTVCC}	SV_{IN} > 4V		3.45	3.6	3.75	V
$INTV_{cc}$ UVLO	V_{UVLO}	Rising			2.55	2.65	V
		Falling			2.4		
BUCK Regulator Loop							
FB regulation Voltage[3]	V_{FB}	ITH = 1V	-40°C ≤ T_J ≤ 125°C	496	500	504	mV
FB Line and Load Regulation[3]	$\Delta V_{FB(LINE+LOAD)}$	AVPSEL = 0V	-40°C ≤ T_J ≤ 125°C		0.05	0.3	%
		AVPSEL = Float, ITH > 1V			1		
		AVPSEL = $INTV_{cc}$, ITH > 1V			1.5		
FB Pin Input Current	I_{FB}	-40°C ≤ T_J ≤ 125°C		-50		50	nA
Error Amplifier gm	$GM_{(EA)}$	ITH = 1V		0.85	1	1.15	mS
Minimum On-Time	$t_{ON(MIN)}$	-40°C ≤ T_J ≤ 125°C			15	25	ns
Minimum Off-Time	$t_{OFF(MIN)}$				30		ns
Positive Inductor Valley Current Limit[4]	$I_{LIM-POS}$	FB = 0.48V		20	25	30	A
Current Threshold vs. ITH Voltage	$I_{LIM-ITH}$	ITH = 1.3V			25		A
		ITH = 1.0V			0		
		ITH = 0.7V			-25		
Negative Inductor Valley Current Limit	$I_{LIM-NEG}$	FB = 0.52V			-60		A
Top Power NMOS On Resistance	R_{ON-TOP}	$INTV_{cc}$ = 3.6V			1.8		mΩ
Bottom Power NMOS On Resistance	R_{ON-BOT}	$INTV_{cc}$ = 3.6V			0.7		mΩ
Top Switch Leakage	I_{SW-TOP}	V_{IN} = 5V, V_{SW} = 0V			0.5		µA
Bottom Switch Leakage	$I_{BOT-TOP}$	V_{IN} = 5V, V_{SW} = 5V			1		µA

(Specifications are at T_A = 25°C. V_{IN} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Oscillator						
Oscillator Frequency	f_{osc}	R_{RT} = 232kΩ		0.4		MHz
		R_{RT} = 100kΩ	0.85	1	1.15	
		R_{RT} = 20kΩ		5		
SYNC Input Range	f_{SYNC}	% of programmed frequency		±30		%
MODE, SYNC/SPREAD Threshold	$V_{IL(MODE)}$ $V_{IL(SYNC/SPREAD)}$	MODE or SYNC/SPREAD LOW			0.3	V
	$V_{IH(MODE)}$ $V_{IH(SYNC/SPREAD)}$	MODE or SYNC/SPREAD HIGH	1.0			
MODE, SYNC/SPREAD Currents	I_{MODE} $I_{SYNC/SPREAD}$	MODE = 0, SYNC = 0V		6	14	µA
CLKOUT Threshold	$V_{IL(CLKOUT)}$	CLKOUT High	V_{INTVCC} – 0.2	V_{INTVCC}		V
	$V_{IH(CLKOUT)}$	CLKOUT Low		0	0.2	
Phasing						
SYNC to Oscillator	$\phi_{(SYNC\ to\ OSC)}$	PHSMD1 = 0, PHSMD2 = 0		0		Degree
		PHSMD1 = $INTV_{cc}$, PHSMD2 = 0		0		
		PHSMD1 = 0, PHSMD2 = $INTV_{cc}$/2		-30		
		PHSMD1 = $INTV_{cc}$, PHSMD2 = $INTV_{cc}$/2		-45		
		PHSMD1 = 0, PHSMD2 = $INTV_{cc}$		-60		
		PHSMD1 = $INTV_{cc}$, PHSMD2 = $INTV_{cc}$		-90		
Oscillator to CLKOUT	$\phi_{(OSC\ to\ CLKOUT)}$	PHSMD1 = 0, PHSMD2 = 0		180		Degree
		PHSMD1 = $INTV_{cc}$, PHSMD2 = 0		120		
		PHSMD1 = 0, PHSMD2 = $INTV_{cc}$/2		180		
		PHSMD1 = $INTV_{cc}$, PHSMD2 = $INTV_{cc}$/2		180		
		PHSMD1 = 0, PHSMD2 = $INTV_{cc}$		120		
		PHSMD1 = $INTV_{cc}$, PHSMD2 = $INTV_{cc}$		180		
AVPSEL, PHSMD1, PHSMD2, Threshold	V_{IH}	AVPSEL, PHSMD1, PHSMD2 High	V_{INTVCC} – 0.2			V
AVPSEL, PHSMD1, PHSMD2 Threshold	V_{IL}	AVPSEL, PHSMD1, PHSMD2 Low			0.2	V
ILIM						
Reduced Max Current Limit	I_{LIM55}	PHSMD1 = $INTV_{cc}$ /2, PHSMD2 = 0		14		A
	I_{LIM70}	PHSMD1 = $INTV_{cc}$ /2, PHSMD2 = $INTV_{cc}$		18		
Power Good						
PGOOD Over Voltage Threshold	OV	V_{FB} Rising	4	6.5	9	%
		V_{FB} Hysteresis (Falling)		1.5		
PGOOD Under Voltage Threshold	UV	V_{FB} Falling	-9	-6.5	-4	%
		V_{FB} Hysteresis (Rising)		1.5		

(Specifications are at T_A = 25°C. V_{IN} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
PGOOD Leakage Current	I_{PGOOD}				0.5	µA
PGOOD Pull-Down Resistance	R_{PGOOD}	V_{PG} = 0.1V		5		Ω
PGOOD Delay	$PG_{(Delay)}$	PGOOD Low to High		6		Cycles
		PGOOD High to Low		25		
Track/Soft-Start						
Source Current	$I_{TRACK/SS}$	$V_{TRACK/SS}$ = 0V		10	15	µA
Pull-Down Resistance	$R_{TRACK/SS}$	$V_{TRACK/SS}$ = 0.1V		2500		Ω

1 The LT7153SP is tested under pulsed load conditions such that $T_J \approx T_A$. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT7153SP is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

2 The quiescent current in Discontinuous Mode does not include switching loss of the power FETs.

3 V_{FB} is measured in a feedback loop that servos V_{ITH} to a specified voltage.

4 Inductor should be selected such that peak inductor current does not exceed 39A in application.

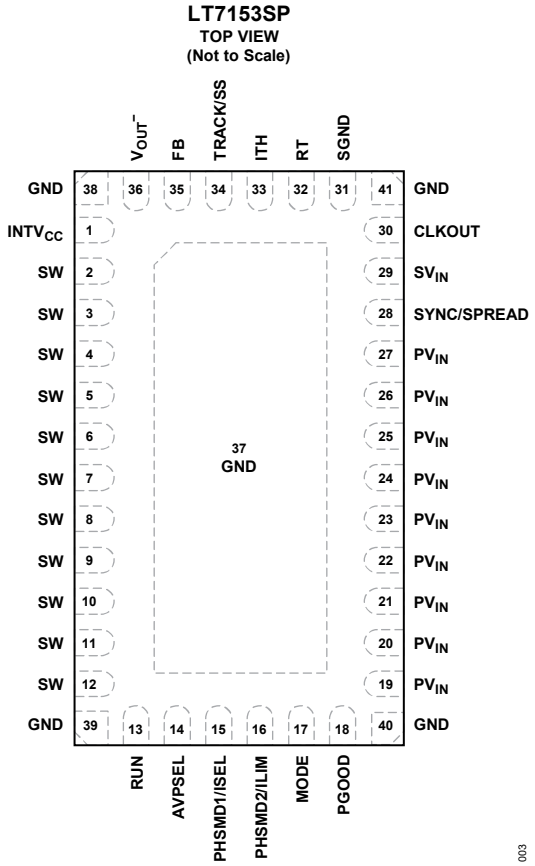
ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
SV_{IN}, PV_{IN}, SW	-0.3V to 5.5V
RUN, PGOOD, TRACK	-0.3V to 5.5V
MODE, SYNC/SPREAD	-0.3V to $INTV_{cc}$ + 0.3V
FB, ITH, RT	-0.3V to $INTV_{cc}$ + 0.3V
PHSMD1/ISEL, PHSMD2/ILIM, CLKOUT, AVPSEL	-0.3V to $INTV_{cc}$ + 0.3V
VOUT-	-0.3V to 0.3V
Operating Junction Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Internal Temperature	125°C
Peak Reflow Solder Body temperature	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



LQFN PACKAGE
36-LEAD (4mm x 7mm x 1.02mm)
T_{JMAX} = 125 °C, θ_{JA} = 15.8°C/W (BASED ON DEMOBOARD), θ_{JCtop} = 0.4°C/W, θ_{JCbot} = 3.4°C/W
EXPOSED PAD (PIN 37) AND CORNER PINS (38~41) ARE GND, MUST BE SOLDERED TO PCB

Figure 3. Pin Configurations

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	$INTV_{cc}$	Internal 3.6V regulator output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR ceramic capacitor.
2-12	SW	Switch node connection of external inductor. Voltage swing of SW is from a diode voltage drop below ground to a diode voltage above PV_{IN}.
13	RUN	Logic controlled RUN input. Do not leave this pin floating. Logic high activates the step-down regulator.
14	AVPSEL	Use this pin to select between three different load lines; tied to GND: 0.2%, float: 1%, $INTV_{cc}$: 1.5%.
15	PHSMD1/ ISEL	Control inputs to the phase selector and ILIM option. A high or low state on this pin, in conjunction with the state of the PHSMD2/ILIM pin, determines the phase relationship between SYNC and the internal oscillator and between the internal oscillator and CLKOUT. When this pin is floated to mid rail (1/2 $INTV_{cc}$), the PHSMD2/ILIM pin can be used to select between three lower ILIM settings.
16	PHSMD2/ ILIM	Control inputs to the phase selector and ILIM set. When PHSMD1/ISEL is high or low, this pin in conjunction with PHSMD1/ILIM determines the phasing between SYNC and the internal oscillator and between the internal oscillator and CLKOUT. When PHSMD1/ISEL is floated to mid rail (1/2 $INTV_{cc}$), this pin can be used to select between three different lower ILIM settings.
17	MODE	Mode select pin. Tie MODE to GND for discontinuous mode of operation. Float or tie MODE to a voltage above 1V selects forced continuous mode.
18	PGOOD	Output power good with open-drain logic. PGOOD is pulled to ground when the voltage of the FB pin is not within ±6.5% of the internal 0.5V reference.
19-27	PV_{IN}	Power V_{IN}. Input voltage to the on-chip power MOSFETs.
28	SYNC/ SPREAD	Spread spectrum select and oscillator synchronization pin. Tie SYNC/SPREAD to GND to disable spread spectrum operation; tie to $INTV_{cc}$ or float to start spread spectrum. Connect to an external clock to synchronize the system clock to the external clock and put the part in forced continuous mode.
29	SV_{IN}	Signal V_{IN}. Filtered input voltage to the on-chip 3.6V regulator. Bypass the signal into the SV_{IN} pin through a 2.2Ω resistor in series with 10µF ceramic capacitor.
30	CLKOUT	Output clock signal for PolyPhase operation. The phase of CLKOUT with respect to SYNC is determined by the state of PHSMD1 and PHSMD2 pins. CLKOUT's peak-to-peak amplitude is $INTV_{cc}$ to GND. Minimize the parasitic capacitance on this pin to reduce phase errors. When RUN is low, this pin defaults high.
31	SGND	Ground for signal ground.
32	RT	Switching frequency programming pin. Connect an external resistor from this pin to GND to program the frequency from 400kHz to 5MHz.

33	ITH	Error amplifier output and switching regulator compensation point. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.3V.
34	TRACK/SS	Output tracking and soft-start pin. Allows to control the rise time of the output voltage. Connecting a voltage between 0V and 0.5V on this pin relative to V_{OUT-} bypasses the internal reference input to the error amplifier. Instead, it servos the FB pin relative to V_{OUT-} to this voltage. There's an internal 10µA pullup current from $INTV_{cc}$ to this pin; so putting a capacitor from this pin to V_{OUT-} provides a soft-start function.
35	FB	Feedback input to the error amplifier of the step-down regulator. Connect the feedback resistor divider center tap to this pin. The output can be adjusted from 0.5V to 4.5V.
36	V_{OUT-}	Negative return of output rail. Connect this pin directly to the bottom terminal of the remote output capacitor near the load in order to minimize error incurred by voltage drops across the metal traces of the PCB.
37	GND	Exposed Pad.
38-41		Corner Ground Pins.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 3.3V, V_{OUT} = 0.5V, unless otherwise specified.

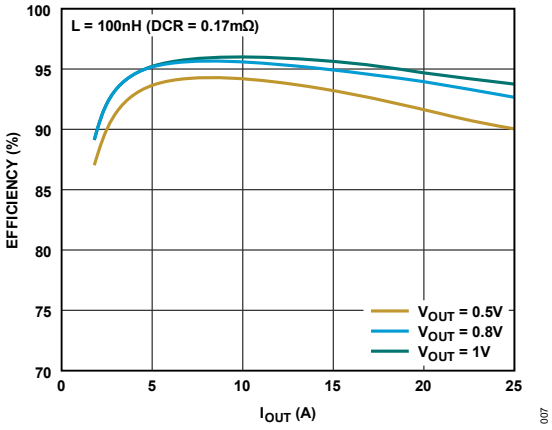


Figure 4. Efficiency vs. Load Current (500kHz)

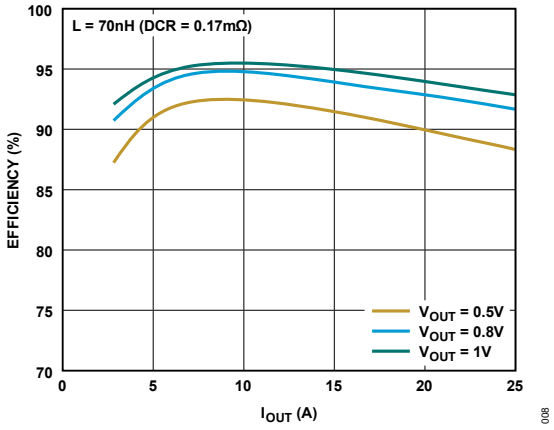


Figure 5. Efficiency vs. Load Current (1MHz)

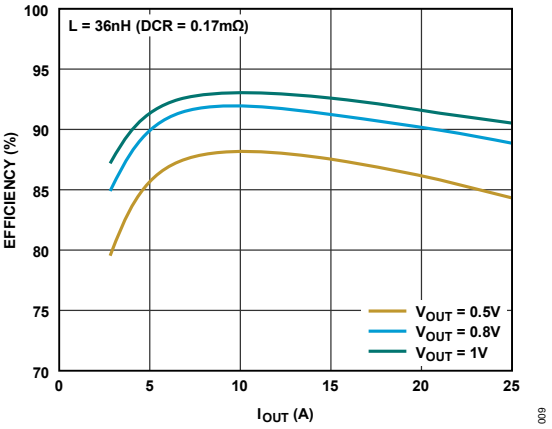


Figure 6. Efficiency vs. Load Current (2MHz)

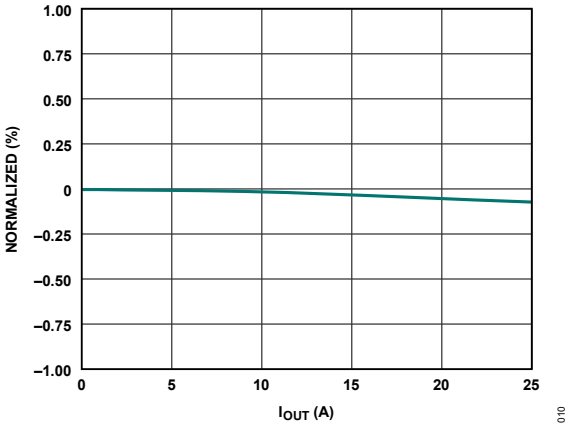


Figure 7. Load Regulation vs. Load Current

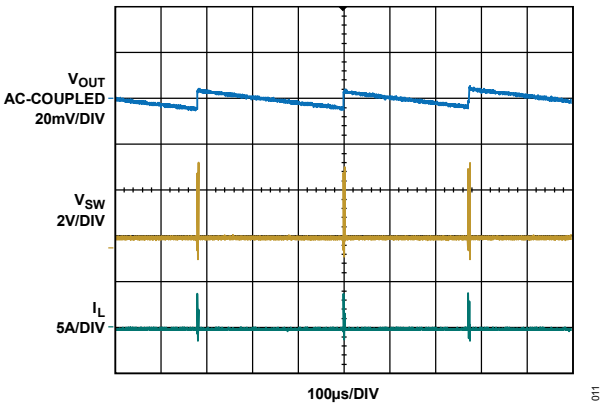


Figure 8. Discontinuous Mode (DCM) Operation

V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 0A, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF

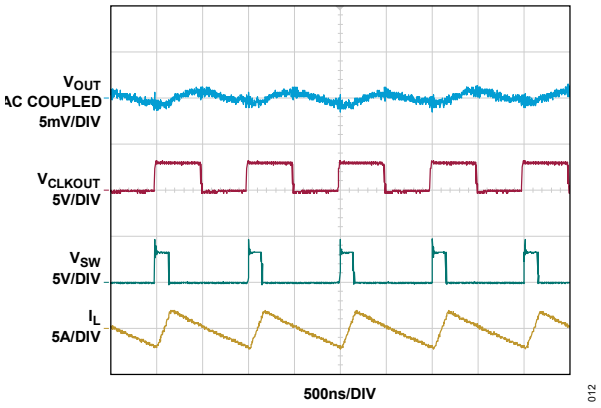


Figure 9. Forced Continuous Mode (FCM) Operation

V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 0A, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF

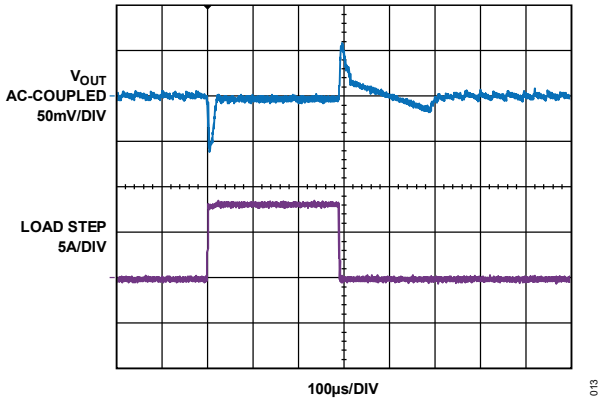


Figure 10. Transient Response, DCM

V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 50mA to 8A, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF

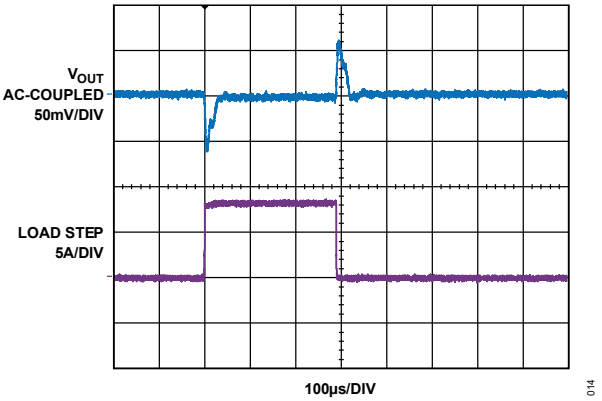


Figure 11. Transient Response, FCM

V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 50mA to 8A, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF

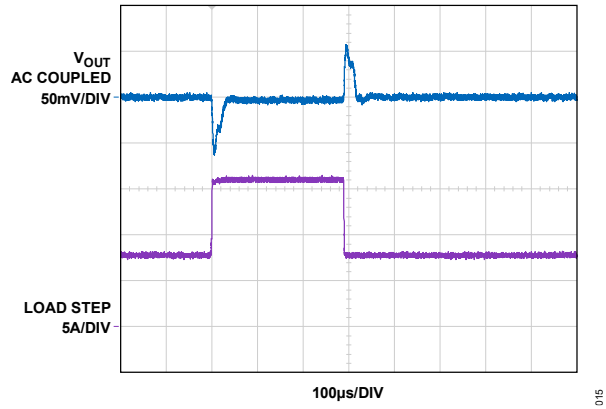


Figure 12. Transient Response, FCM

V_{IN} = 3.3V, V_{OUT} = 0.5V, I_{OUT} = 8A to 16A, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 1kΩ, C_{ITH} = 10nF

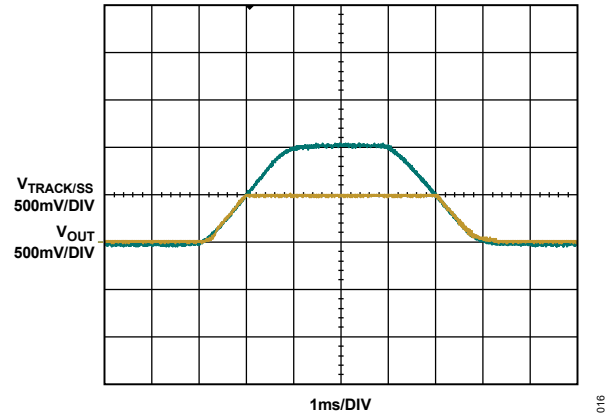


Figure 13. Output Tracking

V_{IN} = 3.3V, V_{OUT} = 0.5V, R_{OUT} = 0.1Ω, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF

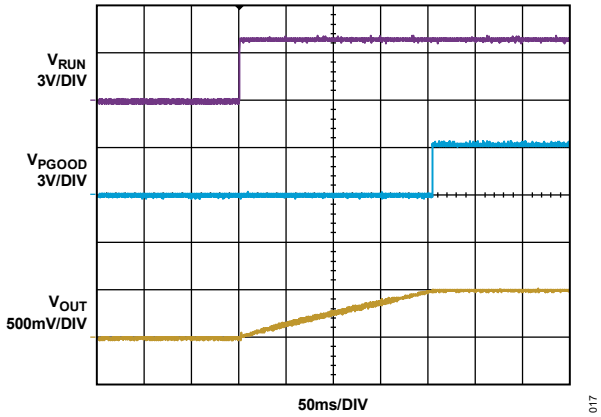


Figure 14. Start-up Waveform

V_{IN} = 3.3V, V_{OUT} = 0.5V, R_{OUT} = 0.1Ω, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF
$C_{TRACK/SS}$ = 4.7µF

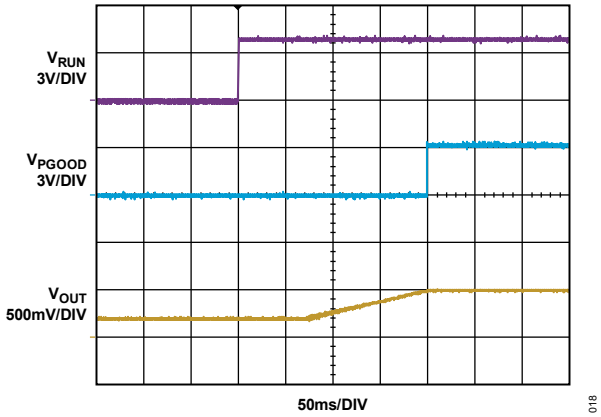


Figure 15. Start-up Waveform (with Prebiased Output)

V_{IN} = 3.3V, V_{OUT} = 0.5V, R_{OUT} = 0.1Ω, f_{SW} = 1MHz
L = 70nH, C_{OUT} = 5x100µF, R_{ITH} = 2kΩ, C_{ITH} = 10nF
$C_{TRACK/SS}$ = 4.7µF

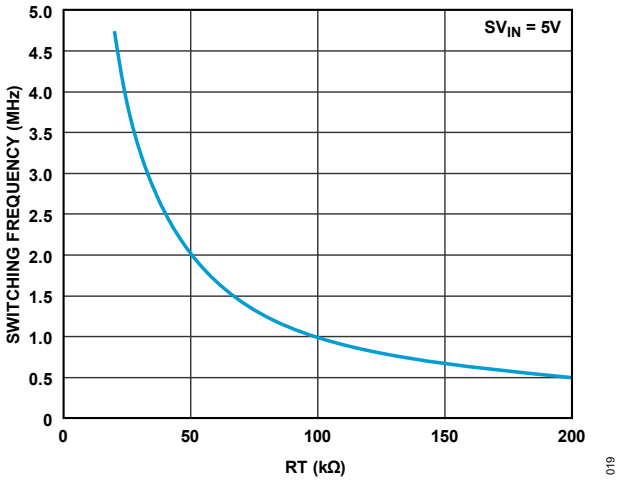


Figure 16. Switching Frequency vs. RT

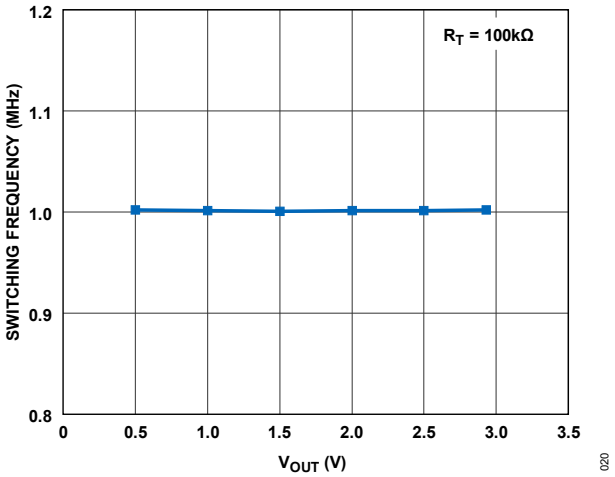


Figure 17. Switching Frequency vs. V_{OUT}

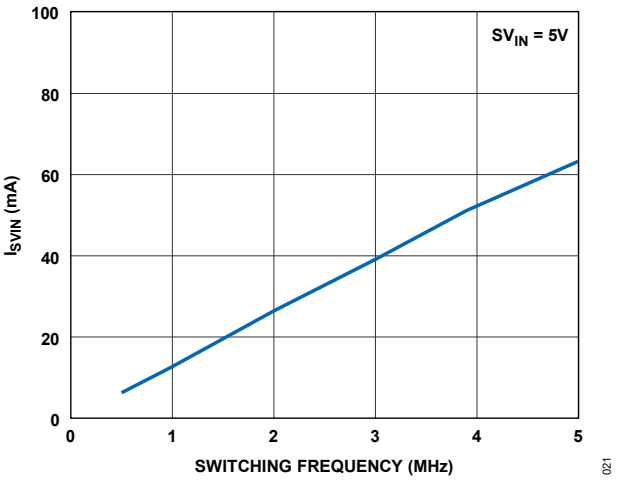


Figure 18. SV_{IN} Current vs. Switching Frequency, CCM

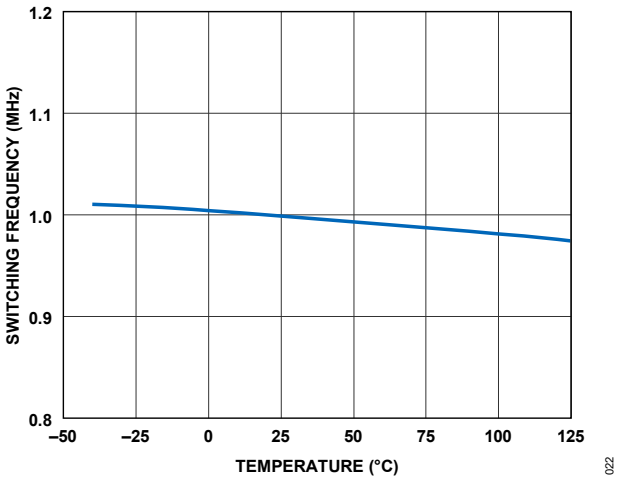


Figure 19. Switching Frequency vs. Temperature

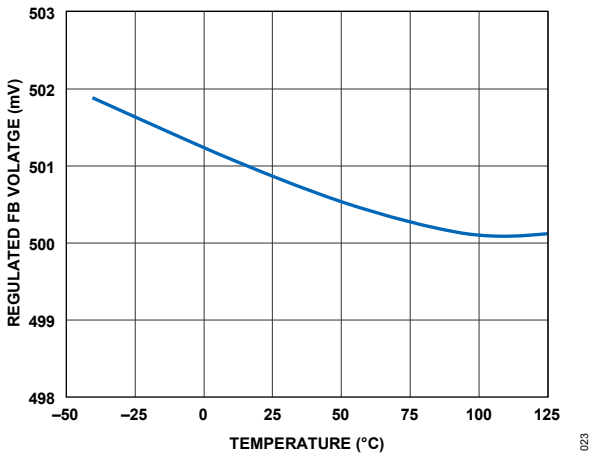


Figure 20. Regulated FB Voltage vs. Temperature

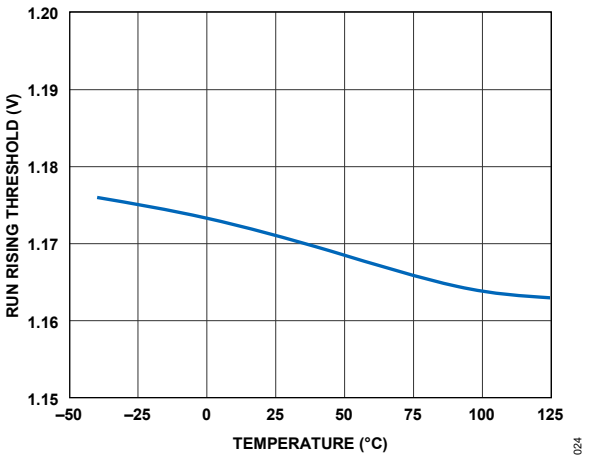


Figure 21. RUN Rising Threshold vs. Temperature

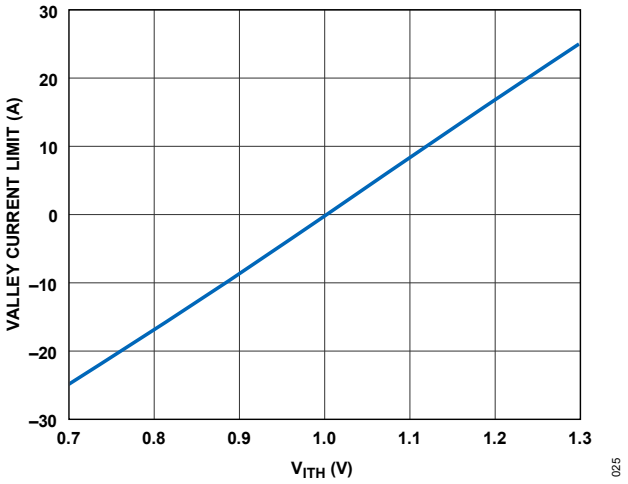


Figure 22. Valley Current Limit vs. V_{ITH}

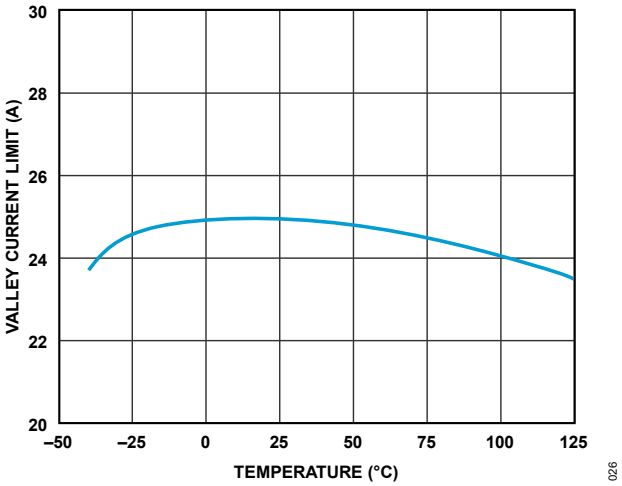


Figure 23. Valley Current Limit vs. Temperature

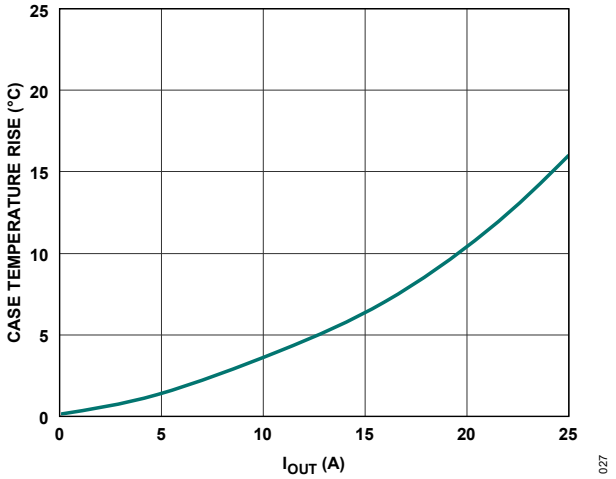


Figure 24. Case Temperature vs. Load

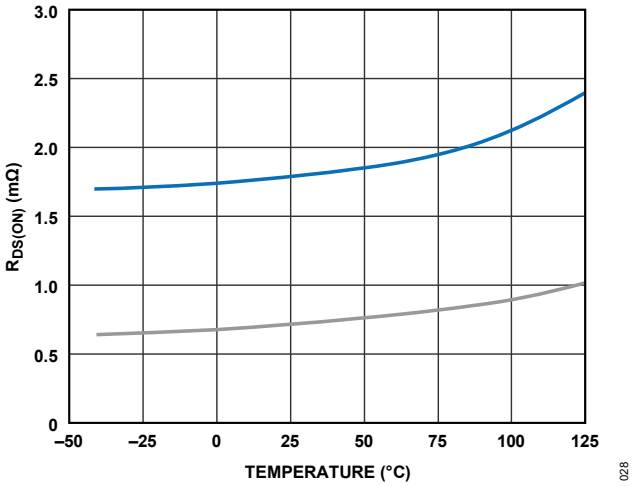


Figure 25. $R_{DS(ON)}$ vs. Temperature

BLOCK DIAGRAM

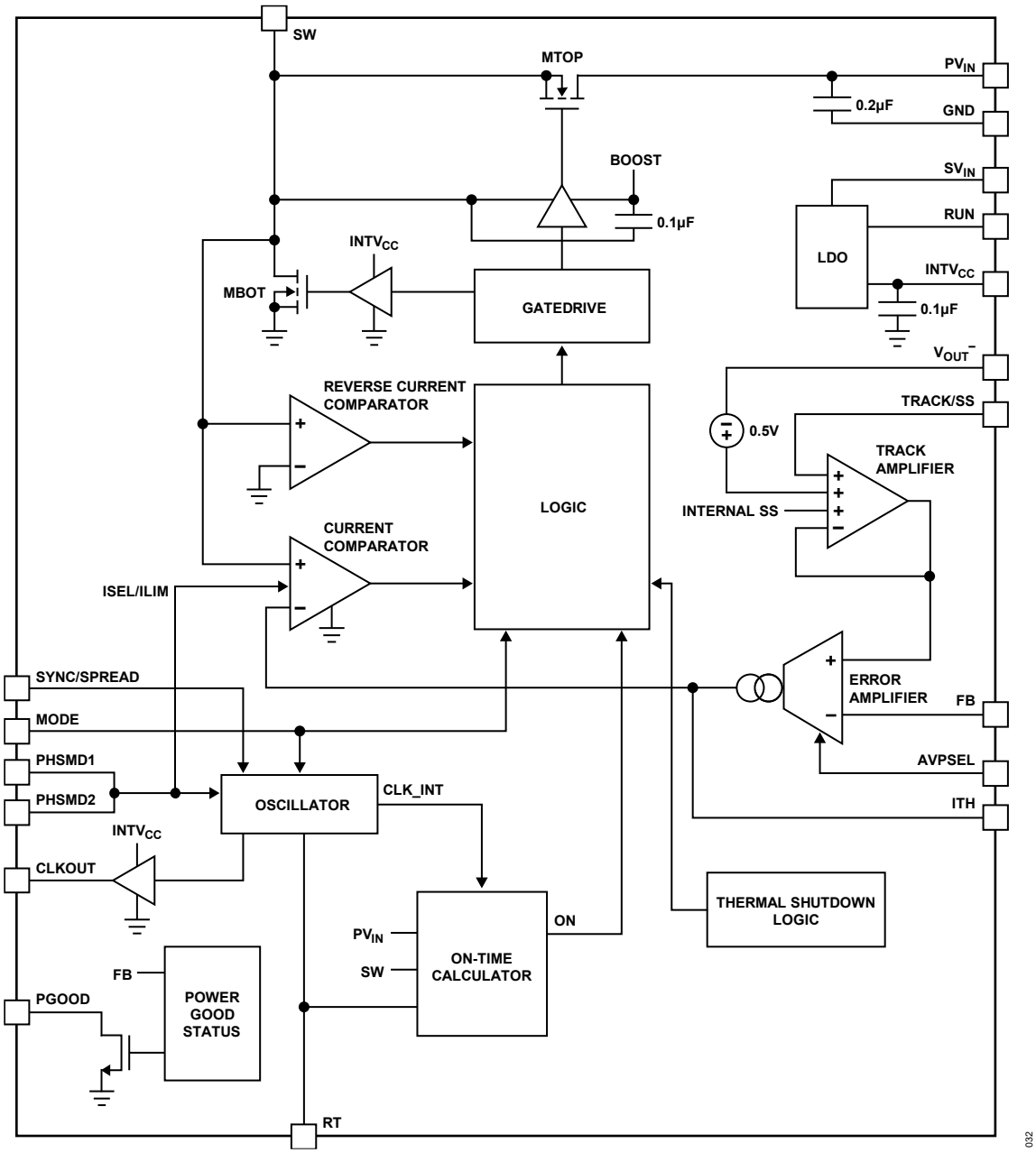


Figure 26. Block Diagram

THEORY OF OPERATION

Main Control Loop

The LT7153SP is a single channel, current-mode monolithic step-down regulator capable of providing ±25A of output current. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer (ON signal in Block Diagram *Figure 26*). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, I_{CMP}, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across SW and GND nodes of the bottom power MOSFET when it is on. The voltage on the ITH pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this ITH voltage by comparing the feedback signal, V_{FB}, with an internal 0.5V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference, the ITH voltage then rises until the average inductor current matches that of the load current.

At light load currents, the inductor current can drop to zero and become negative. In Burst Mode operation, this is detected by the current reversal comparator, I_{REV}, which then shuts off the bottom power MOSFET. Both power MOSFETs remain off with the output capacitor supplying the load current until the ITH voltage rises above zero current level to initiate the next cycle. If continuous mode of operation is desired, simply float the MODE pin or tie it to $INTV_{CC}$.

The operating frequency is determined by the value of the R_{RT} resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the switching regulator on-time to track the internal oscillator and force a constant switching frequency. A clock signal can be applied to the SYNC/SPREAD pin to synchronize the switching frequency to an external clock. The regulator defaults to force continuous operation once the clock signal is present.

The S in LT7153SP refers to the second-generation Silent Switcher technology. The IC has integrated ceramic capacitors for V_{IN}, $INTV_{CC}$, and BOOST to keep all the fast AC current loops small, thus improving the EMI performance. Furthermore, it allows for faster switching edges, which greatly improves efficiency at high switching frequencies.

Low I_Q Shutdown (RUN)

Pulling the RUN pin to ground forces the LT7153SP into its shutdown state, drawing very little current. Bringing RUN above 0.6V turns on the internal reference while keeping the MOSFETs off. Further increasing RUN above the RUN rising threshold of 1.2V nominal, the entire chip turns on. The accurate 1.2V RUN threshold allows programming the SV_{IN} under voltage lockout threshold externally using a resistor divider.

$INTV_{CC}$ Regulator and Bypass Capacitor

An internal low dropout regulator produces the 3.6V supply that powers the drivers and internal bias circuitry. A 10µF ceramic capacitor should be used to bypass $INTV_{CC}$ to ground; 4.7µF is the minimum value recommended. Good bypassing is necessary to supply the high transient currents required by the MOSFET drivers.

For applications running high frequency and high output currents, increased switching currents may result in higher die temperatures due to higher power dissipation across the LDO. In such cases, consider shorting $INTV_{CC}$ to SV_{IN}. SV_{IN} can be a 3.3V or 5V rail, but be aware that 5V operation results in higher switching losses, which will be more critical at higher switching frequencies. PV_{IN} and SV_{IN} do not have to be tied to the same potential, so an external 3.3V supply can be used to power SV_{IN} if one is available. When biasing SV_{IN} and PV_{IN} from different potentials, the two supplies are required to be sequenced such that SV_{IN} is up before PV_{IN} powers up and that PV_{IN} is powered down first.

Adjustable Current Limit

The current limit setting of the LT7153SP can be lowered to 70% or 55% of its full value for applications that do not require the full 25A capability. The state of the two-phase mode pins (PHSMD1/ISEL, PHSMD2/ILIM) determines the current limit setting. See *Table 1* for details.

Overcurrent and Short-Circuit Protection

The LT7153SP has a cycle-by-cycle overcurrent protection scheme by sensing the inductor valley current. When the current limit is reached, the output begins to fall, decreasing the on-time of the top power MOSFET. If the short is prolonged enough for the on-time to reach its minimum, the off-time lengthens, lowering the switching frequency and preventing excess current from being drawn from V_{IN}. After the overcurrent or short is removed, the regulator executes its soft-start function to prevent the output voltage from overshooting.

Multiphase Operation

For output loads that demand more than 25A of current, multiple the LT7153SP outputs can be tied together to run out of phase to provide more output current. See *Table 1* and *Figure 28* for more information. The LT7153SP not only varies the phasing between the internal oscillator and CLKOUT, but it also varies the phasing between the external clock and the internal oscillator, allowing shorted signal chains to minimize accumulating clock jitter.

Power Good Status Output

PGOOD open-drain output is pulled low if the regulator output feedback voltage, V_{FB}, exits a ±6.5% window around the regulation point while the overvoltage (OV) or undervoltage (UV) comparator is tripped. This condition is released once regulation within a ±6.5% window is achieved.

Continuous operation is forced during OV and UV conditions, except during start-up when the TRACK/SS pin is ramping up to 0.5V.

V_{IN} Overvoltage Protection

To protect the internal power MOSFET devices against transient voltage spikes, the LT7153SP constantly monitors the PV_{IN} pin for an overvoltage condition. When the PV_{IN} rises above 8V, the regulator suspends operation by shutting off both power MOSFETs. Once PV_{IN} drops below 7.5V, the regulator immediately resumes normal operation. During an overvoltage event, the internal soft-start voltage is clamped to a voltage slightly higher than the feedback voltage. Thus, the soft-start feature is present upon exiting an overvoltage condition.

Selectable Load Line (AVPSEL)

In order to minimize the amount of output capacitance needed, the LT7153SP allows to pick two different load line settings, in addition to a flat load line setting. Load line settings are accessed via the AVPSEL pin state: flat load line setting when this pin is tied to ground, 1% when floated, and 1.5% when tied to $INTV_{CC}$.

MODE, SYNC, Spread-Spectrum Operation

Connecting the MODE pin to ground enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE pin is tied to INTVcc or floated, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency.

The SYNC/SPREAD pin is a dual-function pin. This pin allows the LT7153SP to sync to an external clock signal and also to activate or deactivate its spread spectrum feature. The LT7153SP detects the presence of the external clock signal on the SYNC/SPREAD pin and synchronizes the internal oscillator to the frequency of the incoming clock. Phasing between the SYNC input and the internal oscillator is determined by the states of the two phase mode pins (PHSMD1/ISEL, PHSMD2/ILIM). When the SYNC/SPREAD pin is tied to INTVcc or floated, spread-spectrum operation is enabled. The LT7153SP varies its frequency between the preset frequency and 20% higher than the preset value. When the SYNC/SPREAD pin is tied to ground, frequency spreading is disabled.

APPLICATIONS INFORMATION

A simplified LT7153SP application circuit is shown on the first page of the data sheet. External component selection is largely driven by the target current ripple, load requirement, and switching frequency. Component selection typically begins with the selection of the inductor L and resistor R_{RT}. Once the inductor is chosen, select the input capacitor, C_{IN}, and the output capacitor, C_{OUT}. Next, select the feedback resistors to set the desired output voltage. Finally, select the remaining optional external components for functions such as external loop compensation, tracking/soft-start, input UVLO, and PGOOD.

Silent Switcher Architecture

The LT7153SP has integrated capacitors that allow it to operate at high switching frequencies efficiently. The internal V_{IN} bypass capacitors allow the SW edges to transition extremely fast, effectively reducing transition loss. The capacitors also greatly reduce SW overshoot during top FET turn-on, which improves the robustness of the device over time.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductors and capacitors. Operating at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductances and capacitances to maintain low output ripple voltage.

Connecting a resistor, R_{RT}, from the RT pin to SGND programs the switching frequency, f_{SW}, from 400kHz to 5MHz according to the following formula:

$$f_{SW}(Hz) = \frac{1e^{11}}{R_{RT}(\Omega)}$$

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the R_{RT} programmed frequency.

Output Voltage Programming

Each regulator's output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.5V \bullet \left(1 + \frac{R1}{R2}\right)$$

The desired output voltage is set by the appropriate selection of resistors R1 and R2, which allow the V_{FB} pin to sense a fraction of the output voltage, as shown in *Figure 27*. Choosing large values for R1 and R2 results in improved zero/light load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the V_{FB} node. Take care to route the V_{FB} trace away from any noise source, such as SW trace. A feedforward compensation capacitor, C_{FF}, can also be placed between V_{OUT} and FB to improve transient performance.

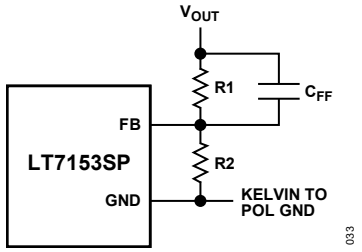


Figure 27.Setting the Output Voltage

If the output voltage is outside the V_{ON} sense range (0.5V ~ 4V), the output voltage stays in regulation, but the switching frequency may deviate from the programmed frequency.

Soft-Start and Output Voltage TRACK

An internal 10µA pulls up the TRACK pin to $INTV_{cc}$. Putting an external capacitor, C_{SS}, from TRACK to ground enables soft starting the output to prevent a current surge on the input supply. The relationship between output rise time, T_{SS}, and soft-start capacitance, C_{SS}, is given by:

$$T_{SS} = 0.5e^5 \bullet C_{SS}$$

Upon start-up time, the LT7153SP operates in discontinuous mode until track voltage is higher than 0.5V. The regulator then operates in forced continuous mode until output is above the UV threshold (V_{FB} > 0.475V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE pin as described above.

The LT7153SP allows the user to program its output voltage ramp rate through the TRACK pin. From 0V to 0.5V, the TRACK voltage overrides the internal 0.5V reference input to the error amplifier, thus regulating the feedback voltage to that of the TRACK pin. When TRACK is above 0.5V, tracking is disabled, and the feedback voltage regulates to the internal reference voltage.

Inductor Selection

For a given input voltage, V_{IN}, output voltage, V_{OUT}, the inductor value, L, and operating frequency, f, determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor current ripple decreases with higher inductor value and higher operating frequency. Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Exceeding 60% of $I_{OUT(MAX)}$ is not recommended. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f_{SW} \bullet \Delta L_{(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire leading to increased DCR and copper losses.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

To avoid overheating and poor efficiency, choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of inductor ripple current:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Different core materials and shapes change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost

more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements.

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, use a low ESR input capacitor sized for the maximum RMS current. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where:

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \bullet \left(\frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} + ESR\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it is important to only use types that are surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Since the ESR of a ceramic capacitor is so low, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, five cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about three times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately.

$$C_{OUT} = 3 \bullet \left(\frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}\right)$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high Q characteristics of some types of ceramic capacitors, take care when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Choose X8R for 150°C applications. More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 47µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PV_{IN} and GND pins as possible.

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LT7153SP is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 30ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached due to a dropping input voltage, for example, then the output drops out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \bullet \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its ON state. This time is typically 15ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of

$$DC_{(MIN)} = f_{SW} \bullet t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is the minimum on-time. Reducing the operating frequency alleviates the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage remains in regulation and the switching frequency decreases from its programmed value. This is an acceptable result in many applications. So, this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of output overvoltage. As the sections on inductors and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

Multiphase Configuration

Polyphase operation allows multiple LT7153SP regulators to run out of phase, 2, 3, 4, 6, 8 or 12 Phases (see *Figure 28*), which reduces the amount of input and output capacitors needed while enables paralleling for higher output currents. By setting up PHASE1/SEL and PHSMD2/ILIM pin (see *Table 4*), it determines the phase relationship between the internal oscillator and CLKOUT and between the internal oscillator and SYNC.

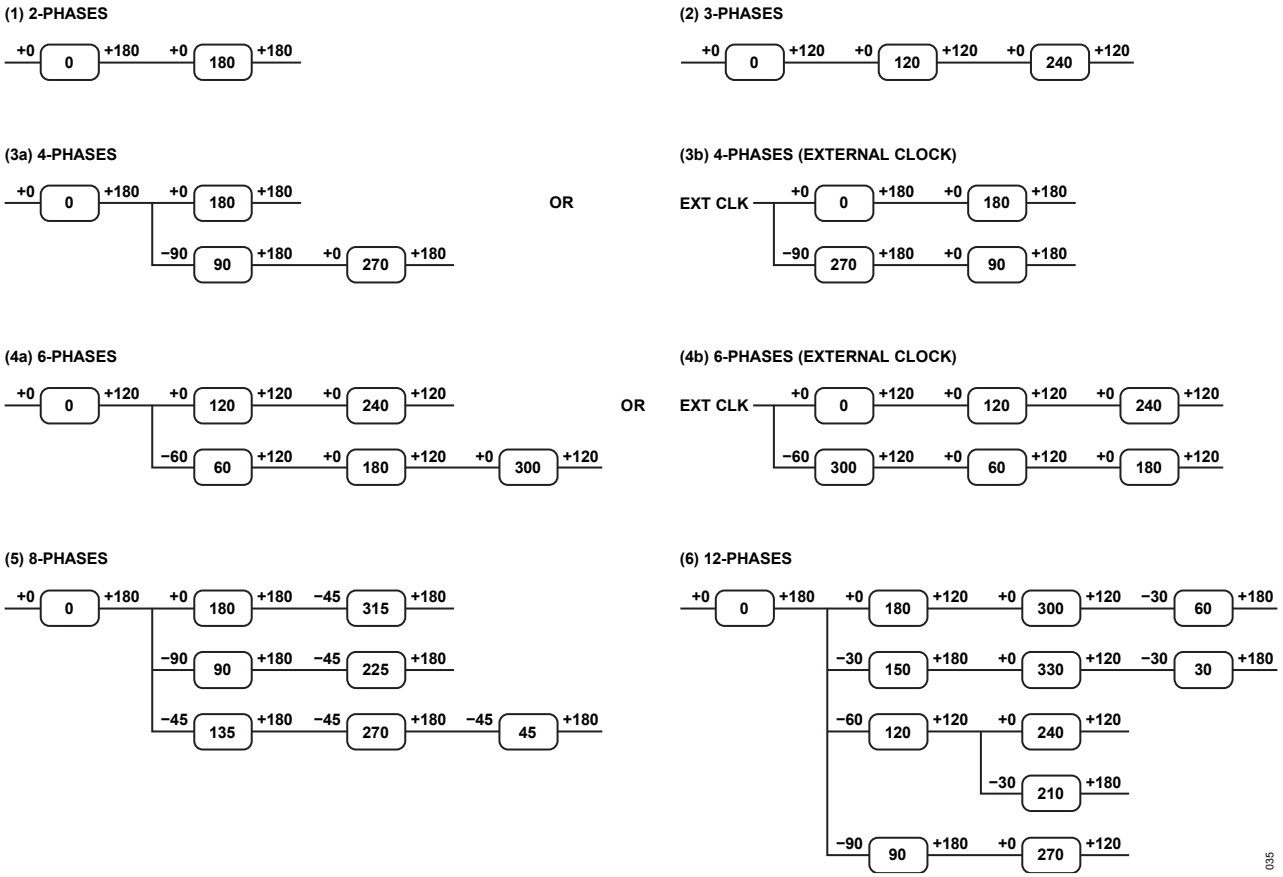


Figure 28. 2, 3, 4, 6, 8, 12 Multiphase Configuration

Table 4. Multiphase Pin Configuration

SYNC to Oscillator	$\phi_{(SYNC\ to\ OSC)}$	PHSMD1 = 0, PHSMD2 = 0	0	Degree
		PHSMD1 = $INTV_{CC}$, PHSMD2 = 0	0	
		PHSMD1 = 0, PHSMD2 = $INTV_{CC}$/2	-30	
		PHSMD1 = $INTV_{CC}$, PHSMD2 = $INTV_{CC}$/2	-45	
		PHSMD1 = 0, PHSMD2 = $INTV_{CC}$	-60	
		PHSMD1 = $INTV_{CC}$, PHSMD2 = $INTV_{CC}$	-90	
Oscillator to CLKOUT	$\phi_{(OSC\ to\ CLKOUT)}$	PHSMD1 = 0, PHSMD2 = 0	180	Degree
		PHSMD1 = $INTV_{CC}$, PHSMD2 = 0	120	
		PHSMD1 = 0, PHSMD2 = $INTV_{CC}$/2	180	
		PHSMD1 = $INTV_{CC}$, PHSMD2 = $INTV_{CC}$/2	180	
		PHSMD1 = 0, PHSMD2 = $INTV_{CC}$	120	
		PHSMD1 = $INTV_{CC}$, PHSMD2 = $INTV_{CC}$	180	

ITH Compensation

Proper ITH components should be selected for OPTI-LOOP® optimization. The compensation network is shown in *Figure 29*. The RC filter sets the dominant pole-zero loop compensation. The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency is kept the same, thereby keeping the phase the same in most critical frequency ranges of the feedback loop.

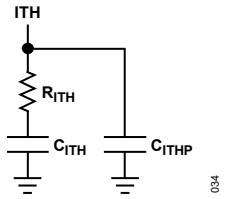


Figure 29. External Compensation Network

For a 1MHz application, an R-C network of 4.7nF and 2kΩ provides a good starting point. A 4.7pF bypass capacitor, C_{ITHP}, on the ITH pin is recommended for the purposes of filtering out high frequency coupling from stray board capacitance. *Table 5* provides a basic guideline for the compensation values to use, given the frequency of the part. Slight tweaks to those values may be required depending on the amount of output capacitance used in the application.

Table 5. Compensation Values

Frequency	R_{ITH}	C_{ITH}	C_{THP}
1MHz	2k	4.7nF	4.7pF
2MHz	2k	2.2nF	4.7pF

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows for optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed loop response test point. The DC step, rise time, and settling at this test point truly reflects these close loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external component shown in the *Table 5* circuit provides an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested value) to optimize transient response once the final PCB layout is done and the particular output capacitor type and value are determined. Select the output capacitors because their various types and values determine the loop feedback factor gain and phase. In addition, add a feedforward capacitor C_{FF} to improve the high frequency response, as shown in *Figure 29*. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2, which improves the phase margin.

An output current pulse of 20% to 100% of full load current having a rise time of ~1µs produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop. Switching regulators may take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the $\Delta I_{LOAD} \times$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that indicates a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance. For detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Analog Devices Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>47µF) input capacitors. The discharge input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Thermal Conditions

In some applications where the LT7153SP is operated at a combination of high ambient temperature, high switching frequency, high V_{IN}, and high output load, the required power dissipation might push the part to exceed its maximum junction temperature. To avoid the LT7153SP from exceeding the maximum junction temperature, maximum current rating is derated depending on the operating conditions. The temperature rise of the part varies depending on the thickness of copper on the PCB board, the number of layers of the board, and the shape of copper trace. In general, a thick continuous piece of copper on the top layer of the PCB for SW and GND pins greatly improves the thermal performance of the part.

The LT7153SP offers exposed die back on the package top for heat sink mount. This option provides the capability to improve thermal performance for the same load if an appropriately sized heat sink is mounted correctly on the package. *Figure 31* shows case temperature rise of the LT7153SP on a standard 6-layer, 2oz copper per layer PCB board (standard demo board).

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change produces the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (\text{L1} + \text{L2} + \text{L3} + \cdots)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LT7153SP circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is chopped between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

$$I^2R \text{ losses} = {I_{OUT}}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from PV_{IN} to ground. The resulting dQ/dt is a current out of IN that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs, and f is the switching frequency. The power loss is thus:

$$\text{Switching Loss} = I_{GATECHG} \bullet PV_{IN}$$

   The gate charge loss shows up as current through the $INTV_{CC}$ pin as well as frequency. Thus, their effects are more pronounced in applications with higher input voltage and higher frequency.

3. Other hidden losses such as transition loss, copper trace, and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these system level losses in the system design. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LT7153SP internal power devices switch quickly enough that these losses are not significant compared to other sources. Other losses including diode conduction losses during dead-time and inductor core losses, which generally account for less than 2% total additional loss.

Design Example

As a design example, consider the LT7153SP in an application with the following specifications:

V_{IN} = 3.3V to 5V

V_{OUT} = 0.875V

$I_{OUT(MAX)}$ = 25A

f_{SW} = 2MHz

First, to program the output to 0.875V, set R2 to be 10kΩ and R1 to be 7.5kΩ, per *Figure 27*. For best accuracy, use a 0.1% resistor.

For a typical soft-start time of 4ms (0% to 100% of final V_{OUT} value), the C_{SS} should be:

$$10\mu A = C_{SS} \bullet \frac{0.875V}{4ms}$$

C_{SS} = 46nF

Use a typical 47nF capacitor for C_{SS}.

Because efficiency is important at both high and low load current, discontinuous mode operation is utilized. Select from the characteristic curves the correct R_T resistor for the 2MHz switching frequency. Based on that, R_{RT} should be 50kΩ. Then calculate the inductor value to achieve a current ripple that is about 40% of the maximum peak current limit (25A) at maximum V_{IN}:

$$L = \frac{V_{OUT}}{f_{SW} \bullet \Delta L_{(MAX)}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$L = \frac{0.875V}{2MHz \bullet 10A} \bullet \left(1 - \frac{0.875V}{5V}\right) = 36nH$$

The closest standard value inductor is 36nH.

Select C_{OUT} based on the ESR that is required to satisfy the output ripple requirement and the bulk capacitance needed for loop stability. For this design, use two 100µF and two 220µF ceramic capacitors.

$$\Delta V_{OUT} < \Delta I_L \bullet \left(\frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} + ESR\right)$$

Size C_{IN} for a maximum current rating of:

$$I_{RMS} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet Sqrt\left(\frac{V_{IN}}{V_{OUT}} - 1\right)$$

$$I_{RMS} = 25A \bullet (0.875V/5V) \bullet ((5V/0.875V) - 1)^{1/2} = 9.5A$$

Decoupling V_{IN} with two 47µF ceramic capacitor, as shown in *Figure 30*, is adequate for most applications.

Board Layout Considerations

When laying out the printed circuit board, use the following checklist to ensure proper operation of the LT7153SP (see *Figure 30*). Check the following in the layout:

1. Place the capacitors C_{IN} connect to the PV_{IN} and GND as close as possible. These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Place the FB dividers close to the part with kelvin connections to V_{OUT} and GND at the point of load.
4. Keep sensitive components away from the SW pin. Route the FB resistors, RT resistor, the compensation component, and the $INTV_{cc}$ bypass caps away from the SW trace and the inductor.
5. A ground plane is preferred.
6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. Connect these copper areas to GND.

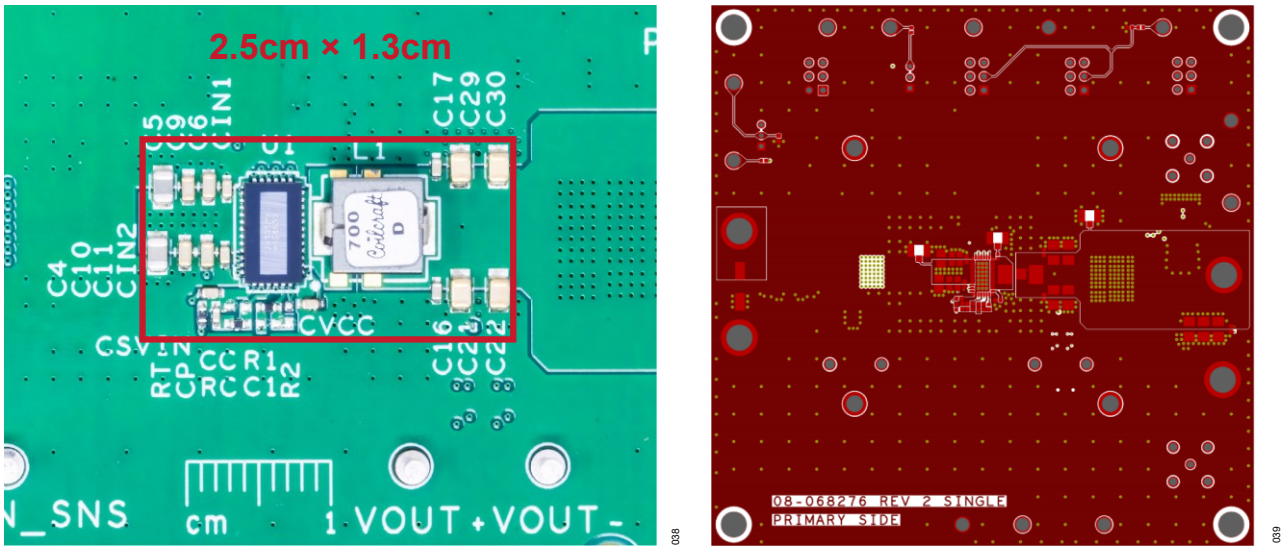


Figure 30. Example of Top Layer PCB Design

TYPICAL APPLICATIONS

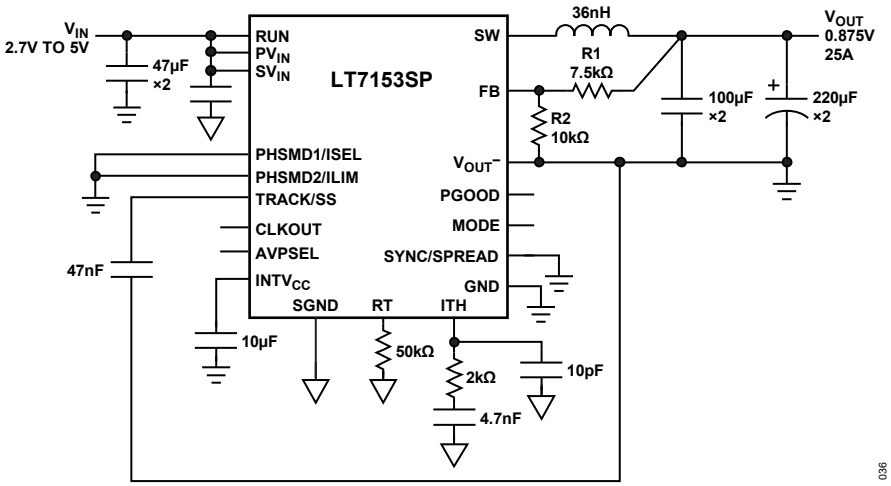


Figure 31. 0.875V/25A, 2MHz, Step-Down Converter (with 1% Load Line)

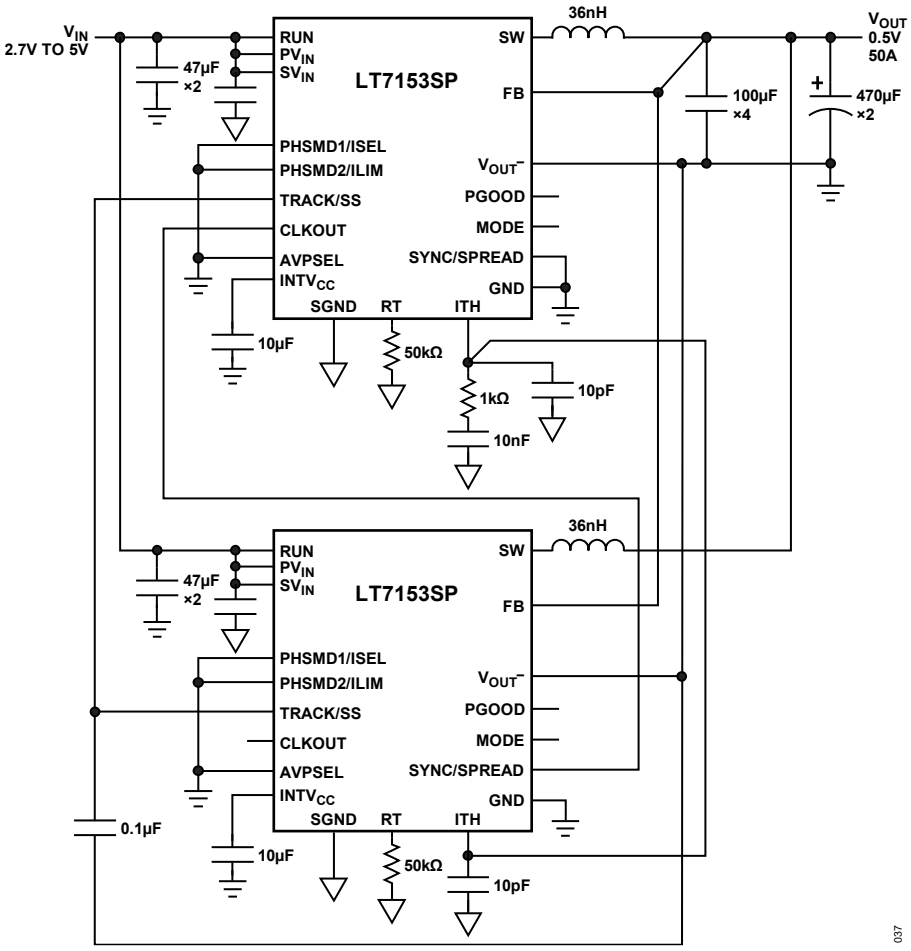
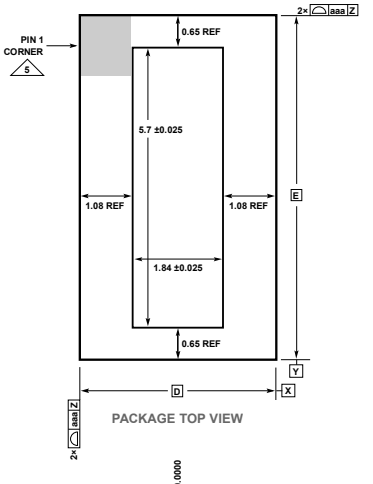
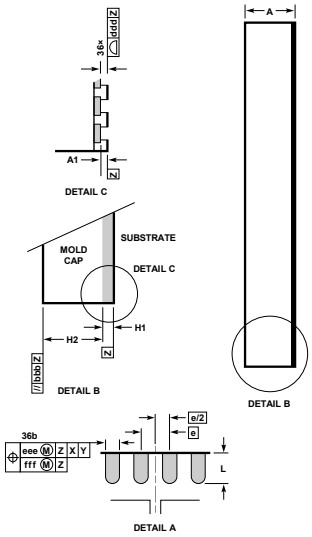


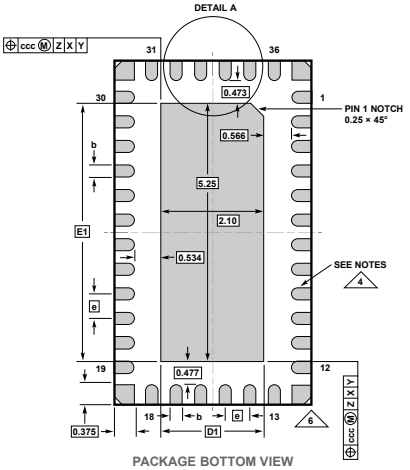
Figure 32. High Efficiency, Dual Phase 0.5V/50A, 2MHz, Step-Down Converter

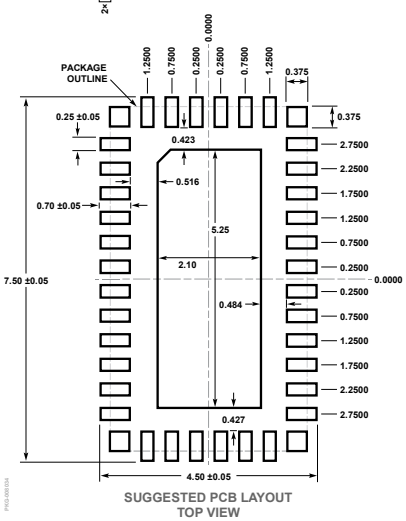
OUTLINE DIMENSIONS

36-Terminal Land Grid Array [LGA]
(7mm x 4mm x 1.02mm)
(Reference DWG # CC-36-3)



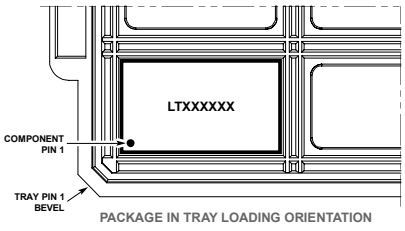






DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.92	1.02	1.12	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		7.00		
D1		2.10		
E1		5.25		
e		0.50		
H1		0.32 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. CORNER SUPPORT PAD CHAMFER IS OPTIONAL



ORDERING GUIDE

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	FINISH CODE	PAD FINISH	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LT7153SPAV#TRMPBF	LT7153SPAV#TRPBF	7153SPV	E4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C

- Parts ending with PBF are RoHS and WEEE compliant.
- Pad and ball finish code is per IPC/JEDEC J-STD-609.
- Temperature grades are identified by a label on the shipping container. Contact the factory for parts specified with wider operating temperature ranges.
- TRM = 500 pieces.
- ***Recommended PCB Assembly and Manufacturing Procedures***.
- ***Package and Tray Drawings***.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT7200S	18V, Quad ±5A/Quad Phase ±20A Silent Switcher®2 Step-Down Regulator	2.9V < V_{IN} < 18V, 0.5V < V_{OUT} < 0.9V_{IN}, 96% Maximum Efficiency, 5mm x 6mm LQFN-48 Package
LTC7150S	20V, 20A Synchronous Step-Down Regulator	3.1V < V_{IN} < 20V, 0.6V < V_{OUT} < 5.5V, 96% Maximum Efficiency, 5mm × 6mm BGA Package
LTC3605/ LTC3605A	20V, 5A Synchronous Step-Down Regulator	4V < V_{IN} < 20V, 0.6V < V_{OUT} < 20V, 96% Maximum Efficiency, 4mm × 4mm QFN-24 Package
LTC3613	24V, 15A Monolithic Step-Down Regulator with Differential Output Sensing	4.5V < V_{IN} < 24V, 0.6V < V_{OUT} < 5.5V, 0.67% Output Voltage Accuracy, Valley Current Mode, Programmable from 200kHz to 1MHz, Current Sensing, 7mm × 9mm QFN-56 Package
LTC3622	17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current	2.7V < V_{IN} < 17V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 3mm × 4mm DFN-14 and MSOP-16 Package
LTC3623	15V, ±5A Rail-to-Rail Synchronous Buck Regulator	4V ≤ V_{IN} ≤ 15V, 96% Maximum Efficiency, 3mm × 5mm QFN Package
LTC3624	17V, 2A Synchronous Step-Down Regulator with 3.5µA Quiescent Current	2.7V < V_{IN} < 17V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 3.5µA I_Q, Zero-Current Shutdown, 3mm × 3mm DFN-8 Package
LTC3633A/ LTC3633A-1	Dual Channel 3A, 20V Monolithic Synchronous Step-Down Regulator	3.6V < V_{IN} < 20V, 0.6V < V_{OUT} < V_{IN}, 95% Maximum Efficiency, 4mm × 5mm QFN-28 and TSSOP-28 Package
LTM4639	Low V_{IN} 20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, 2.375V < V_{IN} < 7V, 0.6V < V_{OUT} < 5.5V, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA Package
LTM4637	20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, 4.5V < V_{IN} < 20V, 0.6V < V_{OUT} < 5.5V, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA or LGA Package
LTC7130	20V, 20A Monolithic Buck Converter with Ultralow DCR Sensing	4.5V < V_{IN} < 20V, 95% Maximum Efficiency, Optimized for Low Duty Cycle Applications, 6.25mm × 7.5mm BGA Package
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2	2.8V < V_{IN} < 18V, 0.6V < V_{OUT} < V_{IN}, 96% Maximum Efficiency, 4mm × 4mm 0.94mm LQFN Package