Quad-Channel, Digital Isolators, Enhanced System-Level ESD Reliability

Enhanced Product

ADuM3400-EP/ADuM3401-EP/ADuM3402-EP

FEATURES

- Enhanced system-level ESD performance per IEC 61000-4-x
- Low power operation
  - 5 V operation
    - 1.4 mA per channel maximum at 0 Mbps to 2 Mbps
    - 4.3 mA per channel maximum at 10 Mbps
  - 3.3 V operation
    - 0.9 mA per channel maximum at 0 Mbps to 2 Mbps
    - 2.4 mA per channel maximum at 10 Mbps
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

ENHANCED FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- General-purpose multichannel isolation
- SPI/data converter isolation
- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM3400-EP/ADuM3401-EP/ADuM3402-EP[1] are 4-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

The ADuM3400-EP/ADuM3401-EP/ADuM3402-EP isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 3.135 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier.

[1] Protected by US Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

FUNCTIONAL BLOCK DIAGRAMS

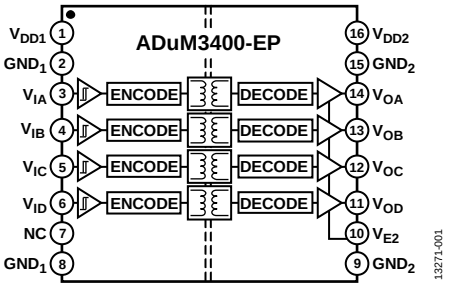

Figure 1. ADuM3400-EP Functional Block Diagram

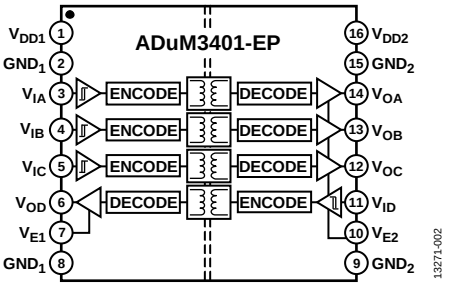

Figure 2. ADuM3401-EP Functional Block Diagram

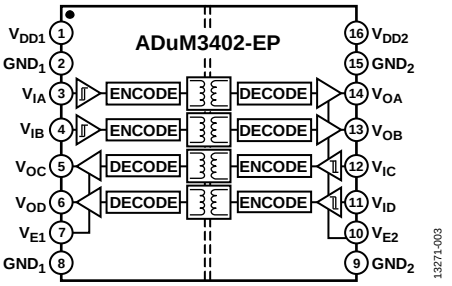

Figure 3. ADuM3402-EP Functional Block Diagram

The ADuM3400-EP/ADuM3401-EP/ADuM3402-EP isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

The ADuM3400-EP/ADuM3401-EP/ADuM3402-EP isolators contain various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD/burst/surge). The precise capability in these tests is determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products*.

Additional application and technical information can be found in the ADuM3400/ADuM3401/ADuM3402 data sheet.

Rev. A Document Feedback

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REVISION HISTORY

5/2017—Rev. 0 to Rev. A

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Changes to Regulatory Information Section and Table 5 ... 9

7/2015—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V and 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.57	0.83	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.29	0.35	mA	
ADuM3400-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.9	3.5	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		9.0	11.6	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		3.0	5.5	mA	5 MHz logic signal frequency
ADuM3401-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		2.5	3.2	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		1.6	2.4	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		7.4	10.6	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		4.4	6.5	mA	5 MHz logic signal frequency
ADuM3402-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		2.0	2.8	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		6.0	7.5	mA	5 MHz logic signal frequency
For All Models						
Input Leakage per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{Ex} Input Pull-Up Current	I_{PU}	−10	−3			V_{Ex} = 0 V
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	5.0		V	I_{Ox}[2] = −20 µA, V_{Ix} = V_{IxH}[3]
	V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.4	4.8		V	I_{Ox}[2] = −4 mA, V_{Ix} = V_{IxH}[3]
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, V_{Ix} = V_{IxL}[4]
	V_{OCL}, V_{ODL}		0.04	0.1	V	I_{Ox}[2] = 400 µA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, V_{Ix} = V_{IxL}[4]
SWITCHING SPECIFICATIONS						
Minimum Pulse Width	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}	20	32	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\|t_{PLH} - t_{PHL}\|$	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel to Channel Matching						
Codirectional Channels	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Opposing Directional Channels	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
For All Models						
Output Propagation Delay						
Disable (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Enable (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity						
Logic High Output[5]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[5]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Dynamic Supply Current per Channel[6]						
Input	$I_{DDI (D)}$		0.20		mA/Mbps	
Output	$I_{DDO (D)}$		0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400-EP/ADuM3401-EP/ADuM3402-EP channel configurations.
[2] I_{Ox} is the Channel x output current, where x = A, B, C, or D.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining the output voltage (V_{OUT}) > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OUT} < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[6] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.135 V ≤ V_{DD1} ≤ 3.6 V and 3.135 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 3.3 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$		0.31	0.49	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$		0.19	0.27	mA	
ADuM3400-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.6	2.1	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.8	7.1	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.8	2.3	mA	5 MHz logic signal frequency
ADuM3401-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.4	1.9	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.1	5.6	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.5	3.3	mA	5 MHz logic signal frequency
ADuM3402-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		1.2	1.7	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		3.3	4.4	mA	5 MHz logic signal frequency

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
For All Models						
Input Leakage per Channel	I_I	−10	+0.01	+10	µA	$0 V \le V_{Ix} \le V_{DDx}$
V_{Ex} Input Pull-Up Current	I_{PU}	−10	−3			$V_{Ex} = 0 V$
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	3.3		V	I_{Ox}[2] = −20 µA, $V_{Ix} = V_{IxH}$[3]
	V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.4	2.8		V	I_{Ox}[2] = −4 mA, $V_{Ix} = V_{IxH}$[3]
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, $V_{Ix} = V_{IxL}$[4]
	V_{OCL}, V_{ODL}		0.04	0.1	V	I_{Ox}[2] = 400 µA, $V_{Ix} = V_{IxL}$[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, $V_{Ix} = V_{IxL}$[4]
SWITCHING SPECIFICATIONS						
Minimum Pulse Width	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}	20	38	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel to Channel Matching						
Codirectional Channels	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Opposing Directional Channels	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Propagation Delay						
Disable (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Enable (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity[5]						
Logic High Output	$\lvert CM_H \rvert$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output	$\lvert CM_L \rvert$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Dynamic Supply Current per Channel[6]						
Input	$I_{DDI (D)}$		0.10		mA/Mbps	
Output	$I_{DDO (D)}$		0.03		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. section. See Figure 8 through Figure 10 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400-EP/ADuM3401-EP/ADuM3402-EP channel configurations.
[2] I_{Ox} is the Channel x output current, where x = A, B, C, or D.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[6] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per channel supply current for unloaded and loaded conditions.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OR 3.3 V/5 V OPERATION

All voltages are relative to their respective ground. For 5 V/3.3 V operation, 4.5 V ≤ V_{DD1} ≤ 5.5 V and 3.135 V ≤ V_{DD2} ≤ 3.6 V, and for 3.3 V/5 V operation, 3.135 V ≤ V_{DD1} ≤ 3.6 V and 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C; V_{DD1} = 3.3 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.3 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current per Channel, Quiescent	$I_{DDI (Q)}$					
5 V/3.3 V Operation			0.57	0.83	mA	
3.3 V/5 V Operation			0.31	0.49	mA	
Output Supply Current per Channel, Quiescent	$I_{DDO (Q)}$					
5 V/3.3 V Operation			0.29	0.27	mA	
3.3 V/5 V Operation			0.19	0.35	mA	
ADuM3400-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3.3 V Operation			2.9	3.5	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			1.6	2.1	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3.3 V Operation			0.7	1.2	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3.3 V Operation			9.0	11.6	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			4.8	7.1	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3.3 V Operation			1.8	2.3	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			3.0	5.5	mA	5 MHz logic signal frequency
ADuM3401-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3.3 V Operation			2.5	3.2	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			1.4	1.9	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3.3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			1.6	2.4	mA	DC to 1 MHz logic signal frequency
10 Mbps						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3.3 V Operation			7.4	10.6	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			4.1	5.6	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3.3 V Operation			2.5	3.3	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			4.4	6.5	mA	5 MHz logic signal frequency
ADuM3402-EP, Total Supply Current[1]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3.3 V Operation			2.0	2.8	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			1.2	1.7	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3.3 V Operation			1.2	1.7	mA	DC to 1 MHz logic signal frequency
3.3 V/5 V Operation			2.0	2.8	mA	DC to 1 MHz logic signal frequency

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
10 Mbps						
V_{DD1} Supply Current	I_{DD1} (10)					
5 V/3.3 V Operation			6.0	7.5	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			3.3	4.4	mA	5 MHz logic signal frequency
V_{DD2} Supply Current	I_{DD2} (10)					
5 V/3.3 V Operation			3.3	4.4	mA	5 MHz logic signal frequency
3.3 V/5 V Operation			6.0	7.5	mA	5 MHz logic signal frequency
For All Models						
Input Leakage per Channel	I_I	−10	+0.01	+10	µA	$0 V \le V_{Ix} \le V_{DDx}$
V_{Ex} Input Pull-Up Current	I_{PU}	−10	−3			$V_{Ex} = 0 V$
Tristate Leakage Current per Channel	I_{OZ}	−10	+0.01	+10	µA	
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3.3 V Operation		2.0			V	
3.3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3.3 V Operation				0.8	V	
3.3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	(V_{DD1} or V_{DD2}) − 0.1	(V_{DD1} or V_{DD2})		V	I_{Ox}[2] = −20 µA, $V_{Ix} = V_{IxH}$[3]
	V_{OCH}, V_{ODH}	(V_{DD1} or V_{DD2}) − 0.4	(V_{DD1} or V_{DD2}) − 0.2		V	I_{Ox}[2] = −4 mA, $V_{Ix} = V_{IxH}$[3]
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.1	V	I_{Ox}[2] = 20 µA, $V_{Ix} = V_{IxL}$[4]
	V_{OCL}, V_{ODL}		0.04	0.1	V	I_{Ox}[2] = 400 µA, $V_{Ix} = V_{IxL}$[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, $V_{Ix} = V_{IxL}$[4]
SWITCHING SPECIFICATIONS						
Minimum Pulse Width	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay	t_{PHL}, t_{PLH}	15	35	50	ns	C_L = 15 pF, CMOS signal levels
Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel to Channel Matching						
Codirectional Channels	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Opposing Directional Channels	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Propagation Delay						
Disable (High/Low-to-High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Enable (High Impedance-to-High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_f					C_L = 15 pF, CMOS signal levels
5 V/3.3 V Operation			3.0		ns	
3.3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity						
Logic High Output[5]	$\lvert CM_H \rvert$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Logic Low Output[5]	$\lvert CM_L \rvert$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3.3 V Operation			1.2		Mbps	
3.3 V/5 V Operation			1.1		Mbps	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current per Channel[6]	$I_{DDI (D)}$					
Input						
5 V/3.3 V Operation			0.20		mA/Mbps	
3.3 V/5 V Operation			0.10		mA/Mbps	
Output	$I_{DDO (D)}$					
5 V/3.3 V Operation			0.03		mA/Mbps	
3.3 V/5 V Operation			0.05		mA/Mbps	

[1] The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. See Figure 8 through Figure 10 for information on per channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 11 through Figure 15 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM3400-EP/ADuM3401-EP/ADuM3402-EP channel configurations.
[2] I_{Ox} is the Channel x output current, where x = A, B, C, or D.
[3] V_{IxH} is the input side logic high.
[4] V_{IxL} is the input side logic low.
[5] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.
[6] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 8 through Figure 10 for information on per-channel supply current for unloaded and loaded conditions.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{IO}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{IO}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Case Thermal Resistance						
Side 1	θ_{JCI}		33		°C/W	Thermocouple located at center of package underside
Side 2	θ_{JCO}		28		°C/W	Thermocouple located at center of package underside

[1] Device considered a 2-terminal device; Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM3400-EP/ADuM3401-EP/ADuM3402-EP are approved by the organizations listed in Table 5.

Table 5.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single Protection, 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 780 V rms (1103 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 390 V rms (551 V peak) maximum working voltage Basic insulation under IEC62020-1, 300 V rms (566 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3400-EP/ADuM3401-EP/ADuM3402-EP is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3400-EP/ADuM3401-EP/ADuM3402-EP is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(PCB)	8.1 min	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 7.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 seconds	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

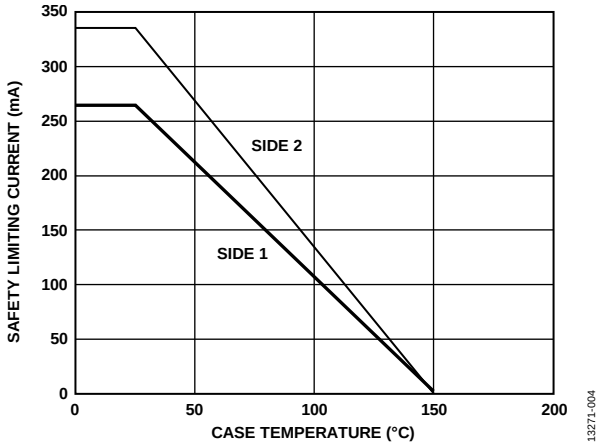


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Rating
Operating Temperature Range (T_A)	−55°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	3.135 V to 5.5 V
Input Signal Rise and Fall Times	1.0 ms

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
Storage Temperature Range (T_{ST})	−65°C to +150°C
Ambient Operating Temperature Range (T_A)	−55°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5 V to +7.0 V
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2})[1, 2]	−0.5 V to V_{DD1} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−18 mA to +18 mA
Side 2 (I_{O2})	−22 mA to +22 mA
Common-Mode Transients (CM_H, CM_L)[4]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 4 for maximum rated current values for various temperatures.
[4] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage			
Bipolar Waveform	565	V peak	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10
DC Voltage			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
Reinforced Insulation	560	V peak	Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10

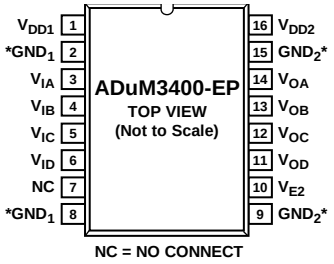
[1] Refers to continuous voltage magnitude imposed across the isolation barrier.

Table 11. Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{Ex} Input[3, 2]	V_{DDI} State[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
H	H or NC	Powered	Powered	H	
L	H or NC	Powered	Powered	L	
X	L	Powered	Powered	Z	
X	H or NC	Unpowered	Powered	H	Outputs return to the input state within 1 µs of V_{DDI} power restoration.
X	L	Unpowered	Powered	Z	
X	X	Powered	Unpowered	Indeterminate	Outputs return to the input state within 1 µs of V_{DDO} power restoration if V_{Ex} state is H or NC. Outputs return to high impedance state within 8 ns of V_{DDO} power restoration if V_{Ex} state is L.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.
[2] H is high, L is low, X is don't care, and NC is no connect.
[3] In noisy environments, connecting V_{Ex} to an external logic high or low is recommended.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



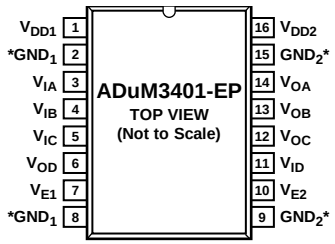
*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_2 IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401-EP/ADuM3402-EP AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

13271-005

Figure 5. ADuM3400-EP Pin Configuration

Table 12. ADuM3400-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	NC	No Connect.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.



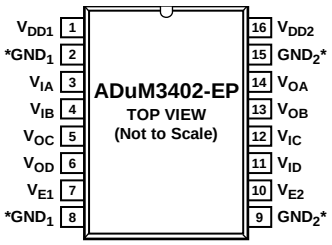
*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_2 IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401-EP/ADuM3402-EP AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

13271-006

Figure 6. ADuM3401-EP Pin Configuration

Table 13. ADuM3401-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OD} output is enabled when V_{E1} is high or disconnected. V_{OD} is disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA}, V_{OB}, and V_{OC} outputs are enabled when V_{E2} is high or disconnected. V_{OA}, V_{OB}, and V_{OC} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.



*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_1 IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED AND CONNECTING BOTH TO GND_2 IS RECOMMENDED. IN NOISY ENVIRONMENTS, CONNECTING OUTPUT ENABLES (PIN 7 FOR ADuM3401-EP/ADuM3402-EP AND PIN 10 FOR ALL MODELS) TO AN EXTERNAL LOGIC HIGH OR LOW IS RECOMMENDED.

13271-007

Figure 7. ADuM3402-EP Pin Configuration

Table 14. ADuM3402-EP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.135 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	V_{E1}	Output Enable 1. Active high logic input. V_{OC} and V_{OD} outputs are enabled when V_{E1} is high or disconnected. V_{OC} and V_{OD} outputs are disabled when V_{E1} is low. In noisy environments, connecting V_{E1} to an external logic high or low is recommended.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2.
10	V_{E2}	Output Enable 2. Active high logic input. V_{OA} and V_{OB} outputs are enabled when V_{E2} is high or disconnected. V_{OA} and V_{OB} outputs are disabled when V_{E2} is low. In noisy environments, connecting V_{E2} to an external logic high or low is recommended.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2, 3.135 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

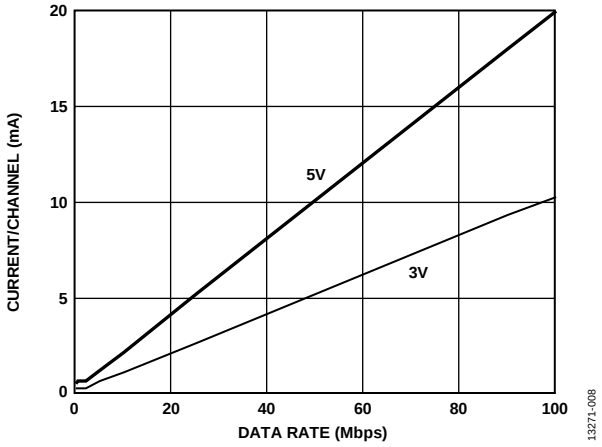


Figure 8. Typical Input Supply Current per Channel vs. Data Rate (No Load)

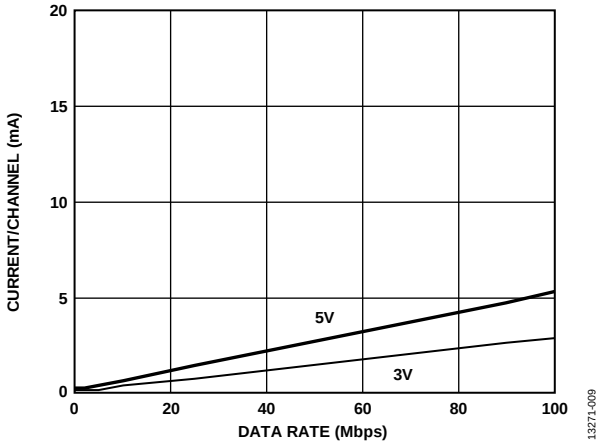


Figure 9. Typical Output Supply Current per Channel vs. Data Rate (No Load)

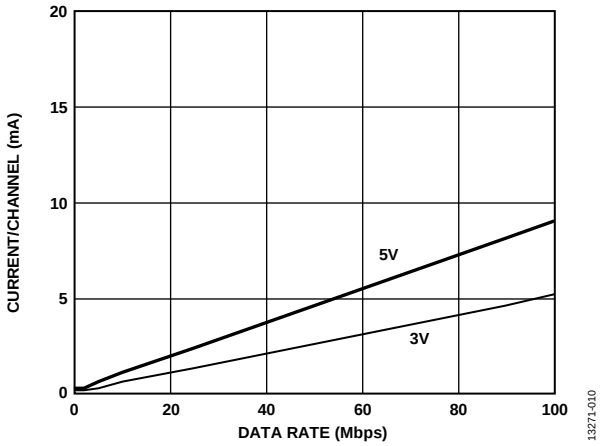


Figure 10. Typical Output Supply Current per Channel vs. Data Rate (15 pF Output Load)

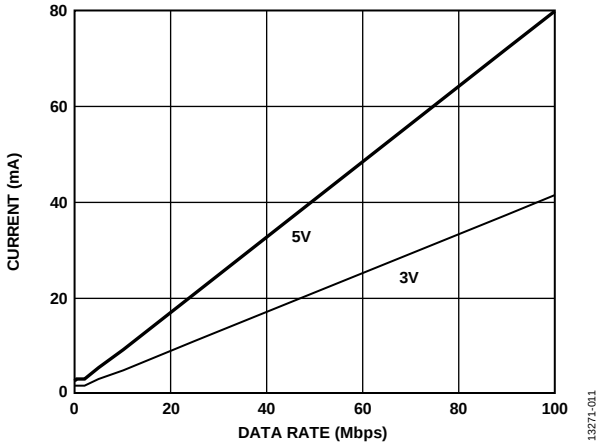


Figure 11. Typical ADuM3400-EP V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

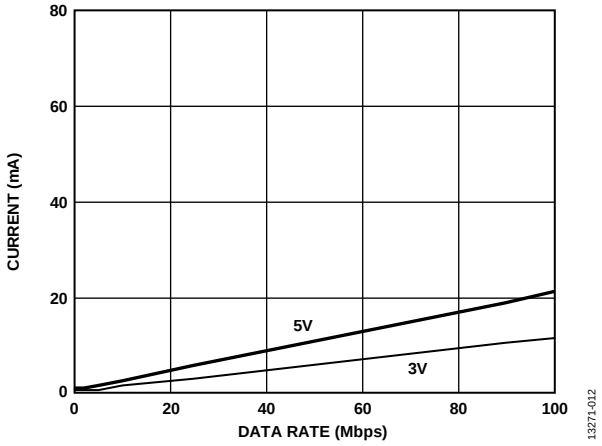


Figure 12. Typical ADuM3400-EP V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

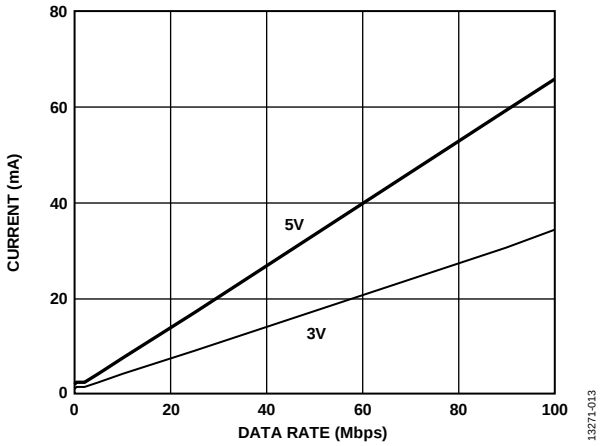


Figure 13. Typical ADuM3401-EP V_{DD1} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

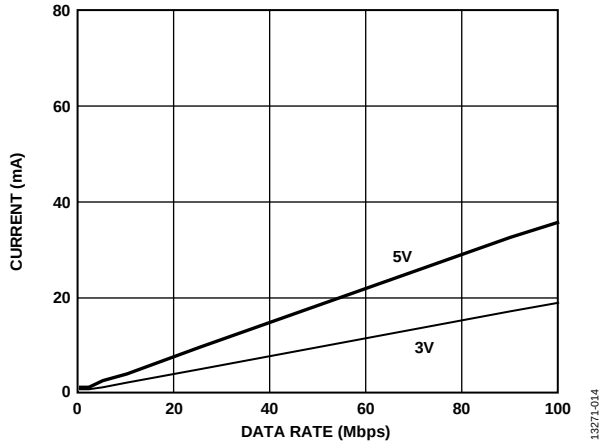


Figure 14. Typical ADuM3401-EP V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

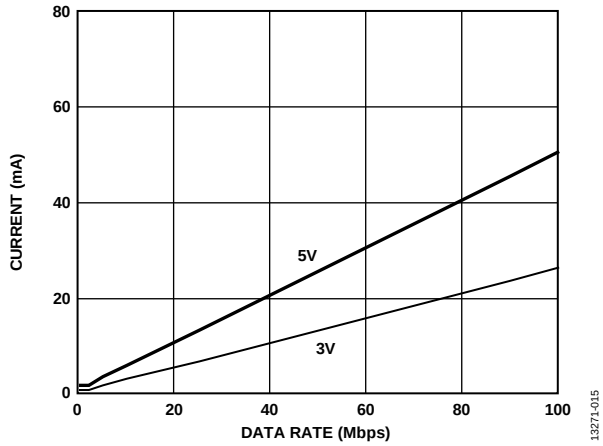


Figure 15. Typical ADuM3402-EP V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

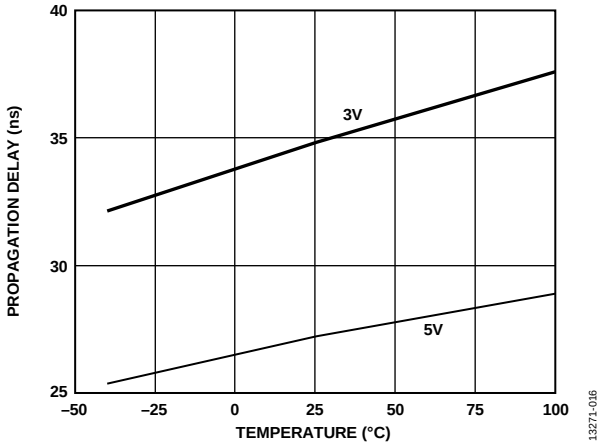
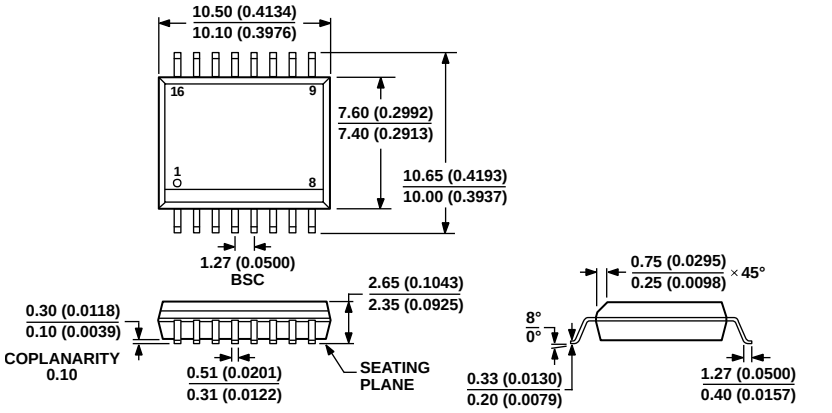


Figure 16. Propagation Delay vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 17. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Temperature Range	Package Description	Package Option
ADUM3400TRWZ-EP	4	0	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16
ADUM3400TRWZ-EP-RL	4	0	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16
ADUM3401TRWZ-EP	3	1	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16
ADUM3401TRWZ-EP-RL	3	1	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16
ADUM3402TRWZ-EP	2	2	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16
ADUM3402TRWZ-EP-RL	2	2	10	50	−55°C to +125°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.