

Isolated Amplifier with Adjustable Gain and Single-Ended Output

FEATURES

- ▶ High-Impedance input for isolated voltage measurement
- ▶ Low offset error and drift (output offset voltage): ± 6 mV (Max) at 25°C and -22 μ V/°C (Typ)
- ▶ Low gain error and drift: $\pm 0.5\%$ (max) and ± 27 ppm/°C (max)
- ▶ Voltage-supply range
 - ▶ V_{DD1} : 4.5 V to 5.5 V
 - ▶ V_{DD2} : 4.5 V to 5.5 V
- ▶ Bandwidth: 210 kHz
- ▶ Isolation voltage
 - ▶ 3000 V rms for ADuM3195
 - ▶ 5000 V rms for ADuM4195
- ▶ Safety and regulatory approvals (pending)
 - ▶ UL recognition (pending)
 - ▶ ADuM3195: 3000 V rms for 1 minute per UL 1577
 - ▶ ADuM4195: 5000 V rms for 1 minute per UL 1577
 - ▶ CSA (pending)
 - ▶ VDE certificate of conformity (pending)
 - ▶ DIN EN IEC 60747-17
 - ▶ ADuM3195: $V_{IORM} = 849$ V peak (reinforced)
 - ▶ ADuM4195: $V_{IORM} = 1401$ V peak (reinforced)
- ▶ Wide temperature range
 - ▶ -40°C to $+125^{\circ}\text{C}$ ambient operation
 - ▶ 150°C maximum junction temperature
- ▶ AEC-Q100 qualified for automotive applications

APPLICATIONS

- ▶ Inverters
- ▶ DC to DC converters
- ▶ On-board chargers

GENERAL DESCRIPTION

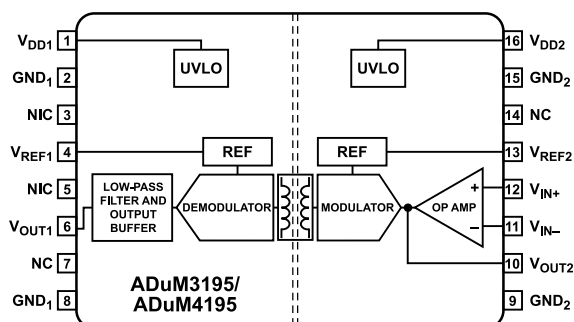
The ADuM3195/ADuM4195¹ are isolation amplifiers based on Analog Devices, Inc., iCoupler® technology. The ADuM3195/ADuM4195 have very low offset and gain error, making them ideal for many isolated voltage sensing applications.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperatures, the ADuM3195/ADuM4195 transfer functions do not change over lifetime, and are stable over a wide temperature range of -40°C to $+125^{\circ}\text{C}$.

Included in the ADuM3195/ADuM4195 are wideband operational amplifiers useful for a variety of commonly used applications, and two high accuracy 2.5 V references outputs.

The ADuM3195 is packaged in a 16-lead quarter small outline package (QSOP) for a 3000 V rms isolation voltage rating according to UL1577. The ADuM4195 is packaged in a 16-lead wide-body SOIC package with increased creepage for a 5000 V rms isolation voltage rating according to UL1577.

FUNCTIONAL BLOCK DIAGRAM



NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN IS NOT CONNECTED INTERNALLY.
2. NC = NO CONNECT.

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Figure 1.

¹ Protected by U.S. Patents 5,952,849, 6,873,065 and 7,075,329. Other patents pending.

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REVISION HISTORY**7/2024—Rev. 0 to Rev. A**

Added ADuM4195 (Universal).....	1
Added 16-Lead SOIC (Universal).....	1
Changes to Features Section.....	1
Changes to General Description Section.....	1
Changes to Table 2.....	4
Changes to Table 3.....	5
Added Table 4; Renumbered Sequentially.....	5
Change to Table 5 Title.....	5
Added Table 6.....	5
Changed DIN VDE V 0884-11:2017-01 Insulation Characteristics (Pending) Section to DIN EC IEC 60747-17 Insulation Characteristics (Pending) Section.....	6
Changes to Table 8 Title and Figure 2 Caption.....	6
Added Table 9 and Figure 3; Renumbered Sequentially.....	7
Added Table 12.....	8
Changes to Table 13.....	9
Changes to Figure 37 to Figure 39.....	17
Changes to Figure 41.....	18
Change to DC Correctness and Magnetic Field Immunity Section.....	18
Updated Outline Dimensions.....	20
Changes to Ordering Guide.....	20
Changes to Evaluation Boards.....	20

4/2023—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD1} = V_{DD2} = 4.5 \text{ V to } 5.5 \text{ V}$ for $T_A = T_{MIN}$ to T_{MAX} . All typical specifications are at $T_A = 25^\circ\text{C}$ and $V_{DD1} = V_{DD2} = 5 \text{ V}$, unless otherwise noted.

Table 1. Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
OPERATIONAL AMPLIFIER (OP AMP)					
Input Offset Voltage (V_{OS})	-0.5		+1.5	mV	$T_A = 25^{\circ}\text{C}$ V_{IN+} or $V_{IN-} = 2.5\text{ V}$
Input Offset Drift	-11		+11	$\mu\text{V}/^{\circ}\text{C}$	
Input Op Amp Gain	85			dB	
Input Common-Mode Range ¹	0.25		$V_{DD2} - 0.7$	V	
Gain-Bandwidth Product		15		MHz	
Common-Mode Rejection		-85		dB	
Input Resistance		10		G Ω	
Input Capacitance		5		pF	
Input-Bias Current ²	-0.2		+0.2	nA	
Input-Bias Current Drift	-25		+75	pA/ $^{\circ}\text{C}$	
Op Amp Output Voltage Range ¹	0.1		V_{DD2}	V	
REFERENCE					
Output Voltage, V_{REF1} , V_{REF2}	2.49	2.50	2.51	V	0 mA to 1 mA load $T_A = 25^{\circ}\text{C}$ $T_A = T_{MIN}$ to T_{MAX}
	2.47	2.50	2.53	V	
Reference Temperature Coefficient (Tempco)		± 25		ppm/ $^{\circ}\text{C}$	
Output Current	1.0			mA	
OUTPUT CHARACTERISTICS					
Linear Output Voltage Range ¹	0.25		$V_{DD2} - 0.7$	V	$V_{OUT1} - V_{IN+}$ (op amp in buffer configuration), $V_{IN+} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$ $V_{IN+} = 2.5\text{ V}$, $T_A = -40$ to 125°C V_{OUT1}/V_{IN+} (op amp in buffer configuration)
Output Offset Voltage	-6.0		+6.0	mV	
Output Offset Drift		-22		$\mu\text{V}/^{\circ}\text{C}$	
Output Gain ³		1			
Output Gain Error	-0.5		+0.5	%	
Output Gain Error Drift	-27		+27	ppm/ $^{\circ}\text{C}$	
Output -3 dB Bandwidth		210		kHz	
Output Delay		3		μs	
Output Rise and Fall time		2		μs	
Output Noise		540		$\mu\text{V rms}$	
SNR		1		mV rms	From V_{OUT1} to V_{IN+} 50% input to 50% output within $V_{IN+} = 1\text{ V}$ to 4 V 10% to 90% within $V_{IN+} = 1\text{ V}$ to 4 V $f_{IN} = 1\text{ kHz}$, bandwidth = 100 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 200 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 100 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 200 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 100 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 200 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 100 kHz $f_{IN} = 1\text{ kHz}$, bandwidth = 200 kHz DC, $V_{DD1} = V_{DD2} = 4.5\text{ V}$ to 5.5 V
Total Harmonic Distortion Plus Noise (THD + N)		69		dB	
Ratio		64		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		57		dB	
		56		dB	
Power-Supply Rejection Ratio (PSRR)		-60		dB	
Output Resistive Load	10			k Ω	
Output Capacitive Load			100	pF	
Common-Mode Transient Immunity (CMTI) ^{2, 4}	100	150		kV/ μs	
POWER SUPPLY					
Operating Range, Side 1	4.5	5.0	5.5	V	V_{DD1}

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comment
Undervoltage Lockout (UVLO) Positive Going Threshold		4.2		V	
UVLO Negative Going Threshold		4.0		V	
Operating Range, Side 2	4.5	5.0	5.5	V	V _{DD2}
UVLO Positive Going Threshold		4.2		V	
UVLO Negative Going Threshold		4.0		V	
V _{OUT1} Impedance		35		Ω	V _{DD1} = 5 V, V _{DD2} < UVLO threshold
		3.7		kΩ	V _{DD1} < UVLO threshold
Supply Current					
I _{DD1}		4.1	4.9	mA	
I _{DD2}		5.9	7.3	mA	

¹ For a maximum deviation of ±1.25% from the best-fit line over the specified input range of 1 V to 3.5 V. Op amp in buffer configuration.

² Guaranteed by design and characterization. Not production tested.

³ Output gain defined as the slope of the best-fit line over the specified input range, with the offset error adjusted out.

⁴ CMTI error is an output disturbance greater than 100 mV lasting more than 2 μs.

PACKAGE CHARACTERISTICS

Table 2. Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE						
Input-to-Output ¹	R _{I-O}		10 ¹³		Ω	
CAPACITANCE						
Input-to-Output ¹	C _{I-O}		2.2		pF	f = 1 MHz
Input Capacitance ²	C _I		4.0		pF	
IC JUNCTION-TO-AMBIENT THERMAL RESISTANCE						
16-Lead QSOP (ADuM3195)	θ _{JA}		83		°C/W	Thermocouple located at the center of package underside
16-Lead SOIC (ADuM4195)	θ _{JA}		55		°C/W	Thermocouple located at the center of package underside

¹ The device is considered a 2-terminal device; Pins 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

SPECIFICATIONS

REGULATORY INFORMATION

Table 3. ADuM3195 Regulatory Information (Pending)

UL (Pending)	CSA (Pending) ¹	VDE (Pending)
Recognized Under 1577 Component Recognition Program ²	Basic insulation per CSA 62638-1-03 and IEC 62638-1, 350 V rms (495 V peak) maximum working voltage	Certified according to DIN EN IEC 60747-17 ³
Single Protection, 3000 V rms Isolation Voltage, 16-Lead QSOP	Reinforced insulation per CSA 62638-1-03 and IEC 62638-1, 175 V rms (247 V peak) maximum working voltage	Reinforced insulation, 849 V peak V_{IOTM} = 4000 V pk, V_{IOSM} = 8000 V pk
File (pending)	File (pending)	File (pending)

¹ Working voltages are quoted for Pollution Degree 2, Material Group III.

² In accordance with UL 1577, each ADuM3195 is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec (current leakage detection limit = 5 μ A).

³ In accordance with DIN EN IEC 60747-17, each ADuM3195 is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN IEC 60747-17 approval.

Table 4. ADuM4195 Regulatory Information (Pending)

UL (Pending)	CSA (Pending) ¹	VDE (Pending)
Recognized Under 1577 Component Recognition Program ²	Basic insulation per CSA 62638-1-03 and IEC 62638-1, 900 V rms (1270 V peak) maximum working voltage	Certified according to DIN EN IEC 60747-17 ³
Single Protection, 5000 V rms Isolation Voltage, 16-Lead SOIC	Reinforced insulation per CSA 62638-1-03 and IEC 62638-1, 400 V rms (565 V peak) maximum working voltage	Reinforced insulation, 1401 V peak V_{IOTM} = 7070 V pk, V_{IOSM} = 12800 V pk
File (pending)	File (pending)	File (pending)

¹ Working voltages are quoted for Pollution Degree 2, Material Group III.

² In accordance with UL 1577, each ADuM4195 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 5 μ A).

³ In accordance with DIN EN IEC 60747-17, each ADuM4195 is proof tested by applying an insulation test voltage ≥ 1988 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN IEC 60747-17 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5. ADuM3195 Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	3.2	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	3.2	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	3.8	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the printed circuit board (PCB) mounting plane
Minimum Internal Gap (Internal Clearance)		0.041	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material Group DIN VDE 0110, 1/89, Table 1

Table 6. ADuM4195 Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air

SPECIFICATIONS

Table 6. ADuM4195 Insulation and Safety Related Specifications (Continued)

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Minimum External Tracking (Creepage)	L (I02)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.041	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material Group DIN VDE 0110, 1/89, Table 1

RECOMMENDED OPERATING CONDITIONS

Table 7. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
OPERATING TEMPERATURE	T_A	-40	+125	°C
SUPPLY VOLTAGES ¹	V_{DD1}, V_{DD2}	4.5	5.5	V

¹ All voltages are relative to their respective grounds.

DIN EC IEC 60747-17 INSULATION CHARACTERISTICS (PENDING)

These isolators are suitable for reinforced isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The asterisk (*) marking branded on the package denotes DIN EC IEC 60747-17 approval (pending).

Table 8. ADuM3195 VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic ¹	Unit
Installation Classification per DIN VDE 0110			I to IV	
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PD(M)}$, 100% production test, $t_{NI} = t_M = 1$ sec, partial discharge < 5 pC	$V_{PD(M)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{PD(M)}$, $t_{NI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC	$V_{PD(M)}$	1273	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PD(M)}$, $t_{NI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC	$V_{PD(M)}$	1018	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4000	V_{PEAK}
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μ s rise time, 50 μ s, 50% fall time	V_{IOSM}	8000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.51	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	>10 ⁹	Ω

¹ For information about t_M , t_{NI} , and V_{IO} , see DIN EN IEC 60747-17.

SPECIFICATIONS

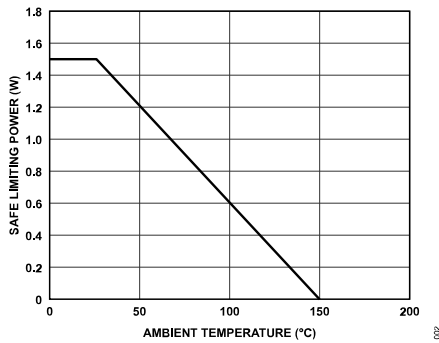


Figure 2. Thermal Derating Curve for the ADuM3195, Dependence of Safety Limiting Values on Case Temperature, Per DIN EN IEC 60747-17

Table 9. ADuM4195 VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic ¹	Unit
Installation Classification per DIN VDE 0110			I to IV	
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Working Insulation Voltage		V_{IORM}	1401	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PD(M)}$, 100% production test, $t_{INI} = t_M = 1$ sec, partial discharge < 5 pC	$V_{PD(M)}$	2627	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{PD(M)}$, $t_{INI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC	$V_{PD(M)}$	2102	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PD(M)}$, $t_{INI} = 60$ sec, $t_M = 10$ sec, partial discharge < 5 pC	$V_{PD(M)}$	1681	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	7070	V_{PEAK}
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	12800	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	2.27	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	>10 ⁹	Ω

¹ For information about t_M , t_{INI} , and V_{IO} , see DIN EN IEC 60747-17.

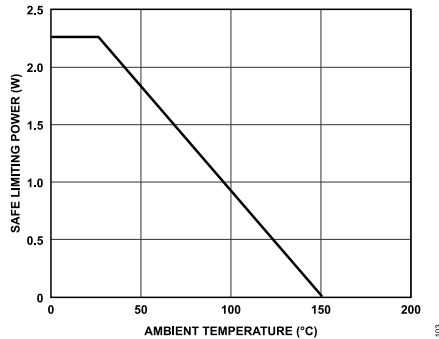


Figure 3. Thermal Derating Curve for the ADuM4195, Dependence of Safety Limiting Values on Case Temperature, Per DIN EN IEC 60747-17

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 10. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature (T_{ST}) Range	-65°C to $+150^\circ\text{C}$
Ambient Operating Temperature (T_A) Range	-40°C to $+125^\circ\text{C}$
Junction Temperature (T_J)	-40°C to $+150^\circ\text{C}$
Supply Voltages V_{DD1}, V_{DD2} ¹	-0.5 V to $+7.0\text{ V}$
Input Voltages V_{IN+}, V_{IN-}	-0.5 V to $V_{DD2} + 0.5\text{ V}$
Output Voltages V_{REF1}, V_{OUT1} V_{REF2}, V_{OUT2}	-0.5 V to $V_{DD1} + 0.5\text{ V}$ -0.5 V to $V_{DD2} + 0.5\text{ V}$
Output Current per Output Pin	-11 mA to $+11\text{ mA}$
Common-Mode Transients ²	$-200\text{ kV}/\mu\text{s}$ to $+200\text{ kV}/\mu\text{s}$

¹ All voltages are relative to their respective grounds.

² Refers to the common-mode transients across the insulation barrier. The common-mode transients exceeding the absolute maximum ratings may cause latchup or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 11. Maximum Continuous Working Voltage for the RQ-16 (QSOP) Package

Parameter ¹	Rating	Constraint
AC Voltage Bipolar Waveform		
Basic Insulation	450 V _{rms}	Basic insulation rating per IEC 60747-17. Accumulative failure rate over lifetime (FROL) $\leq 1000\text{ ppm}$ at 20 years.
Reinforced Insulation	225 V _{rms}	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
DC Voltage		

Table 11. Maximum Continuous Working Voltage for the RQ-16 (QSOP) Package (Continued)

Parameter ¹	Rating	Constraint
Basic Insulation	450 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
Reinforced Insulation	225 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.

¹ Refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment.

Table 12. Maximum Continuous Working Voltage for the RI-16-2 (SOIC_IC) Package

Parameter ¹	Rating	Constraint
AC Voltage Bipolar Waveform		
Basic Insulation	1401 V _{rms}	Basic insulation rating per IEC 60747-17. Accumulative failure rate over lifetime (FROL) $\leq 1000\text{ ppm}$ at 20 years.
Reinforced Insulation	1401 V _{rms}	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	1660 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.
Reinforced Insulation	830 V DC	Rating limited by package creepage per IEC 60664-1:2020 in Pollution Degree 2 environment.

¹ Refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

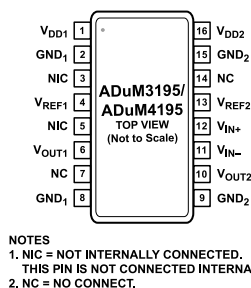


Figure 4. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{DD1}	Supply Voltage for Side 1, Pin 1 to Pin 8 (4.5 V to 5.5 V). Connect a 0.1 μ F and a 1 μ F capacitor between V _{DD1} and GND ₁ .
2	GND ₁	Ground Reference for Side 1.
3	NIC	Not Internally Connected. This pin is not connected internally. Connect this pin to V _{DD1} , GND ₁ , or leave floating.
4	V _{REF1}	Reference Output Voltage for Side 1. The maximum capacitance for this pin (C _{REFOUT1}) must not exceed 22 pF.
5	NIC	Not Internally Connected. This pin is not connected internally. Connect this pin to V _{DD1} , GND ₁ , or leave floating.
6	V _{OUT1}	Isolated Output Voltage.
7	NC	No Connect. Connect this pin to GND ₁ . Do not leave it floating.
8	GND ₁	Ground Reference for Side 1.
9	GND ₂	Ground Reference for Side 2 (Pin 9 to Pin 16).
10	V _{OUT2}	Output of the Op Amp.
11	V _{IN-}	Inverting Op Amp Input.
12	V _{IN+}	Noninverting Op Amp Input.
13	V _{REF2}	Reference Output Voltage for Side 2. Bypass with a 10 nF capacitor to GND ₂ even if V _{REF2} is not used. The maximum capacitance for this pin (C _{REFOUT}) must not exceed 22 nF.
14	NC	No Connect. Connect this pin to GND ₂ . Do not leave it floating.
15	GND ₂	Ground Reference for Side 2.
16	V _{DD2}	Supply Voltage for Side 2 (4.5 V to 5.5 V). Connect a 0.1 μ F and a 1 μ F capacitor between V _{DD1} and GND ₁ .

TYPICAL PERFORMANCE CHARACTERISTICS

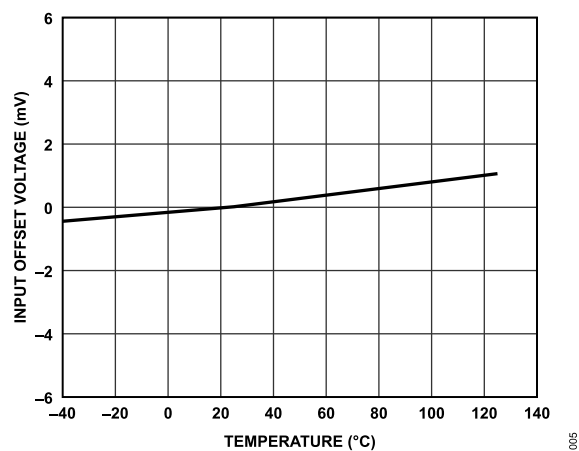


Figure 5. Op Amp Input Offset Voltage vs. Temperature

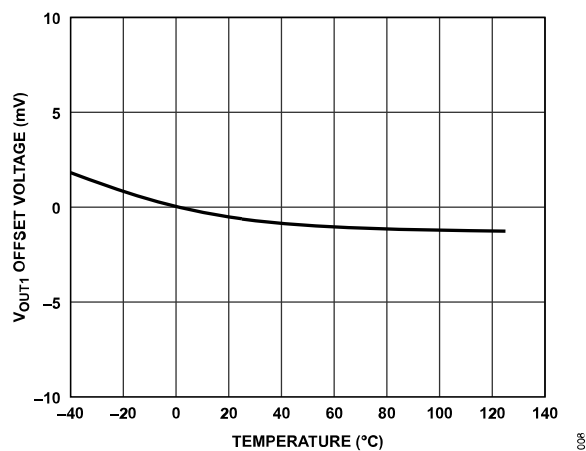
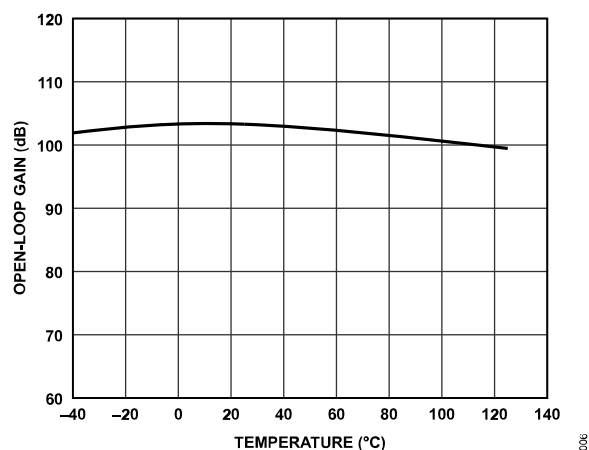
Figure 8. V_{OUT1} Offset Voltage vs. Temperature

Figure 6. Op Amp Open-Loop Gain vs. Temperature

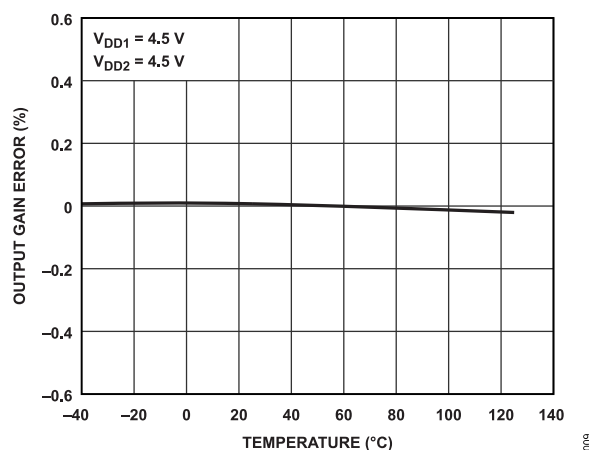
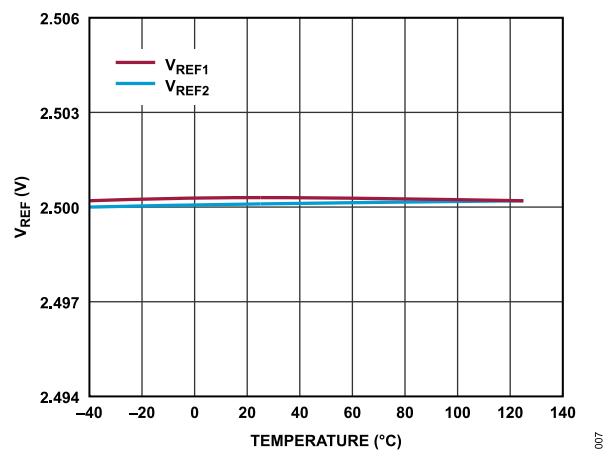
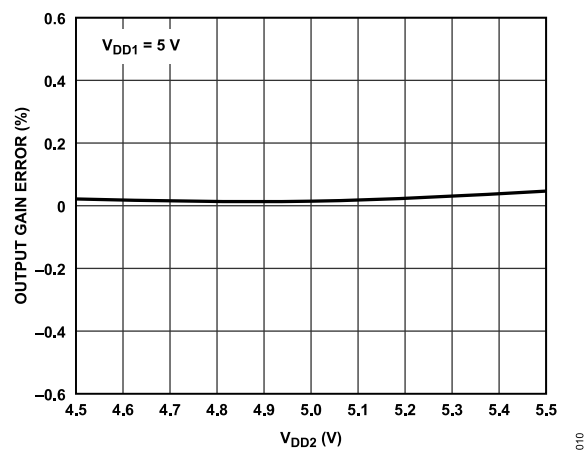


Figure 9. Output Gain Error vs. Temperature

Figure 7. V_{REF} vs. TemperatureFigure 10. Output Gain Error vs. V_{DD2}

TYPICAL PERFORMANCE CHARACTERISTICS

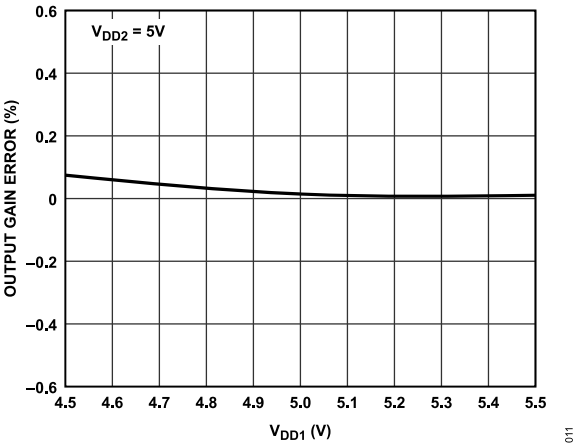


Figure 11. Output Gain Error vs. V_{DD1}

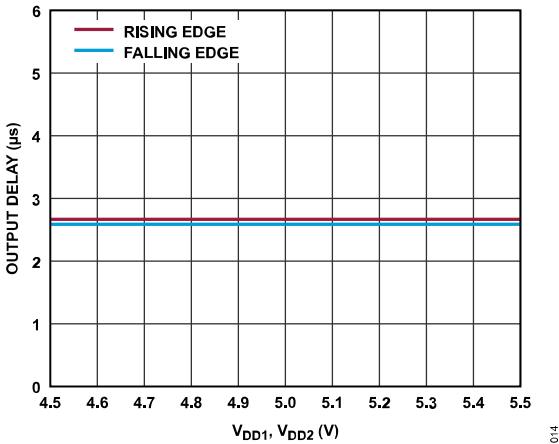


Figure 14. Output Delay vs. Supply Voltage

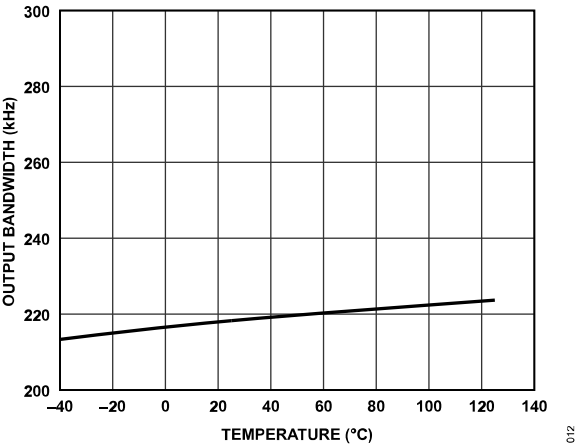


Figure 12. Output Bandwidth vs. Temperature

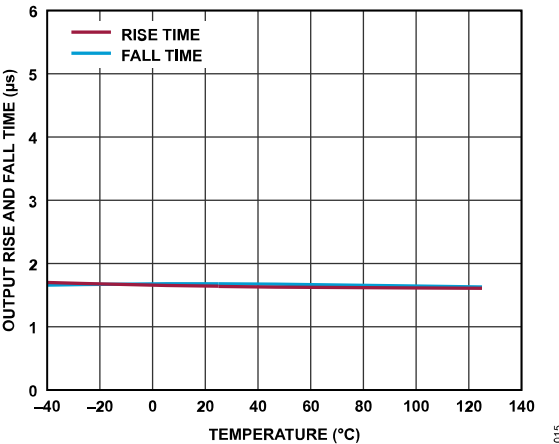


Figure 15. Output Rise and Fall Time vs. Temperature

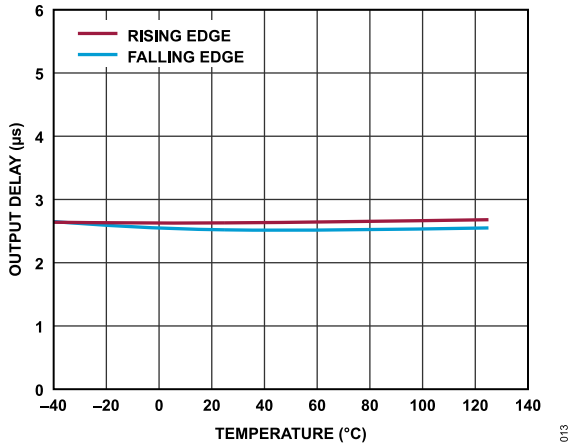


Figure 13. Output Delay vs. Temperature

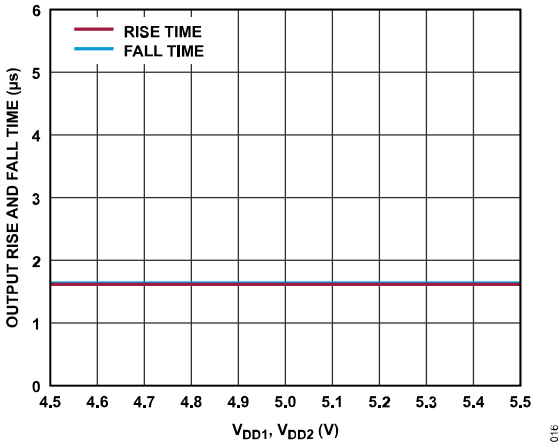


Figure 16. Output Rise and Fall Time vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

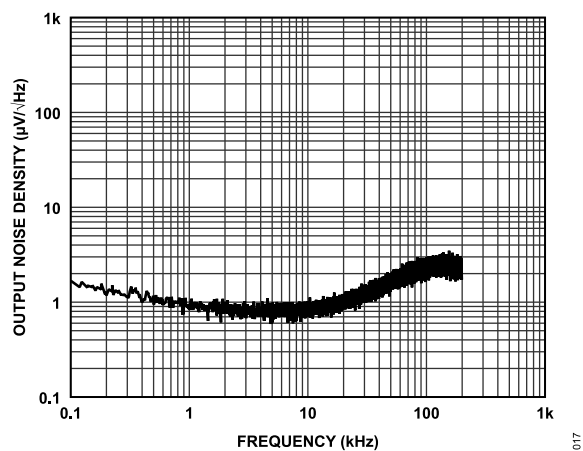


Figure 17. Output Noise Density vs. Frequency

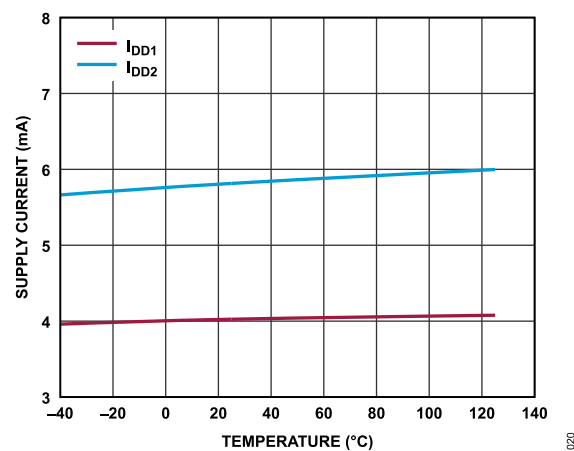


Figure 20. Supply Current vs. Temperature

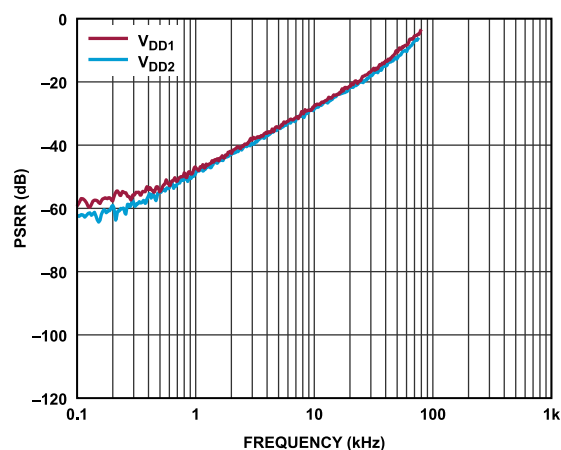


Figure 18. PSRR vs. Frequency

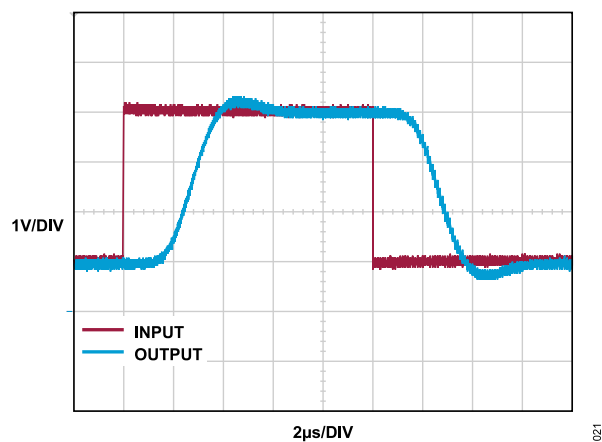
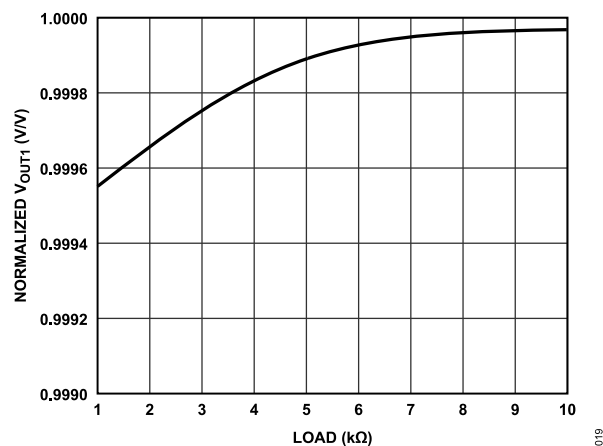
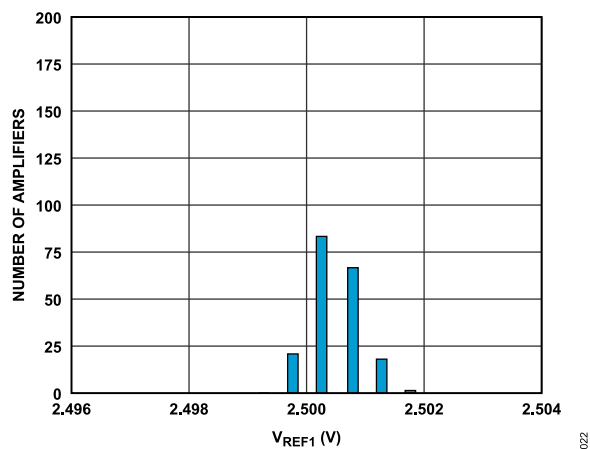
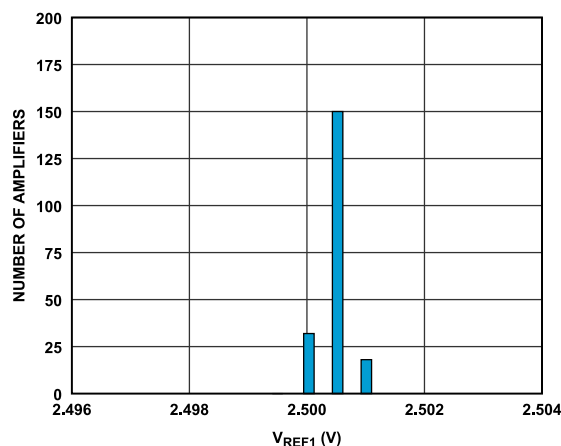
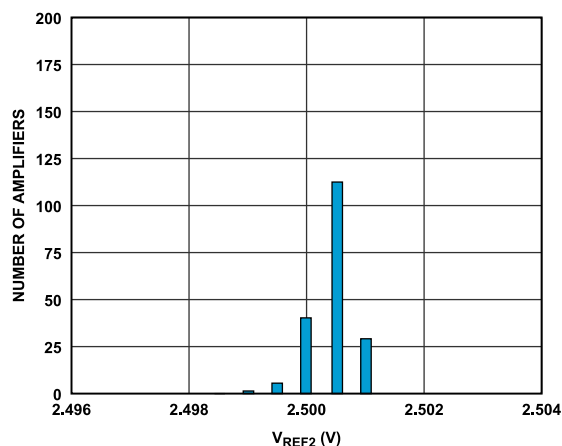
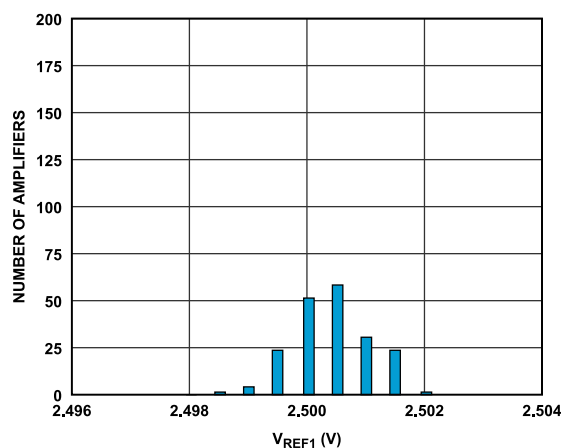
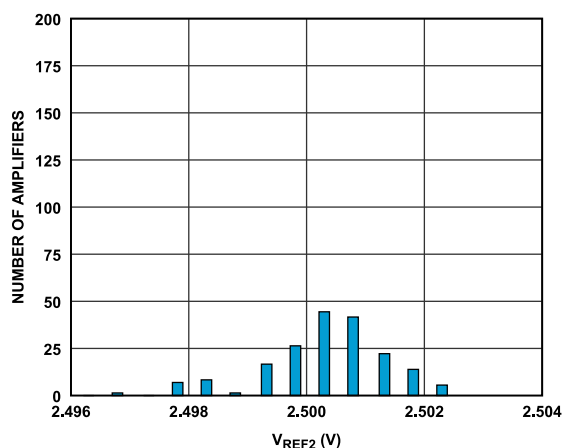
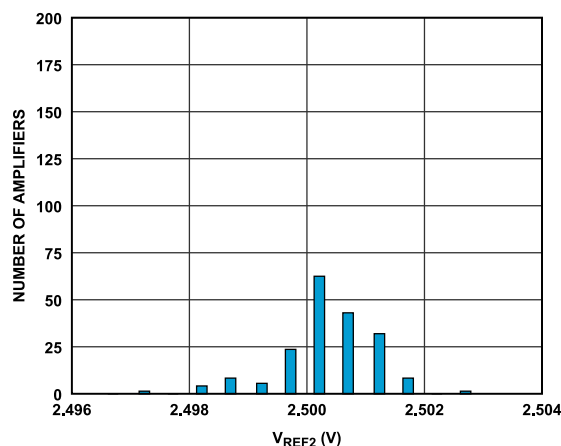
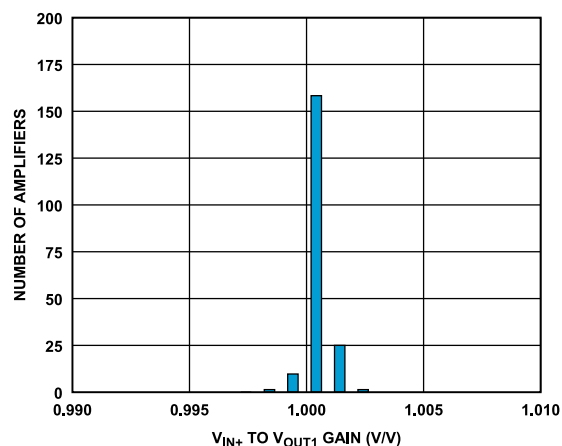


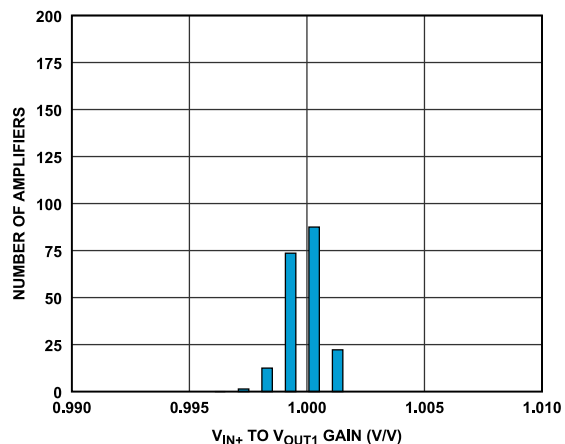
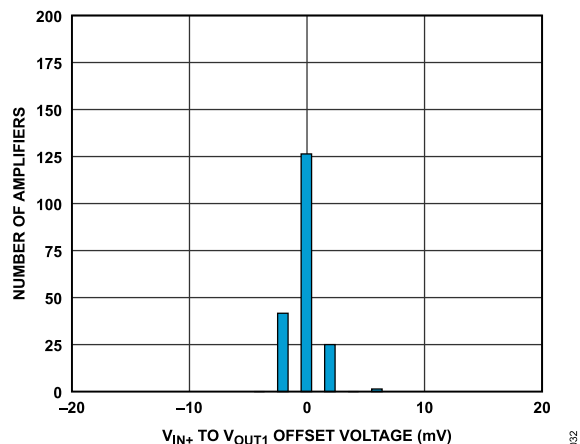
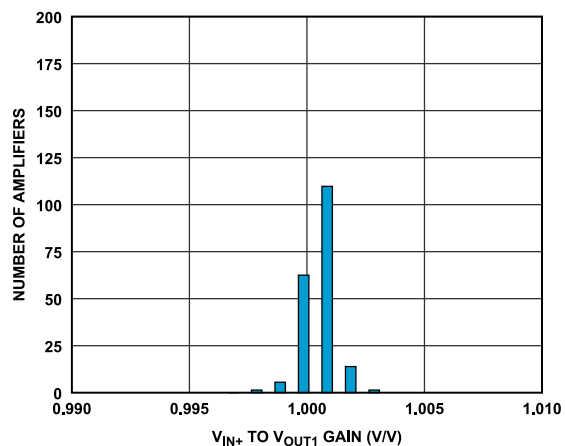
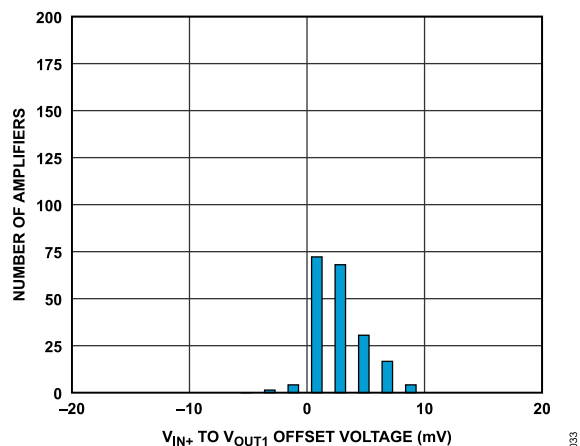
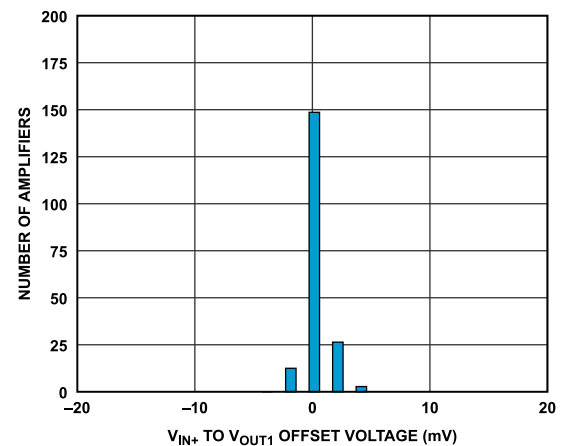
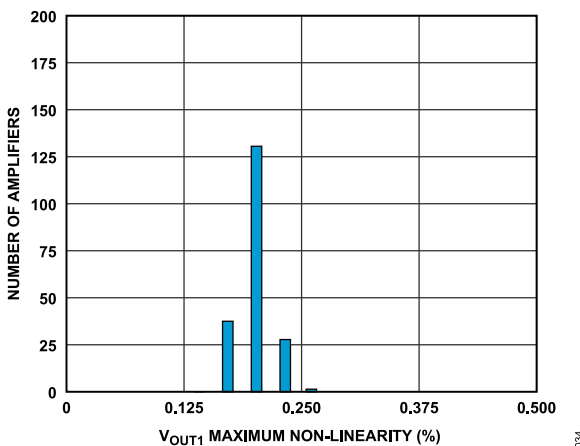
Figure 21. Output Square-Wave Response

Figure 19. Normalized V_{OUT1} vs. LoadFigure 22. V_{REF1} Distribution at 25 $^{\circ}\text{C}$

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 23. V_{REF1} Distribution at 125°CFigure 26. V_{REF2} Distribution at 125°CFigure 24. V_{REF1} Distribution at -40°CFigure 27. V_{REF2} Distribution at -40°CFigure 25. V_{REF2} Distribution at 25°CFigure 28. V_{IN+} to V_{OUT1} Gain Distribution at 25°C

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Figure 29. V_{IN+} to V_{OUT1} Gain Distribution at 125°CFigure 32. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at 125°CFigure 30. V_{IN+} to V_{OUT1} Gain Distribution at -40°CFigure 33. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at -40°CFigure 31. V_{IN+} to V_{OUT1} Offset-Voltage Distribution at 25°C, Output Offset Voltage for $V_{IN+} = 2.5$ V Op Amp in Buffer ConfigurationFigure 34. V_{OUT1} Maximum Non-Linearity Distribution at 25°C, Maximum Non-Linearity Defined Within V_{IN+} Input Range: 1 V to 3.5 V, as an Absolute Value

TYPICAL PERFORMANCE CHARACTERISTICS

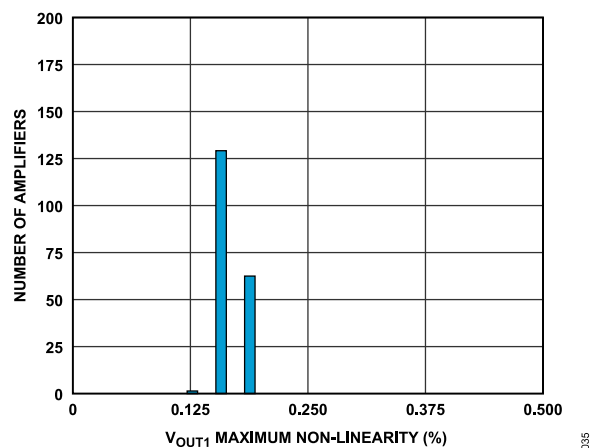


Figure 35. V_{OUT1} Maximum Non-Linearity Distribution at 125°C

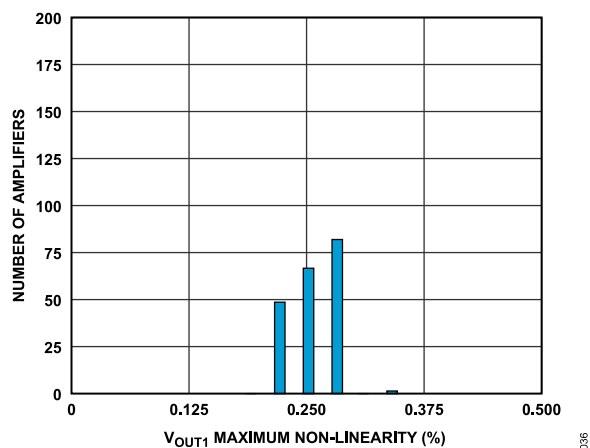


Figure 36. V_{OUT1} Maximum Non-Linearity Distribution at -40°C, Maximum Non-Linearity Defined Within V_{IN+} Input Range: 1 V to 3.5 V, as an Absolute Value

THEORY OF OPERATION

The ADuM3195/ADuM4195 are isolated amplifiers (IA) based on Analog Devices, Inc., iCoupler® technology. The input side of the IA consists of an operational amplifier with input pins V_{IN+} and V_{IN-} , and output pin V_{OUT2} . The V_{IN+} , V_{IN-} , and V_{OUT2} pins can be used to configure the IA for a wide range of applications such as IA with configurable gain, inverting IA, or as a voltage controller in isolated feedback loops for power supplies. A highly linear pulse width modulation (PWM) compares the output of the operational

amplifier to the internal voltage reference V_{REF2} and sends the duty cycle (ratio) information to the demodulator through a coreless transformer. On the output side of the IA, the demodulator uses the ratio information and the reference voltage V_{REF1} to reconstruct the output voltage, which is then low-pass filtered, buffered, and presented at output pin V_{OUT1} . Thus, with the input operational amplifier configured as a voltage follower, the overall signal gain of the IA defaults to 1.

APPLICATIONS INFORMATION

APPLICATION BLOCK DIAGRAM

Figure 37 shows a typical application for the ADuM3195/ADuM4195 as an isolated voltage monitor. The ADuM3195/ADuM4195 offers unique linearity, high common-mode noise immunity, low gain errors, and temperature drift. These features make it a robust and high performance isolated amplifier for industrial applications with high-voltage sensing required. The high-voltage bus is sensed by the R1 voltage divider and the R2 voltage divider. As the input op amp of the IA is configured as a unity-gain amplifier, the voltage on the V_{OUT2} is equal to the sensed bus voltage multiplied by the voltage-divider ratio. Due to the very high input impedance of the V_{IN+} pin, the current through the resistive divider can be kept low without sacrificing accuracy, thereby allowing for a low-power dissipation on the resistors. For very high voltages on the VBUS however, possible pollution on the PCB must also be taken into consideration when planning to design for the low input currents. Also, protective elements (such as diodes or Zener-diodes) in parallel with the R2 voltage divider may negatively affect the accuracy of the voltage divider and must be selected for the lowest reverse leakage currents over the desired temperature range. In such a case, a capacitive protection method as shown in Figure 37 may be a more viable approach.

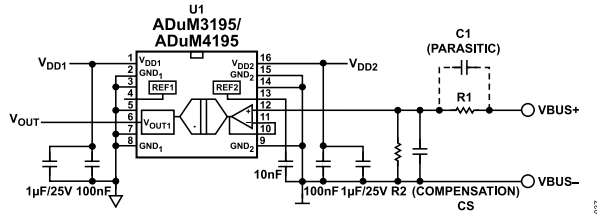


Figure 37. DC Bus Voltage Monitoring Using ADuM3195/ADuM4195

The high-voltage bus is sensed by a voltage divider, which consists of the R1 and the R2. As described in the previous section, the V_{OUT1} voltage follows the V_{IN+} with a typical gain of 1.

When monitoring very high bus voltages, the parasitic capacitances of the R1 can impose a risk of overvoltage spikes on the V_{IN+} during switching events on the VBUS. The recommendation is to connect a compensation capacitor C2 in parallel to the R2. Proper compensation is achieved by selecting C2 such that

$$C2 = R1 \times C1/R2 \quad (1)$$

The value of C2 is not critical but must be selected slightly higher than the calculated value to suppress any overshoot on the V_{IN+} during the switching events on the VBUS. For example, if $VBUS_{max} = 1 \text{ kV DC}$ and $V_{OUT} = 4.3 \text{ V}$, the required divider ratio is approximately 1/233, where $R1 = 2 \text{ M}\Omega$ and $R2 = 8.62 \text{ k}\Omega$. With an estimated parasitic capacitance C1 of approximately 10 pF, the compensation capacitance becomes $C2 \geq 2.3 \text{ nF}$.

Figure 38 shows an AC voltage monitoring application. In Figure 38, the V_{REF2} (Pin 13) is used to create a 2.5 V bias voltage for the input op amp. The bias resistor R3 with the coupling capacitor C3, form the AC coupling circuit and high-pass filter to the AC input

divider of the circuit. With R3 at least an order of magnitude larger than R2, a compensation capacitor in parallel with R2 provides a flat, high-frequency response when tuned to $R1 \times C1 = R2 \times C2$. The low-frequency roll-off is then defined by R3 and C3.

With the supplies V_{DD2} and $V_{DD1} = 5 \text{ V DC}$, the acceptable AC input voltage range across R2 is approximately $V_{R2} = 3.6 \text{ V}$ (peak-to-peak) or 1.27 V (rms).

Note that in this configuration V_{OUT1} is also biased to V_{REF} , therefore an upstream analog-to-digital converter (ADC) can be fed directly without extra biasing.

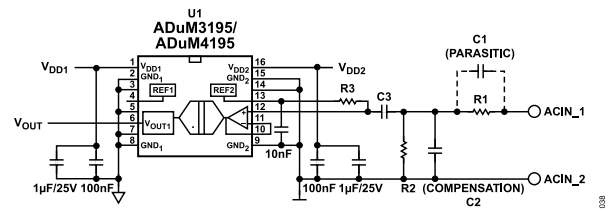


Figure 38. AC Voltage Monitoring Using ADuM3195/ADuM4195

Occasionally, it may be necessary to invert the monitored bus voltage. In such a case, the input stage of the ADuM3195/ADuM4195 can be configured as an inverting amplifier as shown in Figure 39.

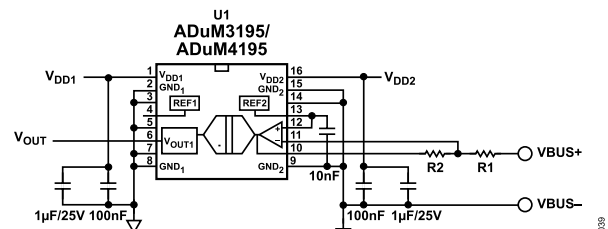


Figure 39. ADuM3195/ADuM4195 Configured as Inverting Amplifier

With the V_{REF2} directly wired to the V_{IN+} , the V_{OUT2} can be calculated as

$$V_{OUT2} = V_{REF2} - R2/R1 \times (VBUS - V_{REF2}) \quad (2)$$

Figure 40 shows another typical application for the ADuM3195/ADuM4195 as an isolated error amplifier in a DC to DC power converter.

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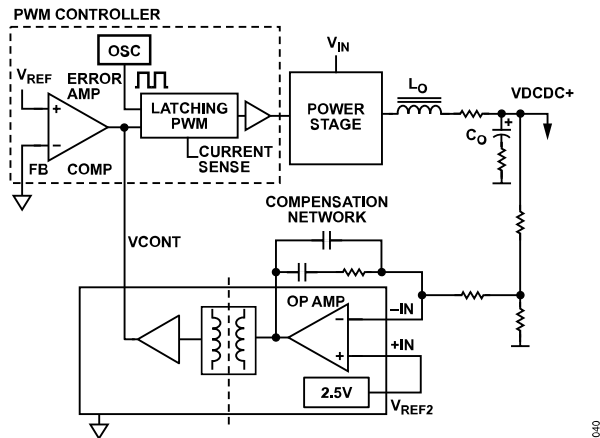
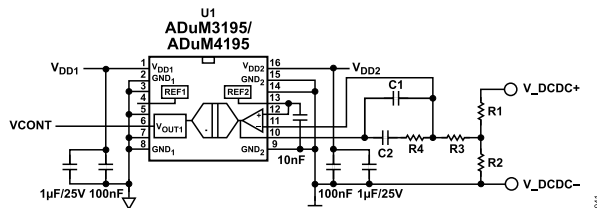


Figure 40. Isolated DC to DC Converter Application Diagram

The output voltage of the converter is sensed through a voltage divider and then connected to the V_{IN-} to compare with the V_{REF2} (see Figure 41). The error between the sensed voltage and the V_{REF2} is accumulated by the compensation network and transmitted to the voltage on V_{OUT1} . V_{OUT1} is then used to generate the PWM signals in a PWM controller. The PWM signals drive the power switches in the converter's power stage to regulate the output voltage.

Figure 41. DC to DC Converter V_{OUT} Setting

The output of the DC to DC power converter, V_{DCDC} , can be determined by the following equation, where $V_{REF2} = 2.5$ V:

$$V_{DCDC} = V_{REF2} \times (R_1 + R_2)/R_2 \quad (3)$$

DESIGN EXAMPLE

For a typical DC bus voltage monitoring application, as shown in Figure 38, the following design procedure can be used:

Table 14. Example Design Parameters

Parameter	Value	Comment
V_{DD2} (min)	5.0 V DC	Lowest V_{DD2} supply
V_{BUS} (max)	1000 V DC	Highest expected bus voltage
I_{DIV}	500 μ A	Limit power loss in divider to 0.5 W

Determine the minimum V_{DD2} in your system. This in turn determines the maximum V_{IN} that can be linearly transmitted across the isolation barrier.

$$V_{IN}(\text{max}) = V_{DD2}(\text{min}) - 0.7 \text{ V} = 5.0 \text{ V} - 0.7 \text{ V} = 4.3 \text{ V} \quad (4)$$

Determine the ratio $1/K$ of the voltage divider R_1 and R_2 for a given maximum of V_{BUS} (max), so that $1/K$ is about 0 to 10% larger than the $V_{BUS}(\text{max})/V_{IN}(\text{max})$.

$$1/K = (R_1 + R_2)/R_2 = V_{BUS}(\text{max})/V_{IN}(\text{max}), \quad (5)$$

$$1/K = 1 \dots 1.1 \times (1000 \text{ V}/4.3 \text{ V}) = 232.558 \dots 255.814 \quad (6)$$

For the given I_{DIV} , the minimum divider input resistance (R_{IN}) must meet as follows:

$$R_{IN} = (R_1 + R_2) > V_{BUS}(\text{max})/I_{DIV} = 1 \text{ kV DC}/500 \mu\text{A} = 2 \text{ M}\Omega \quad (7)$$

Also, the ratio of R_1/R_2 can be expressed as

$$R_1/R_2 = (1/K) - 1 = 231.558 \dots 254.814 \quad (8)$$

Thus, when selecting R_1 as two 1 M Ω high-voltage resistors in a series, R_2 can be calculated as

$$R_2 = 2 \text{ M}\Omega \times K = 8.6 \text{ k}\Omega \dots 7.82 \text{ k}\Omega \quad (9)$$

The divider's output resistance, R_{OUT} , with the input bias current, I_{BIAS} , defines the amount of bias error, which adds to the total error of the system. Bias error can be avoided by selecting R_1 and R_2 so that

$$R_{OUT} = R_1 || R_2 < 100 \text{ k}\Omega, \quad (10)$$

with above calculated resistors R_1 and R_2 ,

$$R_{OUT} = 2 \text{ M}\Omega || 7.82 \text{ k}\Omega = 7.8 \text{ k}\Omega, \quad (11)$$

which is well below the limit for R_{OUT} .

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM3195/ADuM4195 is highly immune to the external magnetic fields. The limitation on the ADuM3195/ADuM4195 magnetic field immunity is set by the condition whereby the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 4.5 V operating condition of the ADuM3195/ADuM4195 is examined because it represents the most susceptible mode of operation. The decoder can tolerate up to a 1.6 V noise induced by an external magnetic field. Assuming that there is a 50% margin, the decoder can safely operate with up to a 0.8 V induced noise. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \Sigma \pi r_n^2, n = 1, 2, \dots, N \quad (12)$$

where:

β is the magnetic field strength (Gs).

r_n is the radius of the n th turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3195/ADuM4195 and an imposed requirement that the induced voltage be,

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at most, 50% of the 1.6 V threshold at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 42.

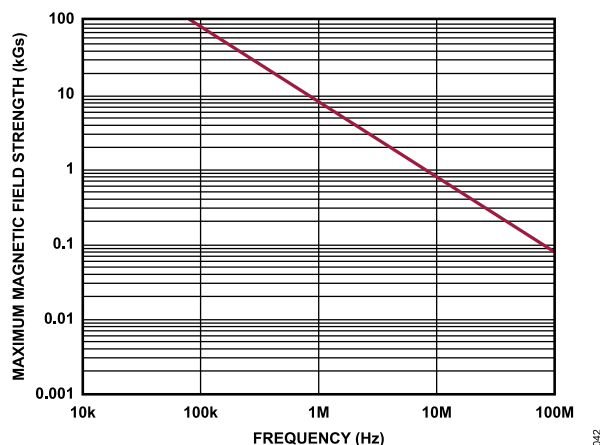


Figure 42. Maximum Allowable External Magnetic Field Strength

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 8 kGs induces a voltage of 0.8 V at the receiving coil. This is approximately 50% of the decoder threshold and does not cause a faulty output transition. The preceding magnetic field strength values correspond to the specific current magnitudes at given distances away from the ADuM3195/ADuM4195 transformers. Figure 43 shows these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 44, the ADuM3195/ADuM4195 is highly immune and can be affected only by extremely large currents operating at a high frequency very close to the component. For the 1 MHz example, a 20 kA current must be placed 5 mm away from the ADuM3195/ADuM4195 to affect the operation of the device.

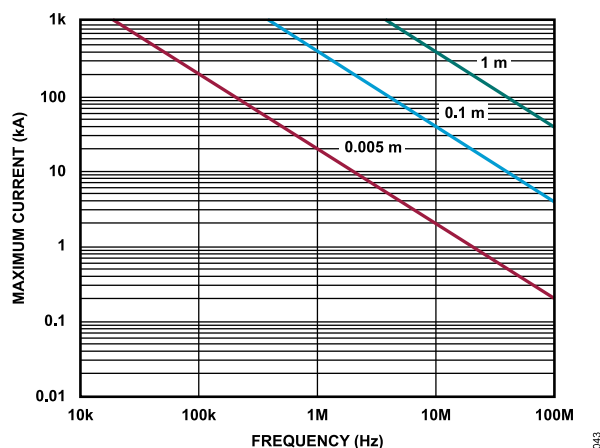


Figure 43. Maximum Allowable Current for Various Current-to-ADuM3195/ADuM4195 Spacings

LAYOUT CONSIDERATIONS

VDD₁ and VDD₂ must be decoupled to their respective GND₁ and GND₂ with capacitors of at least 1 μ F in parallel with 100 nF. In applications involving fast common-mode transients, ensure that the board coupling across the isolation barrier is minimized. To fully use the specified isolation properties of the ADuM3195/ADuM4195, the top and bottom copper layers of the PCB must not reach underneath the package, but must instead only reach as far as the solder-pad area. Place any decoupling used as close to the supply pins as possible. See Figure 44 for component placement suggestion.

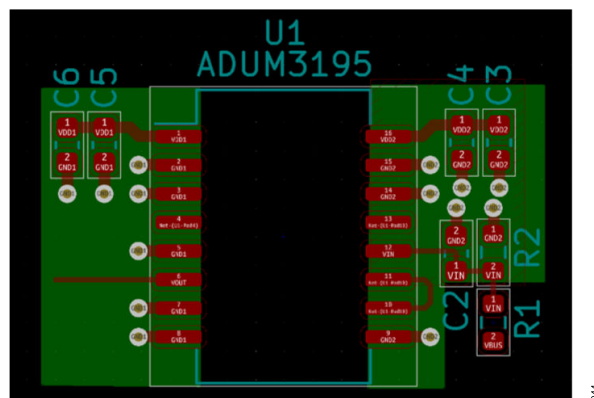


Figure 44. Placement of Decoupling Capacitors and Ground Planes GND₁

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RQ-16	QSOP	16-Lead Shrink Small Outline Package
RI-16-2	SOIC_IC	16-Lead Standard Small Outline Package, with Increased Creepage

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ^{1, 2}	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM3195BRQZ	-40°C to +125°C	16-Lead QSOP	TUBE, 98	RQ-16
ADuM3195BRQZ-RL7	-40°C to +125°C	16-Lead QSOP	REEL, 2500	RQ-16
ADuM3195WBRQZ	-40°C to +125°C	16-Lead QSOP	TUBE, 98	RQ-16
ADuM3195WBRQZ-RL7	-40°C to +125°C	16-Lead QSOP	REEL, 1000	RQ-16
ADuM4195BRIZ	-40°C to +125°C	16-Lead SOIC_IC	TUBE, 37	RI-16-2
ADuM4195BRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	REEL, 1000	RI-16-2
ADuM4195WBRIZ	-40°C to +125°C	16-Lead SOIC_IC	TUBE, 37	RI-16-2
ADuM4195WBRIZ-RL	-40°C to +125°C	16-Lead SOIC_IC	REEL, 1000	RI-16-2

¹ Z = RoHS Compliant Part.

² W = Qualified for Automotive Applications.

EVALUATION BOARDS

Model ¹	Description
EVAL-ADuM3195EBZ	ADuM3195 Evaluation Board
EVAL-ADuM4195EBZ	ADuM4195 Evaluation Board

¹ Z = RoHS Compliant Part.

AUTOMOTIVE PRODUCTS

The ADuM3195 and ADuM4195 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the [Specifications](#) section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.