SPI-/I²C-Compatible Temperature Sensor with 4-Channel ADC and Quad Voltage Output

Known Good Die

ADT7517-KGD

FEATURES

Four 10-bit DACs
Buffered voltage output
Guaranteed monotonic by design over all codes
10-bit temperature-to-digital converter
10-bit, 4-channel ADC
DC input bandwidth
Input range: 0 V to 2.28 V
Temperature range: −40°C to +120°C
Temperature sensor accuracy: ±3°C typical
Supply range: 2.7 V to 5.5 V
DAC output range: 0 V to V_{DD}
Power-down current: <10 µA
Internal 2.28 V_{REF} option
Double-buffered input logic
Buffered reference input
Power-on reset to 0 V DAC output
Simultaneous update of outputs (LDAC function)
On-chip, rail-to-rail output buffer amplifier
Compatible with SPI, I²C, QSPI, MICROWIRE, and DSP
Support for SMBus packet error checking (PEC)
Known good die (KGD): a die that is tested and guaranteed over the full specifications of the data sheet

APPLICATIONS

Process control
Smart battery chargers
Portable equipment

GENERAL DESCRIPTION

The ADT7517-KGD combines a 10-bit temperature-to-digital converter, a 10-bit, 4-channel ADC, and a quad 10-bit DAC in die form. The ADT7517-KGD also includes a band gap temperature sensor and a 10-bit ADC to monitor and digitize the temperature reading to a resolution of 0.25°C.

The ADT7517-KGD operates from a single 2.7 V to 5.5 V supply. The input voltage range on the ADC channels is 0 V to 2.28 V, and the input bandwidth is dc. The reference for the ADC channels is derived internally. The output voltage of the DAC ranges from 0 V to V_{DD}, with an output voltage settling time of 7 µs typical.

The ADT7517-KGD provides two serial interface options: a 4-wire serial interface that is compatible with SPI, QSPI™, MICROWIRE®, and DSP interface standards, and a 2-wire SMBus/I²C interface. The ADT7517-KGD features a standby mode that is controlled through the serial interface.

The reference for the four DACs is derived either internally or from a reference pad. The outputs of all DACs can be updated simultaneously using the software LDAC function or the external $\overline{\text{LDAC}}$ pad. The ADT7517-KGD incorporates a power-on reset circuit, ensuring that the DAC output powers up to 0 V and remains at 0 V until a valid write takes place.

Additional application and technical information can be found in the ADT7517 data sheet.

FUNCTIONAL BLOCK DIAGRAM

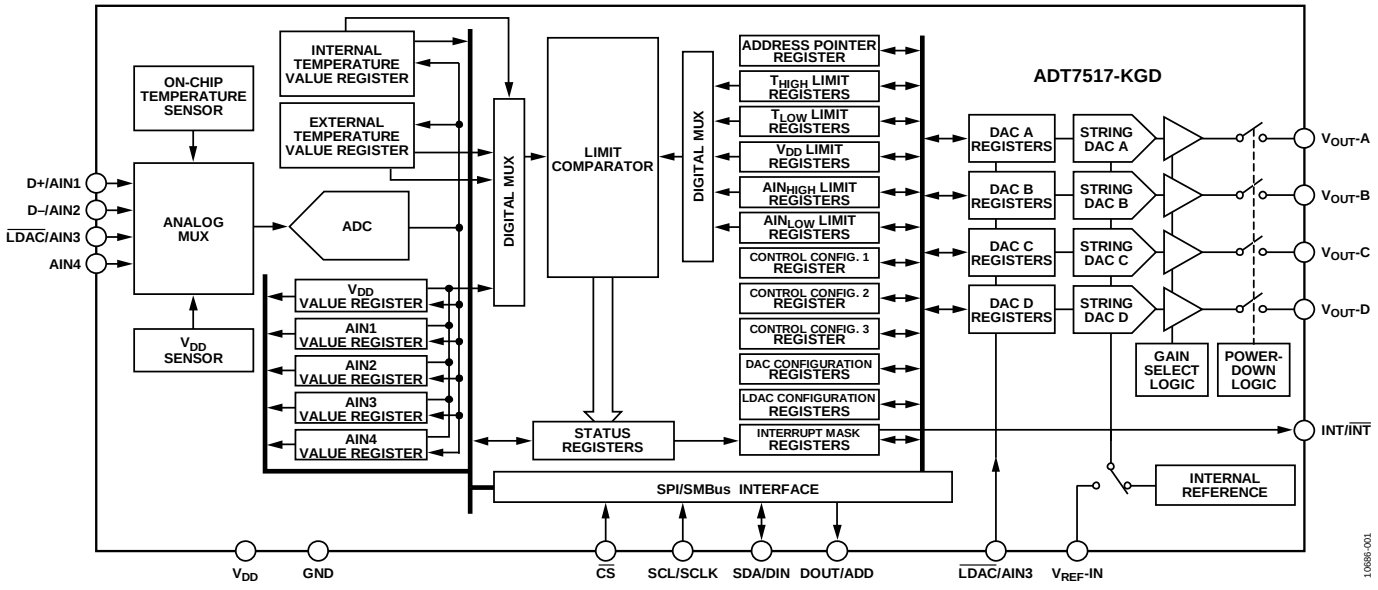

Figure 1.

Rev. A Document Feedback

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REVISION HISTORY

10/14—Rev. 0 to Rev. A

Change to Bond Pad Composition Value, Table 6 11

8/13—Revision 0: Initial Version

SPECIFICATIONS

Temperature range: −40°C to +120°C, V_{DD} = 2.7 V to 5.5 V, GND = 0 V, REF_{IN} = 2.25 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DAC DC PERFORMANCE[1, 2]					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic over all codes
Offset Error		±0.4	±2	% of FSR	
Gain Error		±0.3	±2	% of FSR	
Lower Deadband		20	65	mV	Lower deadband exists only if offset error is negative
Upper Deadband		60	100	mV	Upper deadband exists if $V_{REF} = V_{DD}$ and offset error plus gain error is positive
Offset Error Drift[3]		−12		ppm of FSR/°C	
Gain Error Drift[3]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[3]		−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[3]		200		µV	See Figure 5
ADC DC ACCURACY					Maximum V_{DD} = 5 V
Resolution			10	Bits	
Total Unadjusted Error (TUE)		2	3	% of FSR	V_{DD} = 2.7 V to 5.5 V
			2	% of FSR	V_{DD} = 3.3 V ± 10%
Offset Error			±0.5	% of FSR	
Gain Error			±2	% of FSR	
ADC BANDWIDTH			DC	Hz	
ANALOG INPUTS					
Input Voltage Range	0		2.28	V	AIN1 to AIN4, C4 = 0 in Control Configuration 3
	0		V_{DD}	V	AIN1 to AIN4, C4 = 1 in Control Configuration 3
DC Leakage Current			±1.5	µA	
Input Capacitance		5	20	pF	
Input Resistance		10		MΩ	
THERMAL CHARACTERISTICS					
Internal Temperature Sensor					Internal reference used, averaging on
Accuracy at V_{DD} = 3.3 V ± 10%		±3	±7	°C	T_A = 0°C to 85°C
Accuracy at V_{DD} = 5 V ± 5%		±3	±7	°C	T_A = 0°C to 85°C
Resolution			10	Bits	Equivalent to 0.25°C
Long-Term Drift		0.25		°C	Drift over 10 years if part is operated at 55°C
External Temperature Sensor					External transistor = 2N3906
Accuracy at V_{DD} = 3.3 V ± 10%		±3	±7	°C	T_A = 0°C to 85°C
Accuracy at V_{DD} = 5 V ± 5%		±3	±7	°C	T_A = 0°C to 85°C
Resolution			10	Bits	Equivalent to 0.25°C
Output Source Current		180		µA	High level
		11		µA	Low level
Thermal Voltage Output					
8-Bit DAC Output					
Resolution	1			°C	
Scale Factor		8.97		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		17.58		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C
10-Bit DAC Output					
Resolution	0.25			°C	
Scale Factor		2.2		mV/°C	0 V to V_{REF} output, T_A = −40°C to +120°C
		4.39		mV/°C	0 V to 2 V_{REF} output, T_A = −40°C to +120°C

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CONVERSION TIMES					Single-channel mode
Slow ADC					
V_{DD}/AIN		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
Internal Temperature		11.4		ms	Averaging (16 samples) on
		712		µs	Averaging off
External Temperature		24.22		ms	Averaging (16 samples) on
		1.51		ms	Averaging off
Fast ADC					
V_{DD}/AIN		712		µs	Averaging (16 samples) on
		44.5		µs	Averaging off
Internal Temperature		2.14		ms	Averaging (16 samples) on
		134		µs	Averaging off
External Temperature		14.25		ms	Averaging (16 samples) on
		890		µs	Averaging off
ROUND ROBIN UPDATE RATE[4]					Time to complete one measurement cycle through all channels
Slow ADC at 25°C					
Averaging On		79.8		ms	AIN1 and AIN2 are selected on Pad 8 and Pad 9
Averaging Off		4.99		ms	AIN1 and AIN2 are selected on Pad 8 and Pad 9
Averaging On		94.76		ms	D+ and D− are selected on Pad 8 and Pad 9
Averaging Off		9.26		ms	D+ and D− are selected on Pad 8 and Pad 9
Fast ADC at 25°C					
Averaging On		6.41		ms	AIN1 and AIN2 are selected on Pad 8 and Pad 9
Averaging Off		400.84		µs	AIN1 and AIN2 are selected on Pad 8 and Pad 9
Averaging On		21.77		ms	D+ and D− are selected on Pad 8 and Pad 9
Averaging Off		3.07		ms	D+ and D− are selected on Pad 8 and Pad 9
DAC EXTERNAL REFERENCE INPUT[3]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference
V_{REF} Input Impedance		>10		MΩ	Buffered reference and power-down mode
Reference Feedthrough		−90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz
ON-CHIP REFERENCE[3]					
Reference Voltage	2.2662	2.28	2.2938	V	
Temperature Coefficient		80		ppm/°C	
OUTPUT CHARACTERISTICS[3]					
Output Voltage[5]	0.001		V_{DD} − 0.1	V	This is a measure of the minimum and maximum drive capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short-Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode, V_{DD} = 5 V
		5		µs	Coming out of power-down mode, V_{DD} = 3.3 V
DIGITAL INPUTS[3]					
Input Current			±1	µA	V_{IN} = 0 V to V_{DD}
Input Low Voltage, V_{IL}			0.8	V	
Input High Voltage, V_{IH}	1.89			V	
Pad Capacitance		3	10	pF	All digital inputs
SCL, SDA Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
$\overline{\text{LDAC}}$ Pulse Width	20			ns	Edge triggered input

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL OUTPUT					
Output High Voltage, V_{OH}	2.4			V	$I_{SOURCE} = I_{SINK} = 200$ µA
Output Low Voltage, V_{OL}			0.4	V	$I_{OL} = 3$ mA
Output High Current, I_{OH}			1	mA	$V_{OH} = 5$ V
Output Capacitance, C_{OUT}			50	pF	
INT/$\overline{INT}$ Output Saturation Voltage			0.8	V	$I_{OUT} = 4$ mA
I^2C TIMING CHARACTERISTICS[6, 7]					See Figure 2
Serial Clock Period, t_1	2.5			µs	Fast mode I^2C
Data In Setup Time to SCL High, t_2	50			ns	
Data Out Stable After SCL Low, t_3	0			ns	
SDA Low Setup Time to SCL Low (Start Condition), t_4	50			ns	
SDA High Hold Time After SCL High (Stop Condition), t_5	50			ns	
SDA and SCL Fall Time, t_6			300	ns	
SDA and SCL Rise Time, t_7			300[8]	ns	
SPI TIMING CHARACTERISTICS[3, 9]					See Figure 3
$\overline{CS}$ to SCLK Setup Time, t_1	0			ns	
SCLK High Pulse Width, t_2	50			ns	
SCLK Low Pulse Width, t_3	50			ns	
Data Access Time After SCLK Falling Edge, t_4[10]			35	ns	
Data Setup Time Prior to SCLK Rising Edge, t_5	20			ns	
Data Hold Time After SCLK Rising Edge, t_6	0			ns	
$\overline{CS}$ to SCLK Hold Time, t_7	0			µs	
$\overline{CS}$ to DOUT High Impedance, t_8			40	ns	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	
V_{DD} Settling Time			50	ms	V_{DD} settles to within 10% of its final voltage level
I_{DD} (Normal Mode)[11]			3	mA	$V_{DD} = 3.3$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND
		2.2	3	mA	$V_{DD} = 5$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND
I_{DD} (Power-Down Mode)			10	µA	$V_{DD} = 3.3$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND
			10	µA	$V_{DD} = 5$ V, $V_{IH} = V_{DD}$, and V_{IL} = GND
Power Dissipation			10	mW	$V_{DD} = 3.3$ V, normal mode
			33	µW	$V_{DD} = 3.3$ V, shutdown mode

[1] DC specifications are tested with the outputs unloaded.
[2] Linearity is tested using a reduced code range: Code 28 to Code 1023.
[3] Guaranteed by design and characterization; not production tested.
[4] Round robin is the continuous sequential measurement of the following channels: V_{DD}, internal temperature, external temperature (AIN1, AIN2), AIN3, and AIN4.
[5] For the amplifier output to reach its minimum voltage, the offset error must be negative. For the amplifier output to reach its maximum voltage ($V_{REF} = V_{DD}$), the offset error plus gain error must be positive.
[6] The SDA and SCL timing is measured with the input filters turned on to meet the fast mode I^2C specification. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[7] Guaranteed by design; not production tested. All I^2C timing specifications are for fast mode operation, but the interface is still capable of handling the slower standard rate specifications.
[8] The interface is also capable of handling the I^2C standard mode rise time specification of 1000 ns.
[9] All input signals are specified with $t_R = t_F = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[10] Measured with the load circuit shown in Figure 4.
[11] The I_{DD} specification is valid for all DAC codes and full-scale analog input voltages. Interface inactive. All DACs and ADCs active. Load currents excluded.

DAC AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 4.7 kΩ to GND, C_L = 200 pF to GND, 4.7 kΩ to V_{DD}, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ[2]	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time		7	9	µs	$V_{REF} = V_{DD}$ = 5 V, 1/4 scale to 3/4 scale change (0x100 to 0x300)
Slew Rate		0.7		V/µs	
Major Code Change Glitch Energy		12		nV-sec	1 LSB change around major carry
Digital Feedthrough		0.5		nV-sec	
Digital Crosstalk		1		nV-sec	
Analog Crosstalk		0.5		nV-sec	
DAC-to-DAC Crosstalk		3		nV-sec	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p; frequency = 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] At 25°C.

TIMING DIAGRAMS

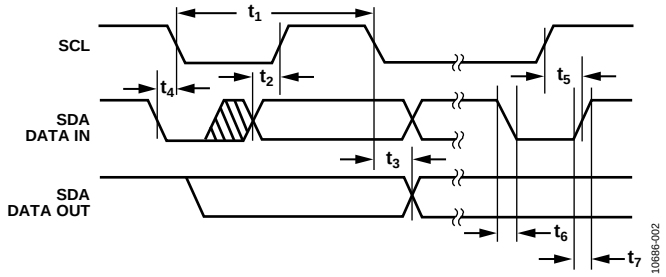

Figure 2. I²C Bus Timing Diagram

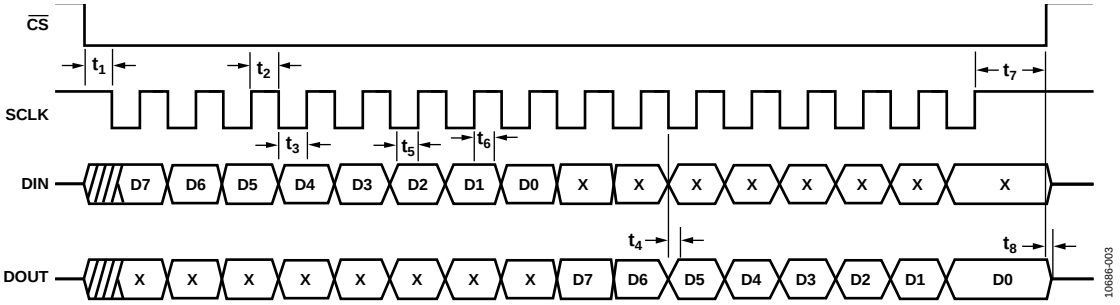

Figure 3. SPI Bus Timing Diagram

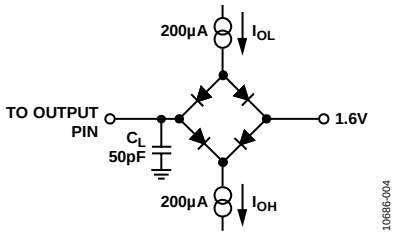

Figure 4. Load Circuit for Access Time and Bus Relinquish Time

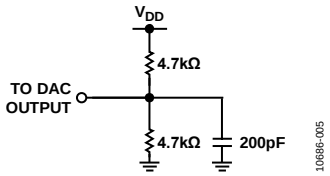

Figure 5. Load Circuit for DAC Outputs

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +120°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
IR Reflow Soldering	
Peak Temperature	220°C (0°C/5°C)
Time at Peak Temperature	10 sec to 20 sec
Ramp-Up Rate	3°C/sec maximum
Ramp-Down Rate	−6°C/sec maximum
Time 25°C to Peak Temperature	6 minutes maximum

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 4. I²C Address Selection

ADD Pad	I²C Address
Low	1001 000
Floating	1001 010
High	1001 011

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

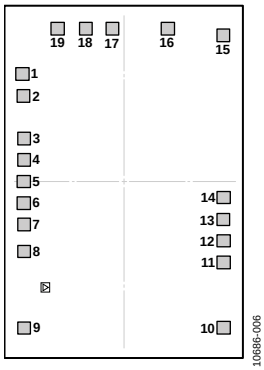

Figure 6. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
1	−764	+763	V_{REF}-IN	Reference Input Pad for All Four DACs. This input is buffered and has an input range from 1 V to V_{DD}.
2	−764	+608	$\overline{CS}$	SPI Active Low Control Input. $\overline{CS}$ is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it enables the input register, and data is transferred in on the rising edges and out on the falling edges of the subsequent serial clocks. It is recommended that this pad be tied high to V_{DD} when operating the serial interface in I^2C mode.
3	−764	+305	GND	Analog Ground.
4	−764	+155	GND	Analog Ground.
5	−764	+1	GND	Analog Ground.
6	−764	−152	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
7	−764	−306	V_{DD}	Positive Supply Voltage, 2.7 V to 5.5 V. The supply should be decoupled to ground.
8	−764	−502	D+/AIN1	Positive Connection to External Temperature Sensor (D+). Analog Input (AIN1). Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
9	−764	−1045	D−/AIN2	Negative Connection to External Temperature Sensor (D−). Analog Input (AIN2). Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
10	+764	−1045	$\overline{LDAC}$/AIN3	Active Low Control Input ($\overline{LDAC}$). Transfers the contents of the input registers to their respective DAC registers. A falling edge on this pad forces any or all DAC registers to be updated if the input registers have new data. A minimum pulse width of 20 ns must be applied to the $\overline{LDAC}$ pad to ensure proper loading of a DAC register. $\overline{LDAC}$ allows the simultaneous updating of all DAC outputs. Bit C3 of the Control Configuration 3 register enables the $\overline{LDAC}$ pad. By default, the $\overline{LDAC}$ pad controls the loading of the DAC registers. Analog Input (AIN3). Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
11	+764	−579	INT/$\overline{INT}$	Over Limit Interrupt. The output polarity of this pad can be set to provide an active low or active high interrupt when temperature, V_{DD}, or AIN limits are exceeded. The default is active low. This open-drain output requires a pull-up resistor.
12	+764	−425	DOUT/ADD	SPI Serial Data Output (DOUT). Logic output. Data is clocked out of any register at this pad on the falling edge of SCLK. This open-drain output requires a pull-up resistor. I^2C Serial Bus Address Selection Pad (ADD). Logic input. When this pad is low, the I^2C address is set to 1001 000; when the pad is left floating, the I^2C address is set to 1001 010; when the pad is high, the I^2C address is set to 1001 011. The I^2C address set by the ADD pad is not latched by the device until after the address is sent twice. On the eighth SCL cycle of the second valid communication, the serial bus address is latched in. Any subsequent change on this pad has no effect on the I^2C serial bus address.

Pad No.	X-Axis (µm)	Y-Axis (µm)	Mnemonic	Description
13	+764	−271	SDA/DIN	I^2C Serial Data Input/Output (SDA). I^2C serial data to be loaded into the registers of the part and read from these registers is provided on this pad. This open-drain configuration requires a pull-up resistor. SPI Serial Data Input (DIN). Serial data to be loaded into the registers of the part is provided on this pad. Data is clocked into a register on the rising edge of SCLK. This open-drain configuration requires a pull-up resistor.
14	+764	−117	SCL/SCLK	I^2C Serial Clock Input (SCL)/SPI Serial Clock Input (SCLK). This pad is the clock input for the serial port. The serial clock is used to clock data out of any register of the ADT7517-KGD and also to clock data into any register that can be written to. This open-drain configuration requires a pull-up resistor.
15	+764	+1043	AIN4	Analog Input. Single-ended analog input channel. Input range is 0 V to 2.28 V or 0 V to V_{DD}.
16	+338	+1092	V_{OUT}-D	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
17	−83	+1092	V_{OUT}-C	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
18	−285	+1092	V_{OUT}-B	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
19	−503	+1092	V_{OUT}-A	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.

OUTLINE DIMENSIONS

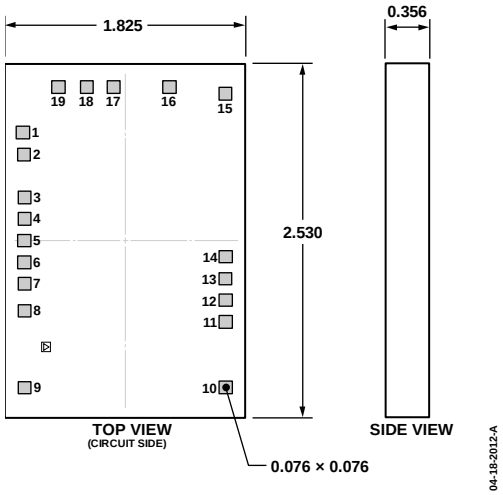

Figure 7. 19-Pad Bare Die [CHIP]
(C-19-1)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 6. Die Specifications

Parameter	Value	Unit
Chip Size	1707 × 2362	µm
Scribe Line Width	118 × 168	µm
Die Size	1825 × 2530	µm
Thickness	356	µm
Bond Pad	76	µm (minimum)
Bond Pad Composition	99.5% Al, 0.5% Cu	%
Backside	Not applicable	Not applicable
Passivation	Nitride	Not applicable

Table 7. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	No special requirements
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Pad 3, Pad 4, and Pad 5 first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADT7517-KGD-DF	−40°C to +120°C	19-Pad Bare Die [CHIP]	C-19-1

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).