

SUMMARY

High performance signal processor for communications, graphics and imaging applications

Super Harvard Architecture

4 independent buses for dual data fetch, instruction fetch, and nonintrusive I/O

32-bit IEEE floating-point computation units—multiplier, ALU, and shifter

Dual-ported on-chip SRAM and integrated I/O peripherals—a complete system-on-a-chip

Integrated multiprocessing features

240-lead thermally enhanced MQFP, PQ4 package, 225-ball plastic ball grid array (PBGA), 240-lead hermetic CQFP package

RoHS compliant packages

KEY FEATURES—PROCESSOR CORE

40 MIPS, 25 ns instruction rate, single-cycle instruction execution

120 MFLOPS peak, 80 MFLOPS sustained performance
Dual data address generators with modulo and bit-reverse addressing)

Efficient program sequencing with zero-overhead looping:
Single-cycle loop setup

IEEE JTAG Standard 1149.1 Test Access Port and on-chip emulation

32-bit single-precision and 40-bit extended-precision IEEE floating-point data formats or 32-bit fixed-point data format

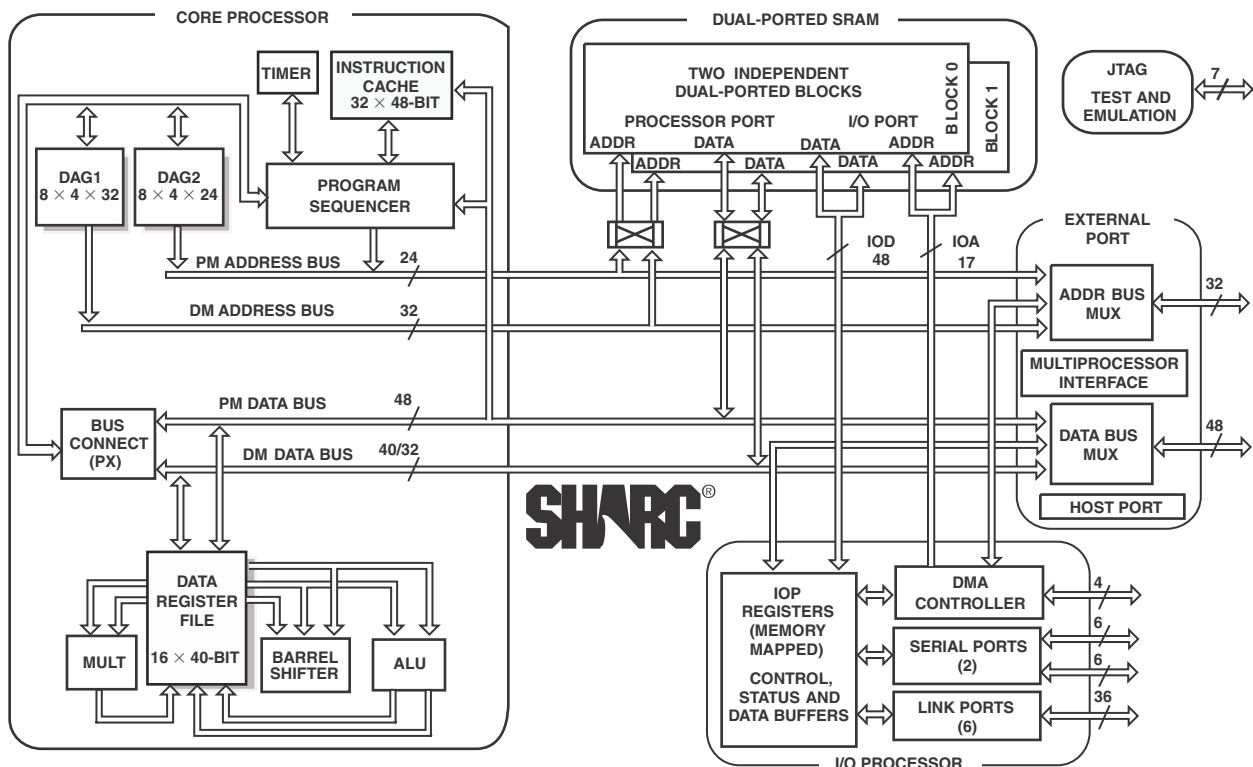


Figure 1. Functional Block Diagram

SHARC and the SHARC logo are registered trademarks of Analog Devices, Inc.

Rev. H

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 U.S.A.
Tel: 781.329.4700 ©2013 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

ADSP-21062/ADSP-21062L

PARALLEL COMPUTATIONS

Single-cycle multiply and ALU operations in parallel with dual memory read/writes and instruction fetch
Multiply with add and subtract for accelerated FFT butterfly computation

UP TO 4M BIT ON-CHIP SRAM

Dual-ported for independent access by core processor and DMA

OFF-CHIP MEMORY INTERFACING

4 gigawords addressable
Programmable wait state generation, page-mode DRAM support

DMA CONTROLLER

10 DMA channels for transfers between ADSP-2106x internal memory and external memory, external peripherals, host processor, serial ports, or link ports
Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

HOST PROCESSOR INTERFACE TO 16- AND 32-BIT MICROPROCESSORS

Host can directly read/write ADSP-2106x internal memory and IOP registers

MULTIPROCESSING

Glueless connection for scalable DSP multiprocessing architecture
Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-2106xs plus host
Six link ports for point-to-point connectivity and array multiprocessing
240 MBps transfer rate over parallel bus
240 MBps transfer rate over link ports

SERIAL PORTS

Two 40 Mbps synchronous serial ports with companding hardware
Independent transmit and receive functions

Table 1. ADSP-2106x SHARC Processor Family Features

| Feature | ADSP-21060 | ADSP-21062 | ADSP-21060L | ADSP-21062L | ADSP-21060C | ADSP-21060LC |
|-------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| SRAM | 4M bits | 2M bits | 4M bits | 2M bits | 4M bits | 4M bits |
| Operating Voltage | 5 V | 5 V | 3.3 V | 3.3 V | 5 V | 3.3 V |
| Instruction Rate | 33 MHz 40 MHz | 33 MHz 40 MHz | 33 MHz 40 MHz | 33 MHz 40 MHz | 33 MHz 40 MHz | 33 MHz 40 MHz |
| Package | MQFP_PQ4 PBGA | MQFP_PQ4 PBGA | MQFP_PQ4 PBGA | MQFP_PQ4 PBGA | CQFP | CQFP |

CONTENTS

| | | | |
|---|----|--|----|
| Summary | 1 | Electrical Characteristics (3.3 V) | 18 |
| General Description | 4 | Internal Power Dissipation (3.3 V) | 19 |
| SHARC Family Core Architecture | 4 | External Power Dissipation (3.3 V) | 20 |
| Memory and I/O Interface Features | 5 | Absolute Maximum Ratings | 20 |
| Development Tools | 8 | ESD Caution | 21 |
| Additional Information | 9 | Package Marking Information | 21 |
| Related Signal Chains | 9 | Timing Specifications | 21 |
| Pin Function Descriptions | 10 | Test Conditions | 48 |
| Target Board Connector for EZ-ICE Probe | 13 | Environmental Conditions | 51 |
| ADSP-21060/ADSP-21062 Specifications | 15 | 225-Ball PBGA Ball Configuration | 52 |
| Operating Conditions (5 V) | 15 | 240-Lead MQFP_PQ4/CQFP Pin Configuration | 54 |
| Electrical Characteristics (5 V) | 15 | Outline Dimensions | 56 |
| Internal Power Dissipation (5 V) | 16 | Surface-Mount Design | 61 |
| External Power Dissipation (5 V) | 17 | Ordering Guide | 62 |
| ADSP-21060L/ADSP-21062L Specifications | 18 | | |
| Operating Conditions (3.3 V) | 18 | | |

REVISION HISTORY

3/13—Rev. G to Rev. H

| | |
|--|----|
| Updated Development Tools | 8 |
| Corrected the power dissipation equation from $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0 \text{ V})$ to $P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3 \text{ V})$ | |
| External Power Dissipation (3.3 V) | 20 |

GENERAL DESCRIPTION

The ADSP-2106x SHARC®—Super Harvard Architecture Computer—is a 32-bit signal processing microcomputer that offers high levels of DSP performance. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 2 shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including up to 4M bit SRAM memory (see Table 1), a host processor interface, DMA controller, serial ports and link port, and parallel bus connectivity for glueless DSP multiprocessing.

Table 2. Benchmarks (at 40 MHz)

| Benchmark Algorithm | Speed | Cycles |
|---|--------------|--------|
| 1024 Point Complex FFT (Radix 4, with reversal) | 0.46 μ s | 18,221 |
| FIR Filter (per tap) | 25 ns | 1 |
| IIR Filter (per biquad) | 100 ns | 4 |
| Divide (y/x) | 150 ns | 6 |
| Inverse Square Root | 225 ns | 9 |
| DMA Transfer Rate | 240 Mbytes/s | |

The ADSP-2106x continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1 illustrates the following architectural features:

- Computation units (ALU, multiplier and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Interval timer
- On-chip SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and multiprocessor Interface
- DMA controller

- Serial ports and link ports
- JTAG Test Access Port

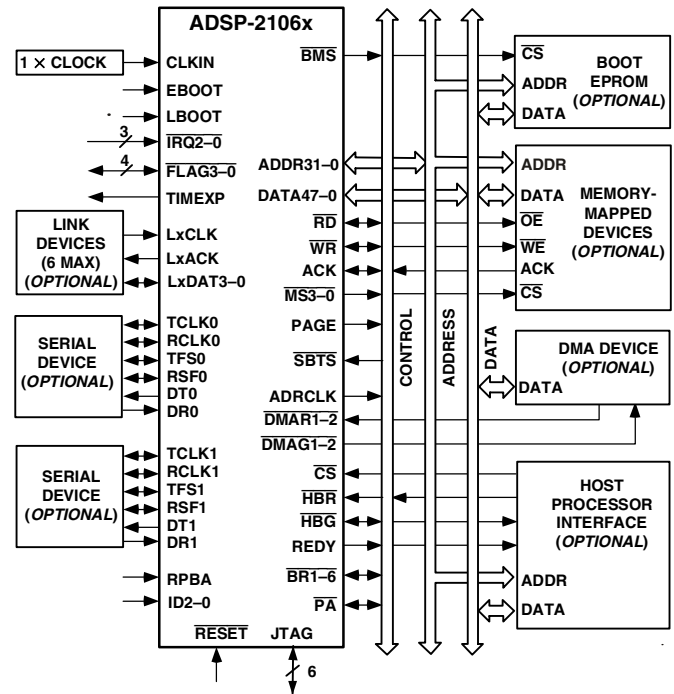


Figure 2. ADSP-2106x System Sample Configuration

SHARC FAMILY CORE ARCHITECTURE

The ADSP-2106x includes the following architectural features of the ADSP-21000 family core.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multi-function instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-2106x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see [Figure 1 on Page 1](#)). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-2106x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-2106x's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-2106x contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2106x can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-2106x processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21062/ADSP-21062L contains two megabits of on-chip SRAM, and the ADSP-21060/ADSP-21060L contains 4M bits of on-chip SRAM. The internal memory is organized as two equal sized blocks of 1M bit each for the ADSP-21062/ADSP-21062L and two equal sized blocks of 2M bits each for the ADSP-21060/ADSP-21060L. Each can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

On the ADSP-21062/ADSP-21062L, the memory can be configured as a maximum of 64k words of 32-bit data, 128k words of 16-bit data, 40k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to two megabits. All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words.

On the ADSP-21060/ADSP-21060L, the memory can be configured as a maximum of 128k words of 32-bit data, 256k words of 16-bit data, 80k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to four megabits. All of the memory can be accessed as 16-bit, 32-bit or 48-bit words.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that can be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

On-Chip Memory and Peripherals Interface

The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus.

Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold and disable time requirements.

Host Processor Interface

The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-2106x's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

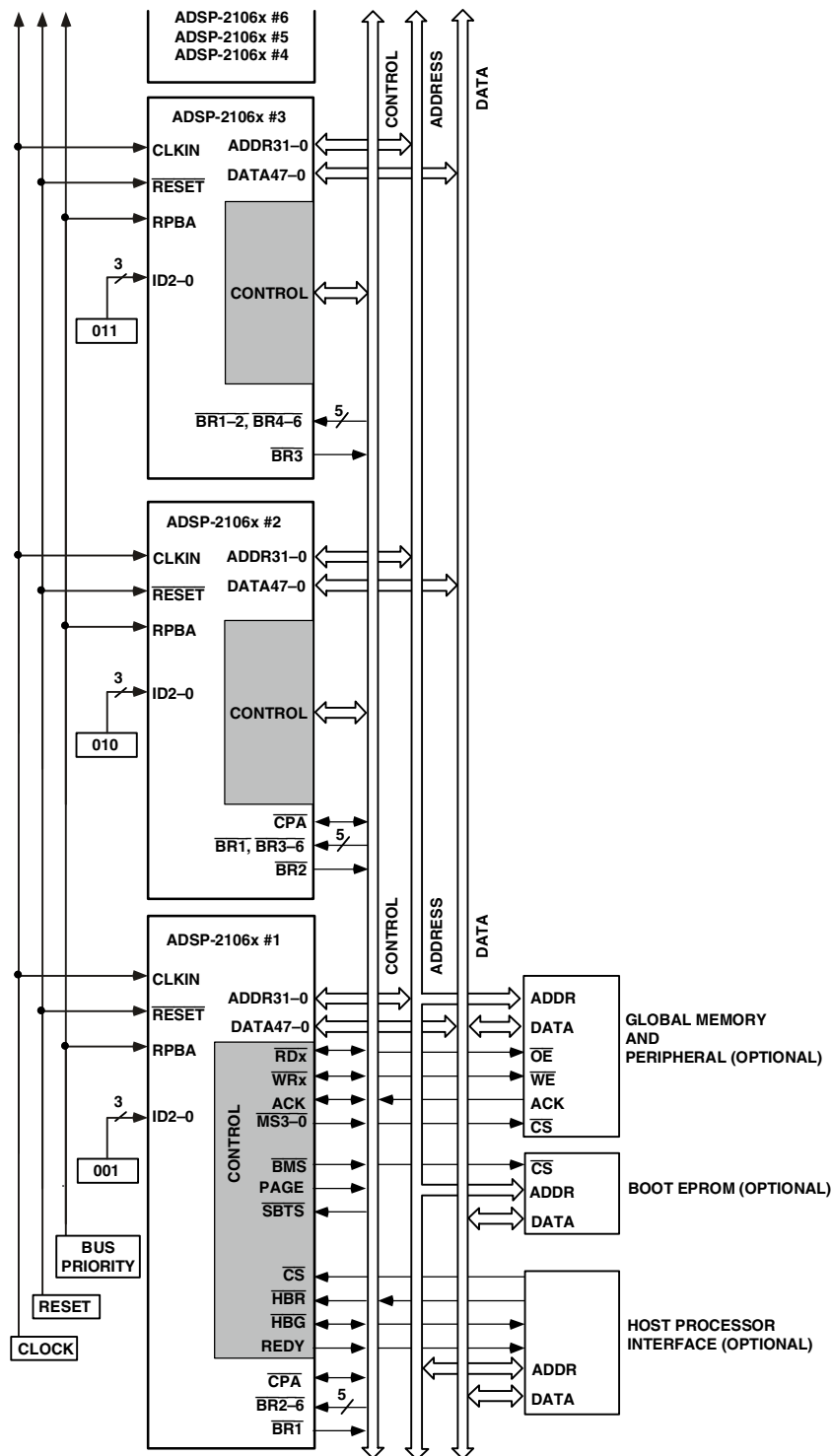


Figure 3. Shared Memory Multiprocessing System

DMA Controller

The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between the ADSP-2106x's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory, or I/O transfers). Four additional link port DMA channels are shared with Serial Port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can

control two DMA channels using DMA request/grant lines (DMARI-2, DMAGI-2). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Multiprocessing

The ADSP-2106x offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240M bytes/s over the link ports or external port. Broadcast writes allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

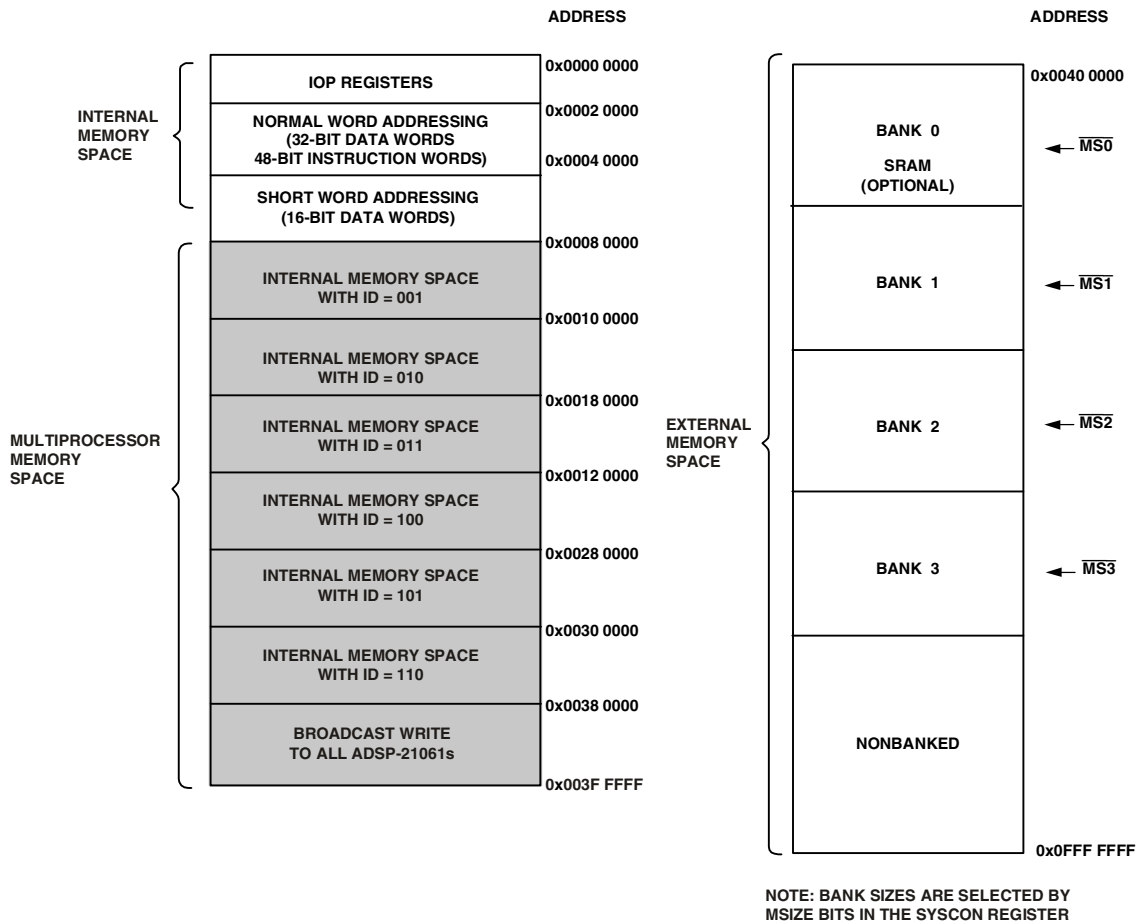


Figure 4. Memory Map

Link Ports

The ADSP-2106x features six 4-bit link ports that provide additional I/O capabilities. The link ports can be clocked twice per cycle, allowing each to transfer eight bits of data per cycle. Link-port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems.

The link ports can operate independently and simultaneously, with a maximum data throughput of 240M bytes/s. Link port data is packed into 32- or 48-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory.

Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Program Booting

The internal memory of the ADSP-2106x can be booted at system power-up from an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the BMS (boot memory select), EBOOT (EPROM Boot), and LBOOT (link/host boot) pins. 32-bit and 16-bit host processors can be used for booting. The processor also supports a no-boot mode in which instruction execution is sourced from the external memory.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip

emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set break-points, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2106x architecture and functionality. For detailed information on the ADSP-21000 family core architecture and instruction set, refer to the *ADSP-2106x SHARC User’s Manual*, Revision 2.1.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the “signal chain” entry in the [Glossary of EE Terms](#) on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (<http://www.analog.com/signalchains>) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

The ADSP-2106x pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for TRST).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31–0, DATA47–0, FLAG3–0, and inputs that have internal pull-up or pull-down resistors (CPA, ACK, DTx, DRx, TCLKx, RCLKx, LxDAT3–0, LxCCLK, LxACK, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 3. Pin Descriptions

| Pin | Type | Function |
|----------|-------|--|
| ADDR31–0 | I/O/T | External Bus Address. The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessor bus master is reading or writing its internal memory or IOP registers. |
| DATA47–0 | I/O/T | External Bus Data. The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47–8 of the bus. 16-bit short word data is transferred over bits 31–16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23–16. Pull-up resistors on unused DATA pins are not necessary. |
| MS3–0 | O/T | Memory Select Lines. These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The MS3–0 lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring, the MS3–0 lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. MS0 can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the MS3–0 lines are output by the bus master. |
| RD | I/O/T | Memory Read Strobe. This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert RD to read from the ADSP-2106x's internal memory. In a multiprocessing system, RD is output by the bus master and is input by all other ADSP-2106xs. |
| WR | I/O/T | Memory Write Strobe. This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert WR to write to the ADSP-2106x's internal memory. In a multiprocessing system, WR is output by the bus master and is input by all other ADSP-2106xs. |
| PAGE | O/T | DRAM Page Boundary. The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master. |
| ADRCLK | O/T | Clock Output Reference. In a multiprocessing system, ADRCLK is output by the bus master. |
| SW | I/O/T | Synchronous Write Select. This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts SW (low) to provide an early indication of an impending write cycle, which can be aborted if WR is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, SW is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. SW is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s). |

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when SBT_S is asserted, or when the ADSP-2106x is a bus slave)

Table 3. Pin Descriptions (Continued)

| Pin | Type | Function |
|-----------------------------|-----------|--|
| ACK | I/O/S | Memory Acknowledge. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-2106x deasserts ACK as an output to add waitstates to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-2106x deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven. |
| $\overline{\text{SBTS}}$ | I/S | Suspend Bus Three-State. External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-2106x attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-2106x deadlock, or used with a DRAM controller. |
| $\overline{\text{IRQ2-0}}$ | I/A | Interrupt Request Lines. May be either edge-triggered or level-sensitive. |
| FLAG3-0 | I/O/A | Flag Pins. Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals. |
| TIMEXP | O | Timer Expired. Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero. |
| $\overline{\text{HBR}}$ | I/A | Host Bus Request. This pin must be asserted by a host processor to request control of the ADSP-2106x's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-2106x places the address, data, select and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-2106x bus requests $\overline{\text{BR6-1}}$ in a multiprocessing system. |
| $\overline{\text{HBG}}$ | I/O | Host Bus Grant. Acknowledges a bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-2106x until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-2106x bus master and is monitored by all others. |
| $\overline{\text{CS}}$ | I/A | Chip Select. Asserted by host processor to select the ADSP-2106x. |
| REDY | O (O/D) | Host Bus Acknowledge. The ADSP-2106x deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted. |
| $\overline{\text{DMAR2-1}}$ | I/A | DMA Request 1 (DMA Channel 7) and DMA Request 2 (DMA Channel 8). |
| $\overline{\text{DMAG2-1}}$ | O/T | DMA Grant 1 (DMA Channel 7) and DMA Grant 2 (DMA Channel 8). |
| $\overline{\text{BR6-1}}$ | I/O/S | Multiprocessing Bus Requests. Used by multiprocessing ADSP-2106xs to arbitrate for bus master-ship. An ADSP-2106x only drives its own $\overline{\text{BRx}}$ line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-2106xs, the unused $\overline{\text{BRx}}$ pins should be pulled high; the processor's own $\overline{\text{BRx}}$ line must not be pulled high or low because it is an output. |
| $\overline{\text{ID2-0}}$ | O (O/D) | Multiprocessing ID. Determines which multiprocessing bus request ($\overline{\text{BR1- BR6}}$) is used by ADSP-2106x. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, etc. ID = 000 in single-processor systems. These lines are a system configuration selection that should be hardwired or changed at reset only. |
| RPBA | I/S | Rotating Priority Bus Arbitration Select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x. |
| $\overline{\text{CPA}}$ | I/O (O/D) | Core Priority Access. Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open drain output that is connected to all ADSP-2106xs in the system. The $\overline{\text{CPA}}$ pin has an internal 5 k Ω pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected. |
| DTx | O | Data Transmit (Serial Ports 0, 1). Each DT pin has a 50 k Ω internal pull-up resistor. |
| DRx | I | Data Receive (Serial Ports 0, 1). Each DR pin has a 50 k Ω internal pull-up resistor. |
| TCLKx | I/O | Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 k Ω internal pull-up resistor. |
| RCLKx | I/O | Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 k Ω internal pull-up resistor. |

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Table 3. Pin Descriptions (Continued)

| Pin | Type | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|--------------|---|---|--------------|---|---------------------|---|---|--------|---|---|---|-----------|----------------|---|---|-----------|-----------|---|---|-----------|--|---|---|-----------|----------|---|---|-----------|----------|
| TFSx | I/O | Transmit Frame Sync (Serial Ports 0, 1). | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RFSx | I/O | Receive Frame Sync (Serial Ports 0, 1). | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LxDAT3–0 | I/O | Link Port Data (Link Ports 0–5). Each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LxCLK | I/O | Link Port Clock (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LxACK | I/O | Link Port Acknowledge (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LPDRD bit of the LCOM register. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| EBOOT | I | EPROM Boot Select. When EBOOT is high, the ADSP-2106x is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LBOOT | I | Link Boot. When LBOOT is high, the ADSP-2106x is configured for link port booting. When LBOOT is low, the ADSP-2106x is configured for host processor booting or no booting. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{BMS}}$ | I/OT | Boot Memory Select. <i>Output:</i> Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. <i>Input:</i> When low, indicates that no booting will occur and that ADSP-2106x will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). <table><tr><td><i>EBOOT</i></td><td><i>LBOOT</i></td><td><i>$\overline{\text{BMS}}$</i></td><td><i>Booting Mode</i></td></tr><tr><td>1</td><td>0</td><td>Output</td><td>EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)</td></tr><tr><td>0</td><td>0</td><td>1 (Input)</td><td>Host Processor</td></tr><tr><td>0</td><td>1</td><td>1 (Input)</td><td>Link Port</td></tr><tr><td>0</td><td>0</td><td>0 (Input)</td><td>No Booting. Processor executes from external memory.</td></tr><tr><td>0</td><td>1</td><td>0 (Input)</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>x (Input)</td><td>Reserved</td></tr></table> | <i>EBOOT</i> | <i>LBOOT</i> | <i>$\overline{\text{BMS}}$</i> | <i>Booting Mode</i> | 1 | 0 | Output | EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) | 0 | 0 | 1 (Input) | Host Processor | 0 | 1 | 1 (Input) | Link Port | 0 | 0 | 0 (Input) | No Booting. Processor executes from external memory. | 0 | 1 | 0 (Input) | Reserved | 1 | 1 | x (Input) | Reserved |
| <i>EBOOT</i> | <i>LBOOT</i> | <i>$\overline{\text{BMS}}$</i> | <i>Booting Mode</i> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Output | EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 (Input) | Host Processor | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 (Input) | Link Port | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 (Input) | No Booting. Processor executes from external memory. | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 (Input) | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | x (Input) | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CLKIN | I | Clock In. External clock input to the ADSP-2106x. The instruction cycle rate is equal to CLKIN. CLKIN should not be halted, changed, or operated below the minimum specified frequency. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RESET}}$ | I/A | Processor Reset. Resets the ADSP-2106x to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TCK | I | Test Clock (JTAG). Provides an asynchronous clock for JTAG boundary scan. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TMS | I/S | Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDI | I/S | Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TDO | O | Test Data Output (JTAG). Serial scan output of the boundary scan path. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{TRST}}$ | I/A | Test Reset (JTAG). Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2106x. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{EMU}}$ | O | Emulation Status. Must be connected to the ADSP-2106x EZ-ICE target board connector only. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ICSA | O | Reserved, leave unconnected. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD | P | Power Supply; nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices. (30 pins). | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GND | G | Power Supply Return. (30 pins). | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| NC | | Do Not Connect. Reserved pins which must be left open and unconnected. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when SBT_S is asserted, or when the ADSP-2106x is a bus slave)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE[®] Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the furthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

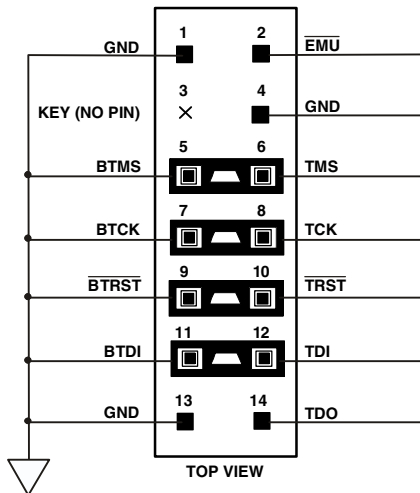


Figure 5. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers on the Bxxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD} . The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 4.

Table 4. Core Instruction Rate/CLKIN Ratio Selection

| Signal | Termination |
|---------------------------------------|---|
| TMS | Driven Through 22 Ω Resistor (16 mA Driver) |
| TCK | Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver) |
| $\overline{\text{TRST}}$ ¹ | Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled-Up by On-Chip 20 k Ω Resistor) |
| TDI | Driven by 22 Ω Resistor (16 mA Driver) |
| TDO | One TTL Load, Split Termination (160/220) |
| CLKIN | One TTL Load, Split Termination (160/220) |
| $\overline{\text{EMU}}$ | Active Low 4.7 k Ω Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP) |

¹ $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software start-up. After software start-up, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-2106x processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-2106xs (more than eight) in your system, then treat them as a “clock tree” using multiple drivers to minimize skew. (See Figure 7 and “JTAG Clock Tree” and “Clock Distribution” in the “High Frequency Design Considerations” section of the ADSP-2106x User’s Manual, Revision 2.1.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$ and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the ADSP-21000 Family JTAG EZ-ICE User’s Guide and Reference.

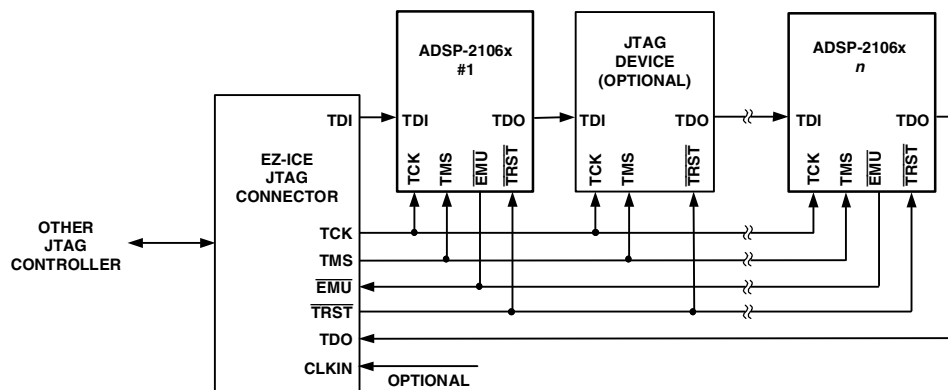


Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

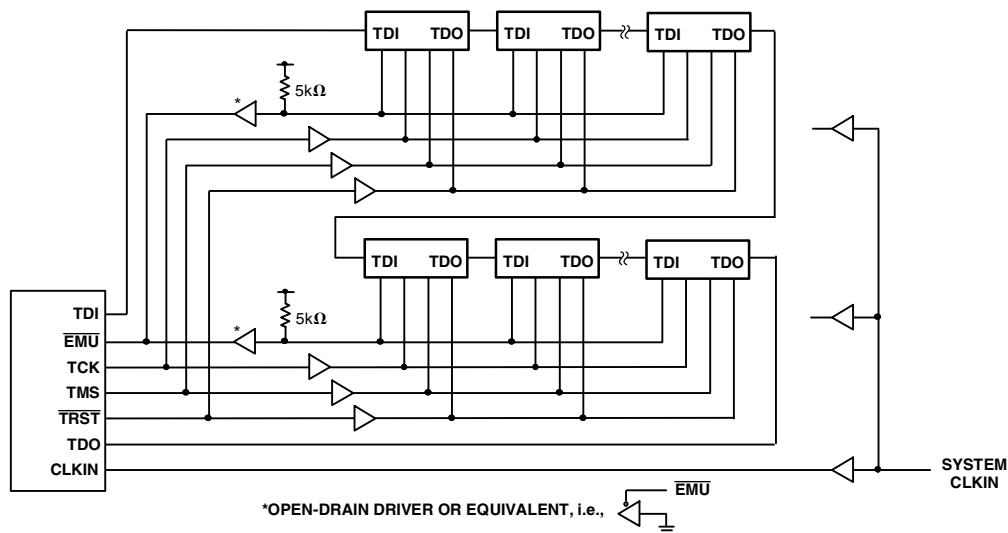


Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

ADSP-21060/ADSP-21062 SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (5 V)

| Parameter | Description | A Grade | | C Grade | | K Grade | | Unit |
|---------------------------------|--|---------|-----------------------|---------|-----------------------|---------|-----------------------|------|
| | | Min | Max | Min | Max | Min | Max | |
| V _{DD} | Supply Voltage | 4.75 | 5.25 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| T _{CASE} | Case Operating Temperature | -40 | +85 | -40 | +100 | -40 | +85 | °C |
| V _{IH} ¹ | High Level Input Voltage @ V _{DD} = Max | 2.0 | V _{DD} + 0.5 | 2.0 | V _{DD} + 0.5 | 2.0 | V _{DD} + 0.5 | V |
| V _{IH} ² | High Level Input Voltage @ V _{DD} = Max | 2.2 | V _{DD} + 0.5 | 2.2 | V _{DD} + 0.5 | 2.2 | V _{DD} + 0.5 | V |
| V _{IL} ^{1, 2} | Low Level Input Voltage @ V _{DD} = Min | -0.5 | +0.8 | -0.5 | +0.8 | -0.5 | +0.8 | V |

¹ Applies to input and bidirectional pins: DATA47-0, ADDR31-0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, ACK, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2-0}}$, FLAG3-0, HGB, CS, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{BR6-1}}$, ID2-0, RPBA, CPA, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCCLK, LxACK, EBOOT, LBOOT, BMS, TMS, TDI, TCK, HBR, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

² Applies to input pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.

ELECTRICAL CHARACTERISTICS (5 V)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--|-----------------------------|--|-----|-----|------|
| V _{OH} ^{1, 2} | High Level Output Voltage | @ V _{DD} = Min, I _{OH} = -2.0 mA | 4.1 | | V |
| V _{OL} ^{1, 2} | Low Level Output Voltage | @ V _{DD} = Min, I _{OL} = 4.0 mA | | 0.4 | V |
| I _{IH} ^{3, 4} | High Level Input Current | @ V _{DD} = Max, V _{IN} = V _{DD} Max | | 10 | μA |
| I _{IL} ³ | Low Level Input Current | @ V _{DD} = Max, V _{IN} = 0 V | | 10 | μA |
| I _{ILP} ⁴ | Low Level Input Current | @ V _{DD} = Max, V _{IN} = 0 V | | 150 | μA |
| I _{OZH} ^{5, 6, 7, 8} | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = V _{DD} Max | | 10 | μA |
| I _{OZL} ^{5, 9} | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = 0 V | | 10 | μA |
| I _{OZHP} ⁹ | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = V _{DD} Max | | 350 | μA |
| I _{OZLC} ⁷ | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = 0 V | | 1.5 | mA |
| I _{OZLA} ¹⁰ | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = 1.5 V | | 350 | μA |
| I _{OZLAR} ⁸ | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = 0 V | | 4.2 | mA |
| I _{OZLS} ⁶ | Three-State Leakage Current | @ V _{DD} = Max, V _{IN} = 0 V | | 150 | μA |
| C _{IN} ^{11, 12} | Input Capacitance | f _{IN} = 1 MHz, T _{CASE} = 25°C, V _{IN} = 2.5 V | | 4.7 | pF |

¹ Applies to output and bidirectional pins: DATA47-0, ADDR31-0, $\overline{\text{MS3-0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, ADRCLK, $\overline{\text{SW}}$, ACK, FLAG3-0, TIMEEXP, HBG, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BR6-1}}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCCLK, LxACK, BMS, TDO, EMU, ICSA.

² See Figure 31, Output Drive Currents 5 V, for typical drive current capabilities.

³ Applies to input pins: ACK, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2-0}}$, HBR, CS, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, ID2-0, RPBA, EBOOT, LBOOT, CLKIN, $\overline{\text{RESET}}$, TCK.

⁴ Applies to input pins with internal pull-ups: DR0, DR1, $\overline{\text{TRST}}$, TMS, TDI.

⁵ Applies to three-statable pins: DATA47-0, ADDR31-0, $\overline{\text{MS3-0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, ADRCLK, $\overline{\text{SW}}$, ACK, FLAG3-0, HBG, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, BMS, $\overline{\text{BR6-1}}$, TFSx, RFSx, TDO, EMU. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-2106x is not requesting bus mastership.)

⁶ Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

⁷ Applies to $\overline{\text{CPA}}$ pin.

⁸ Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-2106xL is not requesting bus mastership).

⁹ Applies to three-statable pins with internal pull-downs: LxDAT3-0, LxCCLK, LxACK.

¹⁰ Applies to ACK pin when keeper latch enabled.

¹¹ Applies to all signal pins.

¹² Guaranteed but not tested.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note “SHARC Power Dissipation Measurements.”

Specifications are based on the operating scenarios.

| Operation | Peak Activity ($I_{DDINPEAK}$) | High Activity ($I_{DDINHIGH}$) | Low Activity ($I_{DDINLOW}$) |
|---------------------|----------------------------------|----------------------------------|--------------------------------|
| Instruction Type | Multifunction | Multifunction | Single Function |
| Instruction Fetch | Cache | Internal Memory | Internal Memory |
| Core memory Access | 2 Per Cycle (DM and PM) | 1 Per Cycle (DM) | None |
| Internal Memory DMA | 1 Per Cycle | 1 Per 2 Cycles | 1 Per 2 Cycles |

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK I_{DDINPEAK} + \%HIGH I_{DDINHIGH} + \%LOW I_{DDINLOW} + \%IDLE I_{DDIDLE} = \text{Power Consumption}$$

| Parameter | Test Conditions | Max | Unit |
|---|--|------------|----------|
| $I_{DDINPEAK}$ Supply Current (Internal) ¹ | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 745 850 | mA mA |
| $I_{DDINHIGH}$ Supply Current (Internal) ² | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 575 670 | mA mA |
| $I_{DDINLOW}$ Supply Current (Internal) ² | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 340 390 | mA mA |
| I_{DDIDLE} Supply Current (Idle) ³ | $V_{DD} = \text{Max}$ | 200 | mA |

¹The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

² $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

³Idle denotes ADSP-2106x state during execution of IDLE instruction.

EXTERNAL POWER DISSIPATION (5 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can

drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K \times 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz ($t_{CK} = 25$ ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0 \text{ V})$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT} . Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 5. External Power Calculations (5 V Devices)

| Pin Type | No. of Pins | % Switching | $\times C$ | $\times f$ | $\times V_{DD}^2$ | = P_{EXT} |
|------------------|-------------|-------------|--------------------------|-------------------------|-----------------------|-------------|
| Address | 15 | 50 | $\times 44.7 \text{ pF}$ | $\times 10 \text{ MHz}$ | $\times 25 \text{ V}$ | = 0.084 W |
| $\overline{MS0}$ | 1 | 0 | $\times 44.7 \text{ pF}$ | $\times 10 \text{ MHz}$ | $\times 25 \text{ V}$ | = 0.000 W |
| \overline{WR} | 1 | – | $\times 44.7 \text{ pF}$ | $\times 20 \text{ MHz}$ | $\times 25 \text{ V}$ | = 0.022 W |
| Data | 32 | 50 | $\times 14.7 \text{ pF}$ | $\times 10 \text{ MHz}$ | $\times 25 \text{ V}$ | = 0.059 W |
| ADDRCLK | 1 | – | $\times 4.7 \text{ pF}$ | $\times 20 \text{ MHz}$ | $\times 25 \text{ V}$ | = 0.002 W |

$P_{EXT} = 0.167 \text{ W}$

ADSP-21060L/ADSP-21062L SPECIFICATIONS

Note that component specifications are subject to change without notice.

OPERATING CONDITIONS (3.3 V)

| Parameter | Description | A Grade | | C Grade | | K Grade | | Unit |
|----------------|--|---------|----------------|---------|----------------|---------|----------------|------|
| | | Min | Max | Min | Max | Min | Max | |
| V_{DD} | Supply Voltage | 3.15 | 3.45 | 3.15 | 3.45 | 3.15 | 3.45 | V |
| T_{CASE} | Case Operating Temperature | -40 | +85 | -40 | +100 | -40 | +85 | °C |
| $V_{IH}^{1,1}$ | High Level Input Voltage @ $V_{DD} = \text{Max}$ | 2.0 | $V_{DD} + 0.5$ | 2.0 | $V_{DD} + 0.5$ | 2.0 | $V_{DD} + 0.5$ | V |
| $V_{IH}^{2,2}$ | High Level Input Voltage @ $V_{DD} = \text{Max}$ | 2.2 | $V_{DD} + 0.5$ | 2.2 | $V_{DD} + 0.5$ | 2.2 | $V_{DD} + 0.5$ | V |
| $V_{IL}^{1,2}$ | Low Level Input Voltage @ $V_{DD} = \text{Min}$ | -0.5 | +0.8 | -0.5 | +0.8 | -0.5 | +0.8 | V |

¹ Applies to input and bidirectional pins: DATA47-0, ADDR31-0, \overline{RD} , \overline{WR} , \overline{SW} , ACK, SBT \overline{S} , $\overline{IRQ2-0}$, FLAG3-0, HGB, CS, DMAR1, DMAR2, BR6-1, ID2-0, RPBA, CPA, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCCLK, LxACK, EBOOT, LBOOT, BMS, TMS, TDI, TCK, HBR, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

² Applies to input pins: CLKIN, \overline{RESET} , \overline{TRST} .

ELECTRICAL CHARACTERISTICS (3.3 V)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---------------------|-----------------------------|---|-----|-----|---------------|
| $V_{OH}^{1,2}$ | High Level Output Voltage | @ $V_{DD} = \text{Min}$, $I_{OH} = -2.0 \text{ mA}$ | 2.4 | | V |
| $V_{OL}^{1,2}$ | Low Level Output Voltage | @ $V_{DD} = \text{Min}$, $I_{OL} = 4.0 \text{ mA}$ | | 0.4 | V |
| $I_{IH}^{3,4}$ | High Level Input Current | @ $V_{DD} = \text{Max}$, $V_{IN} = V_{DD} \text{ Max}$ | | 10 | μA |
| I_{IL}^3 | Low Level Input Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 10 | μA |
| I_{ILP}^4 | Low Level Input Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 150 | μA |
| $I_{OZH}^{5,6,7,8}$ | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = V_{DD} \text{ Max}$ | | 10 | μA |
| $I_{OZL}^{5,9}$ | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 10 | μA |
| I_{OZHP}^9 | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = V_{DD} \text{ Max}$ | | 350 | μA |
| I_{OZLC}^7 | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 1.5 | mA |
| I_{OZLA}^{10} | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 1.5 \text{ V}$ | | 350 | μA |
| I_{OZLAR}^8 | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 4.2 | mA |
| I_{OZLS}^6 | Three-State Leakage Current | @ $V_{DD} = \text{Max}$, $V_{IN} = 0 \text{ V}$ | | 150 | μA |
| $C_{IN}^{11,12}$ | Input Capacitance | $f_{IN} = 1 \text{ MHz}$, $T_{CASE} = 25^\circ\text{C}$, $V_{IN} = 2.5 \text{ V}$ | | 4.7 | pF |

¹ Applies to output and bidirectional pins: DATA47-0, ADDR31-0, $\overline{MS3-0}$, \overline{RD} , \overline{WR} , PAGE, ADRCLK, \overline{SW} , ACK, FLAG3-0, TIMEXP, HBG, REDY, DMAG1, DMAG2, BR6-1, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT3-0, LxCCLK, LxACK, BMS, TDO, EMU, ICSA.

² See Figure 35, Output Drive Currents 3.3 V, for typical drive current capabilities.

³ Applies to input pins: ACK, SBT \overline{S} , $\overline{IRQ2-0}$, HBR, CS, DMAR1, DMAR2, ID2-0, RPBA, EBOOT, LBOOT, CLKIN, \overline{RESET} , TCK.

⁴ Applies to input pins with internal pull-ups: DR0, DR1, \overline{TRST} , TMS, TDI.

⁵ Applies to three-statable pins: DATA47-0, ADDR31-0, $\overline{MS3-0}$, \overline{RD} , \overline{WR} , PAGE, ADRCLK, \overline{SW} , ACK, FLAG3-0, HBG, REDY, DMAG1, DMAG2, BMS, BR6-1, TFSx, RFSx, TDO, EMU. (Note that ACK is pulled up internally with 2 k Ω during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-2106x is not requesting bus mastership.)

⁶ Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

⁷ Applies to \overline{CPA} pin.

⁸ Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 k Ω during reset in a multiprocessor system, when ID2-0 = 001 and another ADSP-2106xL is not requesting bus mastership).

⁹ Applies to three-statable pins with internal pull-downs: LxDAT3-0, LxCCLK, LxACK.

¹⁰ Applies to ACK pin when keeper latch enabled.

¹¹ Applies to all signal pins.

¹² Guaranteed but not tested.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. For a complete discussion of the code used to measure power dissipation, see the technical note “SHARC Power Dissipation Measurements.”

Specifications are based on the operating scenarios.

| Operation | Peak Activity ($I_{DDINPEAK}$) | High Activity ($I_{DDINHIG}$) | Low Activity ($I_{DDINLOW}$) |
|---------------------|----------------------------------|---------------------------------|--------------------------------|
| Instruction Type | Multifunction | Multifunction | Single Function |
| Instruction Fetch | Cache | Internal Memory | Internal Memory |
| Core memory Access | 2 Per Cycle (DM and PM) | 1 Per Cycle (DM) | None |
| Internal Memory DMA | 1 Per Cycle | 1 Per 2 Cycles | 1 Per 2 Cycles |

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK I_{DDINPEAK} + \%HIGH I_{DDINHIG} + \%LOW I_{DDINLOW} + \%IDLE I_{DDIDLE} = \text{Power Consumption}$$

| Parameter | Test Conditions | Max | Unit |
|---|--|-----|------|
| $I_{DDINPEAK}$ Supply Current (Internal) ¹ | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ | 540 | mA |
| | $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 600 | mA |
| $I_{DDINHIG}$ Supply Current (Internal) ² | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ | 425 | mA |
| | $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 475 | mA |
| $I_{DDINLOW}$ Supply Current (Internal) ² | $t_{CK} = 30 \text{ ns}$, $V_{DD} = \text{Max}$ | 250 | mA |
| | $t_{CK} = 25 \text{ ns}$, $V_{DD} = \text{Max}$ | 275 | mA |
| I_{DDIDLE} Supply Current (Idle) ³ | $V_{DD} = \text{Max}$ | 180 | mA |

¹The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

² $I_{DDINHIG}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

³Idle denotes ADSP-2106xL state during execution of IDLE instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can

drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128K \times 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz ($t_{CK} = 25$ ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3 \text{ V})$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT} . Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 6. External Power Calculations (3.3 V Devices)

| Pin Type | No. of Pins | % Switching | $\times C$ | $\times f$ | $\times V_{DD}^2$ | = P_{EXT} |
|------------------|-------------|-------------|------------------|-----------------|-------------------|-------------|
| Address | 15 | 50 | $\times 44.7$ pF | $\times 10$ MHz | $\times 10.9$ V | = 0.037 W |
| $\overline{MS0}$ | 1 | 0 | $\times 44.7$ pF | $\times 10$ MHz | $\times 10.9$ V | = 0.000 W |
| \overline{WR} | 1 | – | $\times 44.7$ pF | $\times 20$ MHz | $\times 10.9$ V | = 0.010 W |
| Data | 32 | 50 | $\times 14.7$ pF | $\times 10$ MHz | $\times 10.9$ V | = 0.026 W |
| ADDRCLK | 1 | – | $\times 4.7$ pF | $\times 20$ MHz | $\times 10.9$ V | = 0.001 W |

$P_{EXT} = 0.074$ W

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed [Table 7](#) may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater

than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

| Parameter | ADSP-21060/ADSP-21060C ADSP-21062 5 V | ADSP-21060L/ADSP-21060LC ADSP-21062L 3.3 V |
|---------------------------------|---|--|
| Supply Voltage (V_{DD}) | –0.3 V to +7.0 V | –0.3 V to +4.6 V |
| Input Voltage | –0.5 V to $V_{DD} + 0.5$ V | –0.5 V to $V_{DD} + 0.5$ V |
| Output Voltage Swing | –0.5 V to $V_{DD} + 0.5$ V | –0.5 V to $V_{DD} + 0.5$ V |
| Load Capacitance | 200 pF | 200 pF |
| Storage Temperature Range | –65°C to +150°C | –65°C to +150°C |
| Lead Temperature (5 seconds) | 280°C | 280°C |
| Junction Temperature Under Bias | 130°C | 130°C |

ESD CAUTION**ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

Figure 8 and Table 8 provide information on detail contained within the package marking for the ADSP-2106x processors (actual marking format may vary). For a complete listing of product availability, see [Ordering Guide on Page 62](#).



Figure 8. Typical Package Brand

Table 8. Package Brand Information

| Brand Key | Field Description |
|-----------|-----------------------|
| t | Temperature Range |
| pp | Package Type |
| Z | Lead (Pb) Free Option |
| ccc | See Ordering Guide |
| vvvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| yyww | Date Code |

TIMING SPECIFICATIONS

The ADSP-2106x processors are available at maximum processor speeds of 33 MHz (–133), and 40 MHz (–160). The timing specifications are based on a CLKIN frequency of 40 MHz ($t_{CK} = 25$ ns). The DT derating factor enables the calculation for timing specifications within the min to max range of the t_{CK} specification (see [Table 9](#)). DT is the difference between the derated CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25 \text{ ns}$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

For voltage reference levels, see [Figure 28 on Page 48](#) under Test Conditions.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices. (O/D) = Open Drain, (A/D) = Active Drive.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

ADSP-21062/ADSP-21062L

Clock Input

Table 9. Clock Input

| | | ADSP-21060 ADSP-21062 40 MHz, 5 V | | ADSP-21060 ADSP-21062 33 MHz, 5 V | | ADSP-21060L ADSP-21062L 40 MHz, 3.3 V | | ADSP-21060L ADSP-21062L 33 MHz, 3.3 V | | |
|---------------------|----------------------------------|---|-----|---|-----|---|-----|---|-----|----|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Timing Requirements | | | | | | | | | | |
| t _{CK} | CLKIN Period | 25 | 100 | 30 | 100 | 25 | 100 | 30 | 100 | ns |
| t _{CKL} | CLKIN Width Low | 7 | | 7 | | 8.75 | | 8.75 ¹ | | ns |
| t _{CKH} | CLKIN Width High | 5 | | 5 | | 5 | | 5 | | ns |
| t _{CKRF} | CLKIN Rise/Fall (0.4 V to 2.0 V) | | 3 | | 3 | | 3 | | 3 | ns |

¹ For the ADSP-21060LC, this specification is 9.5 ns min.

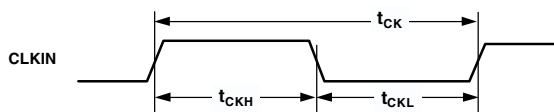


Figure 9. Clock Input

Reset

Table 10. Reset

| Parameter | 5 V and 3.3 V | | Unit |
|--|------------------|-----------------|------|
| | Min | Max | |
| Timing Requirements | | | |
| t _{WRST} $\overline{\text{RESET}}$ Pulse Width Low ¹ | 4t _{CK} | | ns |
| t _{SRST} $\overline{\text{RESET}}$ Setup Before CLKIN High ² | 14 + DT/2 | t _{CK} | ns |

¹ Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 μ s while \overline{RESET} is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

² Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

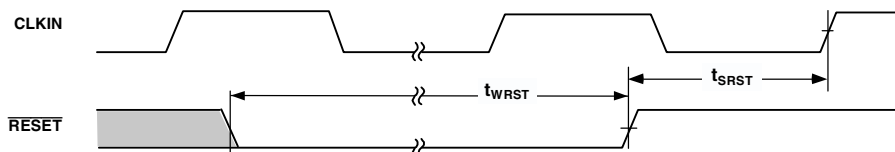


Figure 10. Reset

Interrupts

Table 11. Interrupts

| | | 5 V and 3.3 V | | |
|---------------------|--|---------------------|------------|------|
| Parameter | | Min | Max | Unit |
| Timing Requirements | | | | |
| t _{SIR} | $\overline{IRQ2-0}$ Setup Before CLKIN High ¹ | 18 + 3DT/4 | | ns |
| t _{HIR} | $\overline{IRQ2-0}$ Hold Before CLKIN High ¹ | | 12 + 3DT/4 | ns |
| t _{PW} | $\overline{IRQ2-0}$ Pulse Width ² | 2 + t _{CK} | | ns |

¹ Only required for \overline{IRQx} recognition in the following cycle.

² Applies only if t_{SIR} and t_{HIR} requirements are not met.

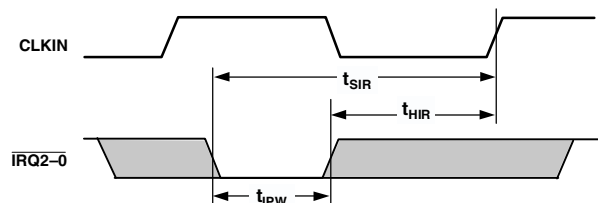


Figure 11. Interrupts

Timer

Table 12. Timer

| Parameter | 5 V and 3.3 V | | Unit |
|--------------------------|----------------------|-----|------|
| | Min | Max | |
| Switching Characteristic | | | |
| t _{DTEX} | CLKIN High to TIMEXP | 15 | ns |

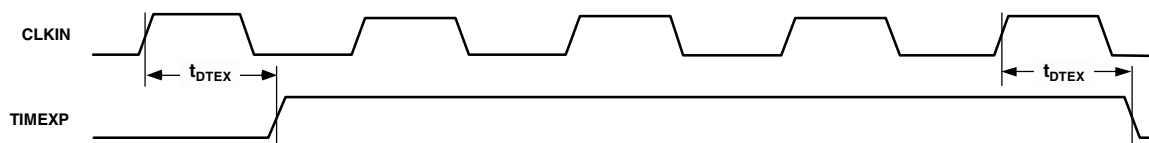


Figure 12. Timer

Flags

Table 13. Flags

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|---|---------------|------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{SFI} | FLAG3–0 IN Setup Before CLKIN High ¹ | 8 + 5DT/16 | | ns |
| t _{HFI} | FLAG3–0 IN Hold After CLKIN High ¹ | 0 – 5DT/16 | | ns |
| t _{DWRFI} | FLAG3–0 IN Delay After $\overline{RD}/\overline{WR}$ Low ¹ | | 5 + 7DT/16 | ns |
| t _{HFIWR} | FLAG3–0 IN Hold After $\overline{RD}/\overline{WR}$ Deasserted ¹ | 0 | | ns |
| Switching Characteristics | | | | |
| t _{DFO} | FLAG3–0 OUT Delay After CLKIN High | | 16 | ns |
| t _{HFO} | FLAG3–0 OUT Hold After CLKIN High | 4 | | ns |
| t _{DFOE} | CLKIN High to FLAG3–0 OUT Enable | 3 | | ns |
| t _{DFOD} | CLKIN High to FLAG3–0 OUT Disable | | 14 | ns |

¹ Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

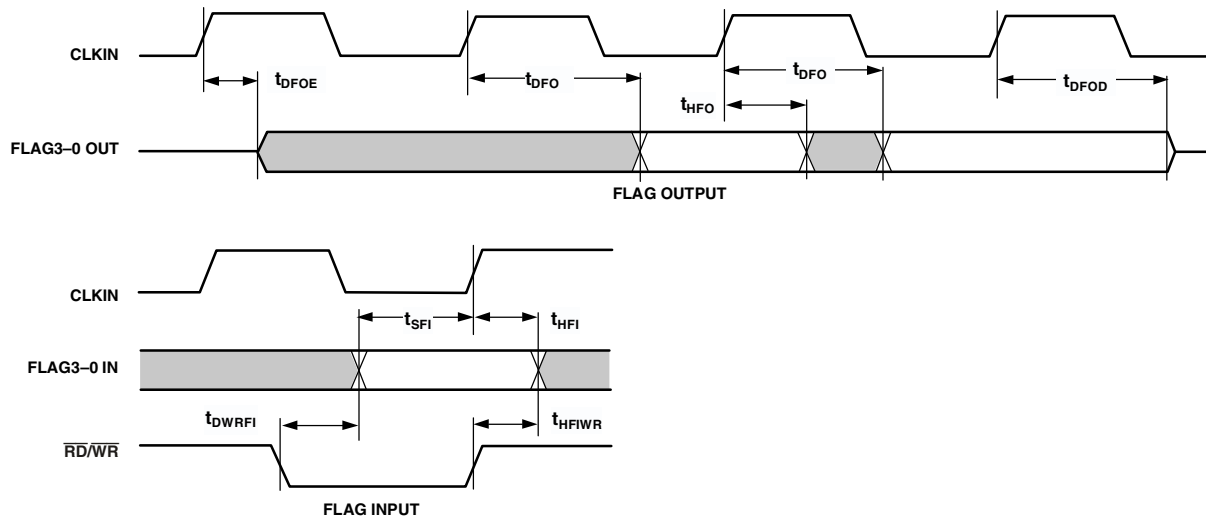


Figure 13. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the

bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, \overline{RD} , \overline{WR} , and \overline{DMAGx} strobe timing parameters only applies to asynchronous access mode.

Table 14. Memory Read—Bus Master

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|--|------------------|----------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{DAD} | Address Selects Delay to Data Valid ^{1, 2} | | 18 + DT + W | ns |
| t _{DRLD} | \overline{RD} Low to Data Valid ¹ | | 12 + 5DT/8 + W | ns |
| t _{HDA} | Data Hold from Address, Selects ³ | 0.5 | | ns |
| t _{HDRH} | Data Hold from \overline{RD} High ³ | 2.0 | | ns |
| t _{DAAK} | ACK Delay from Address, Selects ^{2, 4} | | 14 + 7DT/8 + W | ns |
| t _{DSAK} | ACK Delay from \overline{RD} Low ⁴ | | 8 + DT/2 + W | ns |
| Switching Characteristics | | | | |
| t _{DRHA} | Address Selects Hold After \overline{RD} High | 0 + H | | ns |
| t _{DARL} | Address Selects to \overline{RD} Low ² | 2 + 3DT/8 | | ns |
| t _{RW} | \overline{RD} Pulse Width | 12.5 + 5DT/8 + W | | ns |
| t _{RWR} | \overline{RD} High to \overline{WR} , \overline{RD} , \overline{DMAGx} Low | 8 + 3DT/8 + HI | | ns |
| t _{SADADC} | Address, Selects Setup Before ADRCLK High ² | 0 + DT/4 | | ns |

$W = (\text{number of wait states specified in WAIT register}) \times t_{CK}$.

$HI = t_{CK}$ (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise $HI = 0$).

$H = t_{CK}$ (if an address hold cycle occurs as specified in WAIT register; otherwise $H = 0$).

¹ Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI} .

² The falling edge of \overline{MSx} , \overline{SW} , \overline{BMS} is referenced.

³ Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI} . See [Example System Hold Time Calculation on Page 48](#) for the calculation of hold times given capacitive and dc loads.

⁴ ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

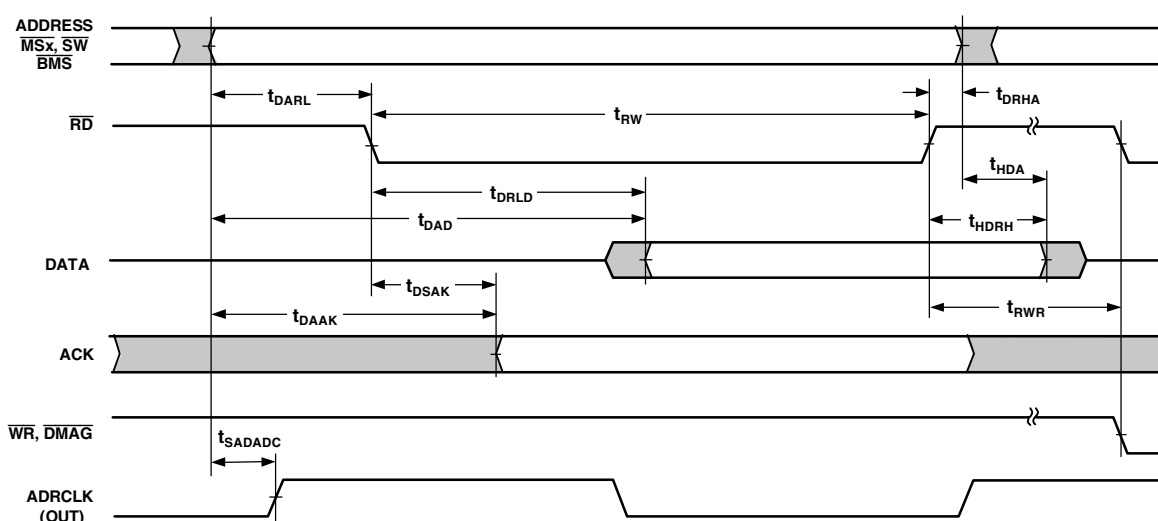


Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the

bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, \overline{RD} , \overline{WR} , and \overline{DMAGx} strobe timing parameters only applies to asynchronous access mode.

Table 15. Memory Write—Bus Master

| Parameter | 5 V and 3.3 V | | Unit |
|---------------------------|--|-------------|------|
| | Min | Max | |
| Timing Requirements | | | |
| t _{DAAK} | ACK Delay from Address, Selects ^{1,2} | | ns |
| t _{DSAK} | ACK Delay from \overline{WR} Low ¹ | | ns |
| Switching Characteristics | | | |
| t _{DAWH} | Address Selects to \overline{WR} Deasserted ² | | ns |
| t _{DAWL} | Address Selects to \overline{WR} Low ² | | ns |
| t _{WW} | \overline{WR} Pulse Width | | ns |
| t _{DDWH} | Data Setup Before \overline{WR} High | | ns |
| t _{DWAH} | Address Hold After \overline{WR} Deasserted | | ns |
| t _{DATRWH} | Data Disable After \overline{WR} Deasserted ³ | 6 + DT/16+H | ns |
| t _{WWR} | \overline{WR} High to \overline{WR} , \overline{RD} , \overline{DMAGx} Low | | ns |
| t _{DDWR} | Data Disable Before \overline{WR} or \overline{RD} Low | | ns |
| t _{WDE} | \overline{WR} Low to Data Enabled | | ns |
| t _{SADADC} | Address, Selects Setup Before ADRCLK High ² | | ns |

W = (number of wait states specified in WAIT register) $\times t_{CK}$.

H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise $H = 0$).

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise $HI = 0$).

I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise $I = 0$).

¹ ACK is not sampled on external memory accesses that use the internal wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes external, either, or both (both, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACK} must be met for wait state modes external, either, or both (both, after internal wait states have completed).

² The falling edge of \overline{MSx} , \overline{SW} , \overline{BMS} is referenced.

³ See [Example System Hold Time Calculation on Page 48](#) for calculation of hold times given capacitive and dc loads.

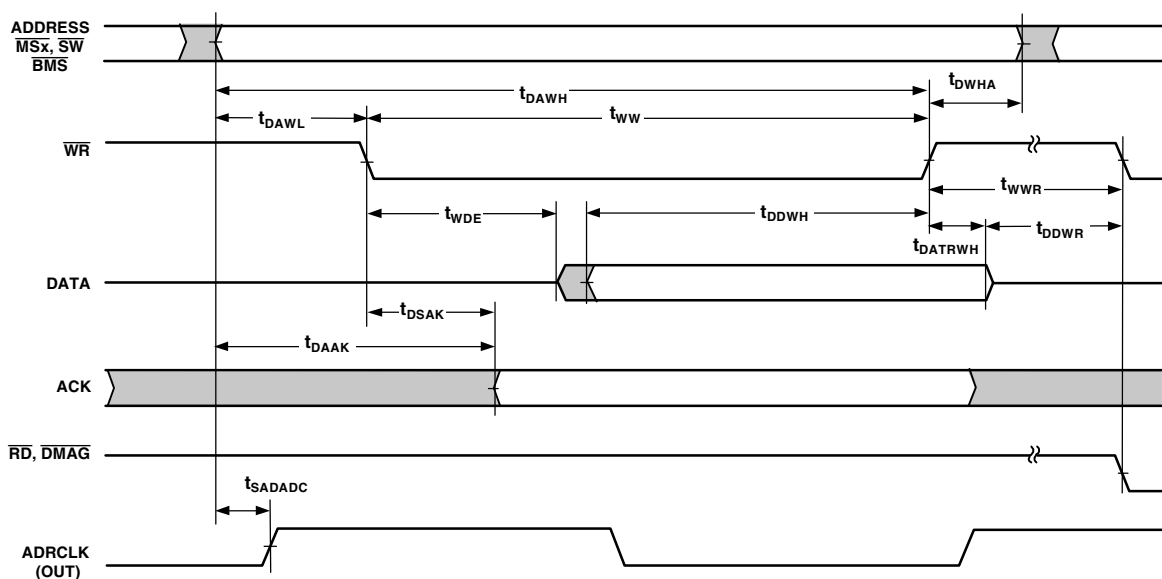


Figure 15. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see [Memory Read—Bus Master on Page 25](#) and [Memory Write—](#)

[Bus Master on Page 26](#)). When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see [Synchronous Read/Write—Bus Slave on Page 30](#)). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 16. Synchronous Read/Write—Bus Master

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|---|--------------------------|----------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| tSSDATI | Data Setup Before CLKIN | 3 + DT/8 | | ns |
| tHSDATI | Data Hold After CLKIN | 3.5 – DT/8 | | ns |
| tDAAK | ACK Delay After Address, Selects ^{1, 2} | | 14 + 7DT/8 + W | ns |
| tSACKC | ACK Setup Before CLKIN ² | 6.5 + DT/4 | | ns |
| tHACK | ACK Hold After CLKIN | –1 – DT/4 | | ns |
| Switching Characteristics | | | | |
| tDADRO | Address, \overline{MSx} , \overline{BMS} , \overline{SW} Delay After CLKIN ¹ | | 7 – DT/8 | ns |
| tHADRO | Address, \overline{MSx} , \overline{BMS} , \overline{SW} Hold After CLKIN | –1 – DT/8 | | ns |
| tDPGC | PAGE Delay After CLKIN | 9 + DT/8 | 16 + DT/8 | ns |
| tDRDO | \overline{RD} High Delay After CLKIN | –2 – DT/8 | 4 – DT/8 | ns |
| tDWRO | \overline{WR} High Delay After CLKIN | –3 – 3DT/16 | 4 – 3DT/16 | ns |
| tDRWL | $\overline{RD}/\overline{WR}$ Low Delay After CLKIN | 8 + DT/4 | 12.5 + DT/4 | ns |
| tSDDATO | Data Delay After CLKIN | | 19 + 5DT/16 | ns |
| tDATTR | Data Disable After CLKIN ³ | 0 – DT/8 | 7 – DT/8 | ns |
| tDADCKK | ADRCLK Delay After CLKIN | 4 + DT/8 | 10 + DT/8 | ns |
| tADRCK | ADRCLK Period | t _{CK} | | ns |
| tADRCKH | ADRCLK Width High | (t _{CK} /2 – 2) | | ns |
| tADRCKL | ADRCLK Width Low | (t _{CK} /2 – 2) | | ns |

¹ The falling edge of \overline{MSx} , \overline{SW} , \overline{BMS} is referenced.

² ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).

³ See [Example System Hold Time Calculation on Page 48](#) for calculation of hold times given capacitive and dc loads.

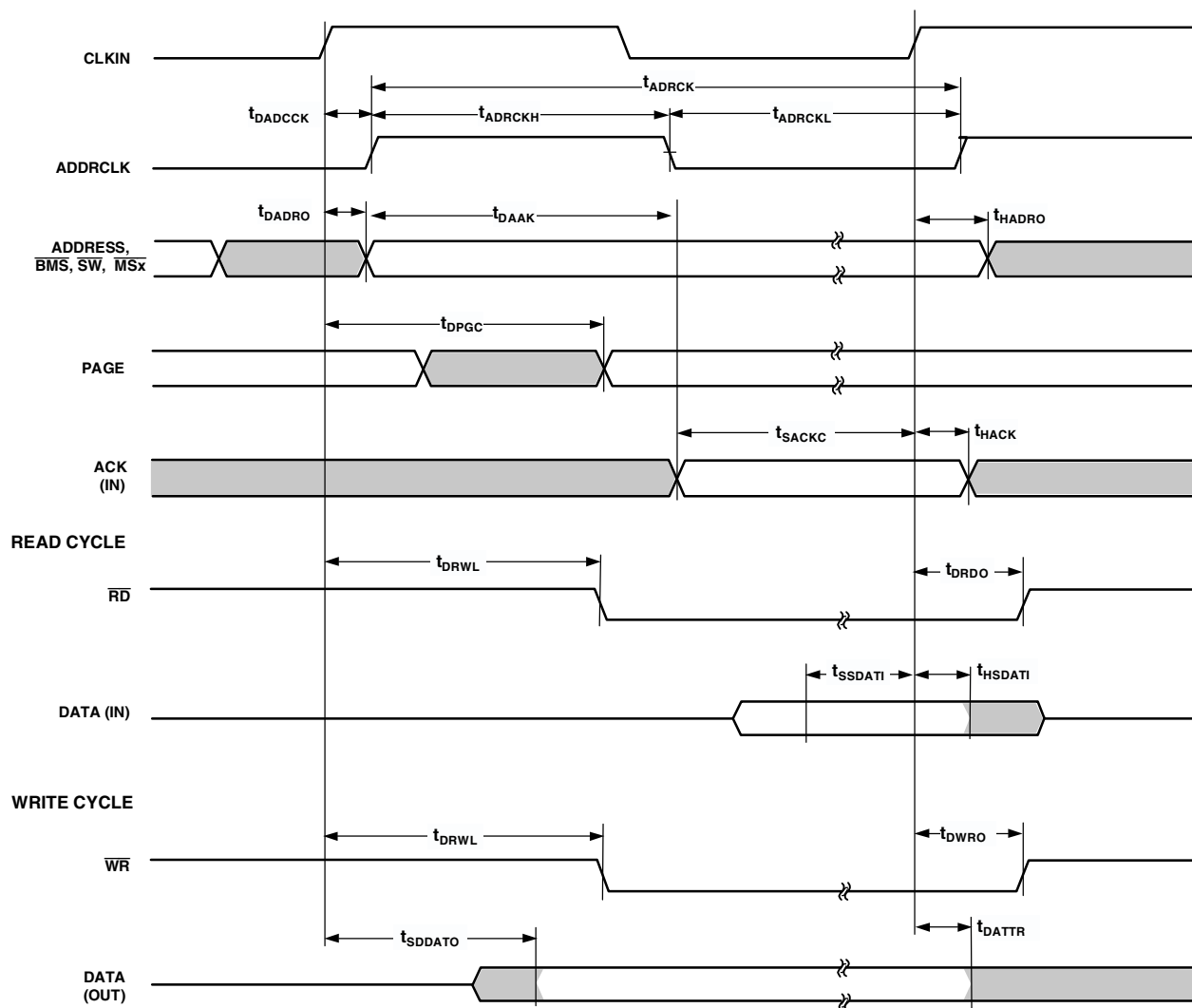


Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet the bus slave timing requirements.

Table 17. Synchronous Read/Write—Bus Slave

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|---|---------------|-------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{SADRI} | Address, \overline{SW} Setup Before CLKIN | 15 + DT/2 | | ns |
| t _{HADRI} | Address, \overline{SW} Hold After CLKIN | | 5 + DT/2 | ns |
| t _{SRWLI} | $\overline{RD}/\overline{WR}$ Low Setup Before CLKIN ¹ | 9.5 + 5DT/16 | | ns |
| t _{HRWLI} | $\overline{RD}/\overline{WR}$ Low Hold After CLKIN ² | −4 − 5DT/16 | 8 + 7DT/16 | ns |
| t _{RWHPI} | $\overline{RD}/\overline{WR}$ Pulse High | 3 | | ns |
| t _{SDATWH} | Data Setup Before \overline{WR} High | 5 | | ns |
| t _{HDATWH} | Data Hold After \overline{WR} High | 1 | | ns |
| Switching Characteristics | | | | |
| t _{SDDATO} | Data Delay After CLKIN ³ | | 18 + 5DT/16 | ns |
| t _{DATTR} | Data Disable After CLKIN ⁴ | 0 − DT/8 | 7 − DT/8 | ns |
| t _{DACKAD} | ACK Delay After Address, \overline{SW} ⁵ | | 9 | ns |
| t _{ACKTR} | ACK Disable After CLKIN ⁵ | −1 − DT/8 | 6 − DT/8 | ns |

¹ $t_{SRWLI}(\min) = 9.5 + 5DT/16$ when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, $t_{SRWLI}(\min) = 4 + DT/8$.

² For ADSP-21060C specification is $-3.5 - 5DT/16$ ns min, $8 + 7DT/16$ ns max; for ADSP-21060LC specification is $-3.75 - 5DT/16$ ns min, $8 + 7DT/16$ ns max.

³ For ADSP-21062/ADSP-21062L/ADSP-21060C specification is $19 + 5DT/16$ ns max; for ADSP-21060LC specification is $19.25 + 5DT/16$ ns max.

⁴ See [Example System Hold Time Calculation on Page 48](#) for calculation of hold times given capacitive and dc loads.

⁵ t_{DACKAD} is true only if the address and \overline{SW} inputs have setup times (before CLKIN) greater than $10 + DT/8$ and less than $19 + 3DT/4$. If the address and inputs have setup times greater than $19 + 3DT/4$, then ACK is valid $14 + DT/4$ (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR} .

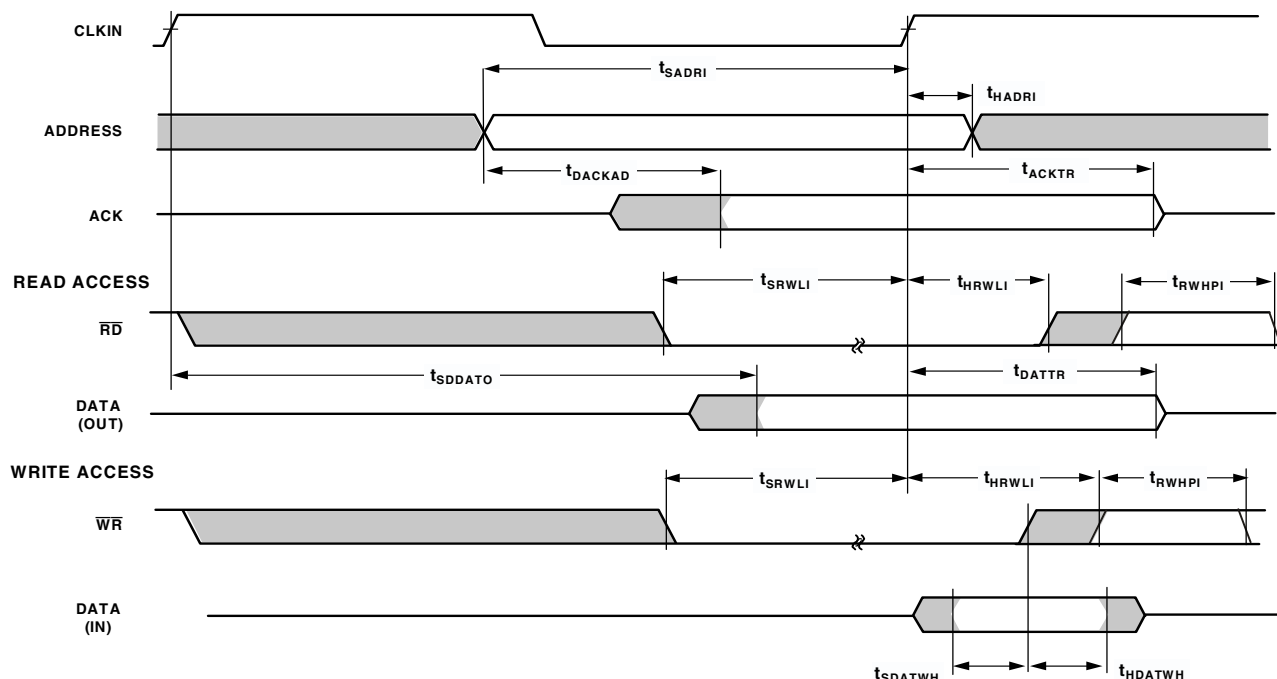


Figure 17. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{\text{BRx}}$) or a host processor, both synchronous and asynchronous ($\overline{\text{HBR}}$, $\overline{\text{HBG}}$).

Table 18. Multiprocessor Bus Request and Host Bus Request

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|--|---------------|------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| tHBGRCSV | HBG Low to RD/WR/CS Valid ¹ | | 20 + 5DT/4 | ns |
| tSHBRI | HBR Setup Before CLKIN ² | 20 + 3DT/4 | | ns |
| tHHBRI | HBR Hold After CLKIN ² | | 14 + 3DT/4 | ns |
| tSHBGI | HBG Setup Before CLKIN | 13 + DT/2 | | ns |
| tHHBGI | HBG Hold After CLKIN High | | 6 + DT/2 | ns |
| tSBRI | BRx, CPA Setup Before CLKIN ³ | 13 + DT/2 | | ns |
| tHBRI | BRx, CPA Hold After CLKIN High | | 6 + DT/2 | ns |
| tSRPBAI | RPBA Setup Before CLKIN | 21 + 3DT/4 | | ns |
| tHRPBAI | RPBA Hold After CLKIN | | 12 + 3DT/4 | ns |
| Switching Characteristics | | | | |
| tDHBGO | HBG Delay After CLKIN | | 7 – DT/8 | ns |
| tHHBGO | HBG Hold After CLKIN | –2 – DT/8 | | ns |
| tDBRO | BRx Delay After CLKIN | | 7 – DT/8 | ns |
| tHBRO | BRx Hold After CLKIN | –2 – DT/8 | | ns |
| tDCPAO | CPA Low Delay After CLKIN ⁴ | | 8 – DT/8 | ns |
| tTRCPA | CPA Disable After CLKIN | –2 – DT/8 | 4.5 – DT/8 | ns |
| tDRDYCS | REDY (O/D) or (A/D) Low from CS and HBR Low ^{5, 6} | | 8.5 | ns |
| tTRDYHG | REDY (O/D) Disable or REDY (A/D) High from HBG ^{6, 7} | 44 + 23DT/16 | | ns |
| tARDYTR | REDY (A/D) Disable from CS or HBR High ⁶ | | 10 | ns |

¹For first asynchronous access after $\overline{\text{HBR}}$ and $\overline{\text{CS}}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{\text{RD}}$ or $\overline{\text{WR}}$ goes low or by t_{HBGRCSV} after $\overline{\text{HBG}}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{\text{HBG}}$ is asserted. See the "Host Processor Control of the ADSP-2106x" section in the ADSP-2106x *SHARC User's Manual, Revision 2.1*.

²Only required for recognition in the current cycle.

³ $\overline{\text{CPA}}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

⁴For ADSP-21060LC, specification is 8.5 – DT/8 ns max.

⁵For ADSP-21060L, specification is 9.5 ns max, For ADSP-21060LC, specification is 11.0 ns max, For ADSP-21062L, specification is 8.75 ns max.

⁶(O/D) = open drain, (A/D) = active drive.

⁷For ADSP-21060C/ADSP-21060LC, specification is 40 + 23DT/16 ns min.

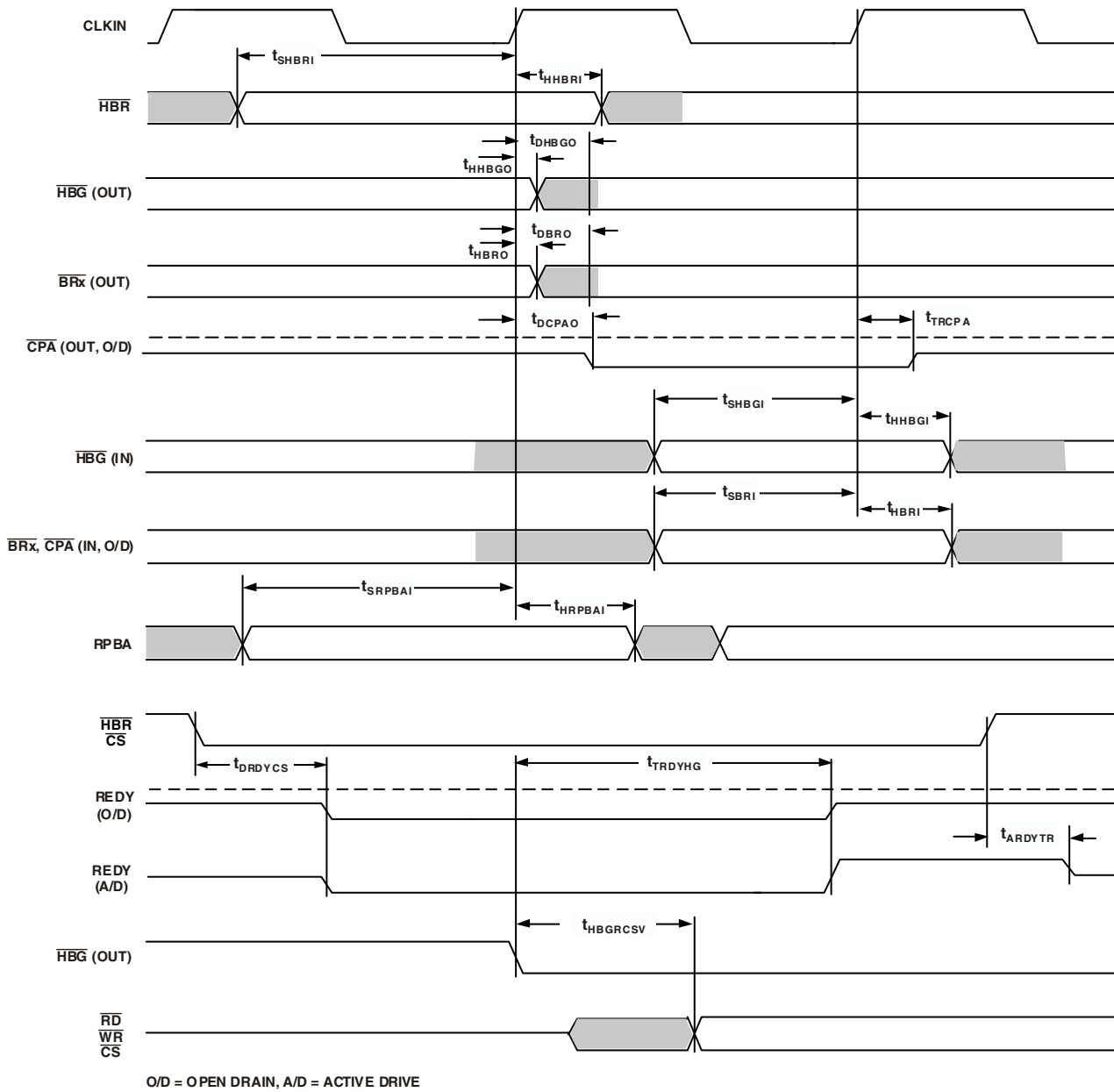


Figure 18. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-2106x

Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted \overline{CS} and \overline{HBR} (low). After \overline{HBG} is returned by the ADSP-2106x, the host can drive the \overline{RD} and \overline{WR} pins to access the ADSP-2106x's internal memory or IOP registers. \overline{HBR} and \overline{HBG} are assumed low for this timing. Not required if address is valid $t_{HBGRCSV}$

after goes low. For first access after asserted, ADDR31–0 must be a non-MMS value $1/2 t_{CLK}$ before or goes low or by $t_{HBGRCSV}$ after goes low. This is easily accomplished by driving an upper address signal high when is asserted. See the “Host Processor Control of the ADSP-2106x” section in the ADSP-2106x *SHARC User's Manual*, Revision 2.1.

Table 19. Read Cycle

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|--|---------------|-----|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{SADRDL} | Address Setup/ \overline{CS} Low Before \overline{RD} Low ¹ | 0 | | ns |
| t _{HADRDH} | Address Hold/ \overline{CS} Hold Low After \overline{RD} | 0 | | ns |
| t _{WRWH} | $\overline{RD}/\overline{WR}$ High Width | 6 | | ns |
| t _{DRDHRDY} | \overline{RD} High Delay After REDY (O/D) Disable | 0 | | ns |
| t _{DRDHRDY} | \overline{RD} High Delay After REDY (A/D) Disable | 0 | | ns |
| Switching Characteristics | | | | |
| t _{SDATRDY} | Data Valid Before REDY Disable from Low | 2 | | ns |
| t _{DRDYRDL} | REDY (O/D) or (A/D) Low Delay After \overline{RD} Low ² | | 10 | ns |
| t _{RDYPRD} | REDY (O/D) or (A/D) Low Pulse Width for Read | 45 + 21DT/16 | | ns |
| t _{HDARWH} | Data Disable After \overline{RD} High ³ | 2 | 8 | ns |

¹Not required if \overline{RD} and address are valid $t_{HBGRCSV}$ after \overline{HBG} goes low. For first access after \overline{HBR} asserted, ADDR31–0 must be a non-MMS value $1/2 t_{CLK}$ before \overline{RD} or \overline{WR} goes low or by $t_{HBGRCSV}$ after \overline{HBG} goes low. This is easily accomplished by driving an upper address signal high when \overline{HBG} is asserted. See the “Host Processor Control of the ADSP-2106x” section in the ADSP-2106x *SHARC User's Manual*, Revision 2.1.

²For ADSP-21060L, specification is 10.5 ns max; for ADSP-21060LC, specification is 12.5 ns max.

³For ADSP-21060L/ADSP-21060LC, specification is 2 ns min, 8.5 ns max.

Table 20. Write Cycle

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|---|---------------|------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{SCSWRL} | \overline{CS} Low Setup Before \overline{WR} Low | 0 | | ns |
| t _{HCSWRH} | \overline{CS} Low Hold After \overline{WR} High | 0 | | ns |
| t _{SADWRH} | Address Setup Before \overline{WR} High | 5 | | ns |
| t _{HADWRH} | Address Hold After \overline{WR} High | 2 | | ns |
| t _{WWRL} | \overline{WR} Low Width | 7 | | ns |
| t _{WRWH} | $\overline{RD}/\overline{WR}$ High Width | 6 | | ns |
| t _{DWRHRDY} | \overline{WR} High Delay After REDY (O/D) or (A/D) Disable | 0 | | ns |
| t _{SDATWH} | Data Setup Before \overline{WR} High | 5 | | ns |
| t _{HDATWH} | Data Hold After \overline{WR} High | 1 | | ns |
| Switching Characteristics | | | | |
| t _{DRDYWRL} | REDY (O/D) or (A/D) Low Delay After $\overline{WR}/\overline{CS}$ Low | | 10 | ns |
| t _{RDYPWR} | REDY (O/D) or (A/D) Low Pulse Width for Write | 15 + 7DT/16 | | ns |
| t _{SRDYCK} | REDY (O/D) or (A/D) Disable to CLKIN | 1 + 7DT/16 | 8 + 7DT/16 | ns |

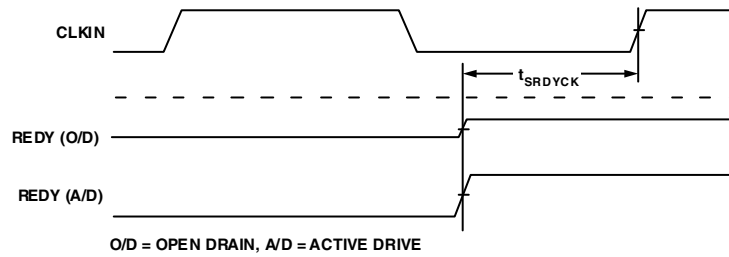
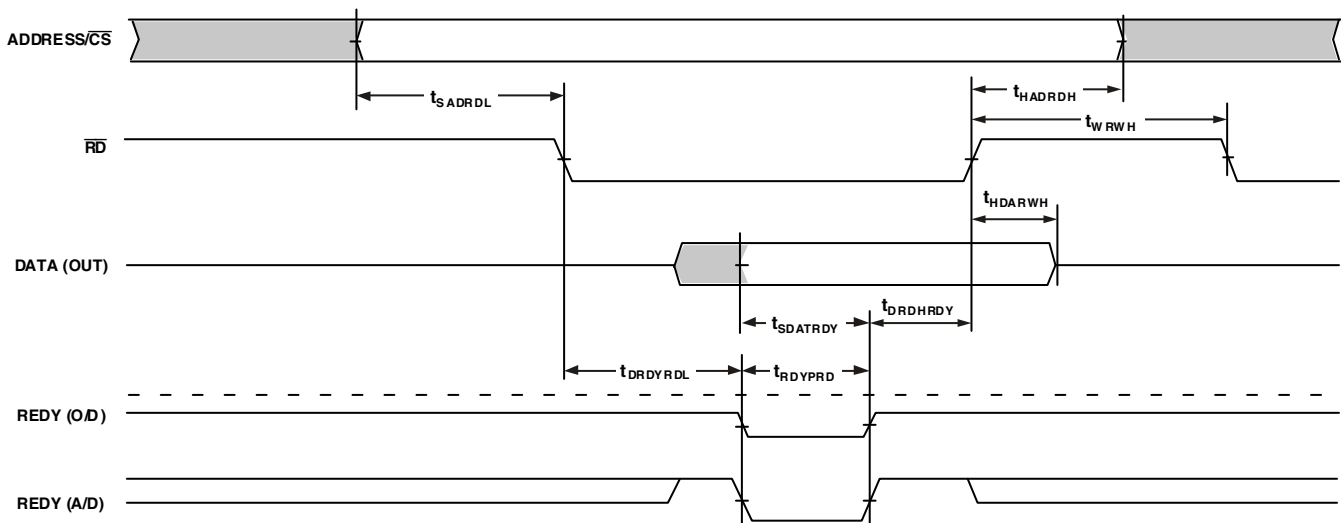


Figure 19. Synchronous REDY Timing

READ CYCLE



WRITE CYCLE

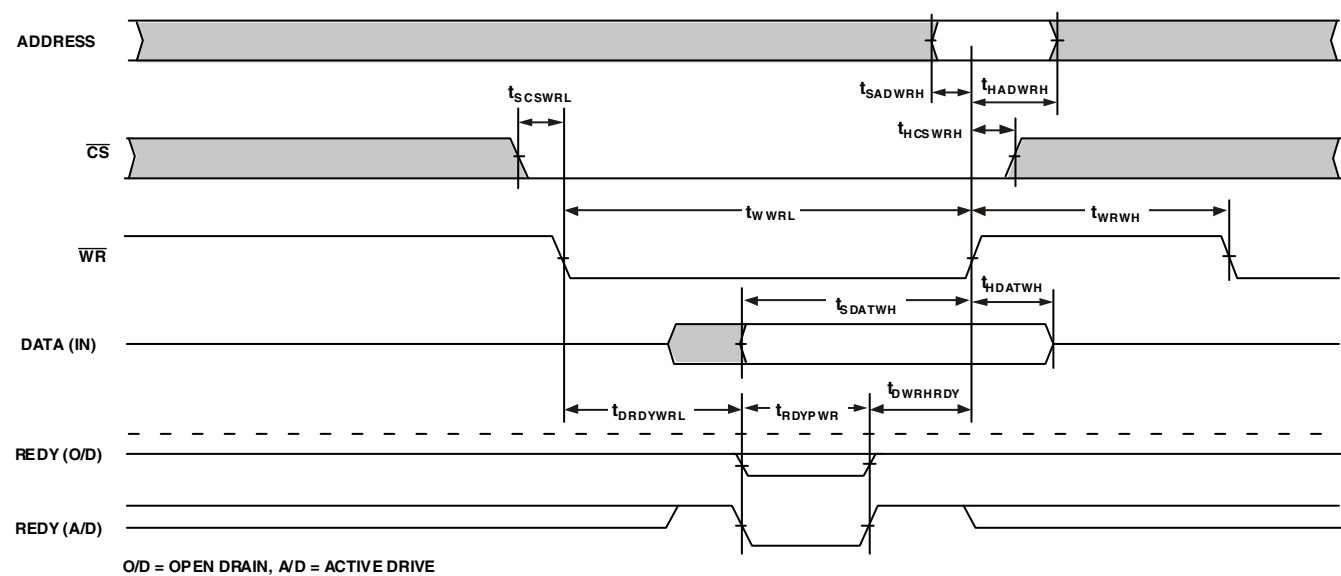


Figure 20. Asynchronous Read/Write—Host to ADSP-2106x

Three-State Timing—Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Table 21. Three-State Timing—Bus Master, Bus Slave

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|--|---------------|------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{STCK} | $\overline{\text{SBTS}}$ Setup Before CLKIN | 12 + DT/2 | | ns |
| t _{HTCK} | $\overline{\text{SBTS}}$ Hold Before CLKIN | | 6 + DT/2 | ns |
| Switching Characteristics | | | | |
| t _{MIENA} | Address/Select Enable After CLKIN ¹ | −1.5 − DT/8 | | ns |
| t _{MIENS} | Strobes Enable After CLKIN ² | −1.5 − DT/8 | | ns |
| t _{MIENHG} | $\overline{\text{HBG}}$ Enable After CLKIN | −1.5 − DT/8 | | ns |
| t _{MITRA} | Address/Select Disable After CLKIN ³ | | 0 − DT/4 | ns |
| t _{MITRS} | Strobes Disable After CLKIN ² | | 1.5 − DT/4 | ns |
| t _{MITRHG} | $\overline{\text{HBG}}$ Disable After CLKIN | | 2.0 − DT/4 | ns |
| t _{DATEN} | Data Enable After CLKIN ⁴ | 9 + 5DT/16 | | ns |
| t _{DATTR} | Data Disable After CLKIN ⁴ | 0 − DT/8 | 7 − DT/8 | ns |
| t _{ACKEN} | ACK Enable After CLKIN ⁴ | 7.5 + DT/4 | | ns |
| t _{ACKTR} | ACK Disable After CLKIN ⁴ | −1 − DT/8 | 6 − DT/8 | ns |
| t _{ADCEN} | ADRCLK Enable After CLKIN | −2 − DT/8 | | ns |
| t _{ADCTR} | ADRCLK Disable After CLKIN | | 8 − DT/4 | ns |
| t _{MTRHBG} | Memory Interface Disable Before $\overline{\text{HBG}}$ Low ⁵ | 0 + DT/8 | | ns |
| t _{MENHRG} | Memory Interface Enable After $\overline{\text{HBG}}$ High ⁵ | 19 + DT | | ns |

¹ For ADSP-21060L/ADSP-21060LC/ADSP-21062L, specification is $-1.25 - \text{DT}/8$ ns min, for ADSP-21062, specification is $-1 - \text{DT}/8$ ns min.

² Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PAGE}}$, $\overline{\text{DMAG}}$, $\overline{\text{BMS}}$, $\overline{\text{SW}}$.

³ For ADSP-21060LC, specification is $0.25 - \text{DT}/4$ ns max.

⁴ In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.

⁵ Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MSx}}$, $\overline{\text{SW}}$, $\overline{\text{PAGE}}$, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode).

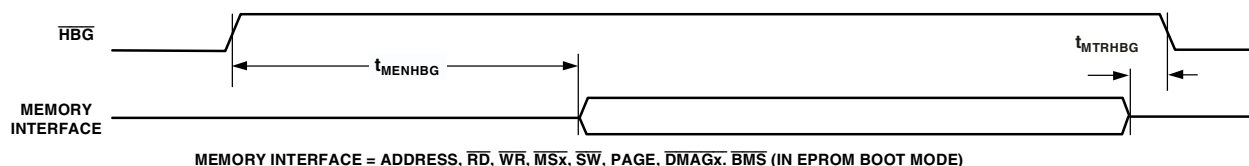


Figure 21. Three-State Timing (Bus Transition Cycle, $\overline{\text{SBTS}}$ Assertion)

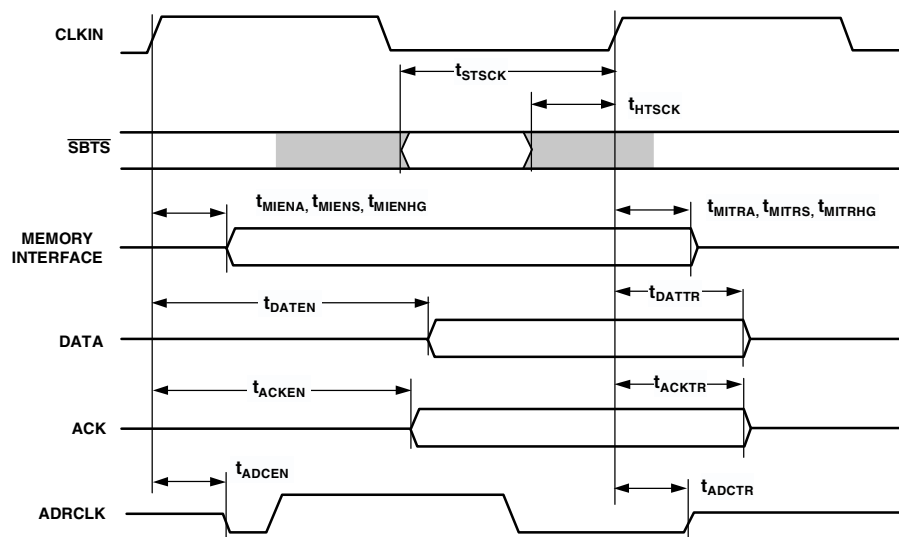


Figure 22. Three-State Timing (Bus Transition Cycle, \overline{SBTS} Assertion)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PAGE, $\overline{\text{MS3-0}}$, ACK,

and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3-0}}$, and ACK (not $\overline{\text{DMAGx}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3-0}}$, PAGE, DATA63–0, and ACK also apply.

Table 22. DMA Handshake

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|---|-----------------|------------|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| tSDRLC | $\overline{\text{DMARx}}$ Low Setup Before CLKIN ¹ | 5 | | ns |
| tSDRHC | $\overline{\text{DMARx}}$ High Setup Before CLKIN ¹ | 5 | | ns |
| tWDR | $\overline{\text{DMARx}}$ Width Low (Nonsynchronous) | 6 | | ns |
| tSDATDGL | Data Setup After $\overline{\text{DMAGx}}$ Low ² | | 10 + 5DT/8 | ns |
| tHDATIDG | Data Hold After $\overline{\text{DMAGx}}$ High | 2 | | ns |
| tDATDRH | Data Valid After $\overline{\text{DMARx}}$ High ² | | 16 + 7DT/8 | ns |
| tDMARLL | $\overline{\text{DMARx}}$ Low Edge to Low Edge | 23 + 7DT/8 | | ns |
| tDMARH | $\overline{\text{DMARx}}$ Width High ² | 6 | | ns |
| Switching Characteristics | | | | |
| tDDGL | $\overline{\text{DMAGx}}$ Low Delay After CLKIN | 9 + DT/4 | 15 + DT/4 | ns |
| tWDGH | $\overline{\text{DMAGx}}$ High Width | 6 + 3DT/8 | | ns |
| tWDGL | $\overline{\text{DMAGx}}$ Low Width | 12 + 5DT/8 | | ns |
| tHDGC | $\overline{\text{DMAGx}}$ High Delay After CLKIN | –2 – DT/8 | 6 – DT/8 | ns |
| tVDATDGH | Data Valid Before $\overline{\text{DMAGx}}$ High ³ | 8 + 9DT/16 | | ns |
| tDATRDGH | Data Disable After $\overline{\text{DMAGx}}$ High ⁴ | 0 | 7 | ns |
| tDGWRL | $\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low ⁵ | 0 | 2 | ns |
| tDGWRH | $\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High | 10 + 5DT/8 + W | | ns |
| tDGWRR | $\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High | 1 + DT/16 | 3 + DT/16 | ns |
| tDGRDL | $\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low | 0 | 2 | ns |
| tDRDGH | $\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High | 11 + 9DT/16 + W | | ns |
| tDGRDR | $\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High | 0 | 3 | ns |
| tDGWR | $\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low | 5 + 3DT/8 + HI | | ns |
| tADAGH | Address/Select Valid to $\overline{\text{DMAGx}}$ High | 17 + DT | | ns |
| tDDGHA | Address/Select Hold After $\overline{\text{DMAGx}}$ High ⁶ | –0.5 | | ns |

W = (number of wait states specified in WAIT register) $\times t_{\text{CK}}$.

HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

¹ Only required for recognition in the current cycle.

² t_{SDATDGL} is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.

³ t_{VDATDGH} is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{\text{VDATDGH}} = t_{\text{CK}} - 0.25t_{\text{CCLK}} - 8 + (n \times t_{\text{CK}})$ where n equals the number of extra cycles that the access is prolonged.

⁴ See [Example System Hold Time Calculation on Page 48](#) for calculation of hold times given capacitive and dc loads.

⁵ For ADSP-21062/ADSP-21062L specification is –2.5 ns min, 2 ns max.

⁶ For ADSP-21060L/ADSP-21062L specification is –1 ns min.

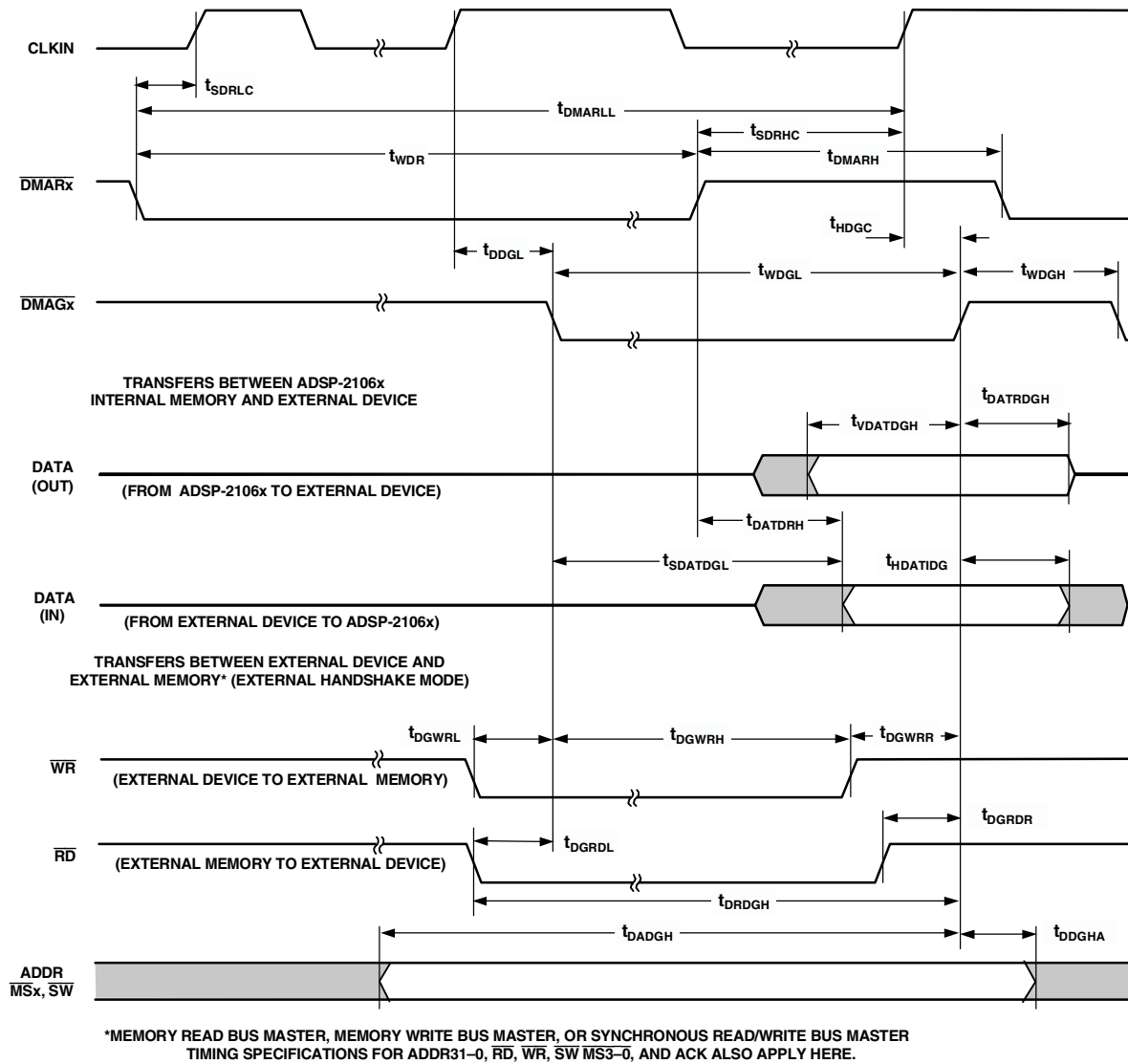


Figure 23. DMA Handshake

Link Ports — 1 × CLK Speed Operation**Table 23. Link Ports—Receive**

| Parameter | | 5 V | | 3.3 V | | Unit |
|---------------------------|--|-----------------|-------------|-----------------|-------------|------|
| | | Min | Max | Min | Max | |
| Timing Requirements | | | | | | |
| t _{SLDCL} | Data Setup Before LCLK Low ¹ | 3.5 | | 3 | | ns |
| t _{HLDC} | Data Hold After LCLK Low | 3 | | 3 | | ns |
| t _{LCLKIW} | LCLK Period (1× Operation) | t _{CK} | | t _{CK} | | ns |
| t _{LCLKRWL} | LCLK Width Low | 6 | | 6 | | ns |
| t _{LCLKRWH} | LCLK Width High | 5 | | 5 | | ns |
| Switching Characteristics | | | | | | |
| t _{DLAHC} | LACK High Delay After CLKIN High ^{2, 3} | 18 + DT/2 | 28.5 + DT/2 | 18 + DT/2 | 28.5 + DT/2 | ns |
| t _{DLALC} | LACK Low Delay After LCLK High | −3 | +13 | −3 | +13 | ns |
| t _{ENDLK} | LACK Enable From CLKIN | 5 + DT/2 | | 5 + DT/2 | | ns |
| t _{TDLK} | LACK Disable From CLKIN | | 20 + DT/2 | | 20 + DT/2 | ns |

¹For ADSP-21062, specification is 3 ns min.²LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.³For ADSP-21060C, specification is 18 + DT/2 ns min, 29 + DT/2 ns max.**Table 24. Link Ports—Transmit**

| Parameter | | 5 V | | 3.3 V | | Unit |
|---------------------------|--|----------------------------|-------------------------------|-----------------------------|---------------------------------|------|
| | | Min | Max | Min | Max | |
| Timing Requirements | | | | | | |
| t _{SLACH} | LACK Setup Before LCLK High ¹ | 18 | | 18 | | ns |
| t _{HLACH} | LACK Hold After LCLK High | −7 | | −7 | | ns |
| Switching Characteristics | | | | | | |
| t _{DLCLK} | Data Delay After CLKIN (1× Operation) ² | | 15.5 | | 15.5 | ns |
| t _{DLDC} | Data Delay After LCLK High ³ | | 3 | | 2.5 | ns |
| t _{HLDC} | Data Hold After LCLK High | −3 | | −3 | | ns |
| t _{LCLKTWL} | LCLK Width Low ⁴ | (t _{CK} /2) − 2 | (t _{CK} /2) + 2 | (t _{CK} /2) − 1 | (t _{CK} /2) + 1.25 | ns |
| t _{LCLKTWH} | LCLK Width High ⁵ | (t _{CK} /2) − 2 | (t _{CK} /2) + 2 | (t _{CK} /2) − 1.25 | (t _{CK} /2) + 1 | ns |
| t _{DLACLK} | LCLK Low Delay After LACK High ⁶ | (t _{CK} /2) + 8.5 | (3 × t _{CK} /2) + 17 | (t _{CK} /2) + 8 | (3 × t _{CK} /2) + 17.5 | ns |
| t _{ENDLK} | LACK Enable From CLKIN | 5 + DT/2 | | 5 + DT/2 | | ns |
| t _{TDLK} | LACK Disable From CLKIN | | 20 + DT/2 | | 20 + DT/2 | ns |

¹For ADSP-21060L/ADSP-21060LC, specification is 20 ns min.²For ADSP-21060L, specification is 16.5 ns max; for ADSP-21060LC, specification is 16.75 ns max.³For ADSP-21062, specification is 2.5 ns max.⁴For ADSP-21062, specification is (t_{CK}/2) − 1 ns min, (t_{CK}/2) + 1.25 ns max; for ADSP-21062L, specification is (t_{CK}/2) − 1 ns min, (t_{CK}/2) + 1.5 ns max; for ADSP-21060LC specification is (t_{CK}/2) − 1 ns min, (t_{CK}/2) + 2.25 ns max.⁵For ADSP-21062, specification is (t_{CK}/2) − 1.25 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21062L, specification is (t_{CK}/2) − 1.5 ns min, (t_{CK}/2) + 1 ns max; for ADSP-21060C specification is (t_{CK}/2) − 2.25 ns min, (t_{CK}/2) + 1 ns max.⁶For ADSP-21062, specification is (t_{CK}/2) + 8.75 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21062L, specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 17 ns max; for ADSP-21060LC specification is (t_{CK}/2) + 8 ns min, (3 × t_{CK}/2) + 18.5 ns max.

Table 25. Link Port Service Request Interrupts: 1× and 2× Speed Operations

| Parameter | 5 V | | 3.3 V | | Unit |
|---|-----|-----|-------|-----|------|
| | Min | Max | Min | Max | |
| Timing Requirements | | | | | |
| t _{SLCK} LACK/LCLK Setup Before CLKIN Low ¹ | 10 | | 10 | | ns |
| t _{HCLK} LACK/LCLK Hold After CLKIN Low ¹ | 2 | | 2 | | ns |

¹ Only required for interrupt recognition in the current cycle.

Link Ports—2× CLK Speed Operation

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK:

$$\text{Setup Skew} = t_{LCLKTWH} \text{ min} - t_{DLCH} - t_{SLDCL}$$

Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA:

$$\text{Hold Skew} = t_{LCLKTWL} \text{ min} - t_{HLDCH} - t_{HLDCL}$$

Calculations made directly from 2 speed specifications will result in unrealistically small skew times because they include multiple tester guardbands.

Note that link port transfers at 2× CLK speed at 40 MHz (t_{CK} = 25 ns) may fail. However, 2× CLK speed link port transfers at 33 MHz (t_{CK} = 30 ns) work as specified.

Table 26. Link Ports—Receive

| Parameter | | 5 V | | 3.3 V | | Unit |
|---------------------------|---|--------------------|-------------|--------------------|-------------|------|
| | | Min | Max | Min | Max | |
| Timing Requirements | | | | | | |
| t _{SLDCL} | Data Setup Before LCLK Low | 2.5 | | 2.25 | | ns |
| t _{HLDCL} | Data Hold After LCLK Low | 2.25 | | 2.25 | | ns |
| t _{LCLKIW} | LCLK Period (2× Operation) | t _{CK} /2 | | t _{CK} /2 | | ns |
| t _{LCLKRWL} | LCLK Width Low ¹ | 4.5 | | 5.25 | | ns |
| t _{LCLKRWH} | LCLK Width High ² | 4.25 | | 4 | | ns |
| Switching Characteristics | | | | | | |
| t _{DLAHC} | LACK High Delay After CLKIN High ³ | 18 + DT/2 | 28.5 + DT/2 | 18 + DT/2 | 29.5 + DT/2 | ns |
| t _{DLALC} | LACK Low Delay After LCLK High ⁴ | 6 | 16 | 6 | 16 | ns |

¹ For ADSP-21060L, specification is 5 ns min.

² For ADSP-21062, specification is 4 ns min, for ADSP-21060LC, specification is 4.5 ns min.

³ LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.

⁴ For ADSP-21060L, specification is 6 ns min, 18 ns max. For ADSP-21060C, specification is 6 ns min, 16.5 ns max. For ADSP-21060LC, specification is 6 ns min, 18.5 ns max.

Table 27. Link Ports—Transmit

| Parameter | | 5 V | | 3.3 V | | Unit |
|---------------------------|---|-----------------------------|---------------------------------|-----------------------------|---------------------------------|------|
| | | Min | Max | Min | Max | |
| Timing Requirements | | | | | | |
| t _{SLACH} | LACK Setup Before LCLK High | 19 | | 19 | | ns |
| t _{HLACH} | LACK Hold After LCLK High | −6.75 | | −6.5 | | ns |
| Switching Characteristics | | | | | | |
| t _{DLCLK} | Data Delay After CLKIN | | 8 | | 8 | ns |
| t _{DLDCH} | Data Delay After LCLK High ¹ | | 2.25 | | 2.25 | ns |
| t _{HLDCH} | Data Hold After LCLK High ² | −2.0 | | −2 | | ns |
| t _{LCLKTWL} | LCLK Width Low ³ | (t _{CK} /4) − 1 | (t _{CK} /4) + 1.25 | (t _{CK} /4) − 0.75 | (t _{CK} /4) + 1.5 | ns |
| t _{LCLKTWH} | LCLK Width High ⁴ | (t _{CK} /4) − 1.25 | (t _{CK} /4) + 1 | (t _{CK} /4) − 1.5 | (t _{CK} /4) + 1 | ns |
| t _{DLACLK} | LCLK Low Delay After LACK High | (t _{CK} /4) + 9 | (3 × t _{CK} /4) + 16.5 | (t _{CK} /4) + 9 | (3 × t _{CK} /4) + 16.5 | ns |

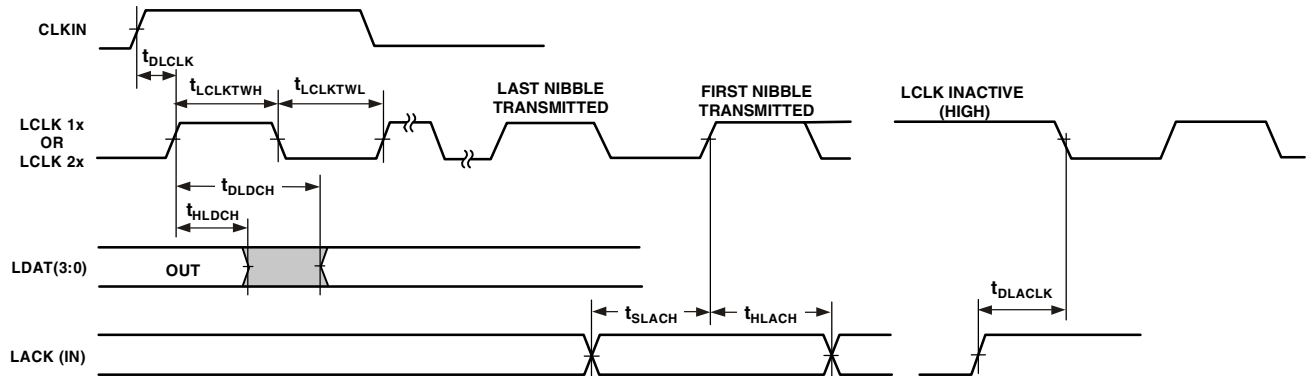
¹For ADSP-21060/ADSP-21060C, specification is 2.5 ns max.

²For ADSP-21062L, specification is –2.25 ns min.

³For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C/ADSP-21062L, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1.5$ ns max.

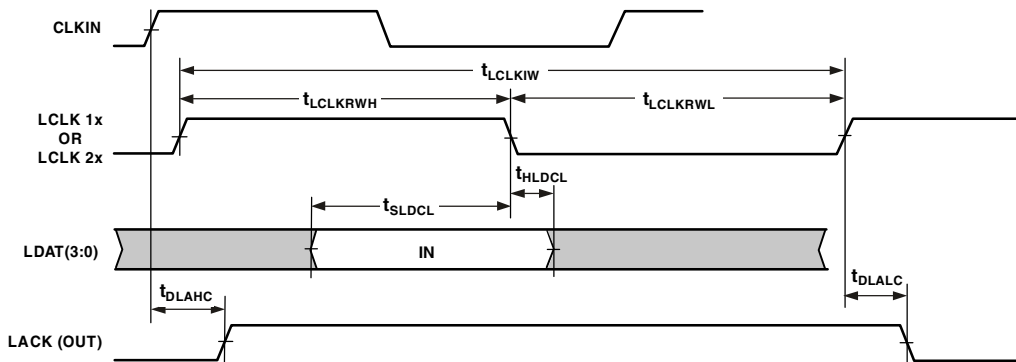
⁴For ADSP-21060, specification is $(t_{CK}/4) - 1$ ns min, $(t_{CK}/4) + 1$ ns max; for ADSP-21060C, specification is $(t_{CK}/4) - 1.5$ ns min, $(t_{CK}/4) + 1$ ns max.

TRANSMIT

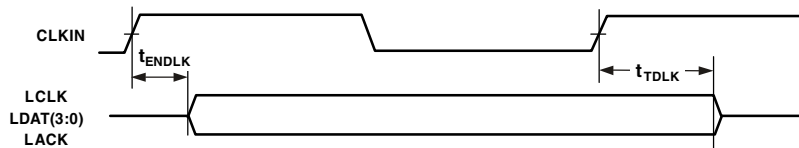


THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME

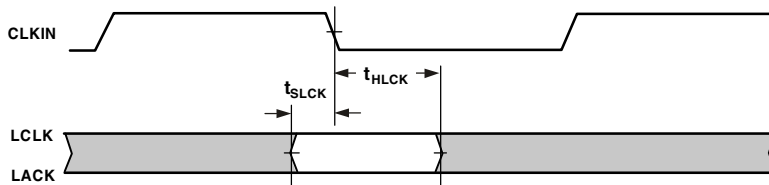


Figure 24. Link Ports—Receive

Serial Ports

For serial ports, see Table 28, Table 29, Table 30, Table 31, Table 32, Table 33, Table 35, Figure 26, and Figure 25. To determine whether communication is possible between two devices

at clock speed n, the following specifications must be confirmed:

1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 28. Serial Ports—External Clock

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------|--|-----------------|-----|------|
| | | Min | Max | |
| Timing Requirements | | | | |
| t _{SFSE} | TFS/RFS Setup Before TCLK/RCLK ¹ | 3.5 | | ns |
| t _{HFSE} | TFS/RFS Hold After TCLK/RCLK ^{1, 2} | 4 | | ns |
| t _{SDRE} | Receive Data Setup Before RCLK ¹ | 1.5 | | ns |
| t _{HDRE} | Receive Data Hold After RCLK ¹ | 6.5 | | ns |
| t _{SCLKW} | TCLK/RCLK Width ³ | 9 | | ns |
| t _{SCLK} | TCLK/RCLK Period | t _{CK} | | ns |

¹Referenced to sample edge.

²RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

³For ADSP-21060/ADSP-21060C/ADSP-21060LC, specification is 9.5 ns min.

Table 29. Serial Ports—Internal Clock

| Parameter | 5 V and 3.3 V | | Unit |
|---------------------|---|-----|------|
| | Min | Max | |
| Timing Requirements | | | |
| t _{SFSI} | TFS Setup Before TCLK ¹ ; RFS Setup Before RCLK ¹ | | ns |
| t _{HFSI} | TFS/RFS Hold After TCLK/RCLK ^{1, 2} | | ns |
| t _{SDRI} | Receive Data Setup Before RCLK ¹ | | ns |
| t _{HDRI} | Receive Data Hold After RCLK ¹ | | ns |

¹Referenced to sample edge.

²RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 30. Serial Ports—External or Internal Clock

| Parameter | 5 V and 3.3 V | | Unit |
|---------------------------|--|-----|------|
| | Min | Max | |
| Switching Characteristics | | | |
| t _{DFSE} | RFS Delay After RCLK (Internally Generated RFS) ¹ | 13 | ns |
| t _{HOFSE} | RFS Hold After RCLK (Internally Generated RFS) ¹ | 3 | ns |

¹Referenced to drive edge.

Table 31. Serial Ports—External Clock

| Parameter | | 5 V and 3.3 V | | Unit |
|---------------------------|--|---------------|-----|------|
| | | Min | Max | |
| Switching Characteristics | | | | |
| t _{DFSE} | TFS Delay After TCLK (Internally Generated TFS) ¹ | | 13 | ns |
| t _{HOFSE} | TFS Hold After TCLK (Internally Generated TFS) ¹ | 3 | | ns |
| t _{DDTE} | Transmit Data Delay After TCLK ¹ | | 16 | ns |
| t _{HDTE} | Transmit Data Hold After TCLK ¹ | 5 | | ns |

¹Referenced to drive edge.

ADSP-21062/ADSP-21062L

Table 32. Serial Ports—Internal Clock

| Parameter | | Min | Max | Unit |
|----------------------------------|--|----------------------------|----------------------------|------|
| <i>Switching Characteristics</i> | | | | |
| t _{DFSI} | TFS Delay After TCLK (Internally Generated TFS) ¹ | | 4.5 | ns |
| t _{HOFSI} | TFS Hold After TCLK (Internally Generated TFS) ¹ | –1.5 | | ns |
| t _{DDTI} | Transmit Data Delay After TCLK ¹ | | 7.5 | ns |
| t _{HDTI} | Transmit Data Hold After TCLK ¹ | 0 | | ns |
| t _{SCLKIW} | TCLK/RCLK Width ² | 0.5t _{SCLK} – 2.5 | 0.5t _{SCLK} + 2.5 | ns |

¹Referenced to drive edge.

²For ADSP-21060L/ADSP-21060C, specification is 0.5t_{SCLK} – 2 ns min, 0.5t_{SCLK} + 2 ns max.

Table 33. Serial Ports—Enable and Three-State

| Parameter | | Min | Max | Unit |
|----------------------------------|---|-----|-------------|------|
| <i>Switching Characteristics</i> | | | | |
| t _{DDTEN} | Data Enable from External TCLK ^{1, 2} | 4 | | ns |
| t _{DDTTE} | Data Disable from External TCLK ^{1, 3} | | 10.5 | ns |
| t _{DDTIN} | Data Enable from Internal TCLK ¹ | 0 | | ns |
| t _{DDTTI} | Data Disable from Internal TCLK ^{1, 4} | | 3 | ns |
| t _{DCLK} | TCLK/RCLK Delay from CLKIN | | 22 + 3 DT/8 | ns |
| t _{DPTR} | SPORT Disable After CLKIN | | 17 | ns |

¹Referenced to drive edge.

²For ADSP-21060L/ADSP-21060C, specification is 3.5 ns min; for ADSP-21062 specification is 4.5 ns min.

³For ADSP-21062L, specification is 16 ns max.

⁴For ADSP-21062L, specification is 7.5 ns max.

Table 34. Serial Ports—GATED SCLK with External TFS (Mesh Multiprocessing)¹

| Parameter | | Min | Max | Unit |
|----------------------------------|------------------------|-----|--------------------|------|
| <i>Switching Characteristics</i> | | | | |
| t _{TFSC} | TFS Setup Before CLKIN | 4 | | ns |
| t _{HTFSC} | TFS Hold After CLKIN | | t _{CK} /2 | ns |

¹Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems.

Table 35. Serial Ports—External Late Frame Sync

| Parameter | | Min | Max | Unit |
|----------------------------------|---|-----|-----|------|
| <i>Switching Characteristics</i> | | | | |
| t _{DDTLFSE} | Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0 ^{1, 2} | | 12 | ns |
| t _{DDTENFS} | Data Enable from Late FS or MCE = 1, MFD = 0 ^{1, 3} | 3.5 | | ns |

¹MCE = 1, TFS enable and TFS valid follow t_{DDTLFSE} and t_{DDTENFS}.

²For ADSP-21062/ADSP-21062L, specification is 12.75 ns max; for ADSP-21060L/ADSP-21060LC, specification is 12.8 ns max.

³For ADSP-21060/ADSP-21060C, specification is 3 ns min.

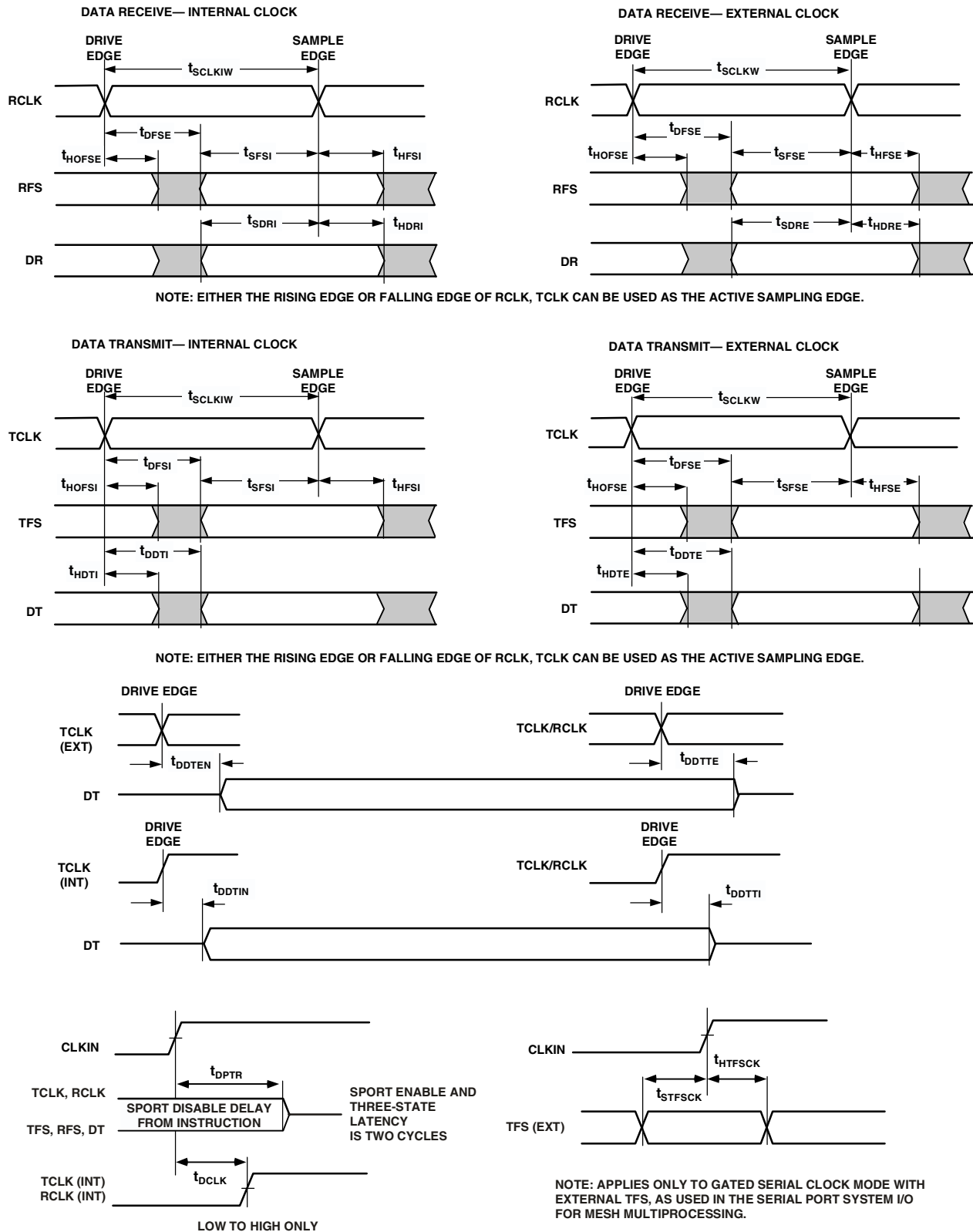


Figure 25. Serial Ports

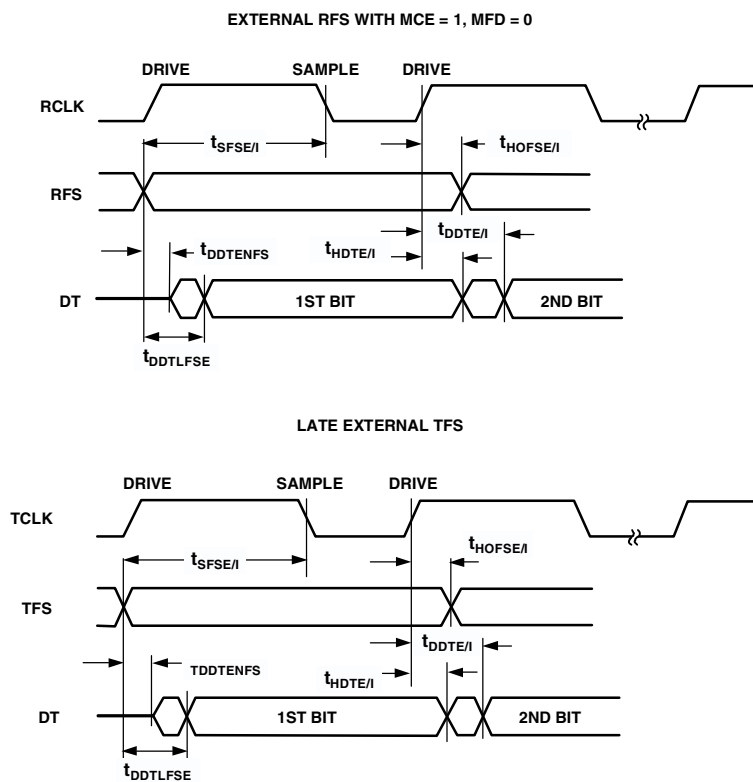


Figure 26. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see [Table 36](#) and [Figure 27](#).

Table 36. JTAG Test Access Port and Emulation

| Parameter | Min | Max | Unit |
|---|-----------|------|------|
| <i>Timing Requirements</i> | | | |
| t_{TCK} TCK Period | t_{CK} | | ns |
| t_{STAP} TDI, TMS Setup Before TCK High | 5 | | ns |
| t_{HTAP} TDI, TMS Hold After TCK High | 6 | | ns |
| t_{SSYS} System Inputs Setup Before TCK Low ¹ | 7 | | ns |
| t_{HSYS} System Inputs Hold After TCK Low ^{1, 2} | 18 | | ns |
| t_{TRSTW} \overline{TRST} Pulse Width | $4t_{CK}$ | | ns |
| <i>Switching Characteristics</i> | | | |
| t_{DIDO} TDO Delay from TCK Low | | 13 | ns |
| t_{DSYS} System Outputs Delay After TCK Low ³ | | 18.5 | ns |

¹System Inputs = DATA63–0, ADDR31–0, \overline{RD} , \overline{WR} , ACK, \overline{SBTS} , HBR, HBG, CS, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6-1}$, ID2–0, RPBA, $\overline{IRQ2-0}$, FLAG3–0, \overline{PA} , BRST, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, EBOOT, LBOOT, BMS, CLKIN, RESET.

²For ADSP-21060L/ADSP-21060LC/ADSP-21062L, specification is 18.5 ns min.

³System Outputs = DATA63–0, ADDR31–0, MS3–0, \overline{RD} , \overline{WR} , ACK, PAGE, CLKOUT, HBG, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6-1}$, \overline{PA} , BRST, \overline{CIF} , FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, LxDAT7–0, LxCLK, LxACK, BMS.

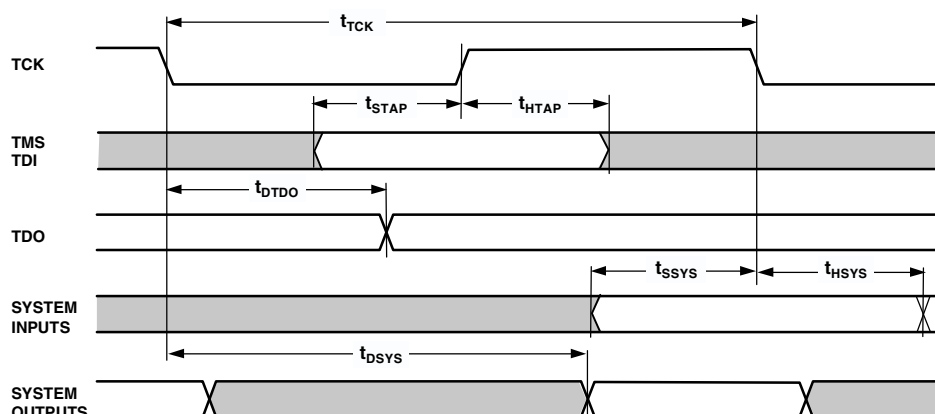


Figure 27. JTAG Test Access Port and Emulation

TEST CONDITIONS

For the ac signal specifications (timing parameters), see [Timing Specifications on Page 21](#). These specifications include output disable time, output enable time, and capacitive loading. The timing specifications for the DSP apply for the voltage reference levels in [Figure 28](#).



Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L , and the load current, I_L . This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in [Figure 29](#). The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L , and with ΔV equal to 0.5 V.

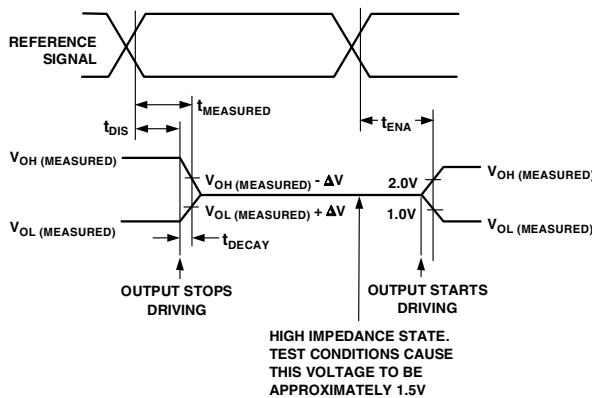


Figure 29. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the

output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram ([Figure 29](#)). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see [Figure 30](#)). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. [Figure 32](#), [Figure 33](#), [Figure 37](#), and [Figure 38](#) show how output rise time varies with capacitance. [Figure 34](#) and [Figure 36](#) show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of [Figure 32](#), [Figure 33](#), [Figure 37](#), and [Figure 38](#) may not be linear outside the ranges shown.

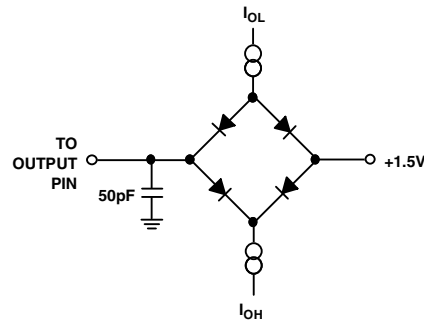


Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Output Drive Characteristics

[Figure 31](#) shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

Output Characteristics (5 V)

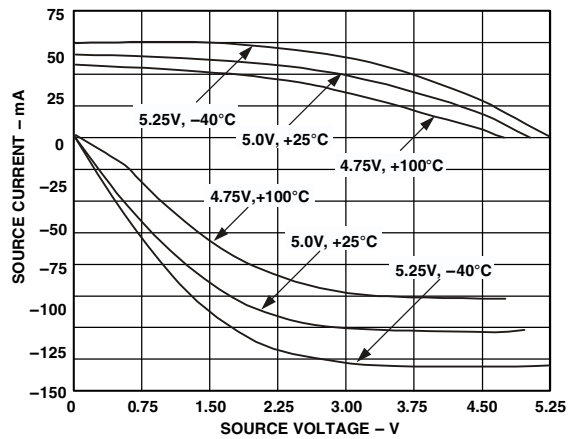


Figure 31. ADSP-21062 Typical Output Drive Currents ($V_{DD} = 5\text{ V}$)

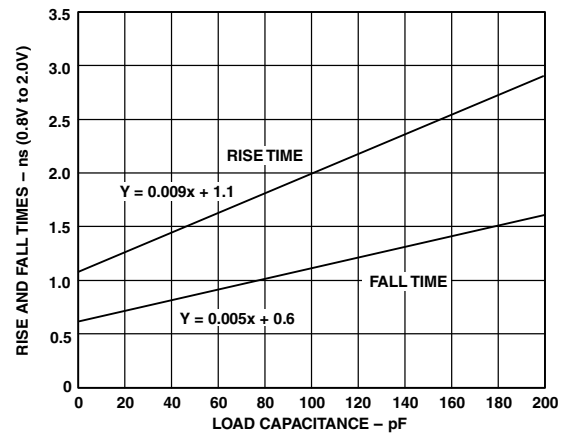


Figure 33. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance ($V_{DD} = 5\text{ V}$)

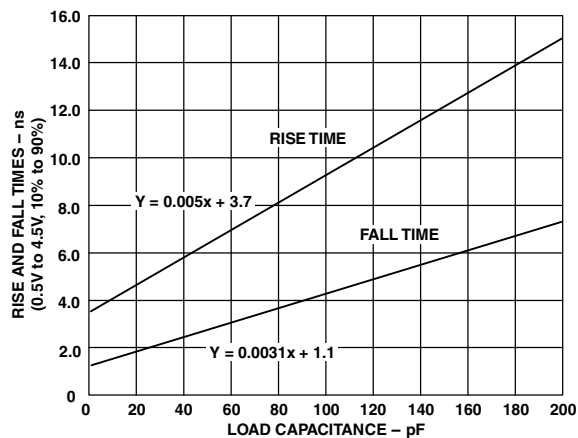


Figure 32. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance ($V_{DD} = 5\text{ V}$)

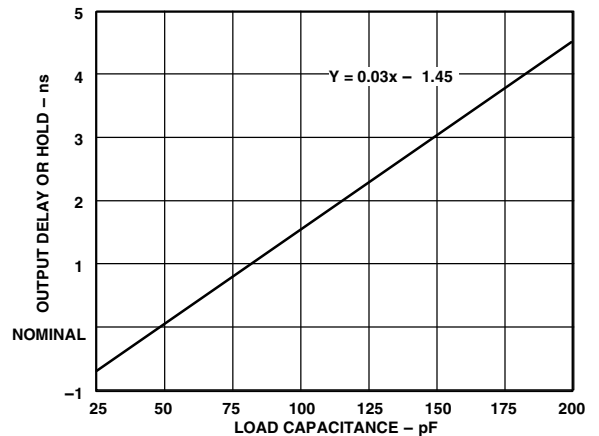


Figure 34. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) ($V_{DD} = 5\text{ V}$)

Output Characteristics (3.3 V)

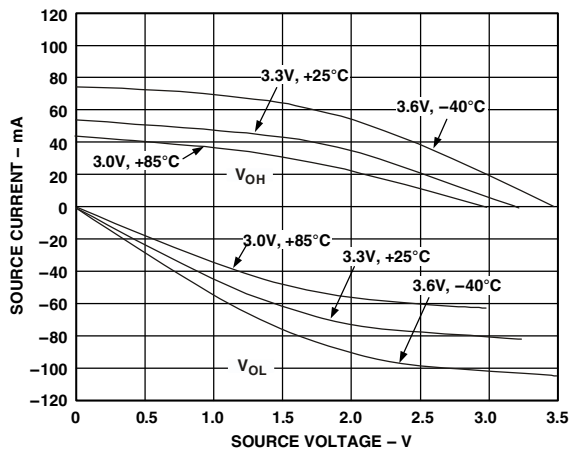


Figure 35. ADSP-21062 Typical Output Drive Currents ($V_{DD} = 3.3\text{ V}$)

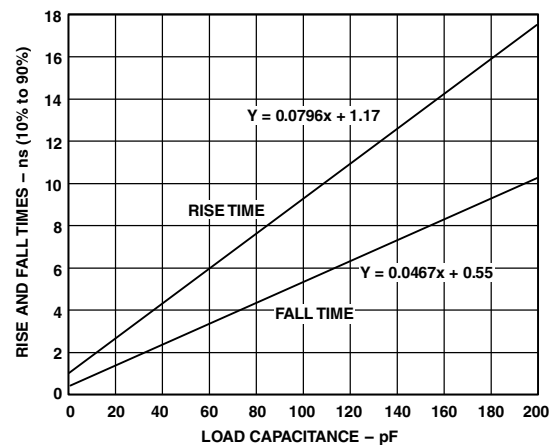


Figure 37. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance ($V_{DD} = 3.3\text{ V}$)

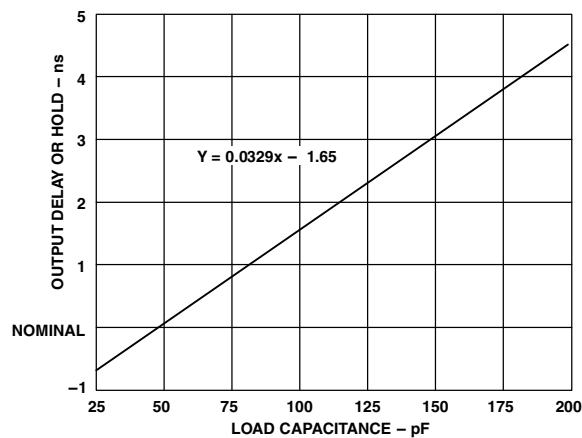


Figure 36. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) ($V_{DD} = 3.3\text{ V}$)

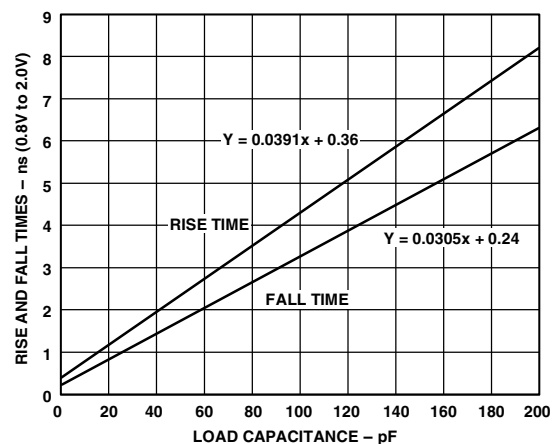


Figure 38. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance ($V_{DD} = 3.3\text{ V}$)

ENVIRONMENTAL CONDITIONS

The ADSP-2106x processors are rated for performance under T_{CASE} environmental conditions specified in the [Operating Conditions \(5 V\) on Page 15](#) and [Operating Conditions \(3.3 V\) on Page 18](#).

Thermal Characteristics for MQFP_PQ4 and PBGA Packages

The ADSP-21060/ADSP-21060L and ADSP-21062/ADSP-21062L are available in 240-lead thermally enhanced MQFP_PQ4 and 225-ball plastic ball grid array packages. The top surface of the thermally enhanced MQFP_PQ4 contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

Both packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an air flow source may be used. A heatsink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} = Values from [Table 37](#) and [Table 38](#) below.

Table 37. Thermal Characteristics for Thermally Enhanced 240-Lead MQFP_PQ4¹

| Parameter | Airflow (LFM ²) | Typical | Unit |
|---------------|-----------------------------|---------|------|
| θ_{CA} | 0 | 10 | °C/W |
| θ_{CA} | 100 | 9 | °C/W |
| θ_{CA} | 200 | 8 | °C/W |
| θ_{CA} | 400 | 7 | °C/W |
| θ_{CA} | 600 | 6 | °C/W |

¹This represents thermal resistance at total power of 5 W. With airflow, no variance is seen in θ_{CA} at 5 W.

θ_{CA} at 0 LFM varies with power:

at 2 W, $\theta_{CA} = 14^{\circ}\text{C/W}$

at 3 W, $\theta_{CA} = 11^{\circ}\text{C/W}$

²LFM = Linear feet per minute of airflow.

Table 38. Thermal Characteristics for BGA

| Parameter | Airflow (LFM ¹) | Typical | Unit |
|---------------|-----------------------------|---------|------|
| θ_{CA} | 0 | 20.70 | °C/W |
| θ_{CA} | 200 | 15.30 | °C/W |
| θ_{CA} | 400 | 12.90 | °C/W |

¹LFM = Linear feet per minute of airflow.

Thermal Characteristics for CQFP Package

The ADSP-21060C/ADSP-21060LC are available in 240-lead thermally enhanced ceramic QFP (CQFP). There are two package versions, one with a copper/tungsten heat slug on top of the package (CZ) for air cooling, and one with the heat slug on the bottom (CW) for cooling through the board. The ADSP-2106x is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. A heatsink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} = Value from [Table 39](#) below.

Table 39. Thermal Characteristics for Thermally Enhanced 240-Lead CQFP¹

| Parameter | Airflow (LFM ²) | Typical | Unit |
|----------------------------|-----------------------------|---------|------|
| ADSP-21060CW/ADSP-21060LCW | | | |
| θ_{CA} | 0 | 19.5 | °C/W |
| θ_{CA} | 100 | 16 | °C/W |
| θ_{CA} | 200 | 14 | °C/W |
| θ_{CA} | 400 | 12 | °C/W |
| θ_{CA} | 600 | 10 | °C/W |
| ADSP-21060CZ/ADSP-21060LCZ | | | |
| θ_{CA} | 0 | 20 | °C/W |
| θ_{CA} | 100 | 16 | °C/W |
| θ_{CA} | 200 | 14 | °C/W |
| θ_{CA} | 400 | 11.5 | °C/W |
| θ_{CA} | 600 | 9.5 | °C/W |

¹This represents thermal resistance at total power of 5 W. With airflow, no variance is seen in θ_{CA} at 5 W.

θ_{CA} at 0 LFM varies with power.

ADSP-21060CW/ADSP-21060LCW:

at 2 W, $\theta_{CA} = 23^{\circ}\text{C/W}$

at 3 W, $\theta_{CA} = 21.5^{\circ}\text{C/W}$

ADSP-21060CZ/ADSP-21060LCZ:

at 2 W, $\theta_{CA} = 24^{\circ}\text{C/W}$

at 3 W, $\theta_{CA} = 21.5^{\circ}\text{C/W}$

$\theta_{JC} = 0.24^{\circ}\text{C/W}$ for all CQFP models.

²LFM = Linear feet per minute of airflow.

225-BALL PBGA BALL CONFIGURATION

Table 40. ADSP-2106x 225-Ball Metric PBGA Ball Assignments (B-225-2)

| Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number | Ball Name | Ball Number |
|-----------|-------------|-----------------|-------------|-----------------|-------------|-----------------|-------------|-----------|-------------|
| BMS | A01 | ADDR25 | D01 | ADDR14 | G01 | ADDR6 | K01 | EMU | N01 |
| ADDR30 | A02 | ADDR26 | D02 | ADDR15 | G02 | ADDR5 | K02 | TDO | N02 |
| DMAR2 | A03 | MS2 | D03 | ADDR16 | G03 | ADDR3 | K03 | IRQ0 | N03 |
| DT1 | A04 | ADDR29 | D04 | ADDR19 | G04 | ADDR0 | K04 | IRQ1 | N04 |
| RCLK1 | A05 | DMAR1 | D05 | GND | G05 | ICSA | K05 | ID2 | N05 |
| TCLK0 | A06 | TFS1 | D06 | V _{DD} | G06 | GND | K06 | L5DAT1 | N06 |
| RCLK0 | A07 | CPA | D07 | V _{DD} | G07 | V _{DD} | K07 | L4CLK | N07 |
| ADRCLK | A08 | HBG | D08 | V _{DD} | G08 | V _{DD} | K08 | L3CLK | N08 |
| CS | A09 | DMAG2 | D09 | V _{DD} | G09 | V _{DD} | K09 | L3DAT3 | N09 |
| CLKIN | A10 | BR5 | D10 | V _{DD} | G10 | GND | K10 | L2DAT0 | N10 |
| PAGE | A11 | BR1 | D11 | GND | G11 | GND | K11 | L1ACK | N11 |
| BR3 | A12 | DATA40 | D12 | DATA22 | G12 | DATA8 | K12 | L1DAT3 | N12 |
| DATA47 | A13 | DATA37 | D13 | DATA25 | G13 | DATA11 | K13 | L0DAT3 | N13 |
| DATA44 | A14 | DATA35 | D14 | DATA24 | G14 | DATA13 | K14 | DATA1 | N14 |
| DATA42 | A15 | DATA34 | D15 | DATA23 | G15 | DATA14 | K15 | DATA3 | N15 |
| MS0 | B01 | ADDR21 | E01 | ADDR12 | H01 | ADDR2 | L01 | TRST | P01 |
| SW | B02 | ADDR22 | E02 | ADDR11 | H02 | ADDR1 | L02 | TMS | P02 |
| ADDR31 | B03 | ADDR24 | E03 | ADDR13 | H03 | FLAG0 | L03 | EBOOT | P03 |
| HBR | B04 | ADDR27 | E04 | ADDR10 | H04 | FLAG3 | L04 | ID0 | P04 |
| DR1 | B05 | GND | E05 | GND | H05 | RPBA | L05 | L5CLK | P05 |
| DT0 | B06 | GND | E06 | V _{DD} | H06 | GND | L06 | L5DAT3 | P06 |
| DR0 | B07 | GND | E07 | V _{DD} | H07 | GND | L07 | L4DAT0 | P07 |
| REDY | B08 | GND | E08 | V _{DD} | H08 | GND | L08 | L4DAT3 | P08 |
| RD | B09 | GND | E09 | V _{DD} | H09 | GND | L09 | L3DAT2 | P09 |
| ACK | B10 | GND | E10 | V _{DD} | H10 | GND | L10 | L2CLK | P10 |
| BR6 | B11 | NC | E11 | GND | H11 | NC | L11 | L2DAT2 | P11 |
| BR2 | B12 | DATA33 | E12 | DATA18 | H12 | DATA4 | L12 | L1DAT0 | P12 |
| DATA45 | B13 | DATA30 | E13 | DATA19 | H13 | DATA7 | L13 | L0ACK | P13 |
| DATA43 | B14 | DATA32 | E14 | DATA21 | H14 | DATA9 | L14 | L0DAT1 | P14 |
| DATA39 | B15 | DATA31 | E15 | DATA20 | H15 | DATA10 | L15 | DATA0 | P15 |
| MS3 | C01 | ADDR17 | F01 | ADDR9 | J01 | FLAG1 | M01 | TCK | R01 |
| MS1 | C02 | ADDR18 | F02 | ADDR8 | J02 | FLAG2 | M02 | IRQ2 | R02 |
| ADDR28 | C03 | ADDR20 | F03 | ADDR7 | J03 | TIMEXP | M03 | RESET | R03 |
| SBTS | C04 | ADDR23 | F04 | ADDR4 | J04 | TDI | M04 | ID1 | R04 |
| TCLK1 | C05 | GND | F05 | GND | J05 | LBOOT | M05 | L5DAT0 | R05 |
| RFS1 | C06 | GND | F06 | V _{DD} | J06 | L5ACK | M06 | L4ACK | R06 |
| TFS0 | C07 | V _{DD} | F07 | V _{DD} | J07 | L5DAT2 | M07 | L4DAT1 | R07 |
| RFS0 | C08 | V _{DD} | F08 | V _{DD} | J08 | L4DAT2 | M08 | L3ACK | R08 |
| WR | C09 | V _{DD} | F09 | V _{DD} | J09 | L3DAT0 | M09 | L3DAT1 | R09 |
| DMAG1 | C10 | GND | F10 | V _{DD} | J10 | L2DAT3 | M10 | L2ACK | R10 |
| BR4 | C11 | GND | F11 | GND | J11 | L1DAT1 | M11 | L2DAT1 | R11 |
| DATA46 | C12 | DATA29 | F12 | DATA12 | J12 | L0DAT0 | M12 | L1CLK | R12 |
| DATA41 | C13 | DATA26 | F13 | DATA15 | J13 | DATA2 | M13 | L1DAT2 | R13 |
| DATA38 | C14 | DATA28 | F14 | DATA16 | J14 | DATA5 | M14 | L0CLK | R14 |
| DATA36 | C15 | DATA27 | F15 | DATA17 | J15 | DATA6 | M15 | L0DAT2 | R15 |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|--------|--------|--------|-------------------------|-------------------------|---------------------------|---------------------------|-------------------------|-------------------------|----------|---------------------------|--------------------------|---------------------------|--------------------------|--------------------------|---|
| DATA42 | DATA44 | DATA47 | $\overline{\text{BR}}3$ | PAGE | CLKIN | $\overline{\text{CS}}$ | ADRCLK | RCLK0 | TCLK0 | RCLK1 | DT1 | $\overline{\text{DMAR}}2$ | ADDR30 | $\overline{\text{BMS}}$ | A |
| DATA39 | DATA43 | DATA45 | $\overline{\text{BR}}2$ | $\overline{\text{BR}}6$ | ACK | $\overline{\text{RD}}$ | REDY | DR0 | DT0 | DR1 | $\overline{\text{HBR}}$ | ADDR31 | SW | $\overline{\text{MS}}0$ | B |
| DATA36 | DATA38 | DATA41 | DATA46 | $\overline{\text{BR}}4$ | $\overline{\text{DMAGT}}$ | WR | RFS0 | TFS0 | RFS1 | TCLK1 | $\overline{\text{SBTS}}$ | ADDR28 | $\overline{\text{MS}}1$ | $\overline{\text{MS}}3$ | C |
| DATA34 | DATA35 | DATA37 | DATA40 | $\overline{\text{BR}}1$ | $\overline{\text{BR}}5$ | $\overline{\text{DMAG2}}$ | $\overline{\text{HBG}}$ | $\overline{\text{CPA}}$ | TFS1 | $\overline{\text{DMART}}$ | ADDR29 | $\overline{\text{MS}}2$ | ADDR26 | ADDR25 | D |
| DATA31 | DATA32 | DATA30 | DATA33 | NC | GND | GND | GND | GND | GND | GND | ADDR27 | ADDR24 | ADDR22 | ADDR21 | E |
| DATA27 | DATA28 | DATA26 | DATA29 | GND | GND | V_{DD} | V_{DD} | V_{DD} | GND | GND | ADDR23 | ADDR20 | ADDR18 | ADDR17 | F |
| DATA23 | DATA24 | DATA25 | DATA22 | GND | V_{DD} | V_{DD} | V_{DD} | V_{DD} | V_{DD} | GND | ADDR19 | ADDR16 | ADDR15 | ADDR14 | G |
| DATA20 | DATA21 | DATA19 | DATA18 | GND | V_{DD} | V_{DD} | V_{DD} | V_{DD} | V_{DD} | GND | ADDR10 | ADDR13 | ADDR11 | ADDR12 | H |
| DATA17 | DATA16 | DATA15 | DATA12 | GND | V_{DD} | V_{DD} | V_{DD} | V_{DD} | V_{DD} | GND | ADDR4 | ADDR7 | ADDR8 | ADDR9 | J |
| DATA14 | DATA13 | DATA11 | DATA8 | GND | GND | V_{DD} | V_{DD} | V_{DD} | GND | ICSA | ADDR0 | ADDR3 | ADDR5 | ADDR6 | K |
| DATA10 | DATA9 | DATA7 | DATA4 | NC | GND | GND | GND | GND | GND | RPBA | FLAG3 | FLAG0 | ADDR1 | ADDR2 | L |
| DATA6 | DATA5 | DATA2 | L0DAT0 | L1DAT1 | L2DAT3 | L3DAT0 | L4DAT2 | L5DAT2 | L5ACK | LBOOT | TDI | TIMEXP | FLAG2 | FLAG1 | M |
| DATA3 | DATA1 | L0DAT3 | L1DAT3 | L1ACK | L2DAT0 | L3DAT3 | L3CLK | L4CLK | L5DAT1 | ID2 | $\overline{\text{IRQ}}1$ | $\overline{\text{IRQ}}0$ | TDO | $\overline{\text{EMU}}$ | N |
| DATA0 | L0DAT1 | L0ACK | L1DAT0 | L2DAT2 | L2CLK | L3DAT2 | L4DAT3 | L4DAT0 | L5DAT3 | L5CLK | ID0 | EBOOT | TMS | $\overline{\text{TRST}}$ | P |
| L0DAT2 | L0CLK | L1DAT2 | L1CLK | L2DAT1 | L2ACK | L3DAT1 | L3ACK | L4DAT1 | L4ACK | L5DAT0 | ID1 | $\overline{\text{RESET}}$ | $\overline{\text{IRQ}}2$ | TCK | R |

Figure 39. ADSP-21060/ADSP-21062 PBGA Ball Assignments (Top View, Summary)

240-LEAD MQFP_PQ4/CQFP PIN CONFIGURATION

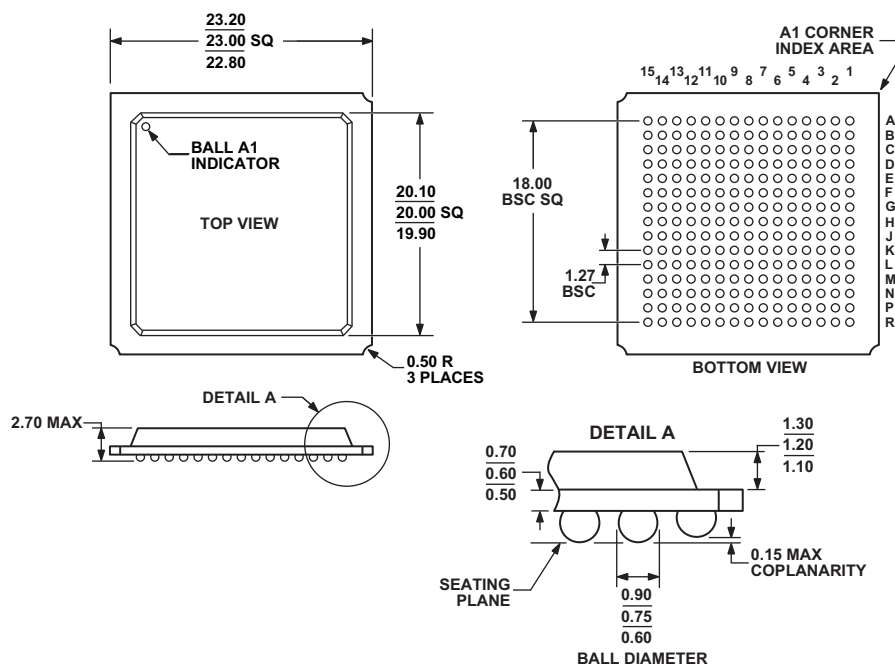
Table 41. ADSP-2106x MQFP_PQ4 and ADSP-21060CZ CQFP Pin Assignments (SP-240-2, QS-240-2A, QS-240-2B)

| Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. |
|--------------------------|---------|---------------------------|---------|---------------------------|---------|-----------------|---------|-----------------|---------|---------------------------|---------|
| TDI | 1 | ADDR20 | 41 | TCLK0 | 81 | DATA41 | 121 | DATA14 | 161 | L2DAT0 | 201 |
| $\overline{\text{TRST}}$ | 2 | ADDR21 | 42 | TFS0 | 82 | DATA40 | 122 | DATA13 | 162 | L2CLK | 202 |
| V _{DD} | 3 | $\overline{\text{GND}}$ | 43 | DR0 | 83 | DATA39 | 123 | DATA12 | 163 | L2ACK | 203 |
| TDO | 4 | ADDR22 | 44 | RCLK0 | 84 | V _{DD} | 124 | GND | 164 | NC | 204 |
| TIMEXP | 5 | ADDR23 | 45 | RFS0 | 85 | DATA38 | 125 | DATA11 | 165 | V _{DD} | 205 |
| $\overline{\text{EMU}}$ | 6 | ADDR24 | 46 | V _{DD} | 86 | DATA37 | 126 | DATA10 | 166 | L3DAT3 | 206 |
| ICSA | 7 | V _{DD} | 47 | V _{DD} | 87 | DATA36 | 127 | DATA9 | 167 | L3DAT2 | 207 |
| FLAG3 | 8 | GND | 48 | GND | 88 | GND | 128 | V _{DD} | 168 | L3DAT1 | 208 |
| FLAG2 | 9 | V _{DD} | 49 | ADRCLK | 89 | NC | 129 | DATA8 | 169 | L3DAT0 | 209 |
| FLAG1 | 10 | ADDR25 | 50 | REDY | 90 | DATA35 | 130 | DATA7 | 170 | L3CLK | 210 |
| FLAG0 | 11 | ADDR26 | 51 | $\overline{\text{HBG}}$ | 91 | DATA34 | 131 | DATA6 | 171 | L3ACK | 211 |
| GND | 12 | ADDR27 | 52 | $\overline{\text{CS}}$ | 92 | DATA33 | 132 | GND | 172 | GND | 212 |
| ADDR0 | 13 | GND | 53 | $\overline{\text{RD}}$ | 93 | V _{DD} | 133 | DATA5 | 173 | L4DAT3 | 213 |
| ADDR1 | 14 | $\overline{\text{MS3}}$ | 54 | $\overline{\text{WR}}$ | 94 | V _{DD} | 134 | DATA4 | 174 | L4DAT2 | 214 |
| V _{DD} | 15 | $\overline{\text{MS2}}$ | 55 | GND | 95 | GND | 135 | DATA3 | 175 | L4DAT1 | 215 |
| ADDR2 | 16 | $\overline{\text{MS1}}$ | 56 | V _{DD} | 96 | DATA32 | 136 | V _{DD} | 176 | L4DAT0 | 216 |
| ADDR3 | 17 | $\overline{\text{MS0}}$ | 57 | GND | 97 | DATA31 | 137 | DATA2 | 177 | L4CLK | 217 |
| ADDR4 | 18 | $\overline{\text{SW}}$ | 58 | CLKIN | 98 | DATA30 | 138 | DATA1 | 178 | L4ACK | 218 |
| GND | 19 | $\overline{\text{BMS}}$ | 59 | ACK | 99 | GND | 139 | DATA0 | 179 | V _{DD} | 219 |
| ADDR5 | 20 | ADDR28 | 60 | $\overline{\text{DMAG2}}$ | 100 | DATA29 | 140 | GND | 180 | GND | 220 |
| ADDR6 | 21 | GND | 61 | $\overline{\text{DMAG1}}$ | 101 | DATA28 | 141 | GND | 181 | V _{DD} | 221 |
| ADDR7 | 22 | V _{DD} | 62 | PAGE | 102 | DATA27 | 142 | L0DAT3 | 182 | L5DAT3 | 222 |
| V _{DD} | 23 | V _{DD} | 63 | V _{DD} | 103 | V _{DD} | 143 | L0DAT2 | 183 | L5DAT2 | 223 |
| ADDR8 | 24 | ADDR29 | 64 | $\overline{\text{BR6}}$ | 104 | V _{DD} | 144 | L0DAT1 | 184 | L5DAT1 | 224 |
| ADDR9 | 25 | ADDR30 | 65 | $\overline{\text{BR5}}$ | 105 | DATA26 | 145 | L0DAT0 | 185 | L5DAT0 | 225 |
| ADDR10 | 26 | ADDR31 | 66 | $\overline{\text{BR4}}$ | 106 | DATA25 | 146 | L0CLK | 186 | L5CLK | 226 |
| GND | 27 | GND | 67 | $\overline{\text{BR3}}$ | 107 | DATA24 | 147 | L0ACK | 187 | L5ACK | 227 |
| ADDR11 | 28 | $\overline{\text{SBTS}}$ | 68 | $\overline{\text{BR2}}$ | 108 | GND | 148 | V _{DD} | 188 | GND | 228 |
| ADDR12 | 29 | $\overline{\text{DMAR2}}$ | 69 | $\overline{\text{BR1}}$ | 109 | DATA23 | 149 | L1DAT3 | 189 | ID2 | 229 |
| ADDR13 | 30 | $\overline{\text{DMAR1}}$ | 70 | GND | 110 | DATA22 | 150 | L1DAT2 | 190 | ID1 | 230 |
| V _{DD} | 31 | $\overline{\text{HBR}}$ | 71 | V _{DD} | 111 | DATA21 | 151 | L1DAT1 | 191 | ID0 | 231 |
| ADDR14 | 32 | DT1 | 72 | GND | 112 | V _{DD} | 152 | L1DAT0 | 192 | LBOOT | 232 |
| ADDR15 | 33 | TCLK1 | 73 | DATA47 | 113 | DATA20 | 153 | L1CLK | 193 | RPBA | 233 |
| GND | 34 | TFS1 | 74 | DATA46 | 114 | DATA19 | 154 | L1ACK | 194 | $\overline{\text{RESET}}$ | 234 |
| ADDR16 | 35 | DR1 | 75 | DATA45 | 115 | DATA18 | 155 | GND | 195 | EBOOT | 235 |
| ADDR17 | 36 | RCLK1 | 76 | V _{DD} | 116 | GND | 156 | GND | 196 | $\overline{\text{IRQ2}}$ | 236 |
| ADDR18 | 37 | RFS1 | 77 | DATA44 | 117 | DATA17 | 157 | V _{DD} | 197 | $\overline{\text{IRQ1}}$ | 237 |
| V _{DD} | 38 | GND | 78 | DATA43 | 118 | DATA16 | 158 | L2DAT3 | 198 | $\overline{\text{IRQ0}}$ | 238 |
| V _{DD} | 39 | $\overline{\text{CPA}}$ | 79 | DATA42 | 119 | DATA15 | 159 | L2DAT2 | 199 | TCK | 239 |
| ADDR19 | 40 | DT0 | 80 | GND | 120 | V _{DD} | 160 | L2DAT1 | 200 | TMS | 240 |

Table 42. ADSP-21060CW/21060LCW CQFP Pin Assignments (QS-240-1A, QS-240-1B)

| Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. |
|------------------------|---------|---------------------------|---------|---------------------------|---------|-------------------------|---------|---------------------------|---------|------------------------|---------|
| GND | 1 | DATA29 | 41 | $\overline{\text{DMAG2}}$ | 81 | ADDR28 | 121 | ADDR5 | 161 | GND | 201 |
| DATA0 | 2 | GND | 42 | ACK | 82 | $\overline{\text{BMS}}$ | 122 | GND | 162 | V_{DD} | 202 |
| DATA1 | 3 | DATA30 | 43 | CLKIN | 83 | $\overline{\text{SW}}$ | 123 | ADDR4 | 163 | L4ACK | 203 |
| DATA2 | 4 | DATA31 | 44 | GND | 84 | $\overline{\text{MS0}}$ | 124 | ADDR3 | 164 | L4CLK | 204 |
| V_{DD} | 5 | DATA32 | 45 | V_{DD} | 85 | $\overline{\text{MS1}}$ | 125 | ADDR2 | 165 | L4DAT0 | 205 |
| DATA3 | 6 | GND | 46 | GND | 86 | $\overline{\text{MS2}}$ | 126 | V_{DD} | 166 | L4DAT1 | 206 |
| DATA4 | 7 | V_{DD} | 47 | $\overline{\text{WR}}$ | 87 | $\overline{\text{MS3}}$ | 127 | ADDR1 | 167 | L4DAT2 | 207 |
| DATA5 | 8 | V_{DD} | 48 | $\overline{\text{RD}}$ | 88 | GND | 128 | ADDR0 | 168 | L4DAT3 | 208 |
| GND | 9 | DATA33 | 49 | $\overline{\text{CS}}$ | 89 | ADDR27 | 129 | GND | 169 | GND | 209 |
| DATA6 | 10 | DATA34 | 50 | $\overline{\text{HBG}}$ | 90 | ADDR26 | 130 | FLAG0 | 170 | L3ACK | 210 |
| DATA7 | 11 | DATA35 | 51 | REDY | 91 | ADDR25 | 131 | FLAG1 | 171 | L3CLK | 211 |
| DATA8 | 12 | NC | 52 | ADRCLK | 92 | V_{DD} | 132 | FLAG2 | 172 | L3DAT0 | 212 |
| V_{DD} | 13 | GND | 53 | GND | 93 | GND | 133 | FLAG3 | 173 | L3DAT1 | 213 |
| DATA9 | 14 | DATA36 | 54 | V_{DD} | 94 | V_{DD} | 134 | ICSA | 174 | L3DAT2 | 214 |
| DATA10 | 15 | DATA37 | 55 | V_{DD} | 95 | ADDR24 | 135 | $\overline{\text{EMU}}$ | 175 | L3DAT3 | 215 |
| DATA11 | 16 | DATA38 | 56 | RFS0 | 96 | ADDR23 | 136 | TIMEXP | 176 | V_{DD} | 216 |
| GND | 17 | V_{DD} | 57 | RCLK0 | 97 | ADDR22 | 137 | TDO | 177 | NC | 217 |
| DATA12 | 18 | DATA39 | 58 | DR0 | 98 | GND | 138 | V_{DD} | 178 | L2ACK | 218 |
| DATA13 | 19 | DATA40 | 59 | TFS0 | 99 | ADDR21 | 139 | $\overline{\text{TRST}}$ | 179 | L2CLK | 219 |
| DATA14 | 20 | DATA41 | 60 | TCLK0 | 100 | ADDR20 | 140 | TDI | 180 | L2DAT0 | 220 |
| V_{DD} | 21 | GND | 61 | DT0 | 101 | ADDR19 | 141 | TMS | 181 | L2DAT1 | 221 |
| DATA15 | 22 | DATA42 | 62 | $\overline{\text{CPA}}$ | 102 | V_{DD} | 142 | TCK | 182 | L2DAT2 | 222 |
| DATA16 | 23 | DATA43 | 63 | GND | 103 | V_{DD} | 143 | $\overline{\text{IRQ0}}$ | 183 | L2DAT3 | 223 |
| DATA17 | 24 | DATA44 | 64 | RFS1 | 104 | ADDR18 | 144 | $\overline{\text{IRQ1}}$ | 184 | V_{DD} | 224 |
| GND | 25 | V_{DD} | 65 | RCLK1 | 105 | ADDR17 | 145 | $\overline{\text{IRQ2}}$ | 185 | GND | 225 |
| DATA18 | 26 | DATA45 | 66 | DR1 | 106 | ADDR16 | 146 | EBOOT | 186 | GND | 226 |
| DATA19 | 27 | DATA46 | 67 | TFS1 | 107 | GND | 147 | $\overline{\text{RESET}}$ | 187 | L1ACK | 227 |
| DATA20 | 28 | DATA47 | 68 | TCLK1 | 108 | ADDR15 | 148 | RPBA | 188 | L1CLK | 228 |
| V_{DD} | 29 | GND | 69 | DT1 | 109 | ADDR14 | 149 | LBOOT | 189 | L1DAT0 | 229 |
| DATA21 | 30 | V_{DD} | 70 | $\overline{\text{HBR}}$ | 110 | V_{DD} | 150 | ID0 | 190 | L1DAT1 | 230 |
| DATA22 | 31 | GND | 71 | $\overline{\text{DMAR1}}$ | 111 | ADDR13 | 151 | ID1 | 191 | L1DAT2 | 231 |
| DATA23 | 32 | $\overline{\text{BR1}}$ | 72 | $\overline{\text{DMAR2}}$ | 112 | ADDR12 | 152 | ID2 | 192 | L1DAT3 | 232 |
| GND | 33 | $\overline{\text{BR2}}$ | 73 | $\overline{\text{SBTS}}$ | 113 | ADDR11 | 153 | GND | 193 | V_{DD} | 233 |
| DATA24 | 34 | $\overline{\text{BR3}}$ | 74 | GND | 114 | GND | 154 | L5ACK | 194 | L0ACK | 234 |
| DATA25 | 35 | $\overline{\text{BR4}}$ | 75 | ADDR31 | 115 | ADDR10 | 155 | L5CLK | 195 | L0CLK | 235 |
| DATA26 | 36 | $\overline{\text{BR5}}$ | 76 | ADDR30 | 116 | ADDR9 | 156 | L5DAT0 | 196 | L0DAT0 | 236 |
| V_{DD} | 37 | $\overline{\text{BR6}}$ | 77 | ADDR29 | 117 | ADDR8 | 157 | L5DAT1 | 197 | L0DAT1 | 237 |
| V_{DD} | 38 | V_{DD} | 78 | V_{DD} | 118 | V_{DD} | 158 | L5DAT2 | 198 | L0DAT2 | 238 |
| DATA27 | 39 | PAGE | 79 | V_{DD} | 119 | ADDR7 | 159 | L5DAT3 | 199 | L0DAT3 | 239 |
| DATA28 | 40 | $\overline{\text{DMAG1}}$ | 80 | GND | 120 | ADDR6 | 160 | V_{DD} | 200 | GND | 240 |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-034-AAJ-2

Figure 40. 225-Ball Plastic Ball Grid Array [PBGA]
(B-225-2)

Dimensions shown in millimeters

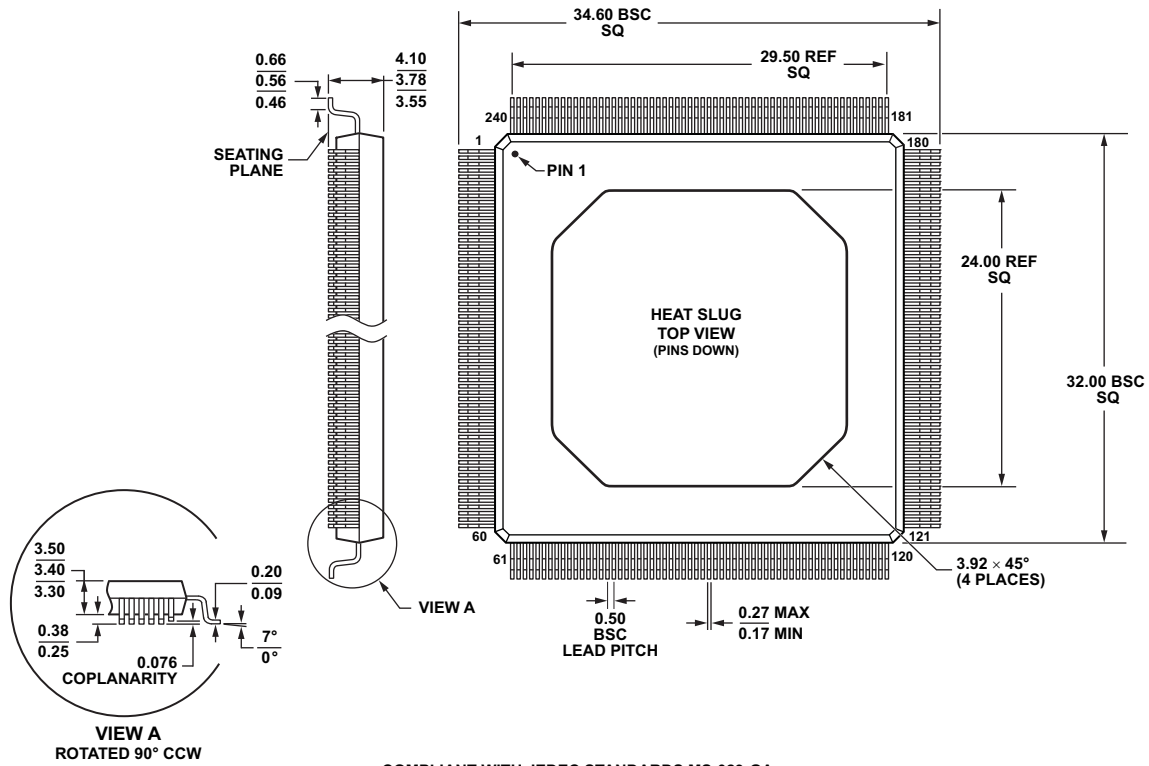


Figure 41. 240-Lead Metric Quad Flat Package, Thermally Enhanced "PowerQuad" [MQFP_PQ4]
(SP-240-2)

Dimensions shown in millimeters

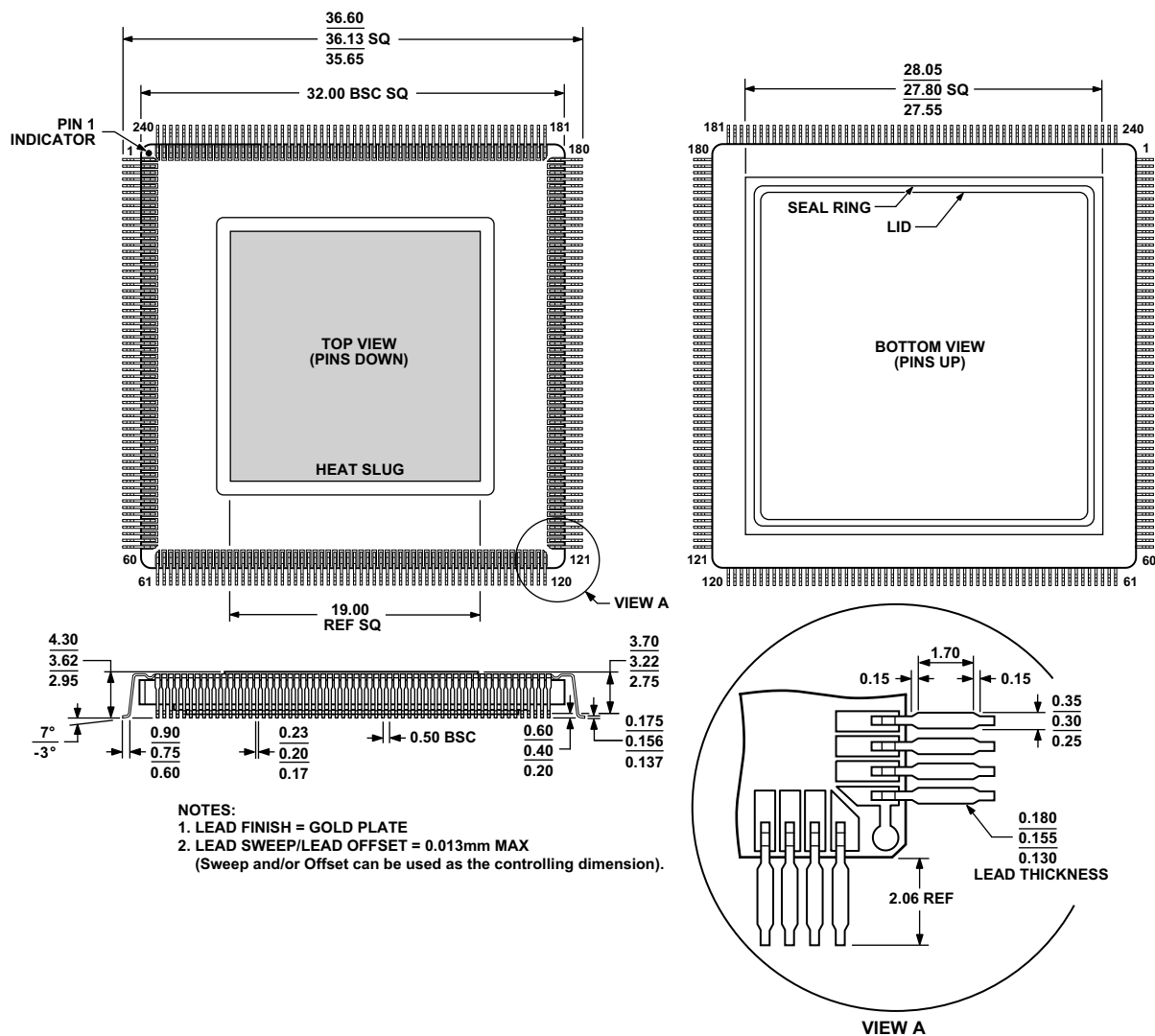


Figure 42. 240-Lead Ceramic Quad Flat Package, Heat Slug Up [CQFP]
(QS-240-2A)

Dimensions shown in millimeters

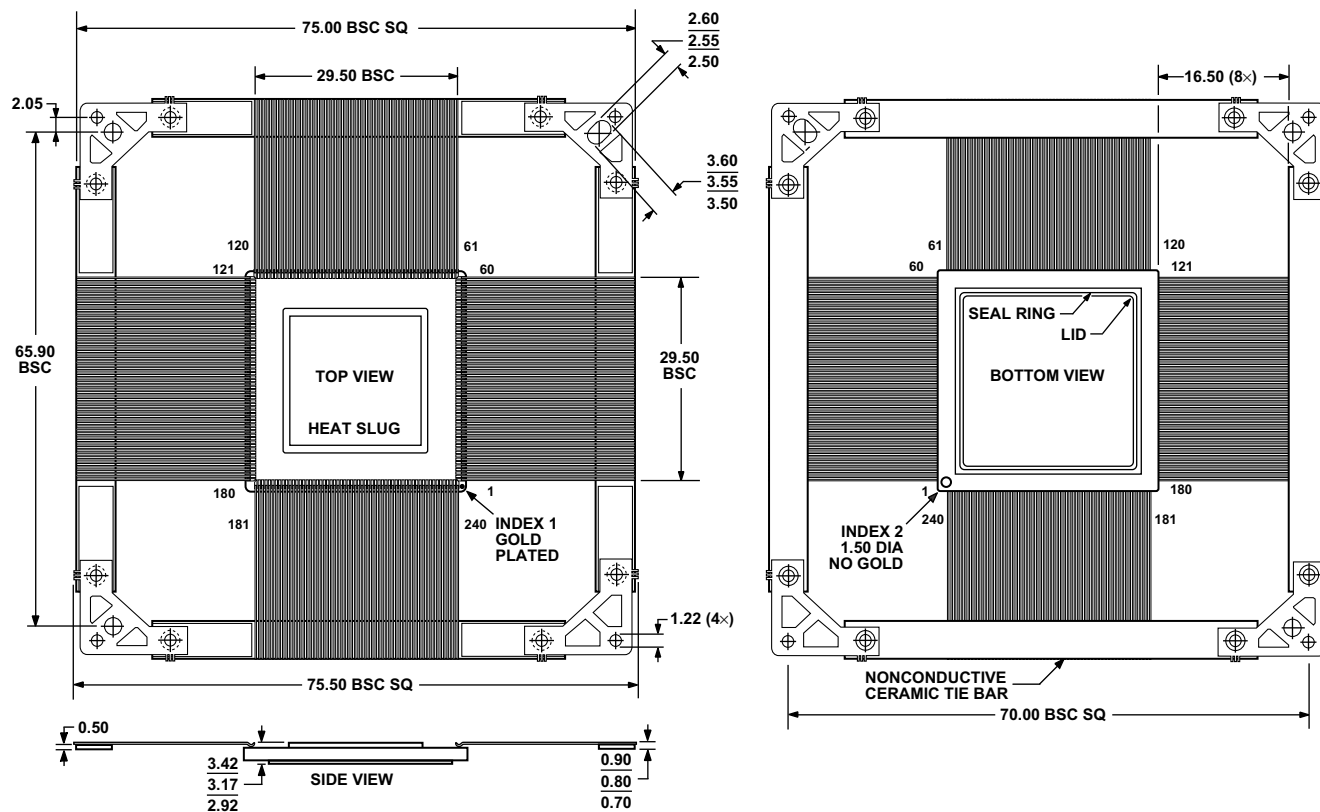


Figure 43. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Down [CQFP]
(QS-240-2B)

Dimensions shown in millimeters

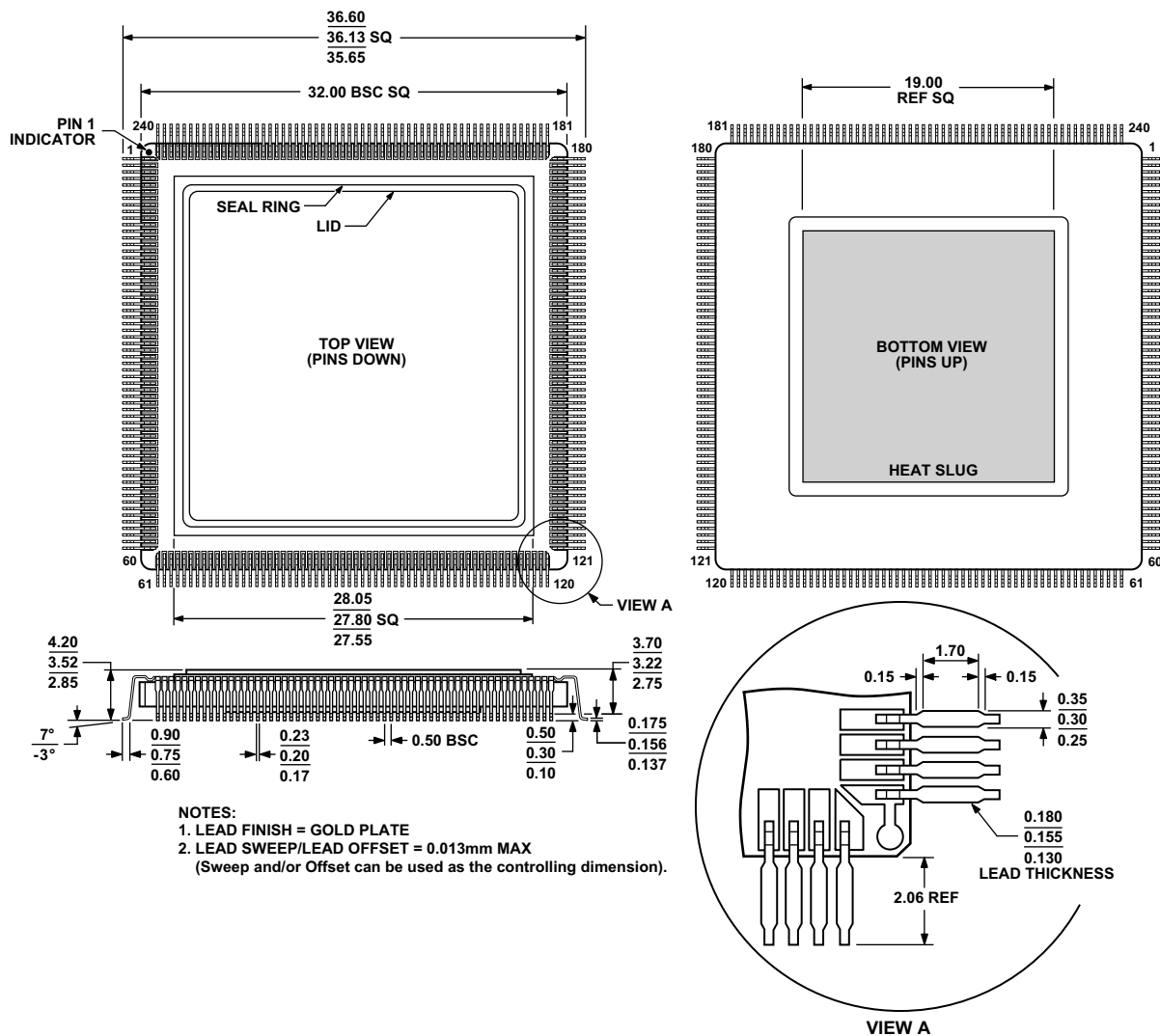


Figure 44. 240-Lead Ceramic Quad Flat Package, Heat Slug Down [CQFP]
(QS-240-1A)

Dimensions shown in millimeters

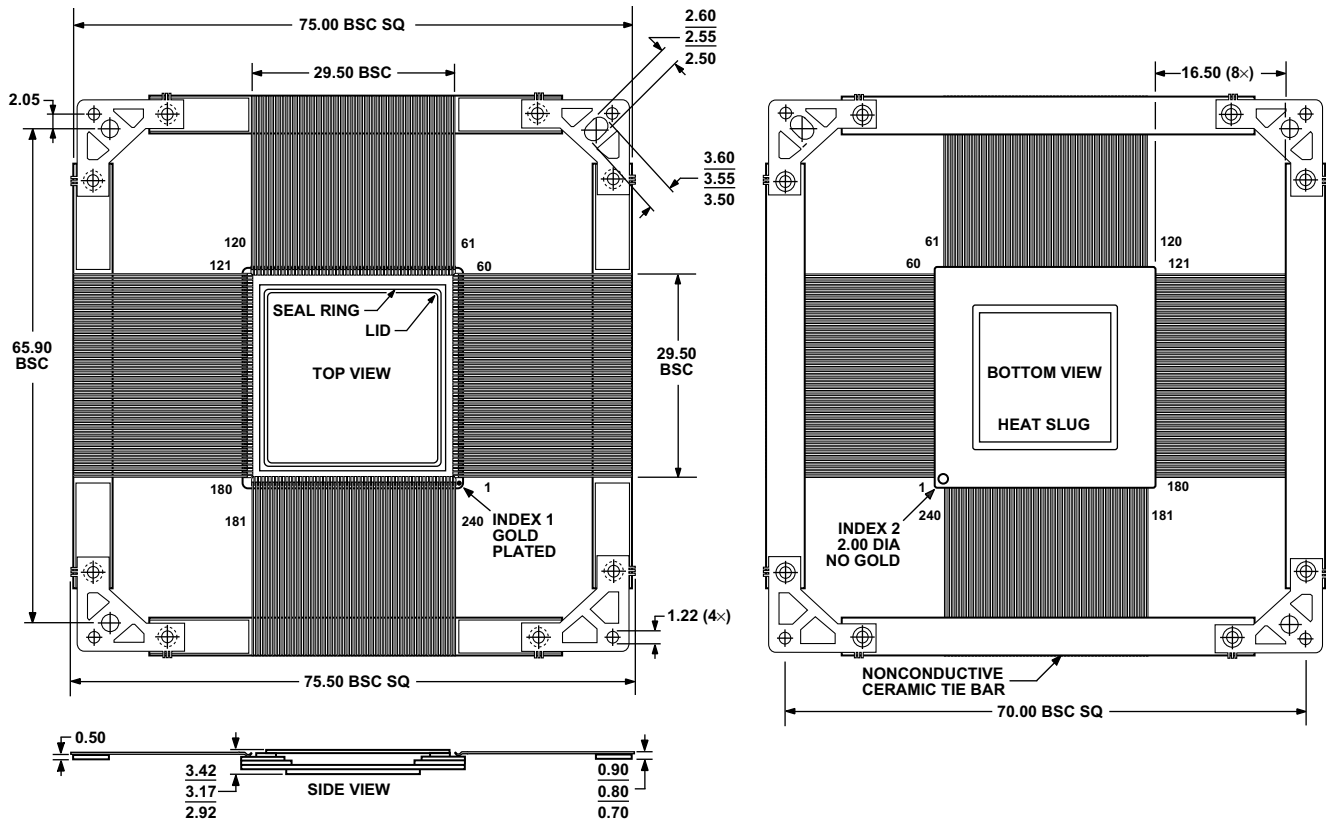


Figure 45. 240-Lead Ceramic Quad Flat Package, Mounted with Cavity Up [CQFP]
(QS-240-1B)

Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 43 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 43. BGA Data for Use with Surface-Mount Design

| Package | Ball Attach Type | Solder Mask Opening | Ball Pad Size |
|----------------------------|---------------------|---------------------|------------------|
| 225-Ball Grid Array (PBGA) | Solder Mask Defined | 0.63 mm diameter | 0.76 mm diameter |

ADSP-21062/ADSP-21062L

ORDERING GUIDE

| Model | Notes | Temperature Range | Instruction Rate | On-Chip SRAM | Operating Voltage | Package Description | Package Option |
|--------------------|-----------------|-------------------|------------------|--------------|-------------------|--------------------------------|----------------|
| ASDP-21060CZ-133 | ^{1, 2} | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CZ-160 | ^{1, 2} | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Up] | QS-240-2A |
| ASDP-21060CW-133 | ^{1, 2} | –40°C to +100°C | 33 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ASDP-21060CW-160 | ^{1, 2} | –40°C to +100°C | 40 MHz | 4M Bit | 5 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21060KS-133 | | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-133 | ² | 0°C to 85°C | 33 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KSZ-160 | ² | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060KB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060KBZ-160 | ² | 0°C to 85°C | 40 MHz | 4M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LKSZ-133 | ² | 0°C to 85°C | 33 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKS-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKSZ-160 | ² | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21060LKB-160 | | 0°C to 85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LAB-160 | | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LABZ-160 | ² | –40°C to +85°C | 40 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCB-133 | | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21060LCBZ-133 | ² | –40°C to +100°C | 33 MHz | 4M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ASDP-21060LCW-160 | ^{1, 2} | –40°C to +100°C | 40 MHz | 4M Bit | 3.3 V | 240-Lead CQFP [Heat Slug Down] | QS-240-1A |
| ADSP-21062KS-133 | | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-133 | ² | 0°C to 85°C | 33 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KSZ-160 | ² | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062KB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062KBZ-160 | ² | 0°C to 85°C | 40 MHz | 2M Bit | 5 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062CS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062CSZ-160 | ² | –40°C to +100°C | 40 MHz | 2M Bit | 5 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-133 | ² | 0°C to 85°C | 33 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKS-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKSZ-160 | ² | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LKB-160 | | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LKBZ-160 | ² | 0°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LAB-160 | | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LABZ-160 | ² | –40°C to 85°C | 40 MHz | 2M Bit | 3.3 V | 225-Ball PBGA | B-225-2 |
| ADSP-21062LCS-160 | | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |
| ADSP-21062LCSZ-160 | ² | –40°C to +100°C | 40 MHz | 2M Bit | 3.3 V | 240-Lead MQFP_PQ4 | SP-240-2 |

¹ Model refers to package with formed leads. For model numbers of unformed lead versions (QS-240-1B, QS-240-2B), contact Analog Devices or an Analog Devices sales representative.

² RoHS compliant part.

