Silicon SP4T Switch, Nonreflective, 9kHz to 20GHz

FEATURES

- Wideband frequency range: 9kHz to 20GHz
- Nonreflective design with on-chip 50Ω terminations
- Low insertion loss
  - 0.7dB typical to 6GHz
  - 0.9dB typical to 12GHz
  - 1.2dB typical to 20GHz
- High isolation
  - 53dB typical to 6GHz
  - 49dB typical to 12GHz
  - 47dB typical to 20GHz
- High linearity
  - Input P0.1dB: 34dBm typical
  - Input IP3: 55dBm typical
- High RF power handling
  - Through path: 33dBm up to 20 GHz
  - Terminated path: 18dBm up to 20 GHz
- Switching on and off time: 8.5µs
- 0.1dB settling time: 15µs
- All off-state control
- Logic select control
- Single-supply operation with derated power handling
- No low frequency spurs, and no internal voltage generation
- 24-terminal, 3mm × 3mm, land grid array (LGA) package
- Pin compatible with the ADRF5042, ADRF5043, ADRF5048, ADRF5049, and ADRF5050

APPLICATIONS

- Test instrumentation
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

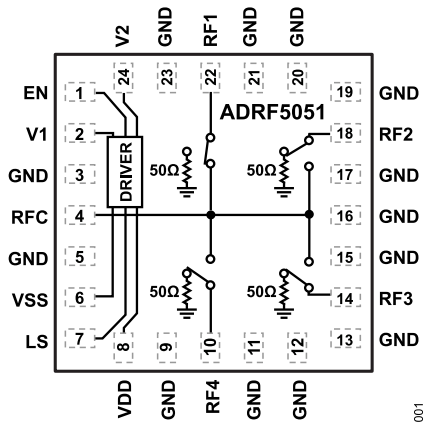

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5051 is a nonreflective SP4T switch manufactured in a silicon on insulator (SOI) process.

The ADRF5051 operates from 9kHz to 20GHz with an insertion loss of lower than 1.20dB and an isolation higher than 47dB. The device has RF input power handling capability of 33dBm through path, 18dBm terminated path, and 30dBm hot switching at the RF common (RFC) port.

The ADRF5051 operates with a dual-supply voltage +3.3V and −3.3V. The device can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply pin (V_{SS}) is tied to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance are derated, see Table 2.

The ADRF5051 employs complimentary metal-oxide semiconductor (CMOS)- and low voltage transistor to transistor logic (LVTTL)-compatible controls.

The device has enable (EN) and logic select (LS) controls. Pulling the EN pin to high activates an all-off state while pulling the LS pin high inverts the throw port selection logic, allowing ease of use for a back-to-back application. See the Theory of Operation section, Table 7, and the Back-to-Back Application section for additional information.

The ADRF5051 is pin compatible with the ADRF5042, ADRF5043, ADRF5048, ADRF5049, and ADRF5050.

The ADRF5051 comes in a 24-terminal, 3mm × 3mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

TABLE OF CONTENTS

REVISION HISTORY

6/2025—Rev. 0 to Rev. A

Change to Table 3.... 6

3/2025—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3V, V_{SS} = −3.3V, Control Input 1 voltage (V_1) and Control Input 2 voltage (V_2) = 0V or V_{DD}, T_{CASE} = 25°C, and a 50Ω system, unless otherwise noted. V_{CTRL} is the voltages of the digital control input pins, V1 and V2, and RFx refers to RF1, RF2, RF3, and RF4.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.009		20000	MHz
INSERTION LOSS						
Between RFC and RFx (On)		9kHz to 6GHz		0.7		dB
		6GHz to 12GHz		0.9		dB
		12GHz to 20GHz		1.2		dB
ISOLATION						
Between RFC and RFx (Off)		9kHz to 6GHz		55		dB
		6GHz to 12GHz		54		dB
		12GHz to 20GHz		48		dB
Between RFx and RFx		9kHz to 6GHz		53		dB
		6GHz to 12GHz		49		dB
		12GHz to 20GHz		47		dB
RETURN LOSS						
RFC		9kHz to 6GHz		23		dB
		6GHz to 12GHz		22		dB
		12GHz to 20GHz		20		dB
RFx (On)		9kHz to 6GHz		23		dB
		6GHz to 12GHz		22		dB
		12GHz to 20GHz		22		dB
RFx (Off)		9kHz to 6GHz		20		dB
		6GHz to 12GHz		16		dB
		12GHz to 20GHz		13		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		3		µs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		8.5		µs
0.1dB Settling Time		50% V_{CTRL} to 0.1dB of final RF_{OUT}		15		µs
INPUT LINEARITY[1]						
0.1dB Power Compression	P0.1dB	f = 1MHz to 20GHz		34		dBm
Third-Order Intercept	IP3	Two-tone input power = 15dBm each tone, f = 1MHz to 20GHz, Δf = 1MHz		55		dBm
Second-Order Intercept	IP2	Two-tone input power = 15dBm each tone, f = 10GHz, Δf = 1MHz		105		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			160		µA
Negative Supply Current	I_{SS}			540		µA
DIGITAL CONTROL INPUTS		V1, V2, EN, and LS pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}	V1 and V2 pins		2.8		µA
		EN pin		40		µA
		LS pin		37		µA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power Handling[2]		f = 1MHz to 20GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)			33	dBm
Terminated Path		RF signal is applied to any unselected RF throw port (unselected RFx)			18	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports			30	dBm
Hot Switching (RFx)		RF signal is applied to a RFx port while switching to or from another RFx port			18	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 23 to Figure 26.

[2] For RF power handling derating over the extended frequency range, see Figure 2.

[3] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specification by 3dB.

SPECIFICATIONS

SINGLE-SUPPLY OPERATION SPECIFICATIONS

V_{DD} = 3.3V, V_{SS} = 0V, V_1 and V_2 = 0V or V_{DD}, T_{CASE} = 25°C, and 50Ω system, unless otherwise noted.

The small signal and bias specifications are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.009		20000	MHz
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		17		µs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		28		µs
0.1dB Settling Time		50% V_{CTRL} to 0.1dB of final RF_{OUT}		32		µs
INPUT LINEARITY [1]						
0.1dB Power Compression	P0.1dB	f = 1MHz to 20GHz		21		dBm
Third-Order Intercept	IP3	Two-tone input power = 15dBm each tone, f = 1MHz to 20GHz, Δf = 1MHz		38		dBm
SUPPLY CURRENT						
Positive Supply Current	I_{DD}			36		µA
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling [2]		f = 1MHz to 20GHz, T_{CASE} = 85°C [3]				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)			21	dBm
Terminated Path		RF signal is applied to any unselected RF throw port (unselected RFx)			18	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports			21	dBm
Hot Switching (RFx)		RF signal is applied to a RFx port while switching to or from another RFx port			18	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 23 to Figure 26.

[2] For RF power handling derating over the extended frequency range, see Figure 2.

[3] For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specification by 3dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
V_{DD}	−0.3V to +3.6V
V_{SS}	−3.6V to +0.3V
Digital Control Inputs[1]	
Voltage	−0.3V to V_{DD} + 0.3V
Current	3mA
RF Input Power[2]	
Dual Supply (V_{DD} = 3.3V, V_{SS} = −3.3V, f = 1MHz to 20GHz, T_{CASE} = 85°C[3])	
Through Path	33.5dBm
Terminated Path	18.5dBm
Hot Switching (RFC)	30.5dBm
Hot Switching (RFx)	18.5dBm
Single Supply (V_{DD} = 3.3V, V_{SS} = 0V, f = 1MHz to 20GHz, T_{CASE} = 85°C[3])	
Through Path	21.5dBm
Terminated Path	18.5dBm
Hot Switching (RFC)	21.5dBm
Hot Switching (RFx)	18.5dBm
Unbiased (V_{DD} = 0V, V_{SS} = 0V)	
RFC	30dBm
RFx	27dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For RF power handling derating over the extended frequency range, see Figure 2.

3 For T_{CASE} = 105°C operation, the RF power handling derates from the T_{CASE} = 85°C specification by 3dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-24-16		
Through Path	110	°C/W
Terminated Path	800	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVE

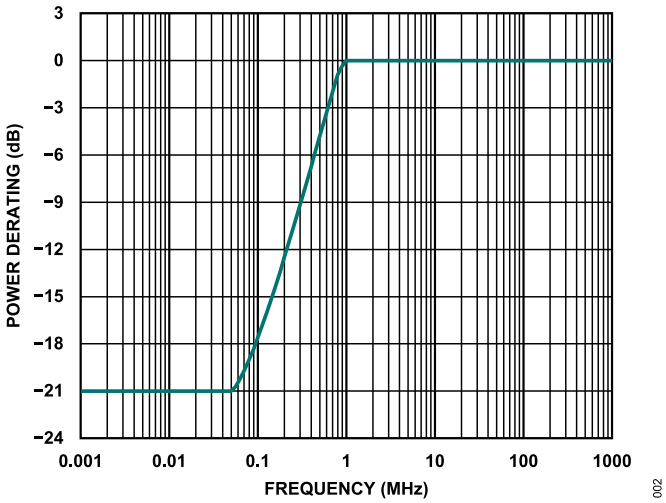

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5051

Table 5. ADRF5051, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	3000	2
Supply and Control Pins	3500	2
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

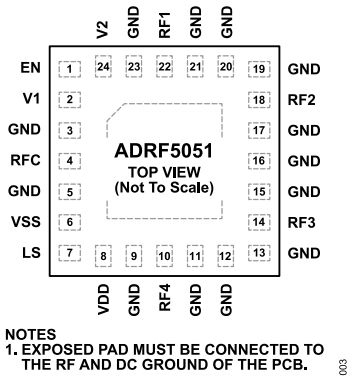

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. See Table 7 for the truth table and Figure 6 for the interface schematic.
2	V1	Control Input 1. See Table 7 for the truth table and Figure 5 for the interface schematic.
3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23	GND	Grounds. The GND pins must be connected to the RF and DC ground of the PCB.
4	RFC	RF Common Port. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
6	VSS	Negative Supply Voltage. See Figure 9 for the interface schematic.
7	LS	Logic Select Input. See Table 7 for the truth table and Figure 7 for the interface schematic.
8	VDD	Positive Supply Voltage. See Figure 8 for the interface schematic.
10	RF4	RF Throw Port 4. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
22	RF1	RF Throw Port 1. No DC blocking capacitor is required when the RF line potential is equal to 0V DC. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See Table 7 for the truth table and Figure 5 for the interface schematic.
	EPAD	Exposed Pad. Exposed pad must be connected to the RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

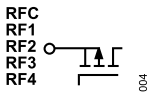

Figure 4. RFC and RF1 to RF4 Pin Interface Schematic

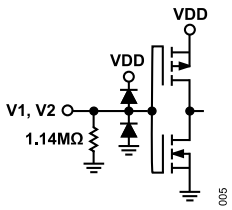

Figure 5. V1 and V2 Pin Interface Schematic

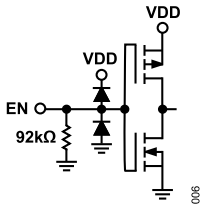

Figure 6. EN Pin Interface Schematic

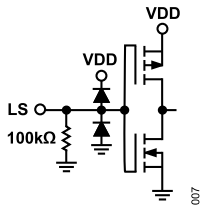

Figure 7. LS Pin Interface Schematic

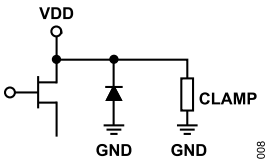

Figure 8. VDD Pin Interface Schematic

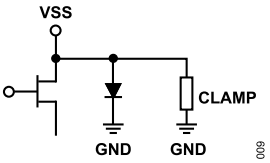

Figure 9. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3V, V_{SS} = −3.3V, LS and EN = 0V, V_1 or V_2 = 0V or V_{DD}, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted.

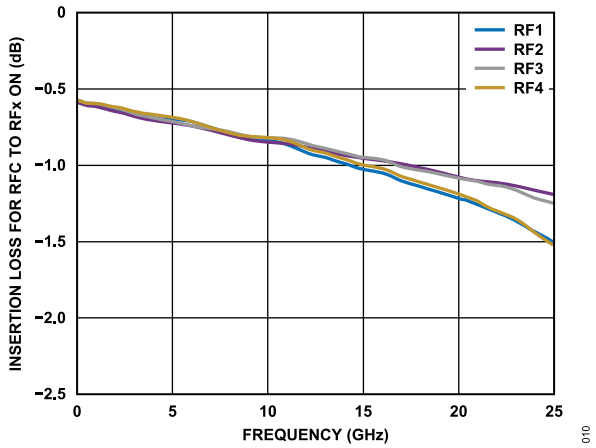

Figure 10. Insertion Loss for RFC to RFx (On) vs. Frequency

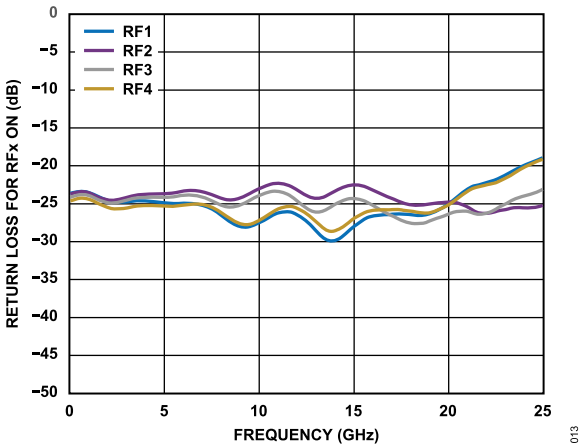

Figure 13. Return Loss for RFx (On) vs. Frequency

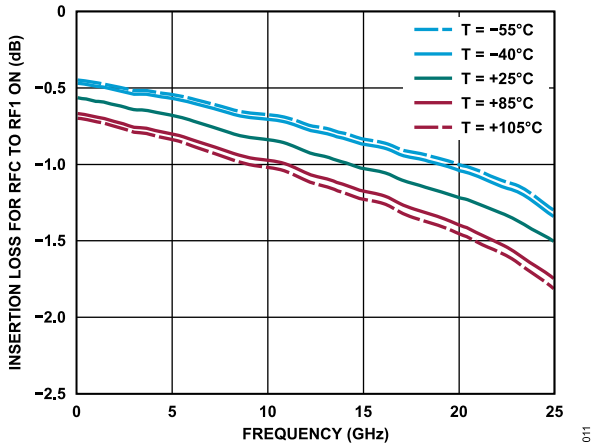

Figure 11. Insertion Loss for RFC to RF1 (On) vs. Frequency over Temperature

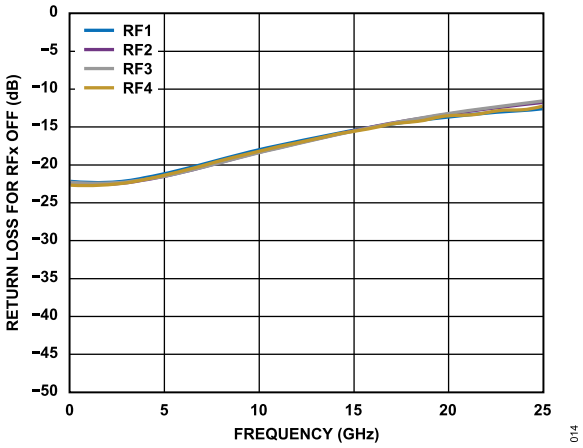

Figure 14. Return Loss for RFx (Off) vs. Frequency

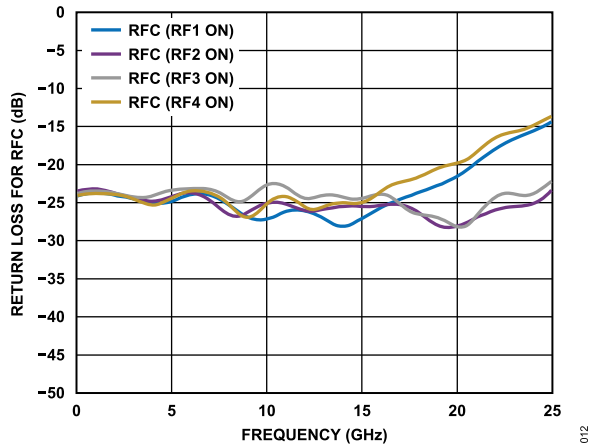

Figure 12. Return Loss for RFC vs. Frequency

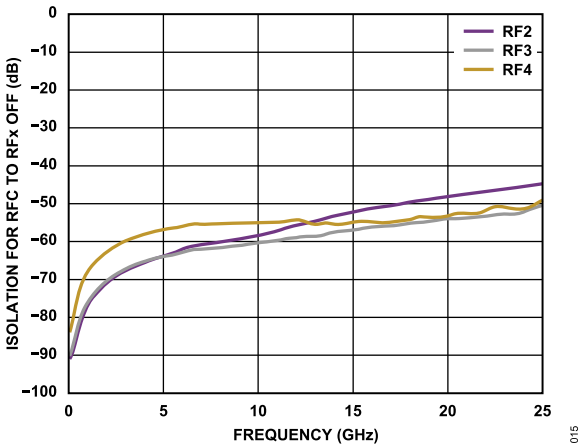

Figure 15. Isolation for RFC to RFx (Off) vs. Frequency, RF1 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

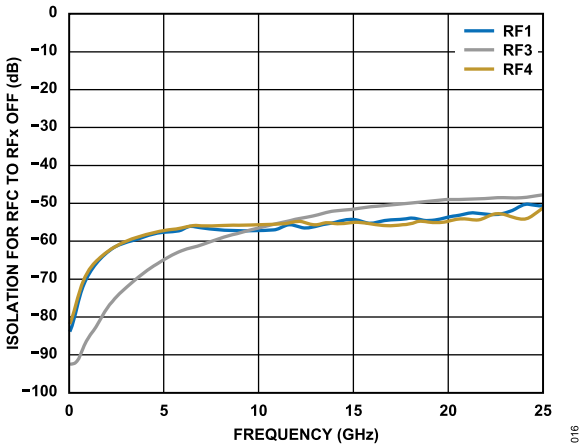

Figure 16. Isolation for RFC to RFx (Off) vs. Frequency, RF2 (On)

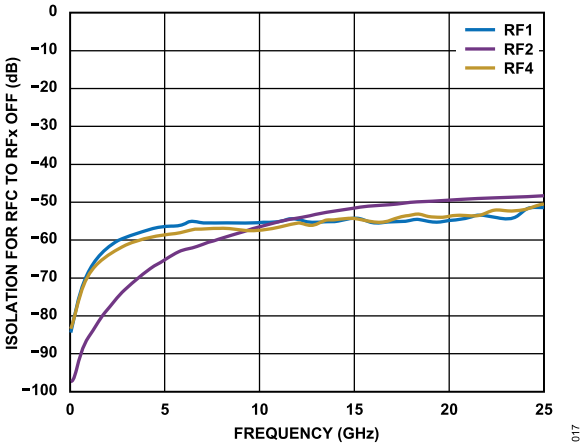

Figure 17. Isolation for RFC to RFx (Off) vs. Frequency, RF3 (On)

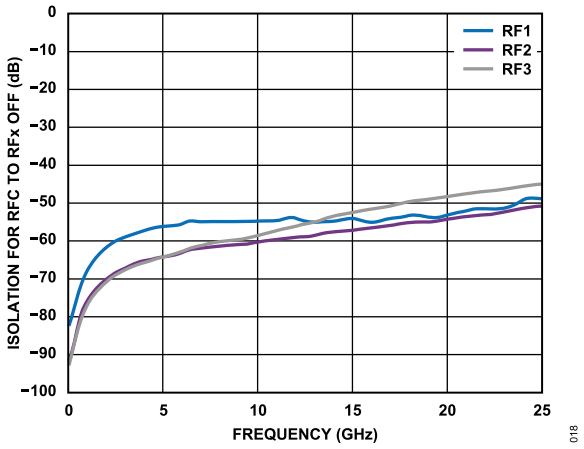

Figure 18. Isolation for RFC to RFx (Off) vs. Frequency, RF4 (On)

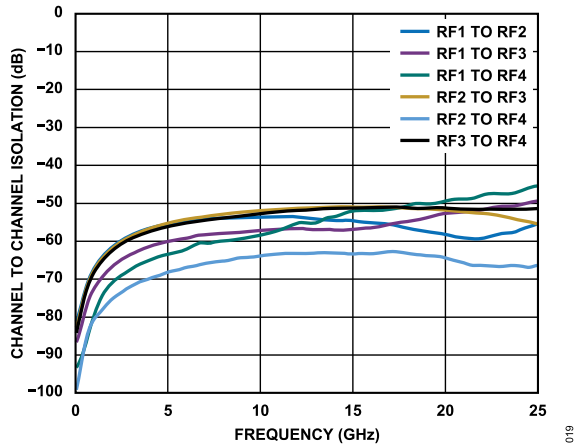

Figure 19. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF1 (On)

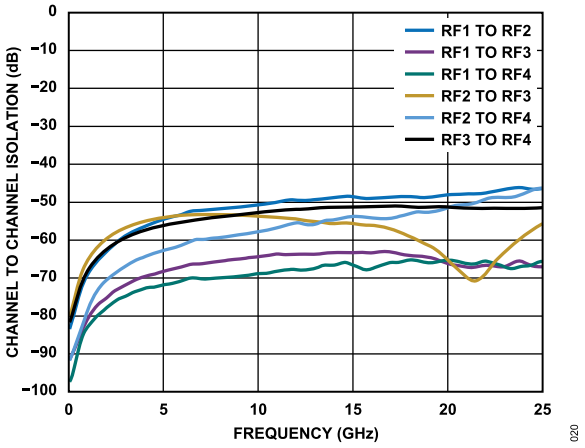

Figure 20. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF2 (On)

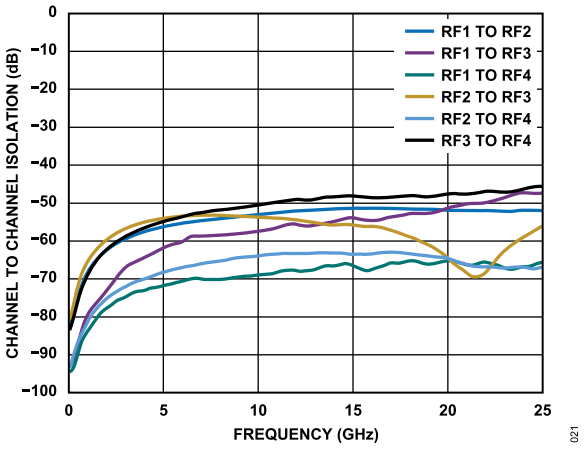

Figure 21. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF3 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

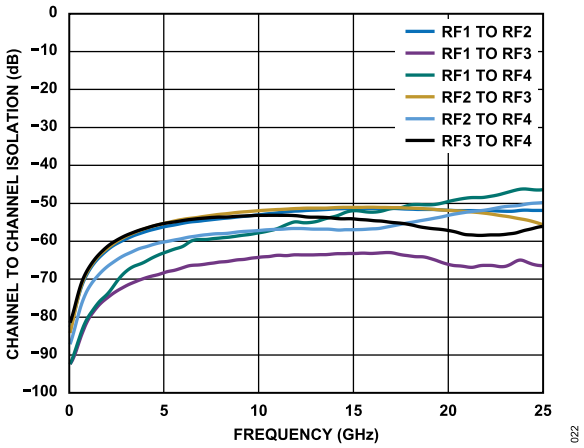

Figure 22. Channel to Channel (RFx to RFx) Isolation vs. Frequency, RF4 (On)

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3V, V_{SS} = −3.3V, LS and EN = 0V, V_1 or V_2 = 0V or V_{DD}, and T_{CASE} = 25°C on a 50Ω system, unless otherwise noted.

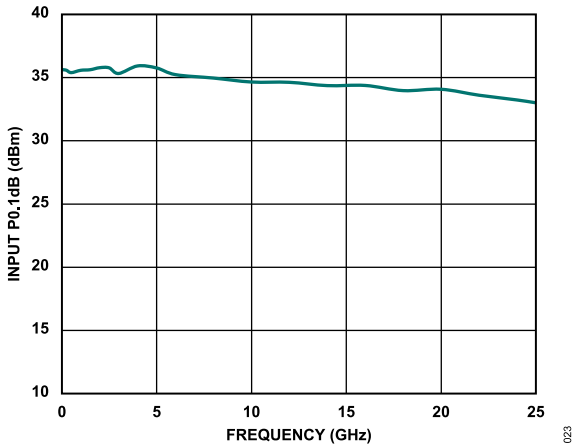

Figure 23. Input P0.1dB vs. Frequency

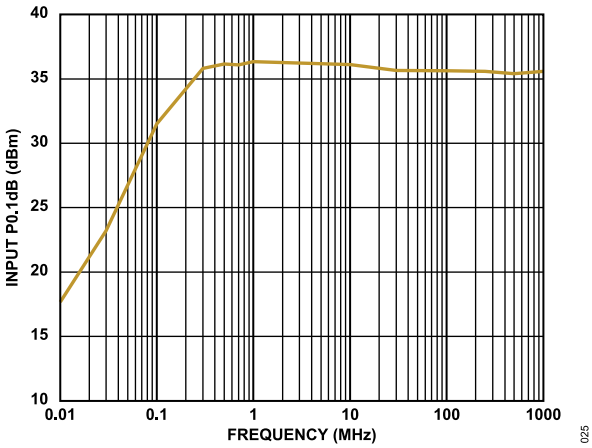

Figure 25. Input P0.1dB vs. Frequency, Low Frequency Detail

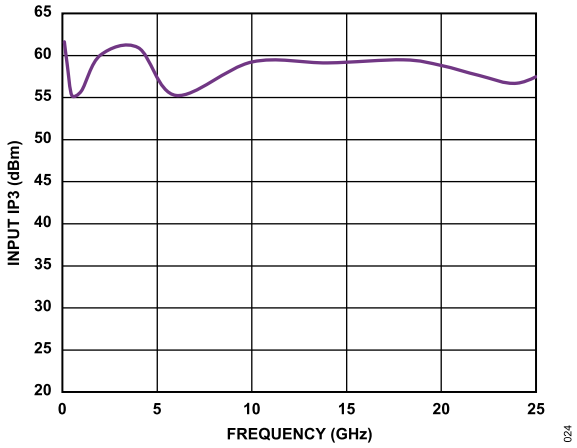

Figure 24. Input IP3 vs. Frequency

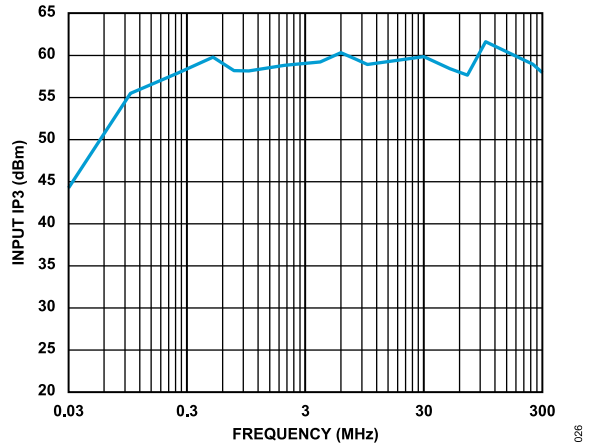

Figure 26. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5051 integrates a CMOS-/LVTTL-compatible control interface. The digital control input pins (EN, LS, V1, and V2) control the state of the RF paths (see Table 7).

The logic levels applied to the V1 and V2 pins determine which RF throw (RFx) port is in the insertion loss state (selected or on). The remaining three RFx ports are in the isolation state (unselected or off).

The LS pin allows the user to invert the RFx port selection logic (see the truth table for V1 and V2, Table 7). See the application example of this feature in the Back-to-Back Application section.

When the EN pin is logic high, all four RF paths are in an isolation state regardless of the logic state of the LS, V1, and V2 pins. The RFx ports are terminated to internal 50Ω resistors, and RFC becomes reflective.

Table 7. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	**LS**	**V1**	**V2**	**RFC to RF1**	**RFC to RF2**	**RFC to RF3**	**RFC to RF4**
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

THEORY OF OPERATION

RF INPUT AND OUTPUT

All of the RF ports (RFC and RF1 to RF4) are biased to ground potential, and a DC blocking capacitor is not required at the RF ports if the RF line potential is equal to ground. The RF ports are internally matched to 50Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. All unselected RF throw ports have high isolation from RFC and the remaining RF throw ports.

POWER SUPPLY

The ADRF5051 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.
3. Apply a control voltage to the digital control inputs (EN, LS, V1, and V2). Applying a control voltage to the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. Use a series 1kΩ resistor to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, the controller output is in a high impedance state) after VDD is powered up, it is recommended to use a pull-up or pull-down resistor.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

SINGLE-SUPPLY OPERATION

The ADRF5051 can operate with a single positive supply voltage applied to the VDD pin and the VSS pin connected to ground. In single-supply operation, the switching characteristics, linearity, and power handling performance are derated, see Table 2 for additional information.

APPLICATIONS INFORMATION

The ADRF5051 has two power supply pins (VDD and VSS) and four control pins (LS, EN, V1, and V2). Figure 27 shows the external components and connections for the supply and control pins. The supply and control pins are decoupled with 100pF multilayer ceramic capacitors. Place the decoupling capacitors as close as possible to the ADRF5051. The device pinout allows the placement of the decoupling capacitors close to the ADRF5051. No other external components are required for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0V. Refer to Pin Configuration and Function Descriptions section for additional information.

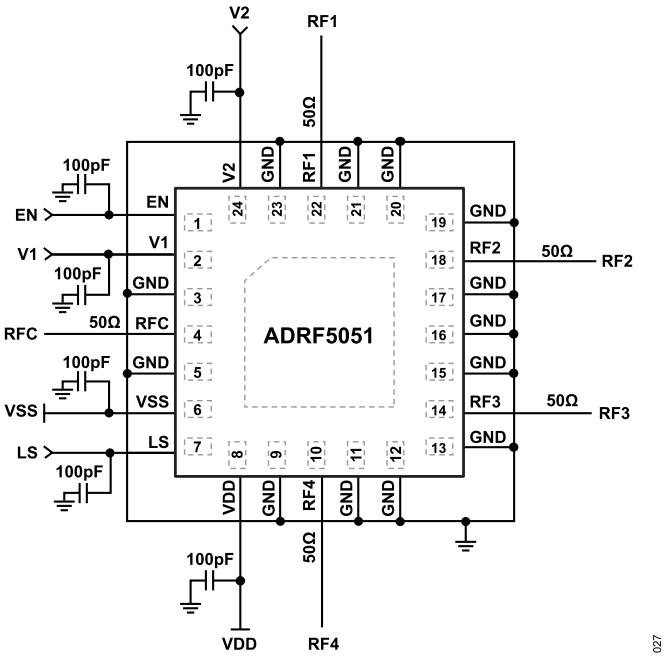

Figure 27. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50Ω characteristic impedance on the PCB. Figure 28 shows the referenced CPWG RF trace design for an RF substrate with 8mil thick Rogers RO4003 dielectric material. RF trace with 14mil width and 7mil clearance is recommended for 1.5mil finished copper thickness.

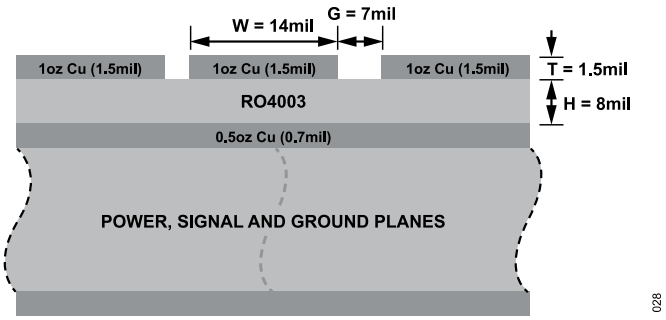

Figure 28. Example PCB Stack-Up

Figure 29 shows the routing of the RF traces, supply, and control signals from the ADRF5051. The ground planes are connected with as many filled, through vias as are allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

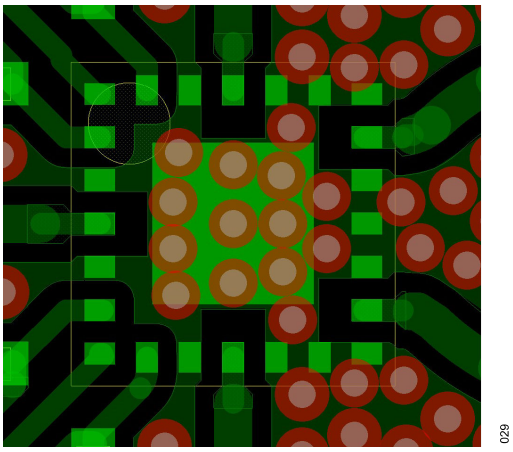

Figure 29. PCB Routings

Figure 30 shows the recommended layout from the device RF pins to the 50Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to the device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended to the device edge and tapered to the RF trace with a 45° angle. The paste mask is designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

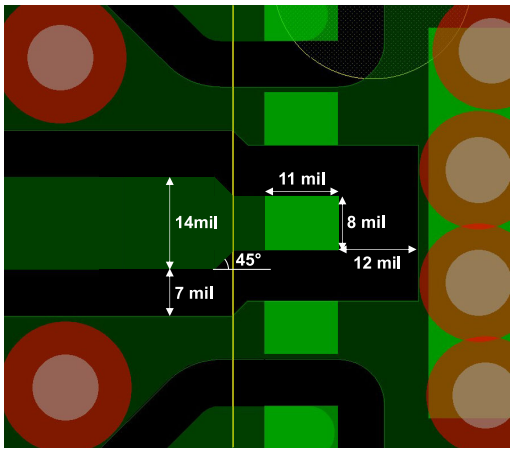

Figure 30. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

APPLICATIONS INFORMATION

BACK-TO-BACK APPLICATION

The switch control input pins, V1 and V2, can be connected together in a back-to-back application by hardwiring the LS pin of one device to GND and of one device to VDD as shown in Figure 31.

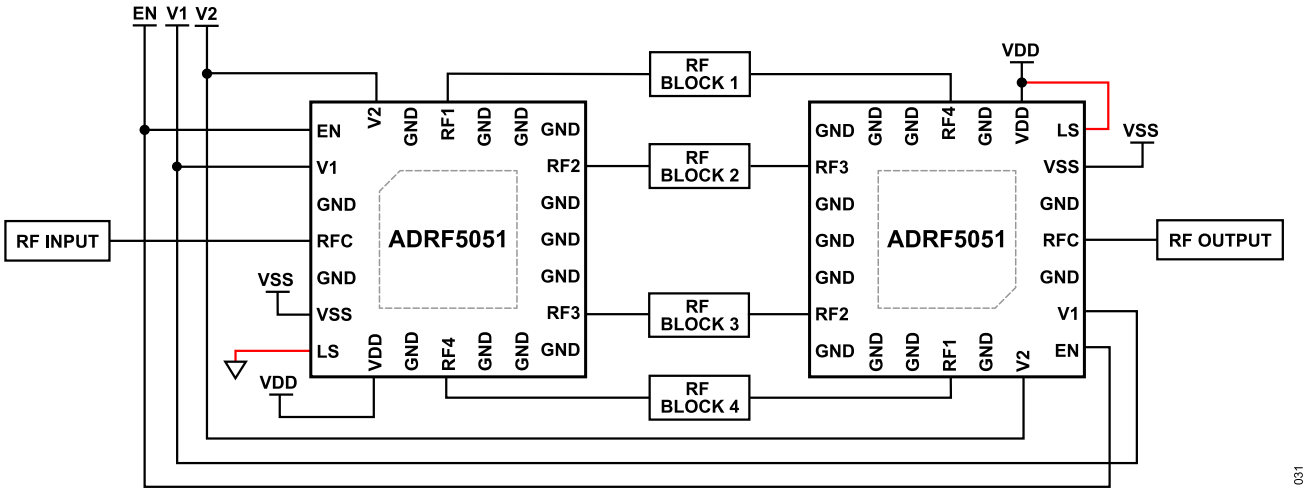

Figure 31. Back-to-Back Application Block Diagram

Table 8. Back-to-Back Application Truth Table

EN	V1	V2	Selected Path
Low	Low	Low	RF Block 1
Low	High	Low	RF Block 2
Low	Low	High	RF Block 3
Low	High	High	RF Block 4
High	Low or high	Low or high	Isolation (off)

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-24-16	LGA	24-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADRF5051BCCZN	−40°C to +105°C	24-Terminal LGA	CC-24-16	YAL
ADRF5051BCCZN-R7	−40°C to +105°C	24-Terminal LGA	CC-24-16	YAL

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Table 9. Evaluation Boards

Model[1]	Description
ADRF5051-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.