Nonreflective, Silicon SP4T Switch, 100 MHz to 20 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 20 GHz
- Nonreflective 50 Ω design
- Low insertion loss
  - 0.9 dB typical to 6 GHz
  - 1.00 dB typical to 12 GHz
  - 1.20 dB typical to 20 GHz
- High isolation Between RFx and RFx
  - 54 dB typical to 6 GHz
  - 50 dB typical to 12 GHz
  - 47 dB typical to 20 GHz
- High input linearity
  - P0.1dB: 34 dBm typical
  - IP3: 55 dBm typical
- High RF power handling
  - Through path: 33 dBm up to 20 GHz
  - Terminated path: 18 dBm up to 20 GHz
- Switching on and off time: 55 ns
- 0.1 dB settling time (50% V_{CTRL} to 0.1 dB final RF_{OUT}): 80 ns
- All off state control
- Logic select control
- Single-supply operation with derated power handling
- No low frequency spurs
- 24-terminal, 3 mm × 3 mm, land grid array (LGA) package
- Pin compatible with the ADRF5042 and ADRF5043

APPLICATIONS

- Test instrumentation
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

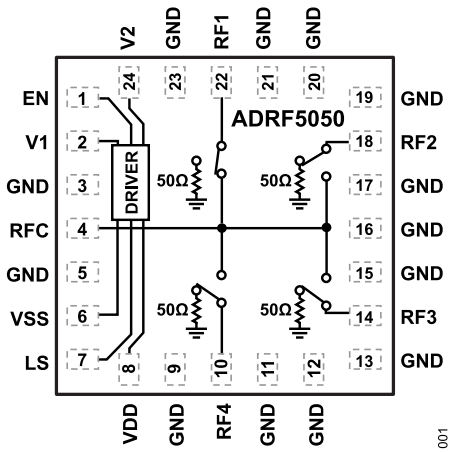

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5050 is a nonreflective SP4T switch manufactured in a silicon on insulator (SOI) process. The ADRF5050 operates from 100 MHz to 20 GHz with insertion loss less than 1.20 dB and isolation higher than 47 dB. The device has RF input power handling capability of 33 dBm for through paths.

The ADRF5050 operates with a dual-supply voltage +3.3 V and −3.3 V. The device can also operate with a single positive supply voltage (VDD) applied while the negative supply pin (VSS) is tied to ground. The single-supply operation condition requires lower operating power while the excellent small signal performance is maintained (see Table 2).

The ADRF5050 employs complimentary metal-oxide semiconductor (CMOS)- and low voltage transistor to transistor logic (LVTTL)-compatible controls. The device has enable and logic select controls to feature all off state and port mirroring, respectively.

The ADRF5050 is pin compatible with the ADRF5042 and ADRF5043.

The ADRF5050 comes in a 24-terminal, 3 mm × 3 mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

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REVISION HISTORY

11/2024—Rev. A to Rev. B

Updated Outline Dimensions ... 14

8/2023—Rev. 0 to Rev. A

Updated Outline Dimensions ... 14

2/2023—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = 3.3 V, negative supply voltage (V_{SS}) = −3.3 V, Control Input 1 voltage (V_1) and Control Input 2 voltage (V_2) = 0 V or V_{DD}, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4. V_{CTRL} is the voltages of the digital control inputs, V_1 and V_2.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		100		20,000	MHz
INSERTION LOSS						
Between RFC and RFx (On)		100 MHz to 6 GHz		0.9		dB
		6 GHz to 12 GHz		1.00		dB
		12 GHz to 20 GHz		1.20		dB
ISOLATION						
Between RFC and RFx		100 MHz to 6 GHz		56		dB
		6 GHz to 12 GHz		54		dB
		12 GHz to 20 GHz		47		dB
Between RFx and RFx		100 MHz to 6 GHz		54		dB
		6 GHz to 12 GHz		50		dB
		12 GHz to 20 GHz		47		dB
RETURN LOSS						
RFC (On)		100 MHz to 6 GHz		26		dB
		6 GHz to 12 GHz		22		dB
		12 GHz to 20 GHz		22		dB
RFx (On)		100 MHz to 6 GHz		24		dB
		6 GHz to 12 GHz		19		dB
		12 GHz to 20 GHz		18		dB
RFx (Off)		100 MHz to 6 GHz		20		dB
		6 GHz to 12 GHz		15		dB
		12 GHz to 20 GHz		12		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		12		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		55		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		80		ns
INPUT LINEARITY[1]						
0.1 dB Power Compression	P0.1dB	f = 100 MHz to 20 GHz		34		dBm
Third-Order Intercept	IP3	Two-tone input power = 15 dBm each tone, f = 100 MHz to 20 GHz, Δf = 1 MHz		55		dBm
Second-Order Intercept	IP2	Two-tone input power = 15 dBm each tone, f = 8 GHz, Δf = 1 MHz		110		dBm
VIDEO FEEDTHROUGH[2]				30		mV p-p
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			155		µA
Negative Supply Current	I_{SS}			530		µA
DIGITAL CONTROL INPUTS		V1, V2, EN, and LS pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}	V1 and V2 pins		3		µA
		LS and EN pins		40		µA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Power Handling[3]		f = 100 MHz to 20 GHz, T_{CASE} = 85°C[4]				
Through Path					33	dBm
Terminated Path					18	dBm
Hot Switching					30	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For input linearity performance over frequency, see Figure 22 to Figure 25.

[2] Video feedthrough is the peak transient measured at the RF ports in a 50 Ω test setup, without an RF signal present while switching the control voltage.

[3] For power derating over frequency, see Figure 2.

[4] For 105°C operation, the power handling degrades from the T_{CASE}= 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = 0 V, V_1 and V_2 = 0 V or V_{DD}, T_{CASE} = 25°C, and 50 Ω system, unless otherwise noted.

The small signal and bias characteristics are maintained for the single-supply operation.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		20,000	MHz
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		85		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		175		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		200		ns
INPUT LINEARITY						
0.1 dB Power Compression	P0.1dB	f = 100 MHz to 20 GHz		17		dBm
Third-Order Intercept	IP3	Two-tone input power = 15 dBm each tone, f = 100 MHz to 20 GHz, Δf = 1 MHz		42		dBm
Second-Order Intercept	IP2	Two-tone input power = 15 dBm each tone, f = 8 GHz, Δf = 1 MHz		86		dBm
RECOMMENDED OPERATING CONDITIONS						
RF Power Handling		f = 100 MHz to 20 GHz, T_{CASE} = 85°C				
Through Path					22	dBm
Terminated Path					12	dBm
Hot Switching					19	dBm
Case Temperature	T_{CASE}		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
V_{DD}	−0.3 V to +3.6 V
V_{SS}	−3.6 V to +0.3 V
Digital Control Inputs[1]	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[2]	
Dual Supply (V_{DD} = 3.3 V, V_{SS} = −3.3 V, frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	33.5 dBm
Terminated Path	18.5 dBm
Hot Switching (RFC)	30.5 dBm
Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, frequency = 100 MHz to 20 GHz, T_{CASE} = 85°C[3])	
Through Path	22.5 dBm
Terminated Path	12.5 dBm
Hot Switching (RFC)	19.5 dBm
Unbiased (V_{DD} = 0 V, V_{SS} = 0 V)	18 dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-24-16		
Through Path	110	°C/W
Terminated Path	200	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

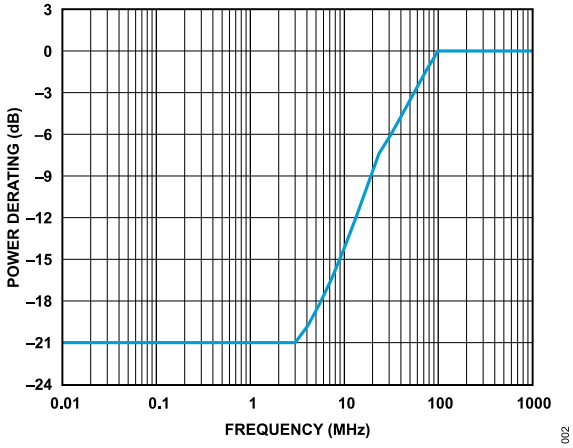

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADRF5050

Table 5. ADRF5050, 24-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM		
RFx and RFC Pins	1000	1C
Supply and Control Pins	2000	2
CDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

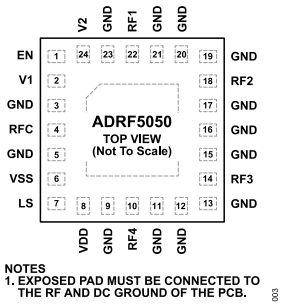

Figure 3. Pin Configuration (Top View)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN	Enable Input. See Table 7 for the truth table and Figure 6 for the interface schematic.
2	V1	Control Input 1. See Table 7 for the truth table and Figure 5 for the interface schematic.
3, 5, 9, 11 to 13, 15 to 17, 19 to 21, 23	GND	Ground. The GND pins must be connected to the RF and dc ground of the PCB.
4	RFC	RF Common Port. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
6	VSS	Negative Supply Voltage.
7	LS	Logic Select Input. See Table 7 for the truth table and Figure 6 for the interface schematic.
8	VDD	Positive Supply Voltage.
10	RF4	RF Throw Port 4. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
14	RF3	RF Throw Port 3. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
18	RF2	RF Throw Port 2. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
22	RF1	RF Throw Port 1. No dc blocking capacitor is required when the RF line potential is equal to 0 V dc. See Figure 4 for the interface schematic.
24	V2	Control Input 2. See Table 7 for the truth table and Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

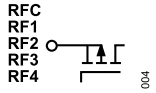

Figure 4. RFC and RF1 to RF4 Pin Interface Schematic

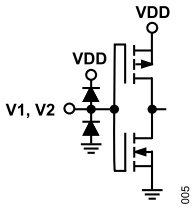

Figure 5. V1 and V2 Pin Interface Schematic

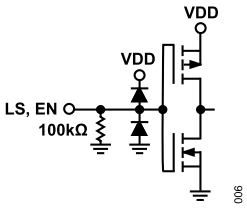

Figure 6. EN and LS Pin Interface Schematic

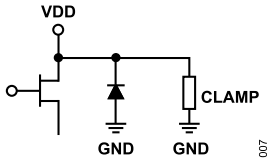

Figure 7. VDD Pin Interface Schematic

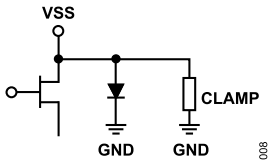

Figure 8. VSS Pin Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3 V, V_{SS} = −3.3 V, LS, EN, V_1, or V_2 = 0 V or V_{DD}, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

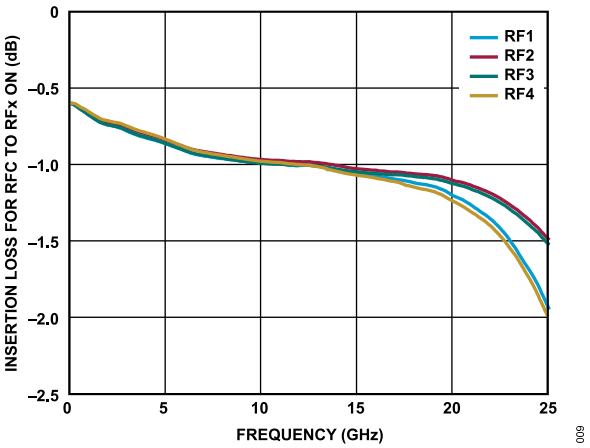

Figure 9. Insertion Loss for RFC to RFx On vs. Frequency

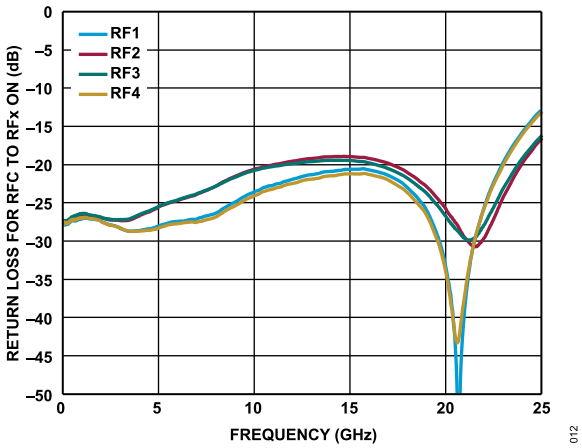

Figure 12. Return Loss for RFC to RFx Path On vs. Frequency

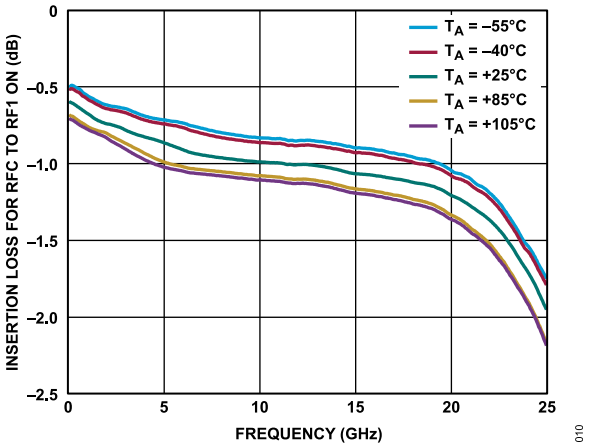

Figure 10. Insertion Loss for RFC to RF1 On vs. Frequency over Temperatures

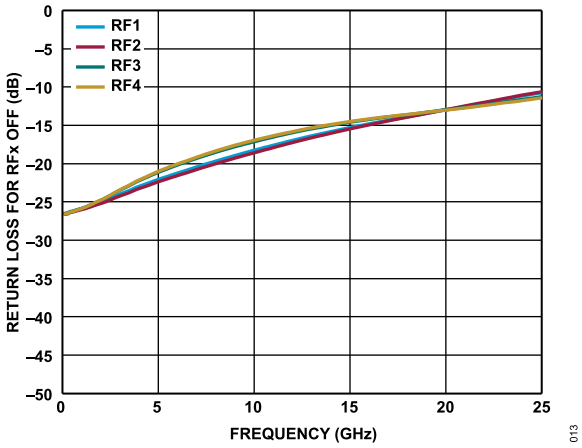

Figure 13. Return Loss for RFx Off vs. Frequency, RFC to RFx Path Off

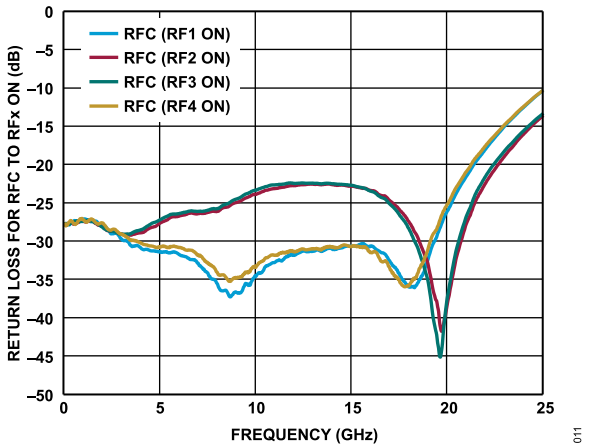

Figure 11. Return Loss for RFC to RFx Path On vs. Frequency

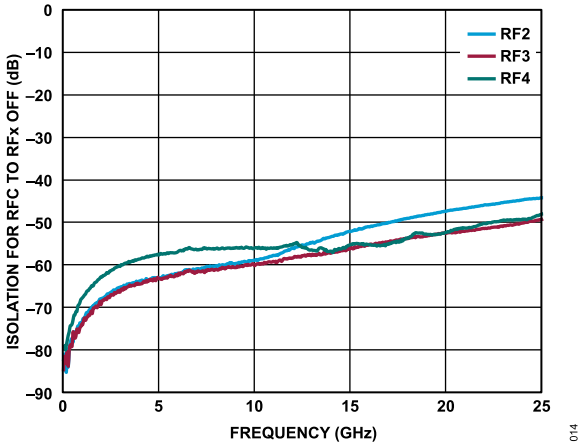

Figure 14. Isolation for RFC to RFx Off vs. Frequency, RFC to RF1 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

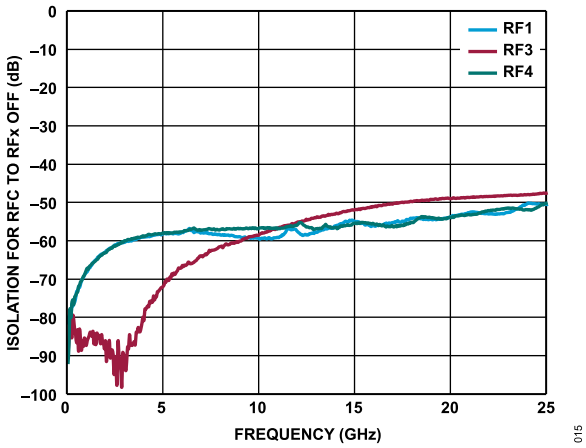

Figure 15. Isolation for RFC to RFx Off vs. Frequency, RFC to RF2 Path On

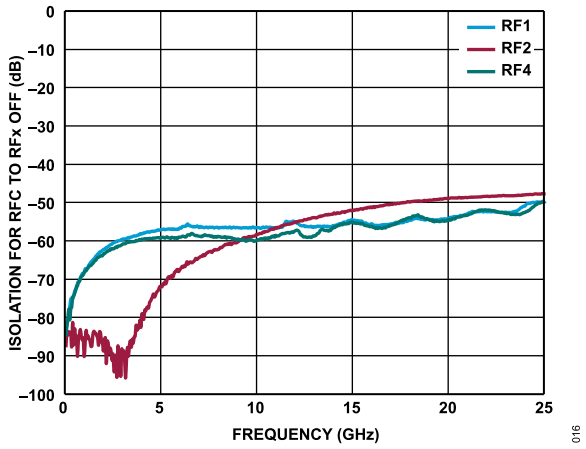

Figure 16. Isolation for RFC to RFx Off vs. Frequency, RFC to RF3 Path On

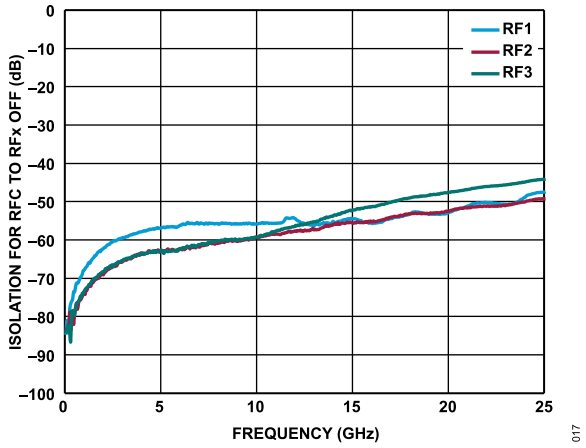

Figure 17. Isolation for RFC to RFx Off vs. Frequency, RFC to R4 Path On

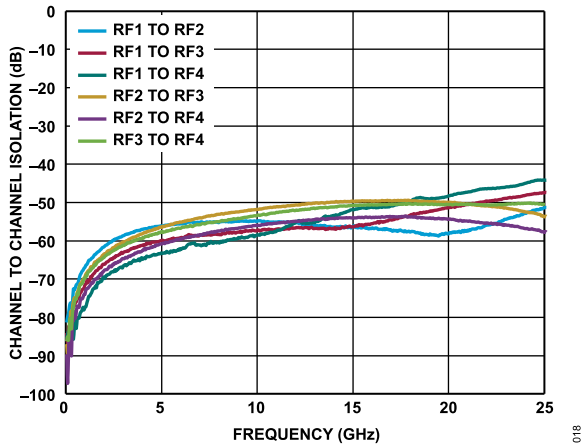

Figure 18. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path On

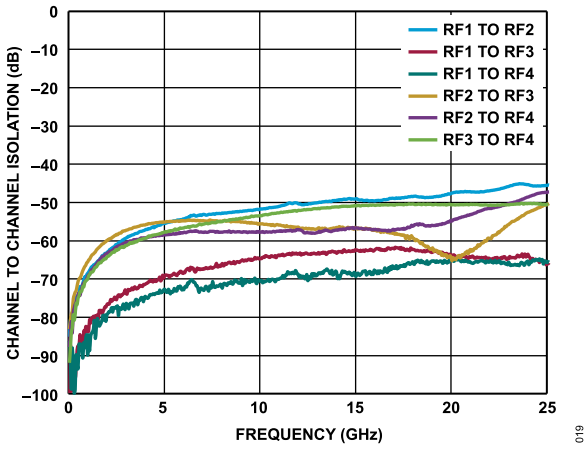

Figure 19. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path On

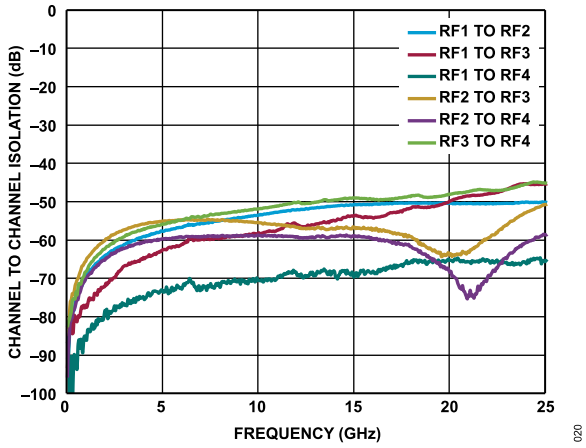

Figure 20. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

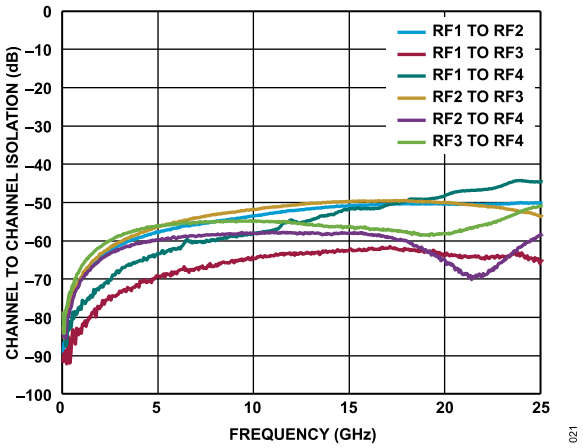

Figure 21. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path On

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3 V, V_{SS} = −3.3 V, LS, EN, V_1, or V_2 = 0 V or V_{DD}, and T_{CASE} = 25°C on a 50 Ω system, unless otherwise noted.

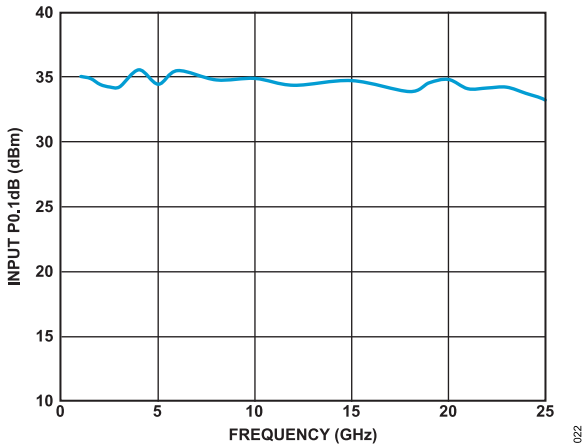

Figure 22. Input P0.1dB vs. Frequency

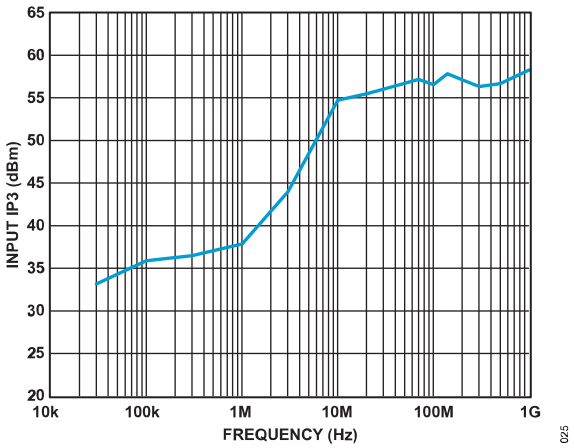

Figure 25. Input IP3 vs. Frequency, Low Frequency Detail

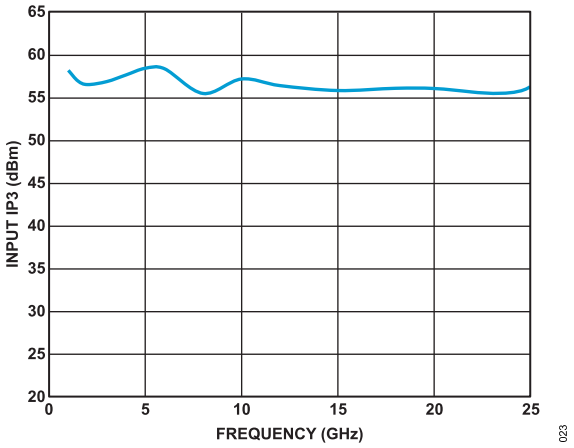

Figure 23. Input IP3 vs. Frequency

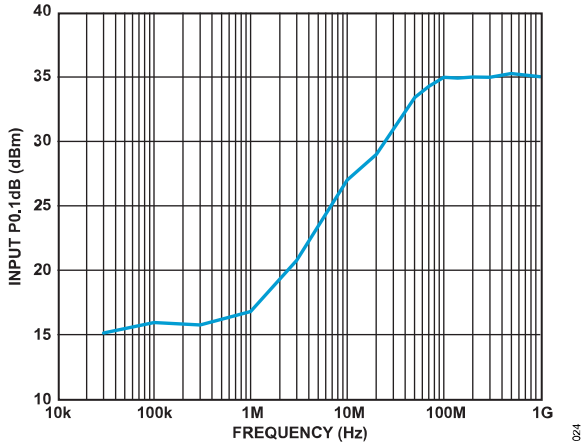

Figure 24. Input P0.1dB vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5050 integrates a driver to perform logic functions internally and to provide the user with the advantage of a simplified CMOS-/LVTTL-compatible control interface. The driver features four digital control input pins (EN, LS, V1, and V2) that control the state of the RFx paths. See Table 7.

The LS input allows the user to define the control input logic sequence for the RF path selections. The logic level applied to the V1 and V2 pins determines which RF port is in the insertion loss state while the other three paths are in the isolation state.

When the EN pin is logic high, all four RF paths are in isolation state regardless of the logic state of LS, V1, and V2. The RF ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1 to RF4) are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports that are terminated to internal 50 Ω resistors.

POWER SUPPLY

The ADRF5050 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin.

Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The ideal power-up sequence is as follows:

1. Connect GND to ground.
2. Power up VDD and VSS. Powering up VSS after VDD avoids current transients on VDD during ramp up.
3. Apply a control voltage to the digital control inputs (EN, LS, V1, and V2). Applying a control voltage to the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. Use a series 1 kΩ resistor to limit the current flowing into the control pin in such cases. If the control pins are not driven to a valid logic state (that is, the controller output is in a high impedance state) after VDD is powered up, it is recommended to use a pull-up or pull-down resistor.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

SINGLE-SUPPLY OPERATION

The ADRF5050 can operate with a single positive supply voltage applied to the VDD pin and VSS pin connected to ground. However, some performance degradations can occur in the input compression and input third-order intercept.

Table 7. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	LS	V1	V2	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

The ADRF5050 has two power supply pins (VDD and VSS) and four control pins (LS, EN, V1, and V2). Figure 26 shows the external components and connections for the supply and control pins. The supply and control pins are decoupled with 100 pF multilayer ceramic capacitor. Place the decoupling capacitors as close as possible to the ADRF5050. The device pinout allows the placement of the decoupling capacitors close to the ADRF5050. No other external components are needed for bias and operation, except DC blocking capacitors on the RFx pins when the RF lines are biased at a voltage different than 0 V. Refer to Pin Configuration and Function Descriptions section for details.

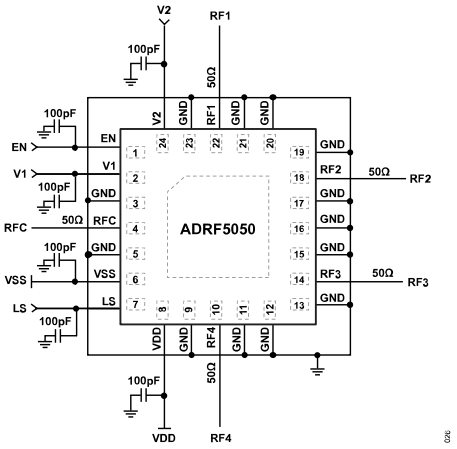

Figure 26. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50 Ω internally and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50 Ω characteristic impedance on the PCB. Figure 27 shows the referenced CPWG RF trace design for an RF substrate with 8 mil thick Rogers RO4003 dielectric material. RF trace with 14 mil width and 7 mil clearance is recommended for 1.5 mil finished copper thickness.

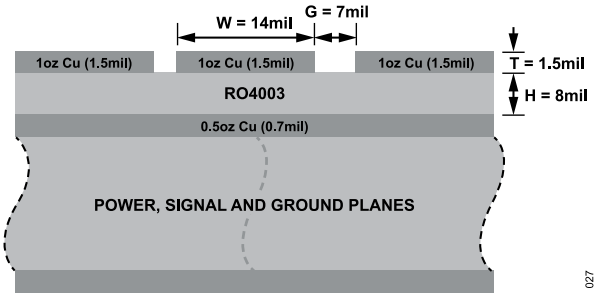

Figure 27. Example PCB Stack Up

Figure 28 shows the routing of the RF traces, supply, and control signals from the ADRF5050. The ground planes are connected with as many filled, through vias as allowed for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

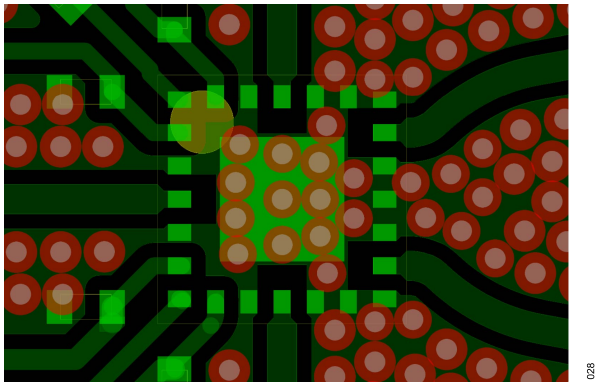

Figure 28. PCB Routings

Figure 29 shows the recommended layout from the device RF pins to the 50 Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width by 2 mils and tapered to RF trace with 45° angle. The paste mask is also designed to match the pad without any aperture reduction. The paste is divided into multiple openings for the paddle.

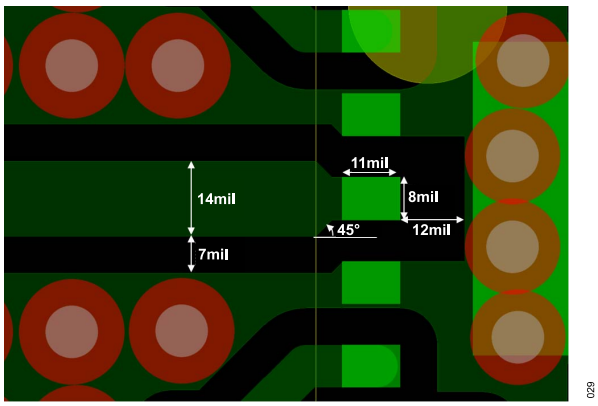

Figure 29. Recommended RF Pin Transitions

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Request for further recommendations.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
CC-24-16	LGA	24-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

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ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5050BCCZN	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-16
ADRF5050BCCZN-R7	-40°C to +105°C	24-Terminal Land Grid Array [LGA]	Reel, 500	CC-24-16

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADRF5050-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.