Data Sheet

ADPL54203

40V$_{IN}$ Micropower No-Opto Isolated Flyback Converter with 60V/3.4A Switch

FEATURES

- **3.4A, 60V Internal DMOS Power Switch**
- **3.2V to 40V Input Voltage Range**
- **No Transformer Third Winding or Opto-Isolator Required for Output Voltage Regulation**
- **Quasi-Resonant Boundary Mode Operation at Heavy Load**
- **Low Ripple Burst Mode® Operation at Light Load**
- **Low Quiescent Current**
  - **115µA in Sleep Mode**
  - **390µA in Active Mode**
- **Minimum Load < 0.5% (Typ) of Full Output**
- Temperature Compensation for Output Diode
- Internal Compensation and Soft-Start
- Output Short-Circuit Protection
- Accurate EN/UVLO Threshold and Hysteresis
- Thermally Enhanced 8-Lead SO Package

APPLICATIONS

- Isolated Auxiliary/Housekeeping Power Supplies
- Isolated Industrial, Medical Power Supplies

GENERAL DESCRIPTION

The ADPL54203 operates from an input voltage range of 3.2V to 40V and delivers up to 17W of isolated output power. It is a monolithic micropower isolated flyback converter. By sampling the isolated output voltage directly from the primary-side flyback waveform, the part requires no third winding or opto-isolator for regulation. The output voltage is programmed with two external resistors and a third optional temperature compensation resistor. Boundary mode operation provides a small magnetic solution with excellent load regulation. Low ripple Burst Mode operation maintains high efficiency at light load while minimizing the output voltage ripple.

A 3.4A, 60V DMOS power switch is integrated along with all the high voltage circuitry and control logic into a thermally enhanced 8-lead SO package. The high level of integration and the use of boundary and low ripple burst modes result in a simple to use, low component count, and high efficiency application solution for isolated power delivery.

SIMPLIFIED APPLICATION DIAGRAM

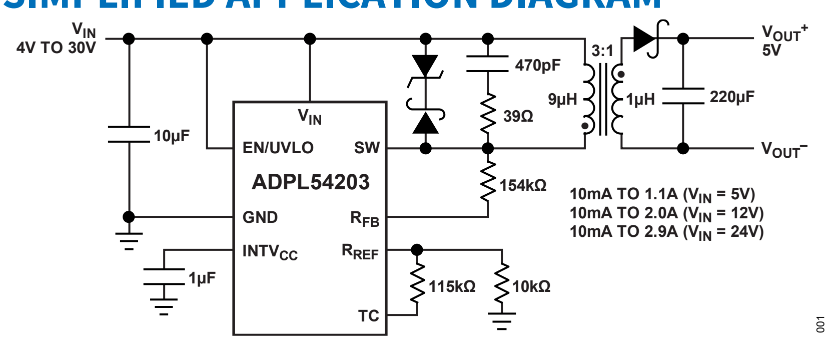

Figure 1. 4V to 30V$_{IN}$/5V$_{OUT}$ Isolated Flyback Converter

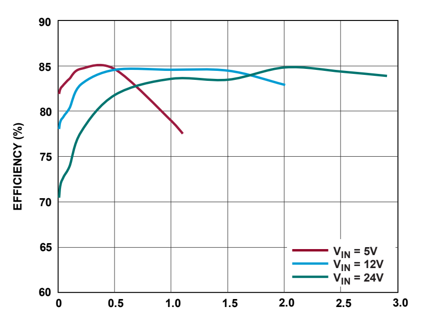

Figure 2. Efficiency vs. Load Current

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REVISION HISTORY

Nature of Change	Page Number
9/23 — Revision 0: Initial Version	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_A = 25°C. V_{IN} = 5V, $V_{EN/UVLO}$ = V_{IN}, C_{INTVCC} = 1µF to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{IN} Voltage Range	V_{IN}	−40°C ≤ T_J ≤ 125°C		3.2		40	V
V_{IN} Quiescent Current	I_Q	$V_{EN/UVLO}$ = 0.2V			0.5	2	µA
		$V_{EN/UVLO}$ = 1.1V			53		
		Sleep Mode (Switch Off)			115		
		Active Mode (Switch On)			390		
EN/UVLO Shutdown Threshold		For Lowest Off I_Q	−40°C ≤ T_J ≤ 125°C	0.2	0.75		V
EN/UVLO Enable Threshold		Falling	−40°C ≤ T_J ≤ 125°C	1.160	1.214	1.268	V
EN/UVLO Enable Hysteresis					14		mV
EN/UVLO Hysteresis Current	I_{HYS}	$V_{EN/UVLO}$ = 0.3V		−0.1	0	0.1	µA
		$V_{EN/UVLO}$ = 1.1V		2.3	2.5	2.7	
		$V_{EN/UVLO}$ = 1.3V		−0.1	0	0.1	
$INTV_{CC}$ Regulation Voltage	V_{INTVCC}	I_{INTVCC} = 0mA to 8mA		2.85	3	3.1	V
$INTV_{CC}$ Current Limit	I_{INTVCC}	V_{INTVCC} = 2.8V		8	13	20	mA
$INTV_{CC}$ UVLO Threshold		Falling		2.38	2.47	2.56	V
$INTV_{CC}$ UVLO Hysteresis					105		mV
(R_{FB} – V_{IN}) Voltage		I_{RFB} = 75µA to 125µA		−50		50	mV
R_{REF} Regulation Voltage		−40°C ≤ T_J ≤ 125°C		0.97	1.00	1.03	V
R_{REF} Regulation Voltage Line Regulation		3.2V ≤ VIN ≤ 40V		−0.01	0	0.01	%/V
TC Pin Voltage	V_{TC}				1.00		V
TC Pin Current	I_{TC}	V_{TC} = 1.2V		7	10	13	µA
		V_{TC} = 0.8V			−200		
Minimum Switching Frequency	f_{MIN}			11.3	12	12.7	kHz
Minimum Switch-On Time	$t_{ON(MIN)}$				160		ns
Maximum Switch-Off Time	$t_{OFF(MAX)}$	Backup Timer			170		µs
Maximum Switch Current Limit	$I_{SW(MAX)}$			3.4	4.5	5.6	A
Minimum Switch Current Limit	$I_{SW(MIN)}$			0.67	0.87	1.07	A

(Specifications are at T_A = 25°C. V_{IN} = 5V, $V_{EN/UVLO}$ = V_{IN}, C_{INTVCC} = 1µF to GND, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Switch On-Resistance	$R_{DS(ON)}$	I_{SW} = 1.5A		100		mΩ
Switch Leakage Current	I_{LKG}	V_{SW} = 60V		0.1	0.5	µA
Soft-Start Timer	t_{SS}			11		ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
SW[1]	60V
V_{IN}	40V
EN/UVLO	V_{IN}
R_{FB}	V_{IN} – 0.5V to V_{IN}
Current Into R_{FB}	200µA
$INTV_{CC}$, R_{REF}, TC	4V
Operating Junction Temperature Range[2, 3]	
ADPL54203	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

1 The SW pin is rated to 60V for transients. Depending on the leakage inductance voltage spike, operating waveforms of the SW pin should be derated to keep the flyback voltage spike below 60V as shown in *Figure 29*.

2 The ADPL54203 is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperature greater than 125°C.

3 The ADPL54203 includes overtemperature protection that is intended to protect the devices during momentary overload conditions. Overtemperature protection is active when the junction temperature exceeds 150°C. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

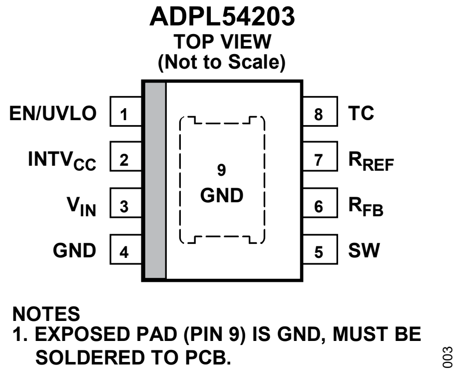

Figure 3. Pin Diagram

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	EN/UVLO	Enable/Undervoltage Lockout. The EN/UVLO pin is used to enable the ADPL54203. Pull the pin below 0.3V to shut down the ADPL54203. This pin has an accurate 1.214V threshold and can be used to program a V_{IN} undervoltage lockout (UVLO) threshold using a resistor divider from V_{IN} to ground. A 2.5µA current hysteresis allows the programming of V_{IN} UVLO hysteresis. If neither function is used, connect this pin directly to V_{IN}.
2	$INTV_{CC}$	Internal 3V Linear Regulator Output. The $INTV_{CC}$ pin is supplied from V_{IN} and powers the internal control circuitry and gate driver. Do not overdrive the $INTV_{CC}$ pin with any external supply, such as a third winding supply. Locally bypass this pin to ground with a minimum 1µF ceramic capacitor.
3	V_{IN}	Input Supply. The V_{IN} pin supplies current to the internal circuitry and serves as a reference voltage for the feedback circuitry connected to the R_{FB} pin. Locally bypass this pin to ground with a capacitor.
4, Exposed Pad 9	GND	Ground. The exposed pad provides both electrical contact to ground and good thermal contact to the printed circuit board. Solder the exposed pad directly to the ground plane.
5	SW	Drain of the Internal DMOS Power Switch. Minimize trace area at this pin to reduce EMI and voltage spikes.
6	R_{FB}	Input Pin for External Feedback Resistor. Connect a resistor from this pin to the transformer primary SW pin. The ratio of the R_{FB} resistor to the R_{REF} resistor, times the internal voltage reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). Minimize trace area at this pin.
7	R_{REF}	Input Pin for External Ground Referred Reference Resistor. The resistor at this pin should be in the range of 10k, but for convenience in selecting a resistor divider ratio, the value may range from 9.09k to 11.0k.
8	TC	Output Voltage Temperature Compensation. The voltage at this pin is proportional-to-absolute-temperature (PTAT) with temperature coefficient equal to 3.35mV/°K, that is, equal to 1V at room temperature 25°C. The TC pin voltage can be used to estimate the

		ADPL54203 junction temperature. Connect a resistor from this pin to the R_{REF} pin to compensate the output diode temperature coefficient.

BLOCK DIAGRAM

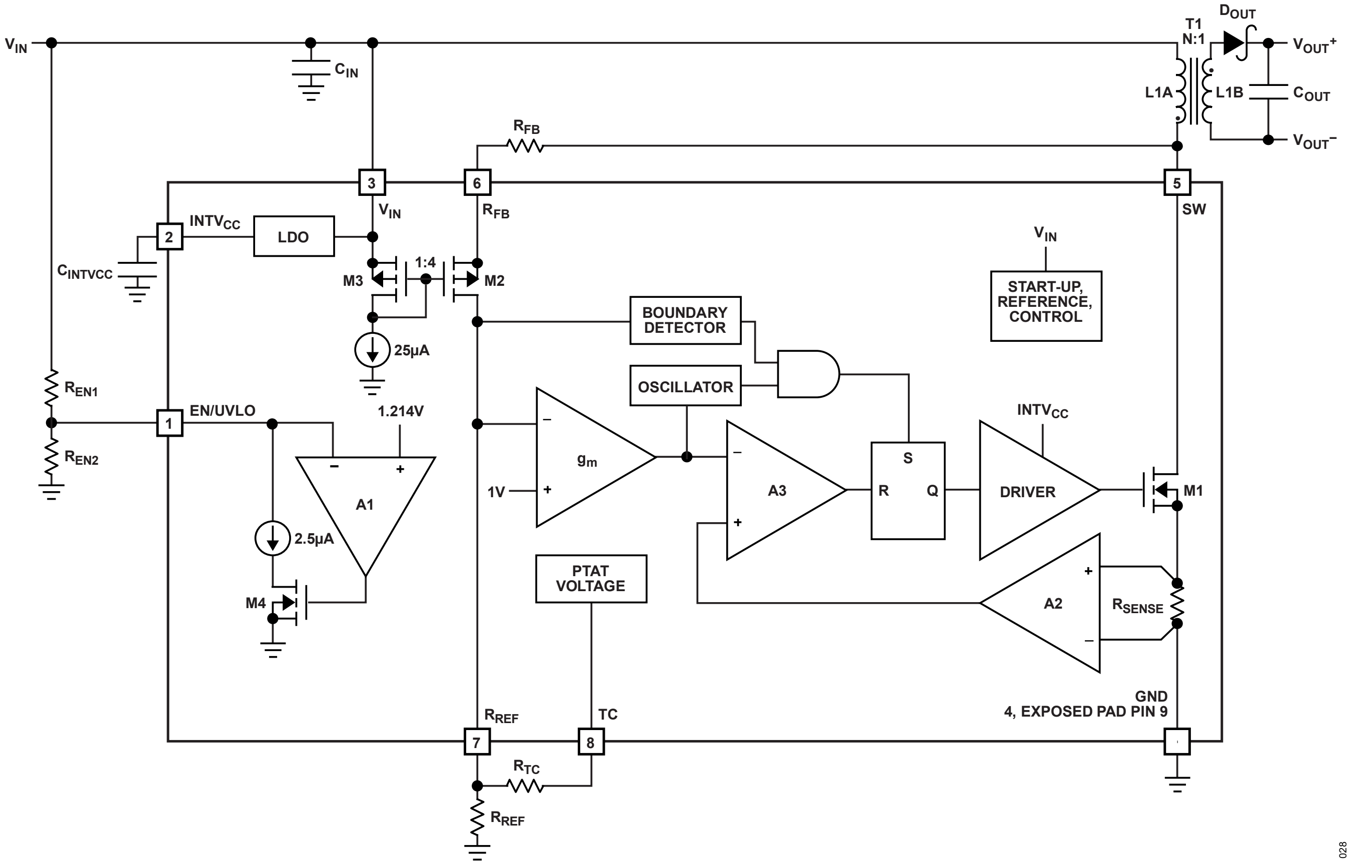

Figure 4. BLOCK DIAGRAM

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

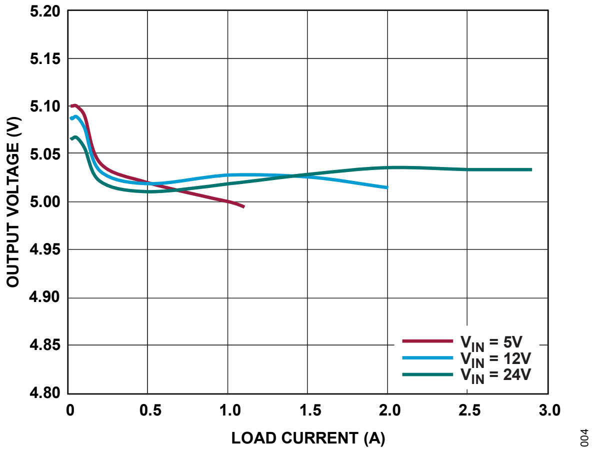

Figure 5. Output Load and Line Regulation

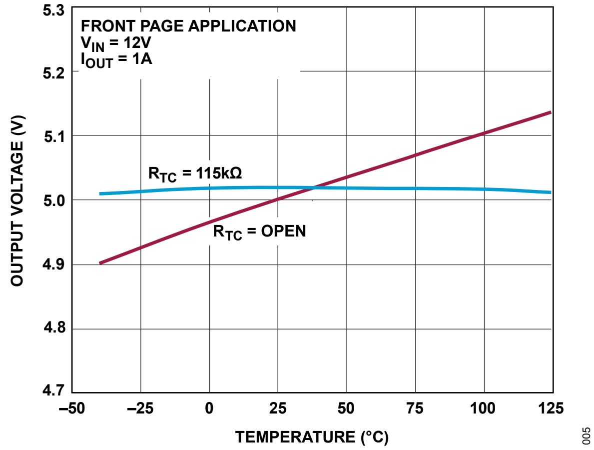

Figure 6. Output Temperature Variation

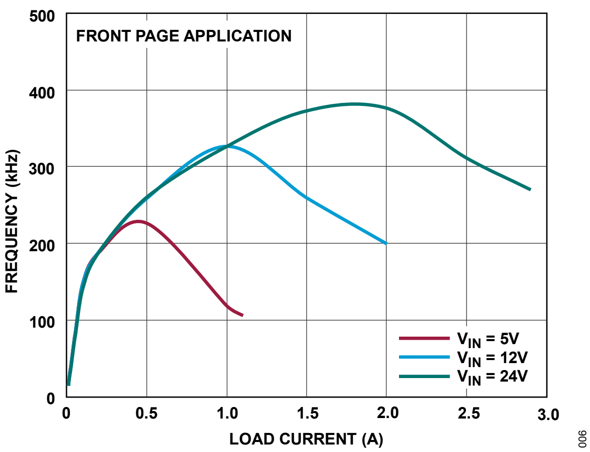

Figure 7. Switching Frequency vs. Load Current

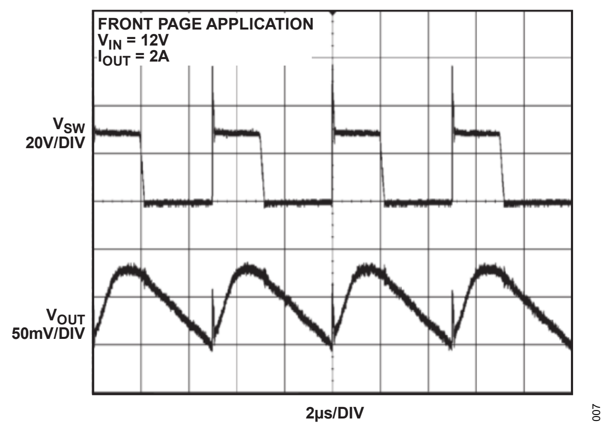

Figure 8. Boundary Mode Waveforms

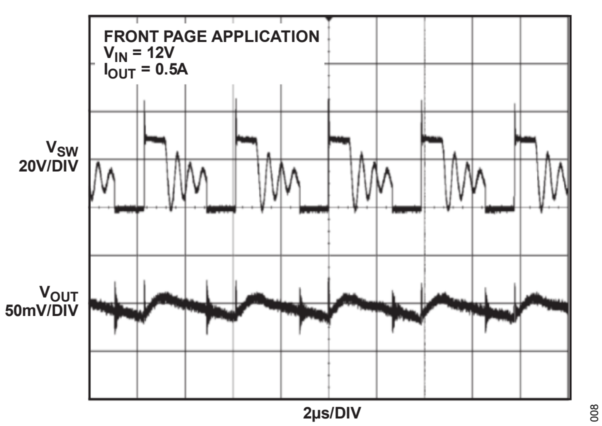

Figure 9. Discontinuous Mode Waveforms

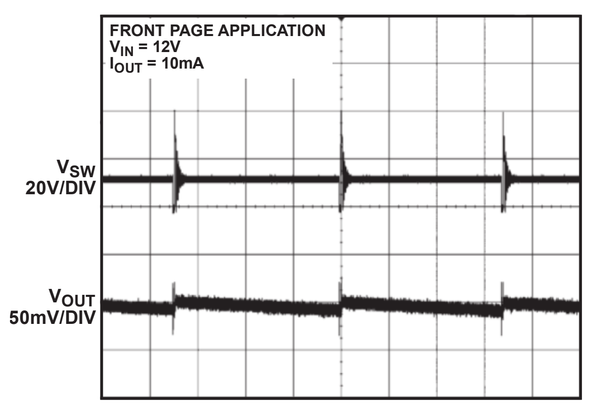

Figure 10. Burst Mode Waveforms

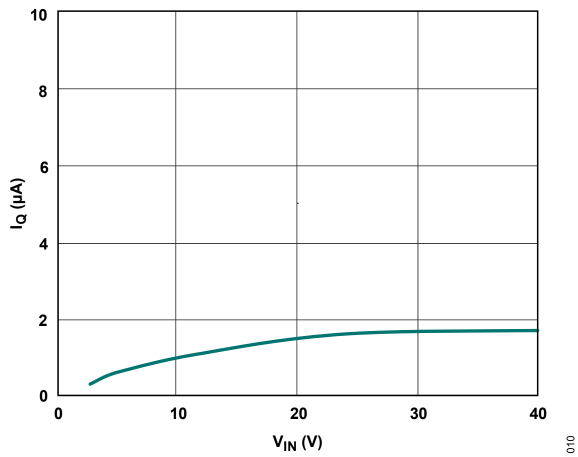

Figure 11. V_{IN} Shutdown Current

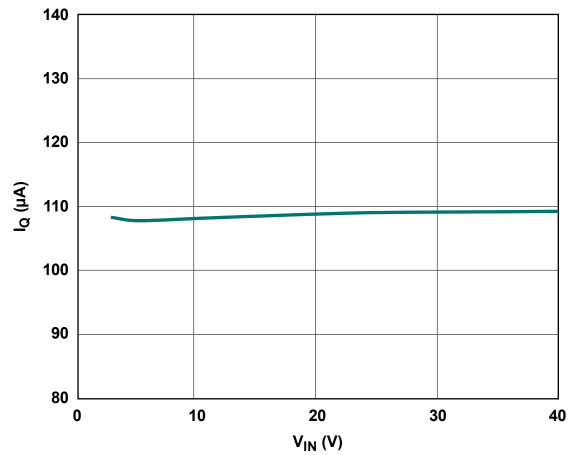

Figure 12. V_{IN} Quiescent Current, Sleep Mode

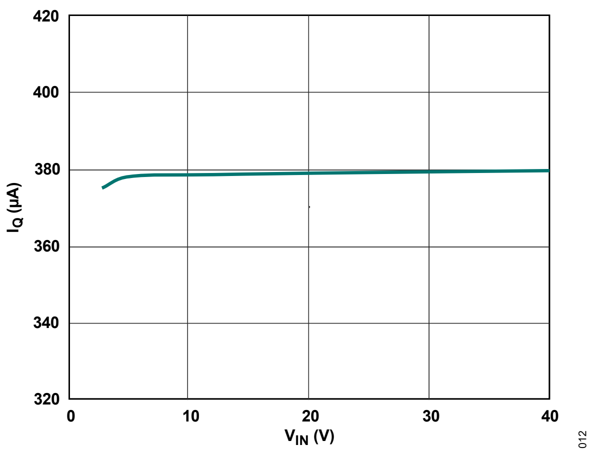

Figure 13. V_{IN} Quiescent Current, Active Mode

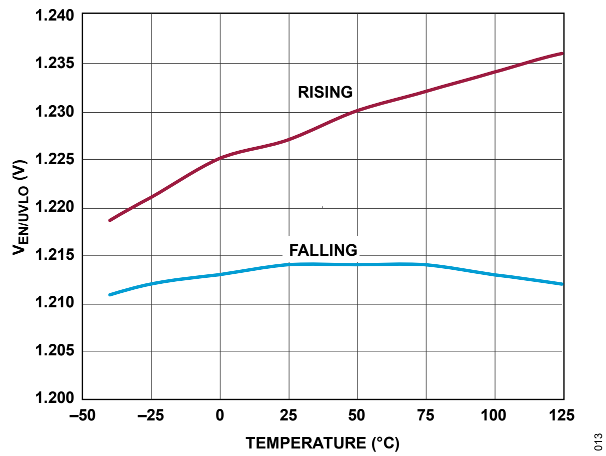

Figure 14. EN/UVLO Enable Threshold

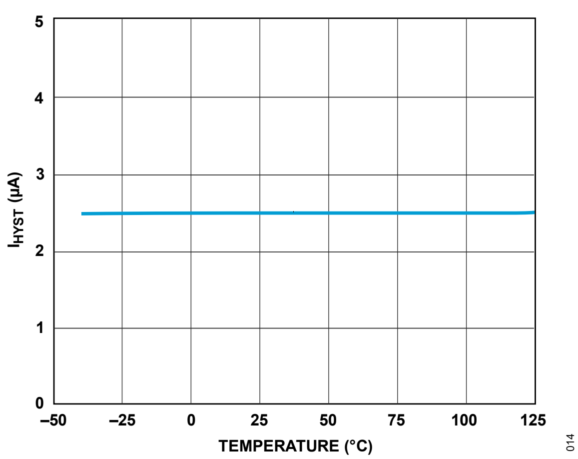

Figure 15. EN/UVLO Hysteresis Current

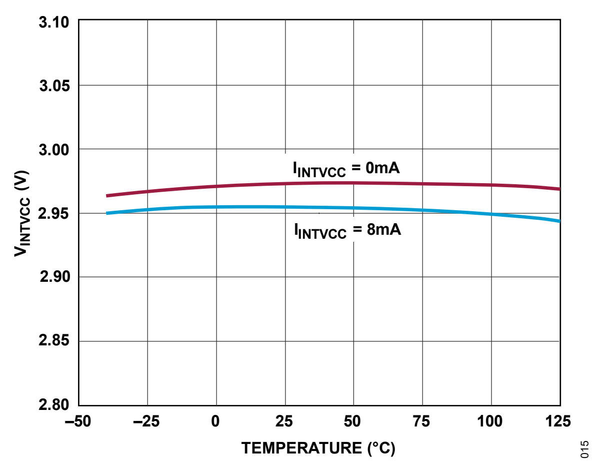

Figure 16. $INTV_{CC}$ Voltage vs. Temperature

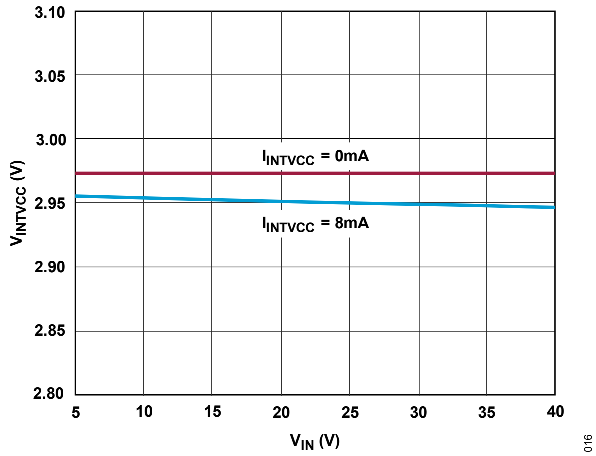

Figure 17. $INTV_{CC}$ Voltage vs. V_{IN}

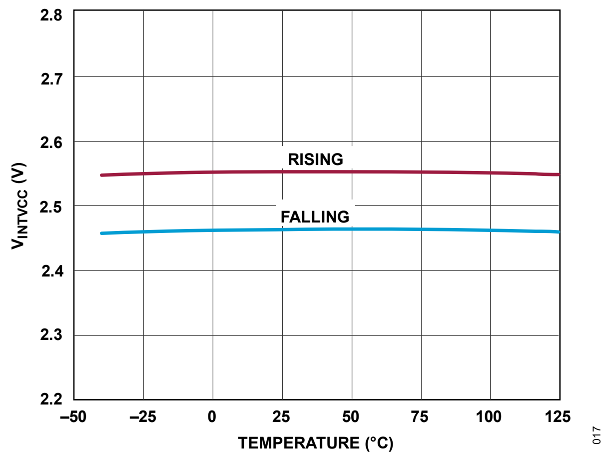

Figure 18. $INTV_{CC}$ UVLO Threshold

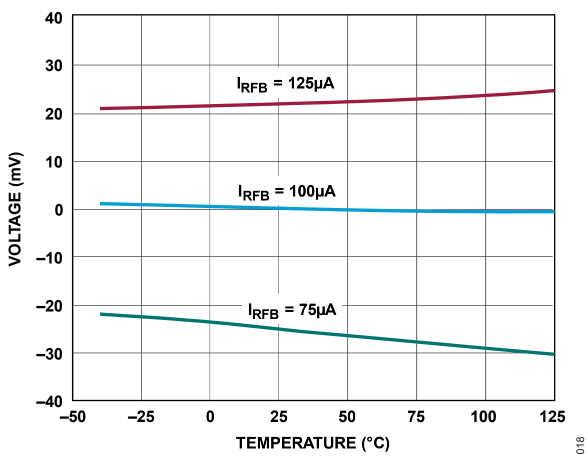

Figure 19. (R_{FB} - V_{IN}) Voltage

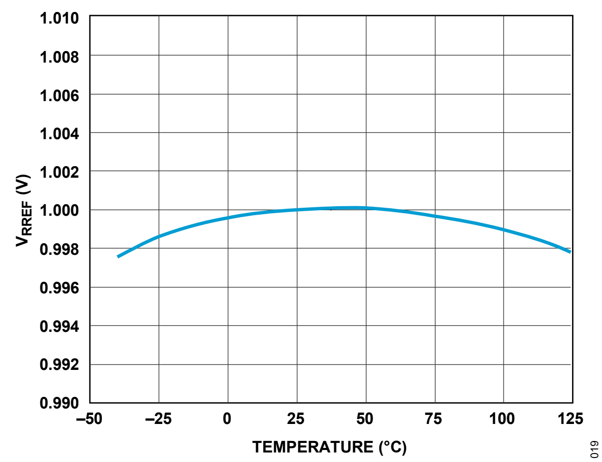

Figure 20. R_{REF} Regulation Voltage

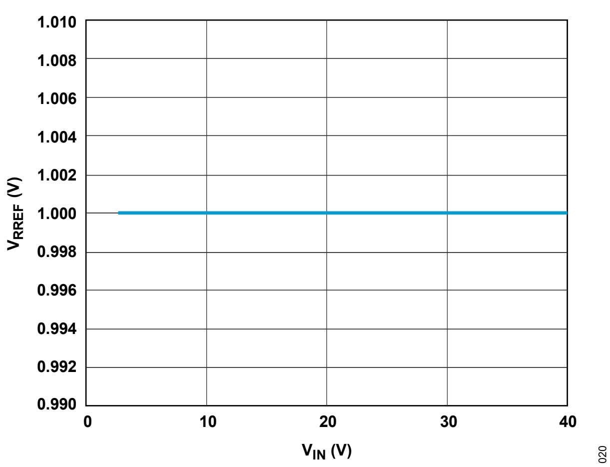

Figure 21. R_{REF} Line Regulation

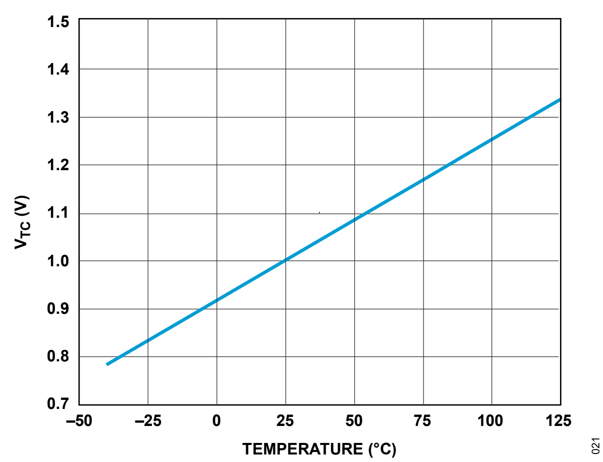

Figure 22. TC Pin Voltage

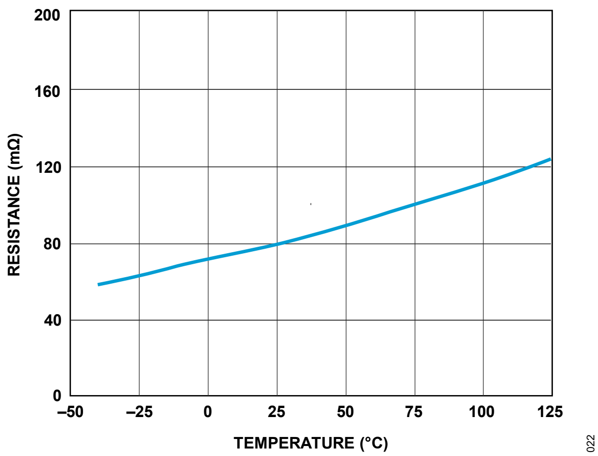

Figure 23. $R_{DS(ON)}$

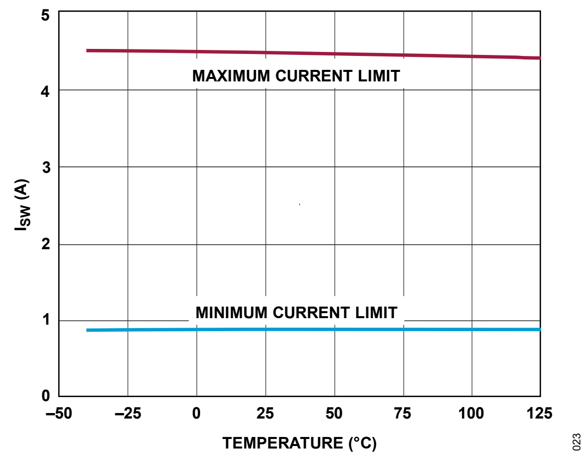

Figure 24. Switch Current Limit

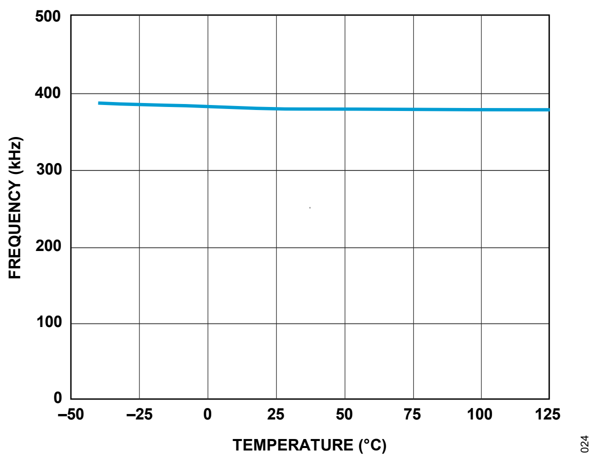

Figure 25. Maximum Switching Frequency

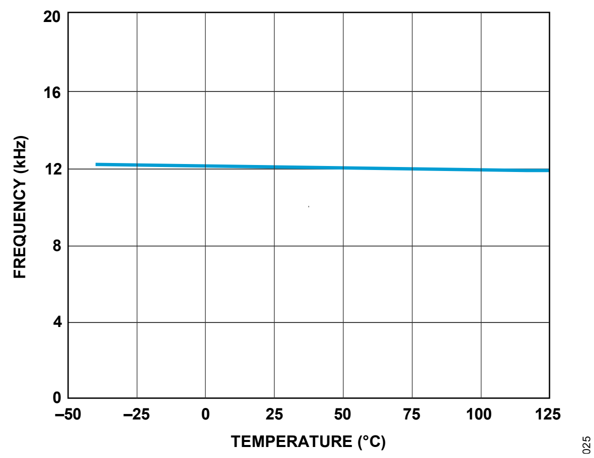

Figure 26. Minimum Switching Frequency

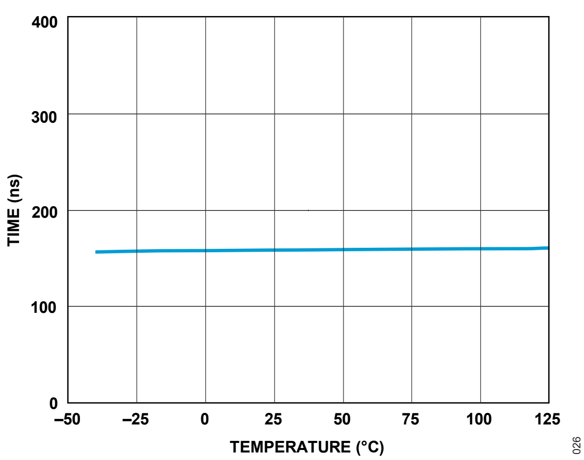

Figure 27. Minimum Switch-On Time

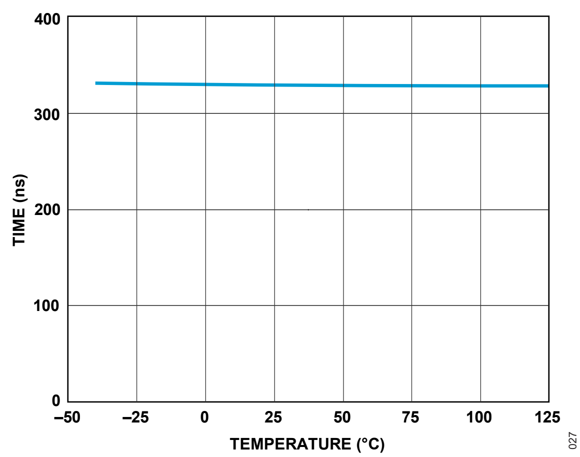

Figure 28. Minimum Switch-Off Time

THEORY OF OPERATION

The ADPL54203 is a current-mode switching regulator IC designed specially for the isolated flyback topology. The key problem in isolated topologies is how to communicate the output voltage information from the isolated secondary side of the transformer to the primary side for regulation. Historically, opto-isolators or extra transformer windings communicate this information across the isolation boundary. Opto-isolator circuits waste output power, and the extra components increase the cost and physical size of the power supply. Opto-isolators can also cause system issues due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over lifetime. Circuits employing extra transformer windings also exhibit deficiencies, as using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The ADPL54203 samples the isolated output voltage through the primary-side flyback pulse waveform. In this manner, neither opto-isolator nor extra transformer winding is required for regulation. Since the ADPL54203 operates in either boundary or discontinuous conduction mode, the output voltage is always sampled on the SW pin when the secondary current is zero. This method improves load regulation without the need of external load compensation components.

The ADPL54203 is a simple to use micropower isolated flyback converter housed in a thermally enhanced 8-lead SO package. The output voltage is programmed with two external resistors. An optional TC resistor provides easy output diode temperature compensation. By integrating the loop compensation and soft-start inside, the part reduces the number of external components. As shown in *Figure 4*, many of the blocks are similar to those found in traditional switching regulators including reference, regulators, oscillator, logic, current amplifier, current comparator, driver, and power switch. The novel sections include a flyback pulse sense circuit, a sample-and-hold error amplifier, and a boundary mode detector, as well as the additional logic for boundary conduction mode, discontinuous conduction mode, and low ripple Burst Mode operation.

Quasi-Resonant Boundary Mode Operation

The ADPL54203 features quasi-resonant boundary conduction mode operation at heavy load, where the chip turns on the primary power switch when the secondary current is zero and the SW rings to its valley. Boundary conduction mode is a variable frequency, variable peak-current switching scheme. The power switch turns on and the transformer primary current increases until an internally controlled peak current limit. After the power switch turns off, the voltage on the SW pin rises to the output voltage multiplied by the primary-to-secondary transformer turns ratio plus the input voltage. When the secondary current through the output diode falls to zero, the SW pin voltage collapses and rings around V_{IN}. A boundary mode detector senses this event and turns the power switch back on at its valley.

Boundary conduction mode returns the secondary current to zero every cycle, so parasitic resistive voltage drops do not cause load regulation errors. Boundary conduction mode also allows the use of smaller transformers compared to continuous conduction mode and does not exhibit subharmonic oscillation.

Discontinuous Conduction Mode Operation

As the load gets lighter, boundary conduction mode increases the switching frequency and decreases the switch peak current at the same ratio. Running at a higher switching frequency up to several MHz increases switching and gate charge losses. To avoid this scenario, the ADPL54203 has an additional internal oscillator, which clamps the maximum switching frequency to be less than 380kHz. Once the switching frequency hits the internal frequency clamp, the part starts to delay the switch turn-on and operates in discontinuous conduction mode.

Low Ripple Burst Mode Operation

Unlike traditional flyback converters, the ADPL54203 has to turn on and off at least for a minimum amount of time and with a minimum frequency to allow accurate sampling of the output voltage. The inherent minimum switch current limit and minimum switch-off time are necessary to guarantee the correct operation of specific applications.

As the load gets very light, the ADPL54203 starts to fold back the switching frequency while keeping the minimum switch current limit. So the load current is able to decrease while still allowing minimum switch-off time for the sample-and-hold error amplifier. Meanwhile, the part switches between sleep and active mode, therefore reducing the effective quiescent current to improve light load efficiency. In this condition, the ADPL54203 runs in low ripple Burst Mode operation. The typical 12kHz minimum switching frequency determines how often the output voltage is sampled and also the minimum load requirement

APPLICATIONS INFORMATION

Output Voltage

As shown in *Figure 4*, the R_{FB} and R_{REF} are external resistors used to program the output voltage. The ADPL54203 operates similarly to traditional current mode switchers, except in the use of a unique flyback pulse sense circuit and a sample-and-hold error amplifier, which sample and therefore regulate the isolated output voltage from the flyback pulse.

Operation is as follows: when the power switch M1 turns off, the SW pin voltage rises above the V_{IN} supply. The amplitude of the flyback pulse, that is, the difference between the SW pin voltage and V_{IN} supply, is given as:

$$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \times ESR) \times N_{PS}$$

$$V_F = \text{Output diode forward voltage}$$

$$I_{SEC} = \text{Transformer secondary current}$$

$$ESR = \text{Total impedance of secondary circuit}$$

$$N_{PS} = \text{Transformer effective primary} - \text{to} - \text{secondary turns ratio}$$

The flyback voltage is then converted to a current, I_{RFB}, by the R_{FB} resistor and the flyback pulse sense circuit (M2 and M3). This current, I_{RFB}, also flows through the R_{REF} resistor to generate a ground-referred voltage. The resulting voltage feeds to the inverting input of the sample-and-hold error amplifier. Since the sample-and-hold error amplifier samples the voltage when the secondary current is zero, the (I_{SEC} × ESR) term in the V_{FLBK} equation can be assumed to be zero.

The internal reference voltage, V_{REF}, 1.00V, feeds to the noninverting input of the sample-and-hold error amplifier. The relatively high gain in the overall loop causes the voltage at the R_{REF} pin to be nearly equal to the internal reference voltage V_{REF}. The resulting relationship between V_{FLBK} and V_{REF} can be expressed as:

$$\left(\frac{V_{FLBK}}{R_{FB}}\right) \times R_{REF} = V_{REF}$$

$$V_{FLBK} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}}\right)$$

V_{REF} = Internal reference voltage 1.00V

Combination with the previous V_{FLBK} equation yields an equation for V_{OUT}, in terms of the R_{FB} and R_{REF} resistors, transformer turns ratio, and diode forward voltage:

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}}\right) \times \left(\frac{1}{N_{PS}}\right) - V_F$$

Output Temperature Compensation

The first term in the V_{OUT} equation does not have temperature dependence, but the output diode forward voltage, V_F, has a significant negative temperature coefficient (–1mV/°C to –2mV/°C). Such a negative temperature coefficient produces approximately 200mV to 300mV voltage variation on the output voltage across temperature.

For higher voltage outputs, such as 12V and 24V, the output diode temperature coefficient has a negligible effect on the output voltage regulation. For lower voltage outputs, such as 3.3V and 5V, however, the output diode temperature coefficient does count for an extra 2% to 5% output voltage regulation.

The ADPL54203 junction temperature usually tracks the output diode junction temperature to the first sequence. To compensate the negative temperature coefficient of the output diode, a resistor, R_{TC}, connected between the TC and R_{REF} pins generates a PTAT current. The PTAT current is zero at 25°C, flows into the R_{REF} pin at hot temperature, and flows out of the R_{REF} pin at cold temperature. With the R_{TC} resistor in place, the output voltage equation is revised as follows:

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}}\right) \times \left(\frac{1}{N_{PS}}\right) - V_F\ (TO) - (\delta V_{TC}/\delta T) \times$$

$$(T - TO) \times (\frac{R_{FB}}{R_{TC}}) \times (\frac{1}{N_{PS}})\ - (\delta V_F/\delta T) \times (T - TO)$$

$$TO = \text{Room temperature } 25°C$$

$$(\delta VF/\delta T)\ =\ \text{Output diode forward voltage temperature coefficient}$$

$$(\delta VTC/\delta T) = 3.35mV/C$$

To cancel the output diode temperature coefficient, the following two equations should be satisfied:

$$V_{OUT} = V_{REF} \times \left(\frac{R_{FB}}{R_{REF}}\right) \times \left(\frac{1}{N_{PS}}\right) - V_F\ (TO)$$

$$(\delta V_{TC}/\delta T) \times (\frac{R_{FB}}{R_{TC}}) \times (\frac{1}{N_{PS}}) = -(\delta V_F/\delta T)$$

Selecting Actual R_{REF}, R_{FB}, R_{TC} Resistor Values

The ADPL54203 uses a unique sampling scheme to regulate the isolated output voltage. Due to the sampling nature, the scheme contains repeatable delays and error sources, which affects the output voltage and force a re-evaluation of the R_{FB} and R_{TC} resistor values. Therefore, a simple 2-step sequential process is recommended for selecting resistor values.

Rearrangement of the expression for VOUT in the previous sections yields the starting value for R_{FB}:

$$R_{FB} = \frac{R_{REF} \times N_{PS} \times (V_{OUT} + V_F\ (TO))}{V_{REF}}$$

$$V_{OUT} = \text{Output voltage}$$

$$V_F(TO) = \text{Output diode forward voltage at } 25°C = \sim 0.3V$$

$$N_{PS} = \text{Transformer effective primary} - \text{to} - \text{secondary turns ratio}$$

The equation shows that the R_{FB} resistor value is independent of the R_{TC} resistor value. Any R_{TC} resistor connected between the TC and R_{REF} pins has no effect on the output voltage setting at 25°C because the TC pin voltage is equal to the R_{REF} regulation voltage at 25°C.

The R_{REF} resistor value should be approximately 10k because the ADPL54203 is trimmed and specified using this value. If the R_{REF} resistor value varies considerably from 10k, additional errors occur. However, a variation in R_{REF} up to 10% is acceptable. This yields a bit of freedom in selecting standard 1% resistor values to yield nominal R_{FB}/R_{REF}. First, build and power up the application with the starting R_{REF}, R_{FB} values (no R_{TC} resistor yet) and other components connected, and measure the regulated output voltage, $V_{OUT(MEAS)}$. The new R_{FB} value can be adjusted to:

$$R_{FB(NEW)} = \frac{V_{OUT}}{V_{OUT(MEAS)}} \times R_{FB}$$

Second, with a new R_{FB} resistor value selected, the output diode temperature coefficient in the application can be tested to determine the R_{TC} value. Still without the R_{TC} resistor, the V_{OUT} should be measured over temperature at a required target output load. It is very important for this evaluation that uniform temperature be applied to both the output diode and the ADPL54203. If freeze spray or a heat gun is used, there can be a significant mismatch in temperature between the two devices that causes significant error. Attempting to derive the data from a diode data sheet is another option if there is no method to apply uniform heating or cooling such as an oven. With at least two data points spreading across the operating temperature range, the output diode temperature coefficient can be determined by:

$$-(\delta V_F/\delta T) = \frac{V_{OUT}\,(T1) - V_{OUT}\,(T2)}{T1 - T2}$$

Using the measured output diode temperature coefficient, an exact R_{TC} value can be selected with the following equation:

$$R_{TC} = \frac{(\delta V_{TC}/\delta T)}{-(\delta V_F/\delta T)} \times (\frac{R_{FB}}{N_{PS}})$$

Once the R_{REF}, R_{FB}, and R_{TC} values are selected, the regulation accuracy from board-to-board for a given application is very consistent, typically under ±5% when including device variation of all the components in the system (assuming resistor tolerances and transformer windings matching within ±1%). However, if the transformer or the output diode is changed, or the layout is dramatically altered, there may be some change in $V_{OUT.}$

Output Power

A flyback converter has a complicated relationship between the input and output currents compared to a buck or a boost converter. A boost converter has a relatively constant maximum input current regardless of input voltage and a buck converter has a relatively constant maximum output current regardless of input voltage. This is due to the continuous nonswitching behavior of the two currents. A flyback converter has both discontinuous input and output currents which make it similar to a nonisolated buckboost converter. The duty cycle affects the input and output currents, which makes it hard to predict output power. In addition, the winding ratio can be changed to multiply the output current at the expense of a higher switch voltage.

The equations below calculate output power:

$$P_{OUT} = \eta \times V_{IN} \times D \times I_{SW(MAX)} \times 0.5$$

$$\eta = \text{Efficiency} = {\sim}85\%$$

$$D = \text{Duty Cycle} = \frac{(V_{OUT} + V_F) \times N_{PS}}{(V_{OUT} + V_F) \times N_{PS} + V_{IN}}$$

$$I_{SW(MAX)} = \text{Maximum switch current limit} = 3.4\text{A(MIN)}$$

Primary Inductance Requirement

The ADPL54203 obtains output voltage information from the reflected output voltage on the SW pin. The conduction of secondary current reflects the output voltage on the primary SW pin. The sample-and-hold error amplifier needs a minimum 350ns to settle and sample the reflected output voltage. To ensure proper sampling, the secondary winding needs to conduct current for a minimum of 350ns. The following equation gives the minimum value for primary-side magnetizing inductance:

$$L_{PRI} = \frac{t_{OFF(MIN)} \times N_{PS} \times (V_{OUT} + V_F)}{I_{SW(MIN)}}$$

$$t_{OFF(MIN)} = \text{Minimum switch} - \text{off time} = 350\text{ns}(\text{TYP})$$

$$I_{SW(MIN)} = \text{Minimum switch current limit} = 0.87\text{A}(\text{TYP})$$

In addition to the primary inductance requirement for the minimum switch-off time, the ADPL54203 has minimum switch-on time that prevents the chip from turning on the power switch shorter than approximately 160ns. This minimum switch-on time is mainly for leading-edge blanking the initial switch turn-on current spike. If the inductor current exceeds the required current limit during that time, oscillation may occur at the output as the current control loop loses its ability to regulate. Therefore, the following equation relating to maximum input voltage must also be followed in selecting primary-side magnetizing inductance:

$$L_{PRI} \geq \frac{t_{ON(MIN)} \times V_{IN(MAX)}}{I_{SW(MIN)}}$$

$$t_{ON(MIN)} = \text{Minimum switch} - \text{on time} = 160\text{ns}(\text{TYP})$$

In general, choose a transformer with its primary magnetizing inductance about 40% to 60% larger than the minimum values calculated above. A transformer with much larger inductance have a bigger physical size and may cause instability at light load.

Selecting a Transformer

Transformer specification and design is perhaps the most critical part of successfully applying the ADPL54203. In addition to the usual list of guidelines dealing with high frequency isolated power supply transformer design, the following information should be carefully considered.

Analog Devices has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the ADPL54203. *Table 4* shows the details of these transformers.

Table 4. Predesigned Transformers – Typical Specifications

TRANSFORMER PART NUMBER	DIMENSIONS (W × L × H) (mm)	L_{PRI} (µH)	L_{LKG} (µH)	N_P:N_S	R_{PRI} (mΩ)	R_{SEC} (mΩ)	VENDOR	TARGET APPLICATION		
								V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)
750311625	17.75 × 13.46 × 12.70	9	0.35	4:1	43	6	Wurth Elektronik	8 to 32	3.3	2.1
750311564	17.75 × 13.46 × 12.70	9	0.12	3:1	36	7	Wurth Elektronik	8 to 32	5	1.5
750313441	15.24 × 13.34 × 11.43	9	0.6	2:1	75	18	Wurth Elektronik	8 to 32	5	1.3
750311624	17.75 × 13.46 × 12.70	9	0.18	3:2	34	21	Wurth Elektronik	8 to 32	8	0.9
12387-TO79	15.5 × 12.5 × 11.5	9	0.5	1:1:1	55	90	Sumida	8 to 36	±12	0.3
750313445	15.24 × 13.34 × 11.43	9	0.25	1:2	85	190	Wurth Elektronik	8 to 36	24	0.3
750313457	15.24 × 13.34 × 11.43	9	0.25	1:4	85	770	Wurth Elektronik	8 to 36	48	0.15
750313460	15.24 × 13.34 × 11.43	12	0.7	4:1	85	11	Wurth Elektronik	4 to 18	5	0.9
750311342	15.24 × 13.34 × 11.43	15	0.44	2:1	85	22	Wurth Elektronik	4 to 18	12	0.4
750313439	15.24 × 13.34 × 11.43	12	0.6	2:1	115	28	Wurth Elektronik	18 to 42	3.3	2.1
750313442	15.24 × 13.34 × 11.43	12	0.75	3:2	150	53	Wurth Elektronik	18 to 42	5	1.6

Turns Ratio

Note that when choosing an R_{FB}/R_{REF} resistor ratio to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application. In contrast, the use of simple ratios of small integers, for example, 3:1, 2:1, and 1:1, provides more freedom in settling total turns and mutual inductance.

Typically, choose the transformer turns ratio to maximize available output power. For low output voltages (3.3V or 5V), a N:1 turns ratio can be used with multiple primary windings relative to the secondary to maximize the transformer's current gain (and output power). However, remember that the SW pin sees a voltage that is equal to the maximum input supply voltage plus the output voltage multiplied by the turns ratio. In addition, leakage inductance causes a voltage spike ($V_{LEAKAGE}$) on top of this reflected voltage. This total quantity needs to remain below the 60V absolute maximum rating of the SW pin to prevent breakdown of the internal power switch. Together these conditions place an upper limit on the turns ratio, N_{PS}, for a given application. Choose a turns ratio low enough to ensure:

$$N_{PS} \leq \frac{60V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

For larger N:1 values, choose a transformer with a larger physical size to deliver additional current. In addition, choose a large enough inductance value to ensure that the switch-off time is long enough to accurately sample the output voltage.

For lower output power levels, choose a 1:1 or 1:N transformer for the absolute smallest transformer size. A 1:N transformer minimizes the magnetizing inductance (and minimize size), but also limits the available output power. A higher 1:N turns ratio makes it possible to have very high output voltages without exceeding the breakdown voltage of the internal power switch.

The turns ratio is an important element in the isolated feedback scheme, and directly affects the output voltage accuracy. Make sure that the transformer manufacturer specifies turns ratio accuracy within ±1%.

Saturation Current

The current in the transformer windings should not exceed its rated saturation current. Energy injected once the core is saturated is not transferred to the secondary and instead dissipated in the core. When designing custom transformers to be used with the ADPL54203, the saturation current should always be specified by the transformer manufacturers.

Winding Resistance

Resistance in either the primary or secondary windings reduces overall power efficiency. Good output voltage regulation is maintained independent of winding resistance due to the boundary/discontinuous conduction mode operation of the ADPL54203.

Leakage Inductance and Snubbers

Transformer leakage inductance on either the primary or secondary causes a voltage spike to appear on the primary after the power switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. It is very important to minimize transformer leakage inductance.

When designing an application, adequate margin should be kept for the worst-case leakage voltage spikes even under overload conditions. In most cases shown in *Figure 29*, the reflected output voltage on the primary plus V_{IN} should be kept below 45V. This leaves at least 15V margin for the leakage spike across line and load conditions. A larger voltage margin is required for poorly wound transformers or for excessive leakage inductance.

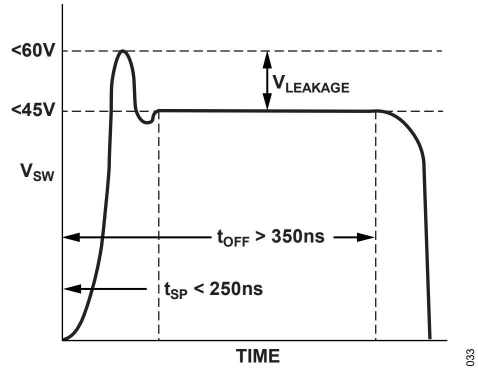

Figure 29. Maximum Voltages for SW Pin Flyback Waveform

In addition to the voltage spikes, the leakage inductance also causes the SW pin ringing for a while after the power switch turns off. To prevent the voltage ringing falsely trigger boundary mode detector, the ADPL54203 internally blanks the boundary mode detector for approximately 250ns. Any remaining voltage ringing after 250ns may turn the power switch back on again before the secondary current falls to zero. In this case, the ADPL54203 enters continuous conduction mode. So the leakage inductance spike ringing should be limited to less than 250ns.

To clamp and damp the leakage voltage spikes, a (RC + DZ) snubber circuit shown in Figure 30 is recommended. The RC (resistor-capacitor) snubber quickly damps the voltage spike ringing and provides great load regulation and EMI performance. And the DZ (diode-Zener) ensures well defined and consistent clamping voltage to protect SW pin from exceeding its 60V absolute maximum rating.

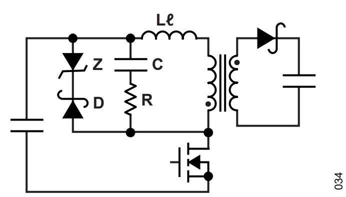

Figure 30. (RC + DZ) Snubber Circuit

The recommended approach for designing an RC snubber is to measure the period of the ringing on the SW pin when the power switch turns off without the snubber and then add capacitance until the period of the ringing is 1.5 to 2 times longer. The change in period determines the value of the parasitic capacitance, from which the parasitic inductance can be also determined from the initial period. Once the value of the SW node capacitance and inductance is known, a series resistor can be added to the snubber capacitance to dissipate power and critically damp the ringing. The equation for deriving the optimal series resistance using the observed periods (t_{PERIOD} and $t_{PERIOD(SNUBBED)}$) and snubber capacitance ($C_{SNUBBER}$) is:

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{T_{PERIOD}{}^2}{C_{PAR} \times 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

Note that energy absorbed by the RC snubber will be converted to heat and will not be delivered to the load. In high voltage or high current applications, the snubber needs to be sized for thermal dissipation. A 470pF capacitor in series with a 39Ω resistor is a good starting point.

For the DZ snubber, proper care should be taken when choosing both the diode and the Zener diode. Schottky diodes are typically the best choice, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. Choose a diode that has a reverse-voltage rating higher than the maximum SW pin voltage. The Zener diode breakdown voltage should be chosen to balance power loss and switch voltage protection. The best compromise is to choose the largest voltage breakdown with 5V margin. Use the following equation to make the proper choice:

$$V_{ZENER(MAX)} \leq 55V - V_{IN(MAX)}$$

For an application with a maximum input voltage of 32V, choose a 24V Zener diode, the $V_{ZENER(MAX)}$ of which is around 26V and below the 28V maximum. The power loss in the DZ snubber determines the power rating of the Zener diode. A 1.5W Zener diode is typically recommended.

Undervoltage Lockout (UVLO)

A resistive divider from V_{IN} to the EN/UVLO pin implements UVLO. The EN/UVLO enable falling threshold is set at 1.214V with 14mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.214V. This current provides user programmable hysteresis based on the value of R1. The programmable UVLO thresholds are:

$$V_{IN(UVLO^+)} = \frac{1.228V \times (R1 + R2)}{R2} + 2.5\mu A \times R1$$

$$V_{IN(UVLO^-)} = \frac{1.214V \times (R1 + R2)}{R2}$$

Figure 31 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on and puts the ADPL54203 in shutdown with quiescent current less than 2µA.

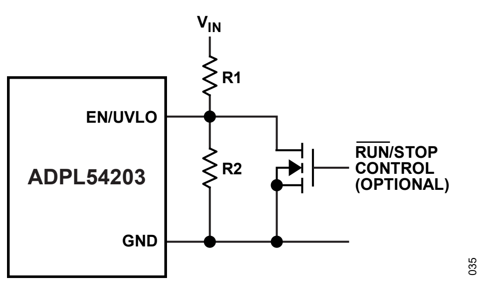

Figure 31. Undervoltage Lockout (UVLO)

Minimum Load Requirement

The ADPL54203 samples the isolated output voltage from the primary-side flyback pulse waveform. The flyback pulse occurs once the primary switch turns off and the secondary winding conducts current. In order to sample the output voltage, the ADPL54203 has to turn on and off for a minimum amount of time and with a minimum frequency. The ADPL54203 delivers a minimum amount of energy even during light load conditions to ensure accurate output voltage information. The minimum energy delivery creates a minimum load requirement, which can be approximately estimated as:

$$I_{LOAD(MIN)} = \frac{L_{PRI} \times I_{SW(MIN)}{}^2 \times f_{MIN}}{2 \times V_{OUT}}$$

$$L_{PRI} = \text{Transformer primary inductance}$$

$$I_{SW(MIN)} = \text{Minimum switch current limit} = 1.07\text{A(MAX)}$$

$$f_{MIN} = \text{Minimum switching frequency} = 12.7\text{kHz(MAX)}$$

The ADPL54203 typically needs less than 0.5% of its full output power as minimum load. Alternatively, a Zener diode with its breakdown of 10% higher than the output voltage can serve as a minimum load if preloading is not acceptable. For a 5V output, use a 5.6V Zener with cathode connected to the output.

Output Short Protection

When the output is heavily overloaded or shorted to ground, the reflected SW pin waveform rings longer than the internal blanking time. After the 350ns minimum switch-off time, the excessive ringing falsely triggers the boundary mode detector and turns the power switch back on again before the secondary current falls to zero. Under this condition, the ADPL54203 runs into continuous conduction mode at 380kHz maximum switching frequency. If the sampled R_{REF} voltage is still less than 0.6V after 11ms (typ) soft-start timer, the ADPL54203 initiates a new soft-start cycle. If the sampled R_{REF} voltage is larger than 0.6V after 11ms, the switch current may run away and exceed the 4.5A maximum current limit. Once the switch current hits 7.2A overcurrent limit, the ADPL54203 also initiates a new soft-start cycle. Under either condition, the new soft-start cycle throttles back both the switch current limit and switch frequency. The output short-circuit protection prevents the switch current from running away and limits the average output diode current.

Design Example

Use the following design example as a guide to designing applications for the ADPL54203. The design example involves designing a 5V output with a 1.5A load current and an input range from 10V to 28V.

$$V_{IN(MIN)} = 10V, V_{IN(NOM)} = 12V, V_{IN(MAX)} = 28V,$$

$$V_{OUT} = 5V, I_{OUT} = 1.5A$$

Step 1: Select the transformer turns ratio.

$$N_{PS} < \frac{60V - V_{INMAX} - V_{LEAKAGE}}{V_{OUT} + V_F}$$

$$V_{LEAKAGE} = \text{Margin for transformer leakage spike} = 15V$$

$$V_F = \text{Output diode forward voltage} = \sim 0.3V$$

Example:

$$N_{PS} < \frac{60V - 28V - 15V}{5V + 0.3V} = 3.2$$

The choice of transformer turns ratio is critical in determining output current capability of the converter. *Table 5* shows the switch voltage stress and output current capability at different transformer turns ratio.

Table 5. Switch Voltage Stress and Output Current Capability vs. Turns Ratio

NPS	$V_{SW(MAX)}$ at $V_{IN(MAX)}$ (V)	$I_{OUT(MAX)}$ at $V_{IN(MIN)}$ (A)	DUTY CYCLE (%)
1:1	33.3	0.94	16-35
2:1	38.6	1.40	27-51
3:1	43.9	1.67	36-61

Clearly, only N_{PS} = 3 can meet the 1.5A output current requirement, so N_{PS} = 3 is chosen as the turns ratio in this example.

Step 2: Determine the primary inductance.

Primary inductance for the transformer must be set above a minimum value to satisfy the minimum switch-off and switch-on time requirements:

$$L_{PRI} \geq \frac{t_{OFF(MIN)} \times N_{PS} \times (V_{OUT} + V_F)}{I_{SW(MIN)}}$$

$$L_{PRI} \geq \frac{t_{ON(MIN)} \times V_{IN(MAX)}}{I_{SW(MIN)}}$$

$$t_{OFF(MIN)} = 350\text{ns}$$

$$t_{ON(MIN)} = 160\text{ns}$$

$$I_{SW(MIN)} = 0.87\text{A}$$

Example:

$$L_{PRI} \geq \frac{350\text{ns} \times 3\ (5\text{V} + 0.3\text{V})}{0.87\text{A}} = 6.4\mu\text{H}$$

$$L_{PRI} \geq \frac{160\text{ns} \times 28\text{V}}{0.87\text{A}} = 5.1\mu\text{H}$$

Most transformers specify primary inductance with a tolerance of ±20%. With other component tolerance considered, choose a transformer with its primary inductance 40% to 60% larger than the minimum values calculated above. L_{PRI} = 9µH is then chosen in this example.

Once the primary inductance is determined, the maximum load switching frequency can be calculated as:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\frac{L_{PRI} \times I_{SW}}{V_{IN}} + \frac{L_{PRI} \times I_{SW}}{N_{PS} \times (V_{OUT} + V_F)}}$$

$$I_{SW} = \frac{V_{OUT} \times I_{OUT} \times 2}{\eta \times V_{IN} \times D}$$

Example:

$$D = \frac{(5V + 0.3V) \times 3}{(5V + 0.3V) \times 3 + \ 12V} = 0.57$$

$$I_{SW} = \frac{5V \times 1.5A \times 2}{0.8 \times 12V \times 0.57}$$

$$f_{SW} = 277kHz$$

The transformer also needs to be rated for the correct saturation current level across line and load conditions. A saturation current rating larger than 7A is necessary to work with the ADPL54203. The 750311564 from Wurth is chosen as the flyback transformer.

Step 3: Choose the output diode.

Two main criteria for choosing the output diode include forward-current and reverse-voltage rating. The maximum load requirement is a good first-sequence guess at the average current requirement for the output diode. Under output short-circuit condition, the output diode needs to conduct much higher current. Therefore, a conservative metric is 60% of the maximum switch current limit multiplied by the turns ratio:

$$I_{DIODE(MAX)} = 0.6 \times I_{SW(MAX)} \times N_{PS}$$

Example:

$$I_{DIODE(MAX)} = 8.1A$$

Next, calculate reverse voltage requirement using maximum V_{IN}:

$$V_{REVERSE} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}}$$

Example:

$$V_{REVERSE} = 5V + \frac{28V}{3} = 14.3V$$

The PDS835L (8A, 35V diode) from Diodes Inc. is chosen.

Step 4: Choose the output capacitor.

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Use the following equation to calculate the output capacitance:

$$C_{OUT} = \frac{L_{PRI} \times {I_{SW}}^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

Example:

Design for output voltage ripple less than ±1% of V_{OUT}, that is, 100mV.

$$C_{OUT} = \frac{9\mu H \times (4.5A)^2}{2 \times 5V \times 0.1V} = 182\mu F$$

Remember ceramic capacitors lose capacitance with applied voltage. The capacitance can drop to 40% of quoted capacitance at the maximum voltage rating. So a 220µF, 6.3V rating X5R or X7R ceramic capacitor is chosen.

Step 5: Design snubber circuit.

The snubber circuit protects the power switch from leakage inductance voltage spike. A (RC + DZ) snubber is recommended for this application. A 470pF capacitor in series with a 39Ω resistor is chosen as the RC snubber. The maximum Zener breakdown voltage is set according to the maximum V_{IN}:

$$V_{ZENER(MAX)} \leq 55V - V_{IN(MAX)}$$

Example:

$$V_{ZENER(MAX)} \leq 55V - 28V = 27V$$

A 24V Zener with a maximum of 26V provides optimal protection and minimize power loss. So a 24V, 1.5W Zener from Central Semiconductor (CMZ5934B) is chosen. Choose a diode that is fast and has sufficient reverse voltage breakdown:

$$V_{REVERSE} > V_{SW(MAX)}$$

$$V_{SW(MAX)} = V_{IN(MAX)} + V_{ZENER(MAX)}$$

Example:

$$V_{REVERSE} > 55V$$

A 100V, 1A diode from Diodes Inc. (DFLS1100) is chosen.

Step 6: Select the R_{REF} and R_{FB} resistors.

Use the following equation to calculate the starting values for R_{REF} and R_{FB}:

$$R_{FB} = \frac{R_{REF} \times N_{PS} \times (V_{OUT} + V_F\,(TO))}{V_{REF}}$$

R_{REF} = 10k

Example:

$$R_{FB} = \frac{10K \times 3 \times (5V + 0.3V)}{1.00V} = 159K$$

For 1% standard values, a 158k resistor is chosen.

Step 7: Adjust R_{FB} resistor based on output voltage.

Build and power up the application with application components and measure the regulated output voltage. Adjust R_{FB} resistor based on the measured output voltage:

$$R_{FB(NEW)} = \frac{V_{OUT}}{V_{OUT(MEASURED)}} \times R_{FB}$$

Example:

$$R_{FB} = \frac{5V}{5.14V} \times 158k = 154k$$

Step 8: Select R_{TC} resistor based on output voltage temperature variation.

Measure output voltage in a controlled temperature environment like an oven to determine the output temperature coefficient. Measure output voltage at a consistent load current and input voltage, across the operating temperature range.

Calculate the temperature coefficient of V_F:

$$-(\delta V_F/\delta T) = \frac{V_{OUT}(T1) - V_{OUT}(T2)}{T1 - T2}$$

$$R_{TC} = \frac{3.35mV/°C}{-(\delta V_F/\delta T)} \times (\frac{R_{FB}}{N_{PS}})$$

Example:

$$-(\delta V_F/\delta T) = \frac{5.189V - 5.041V}{100°C - (0°C)} = 1.48mV/°C$$

$$R_{TC} = \frac{3.35mV/°C}{1.48V/°C} \times (\frac{154}{3}) = 115k$$

Step 9: Select the EN/UVLO resistors.

Determine the amount of hysteresis required and calculate R1 resistor value:

$$V_{IN(HYS)} = 2.5\mu A \times R1$$

Example:

Choose 2V of hysteresis, R1 = 806k

Determine the UVLO thresholds and calculate R2 resistor value:

$$V_{IN(UVLO+)} = \frac{1.228V \times (R1 + R2)}{R2} + 2.5\mu A \times R1$$

Example:

Set V_{IN} UVLO rising threshold to 9.5V:

$$R2 = 158k$$

$$V_{IN(UVLO^{+})} = 9.5V$$

$$V_{IN(UNLO^{-})} = 7.5V$$

Step 10: Ensure minimum load.

The theoretical minimum load can be approximately estimated as:

$$I_{LOAD(MIN)} = \frac{9\mu H \times (1.07A)^2 \times 12.7kHz}{2 \times 5V} = 13.1mA$$

Remember to check the minimum load requirement in real application. The minimum load occurs at the point where the output voltage begins to climb up as the converter delivers more energy than what is consumed at the output. The real minimum load for this application is about 10mA. In this example, a 500Ω resistor is selected as the minimum load.

TYPICAL APPLICATIONS

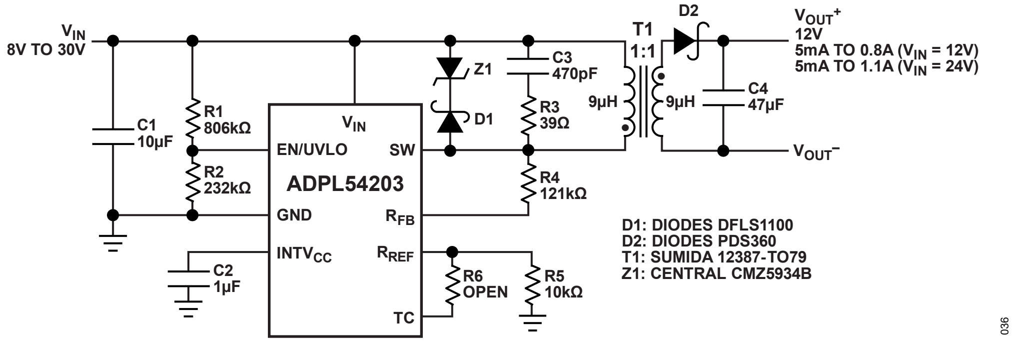

Figure 32. 8V to 30V$_{IN}$/12V$_{OUT}$ Isolated Flyback Converter

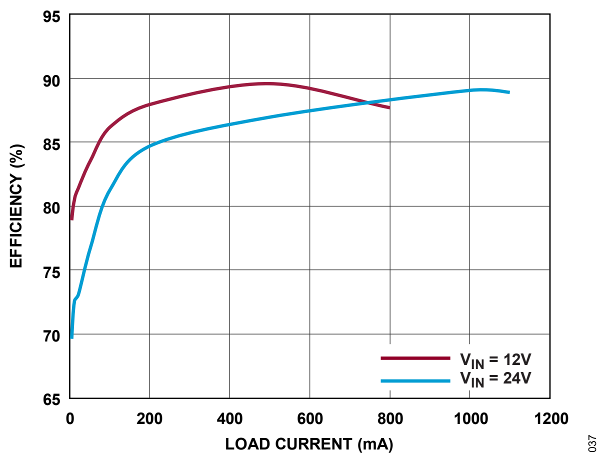

Figure 33. Efficiency vs. Load Current

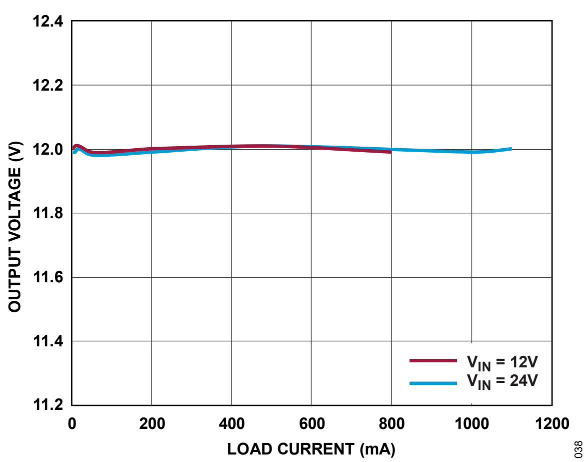

Figure 34. Load and Line Regulation

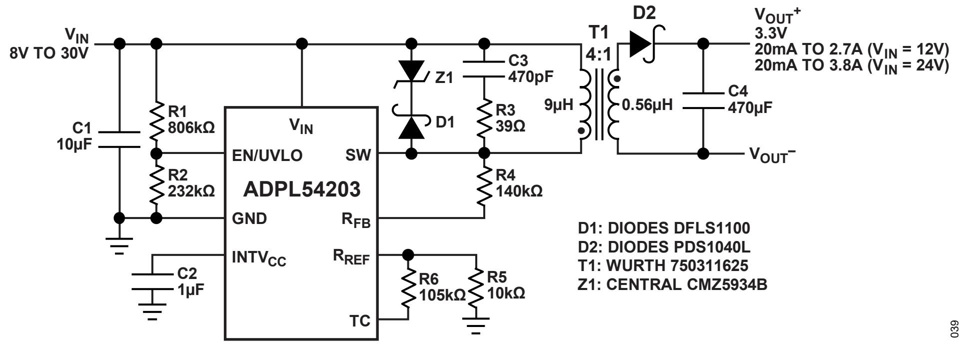

Figure 35. 8V to 30V_{IN}/3.3V_{OUT} Isolated Flyback Converter

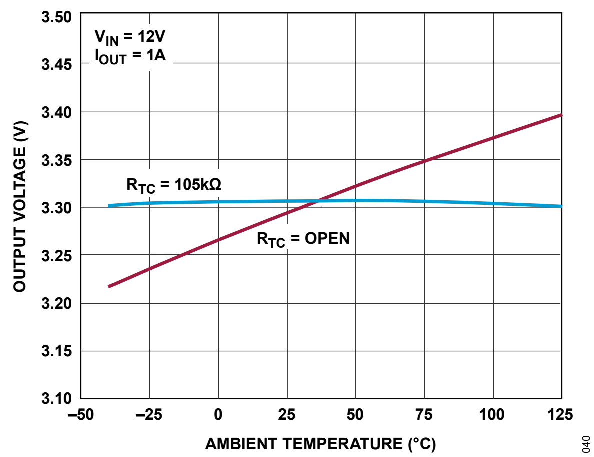

Figure 36. Output Temperature Variation

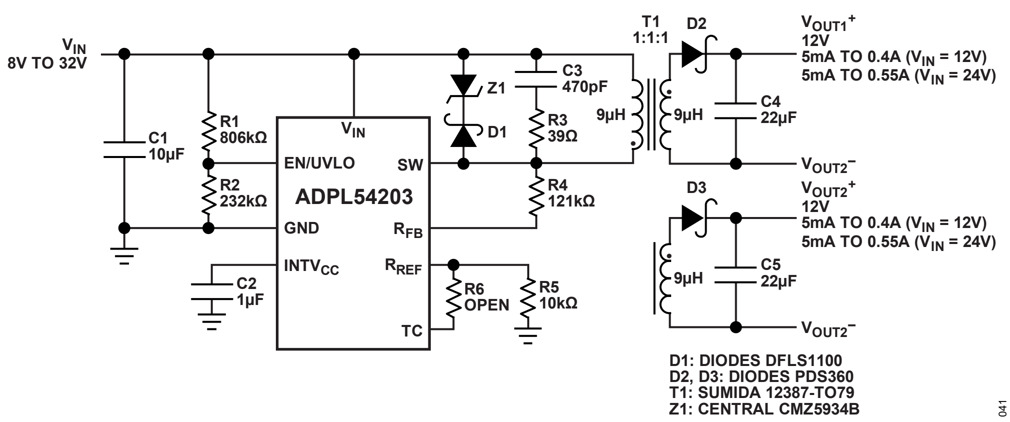

Figure 37. 8V to 32V_{IN}/±12V_{OUT} Isolated Flyback Converter

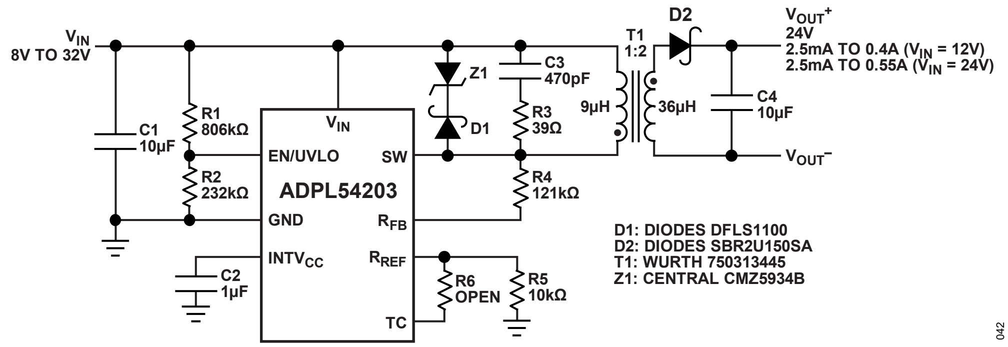

Figure 38. 8V to 32V_{IN}/24V_{OUT} Isolated Flyback Converter

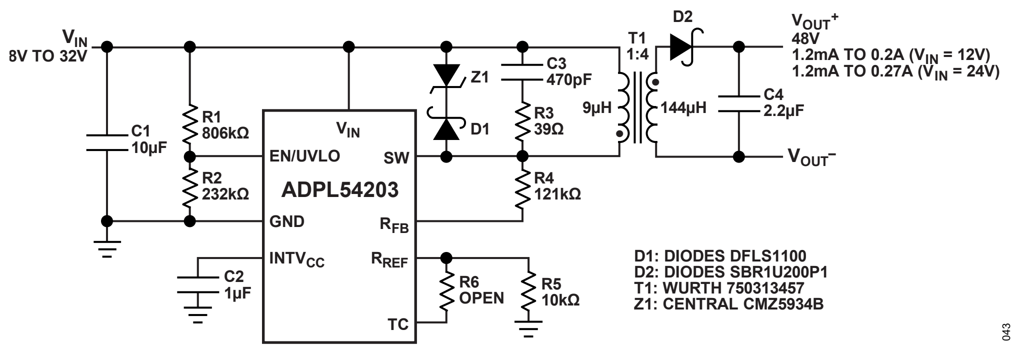

Figure 39. 8V to 32V_{IN}/48V_{OUT} Isolated Flyback Converter

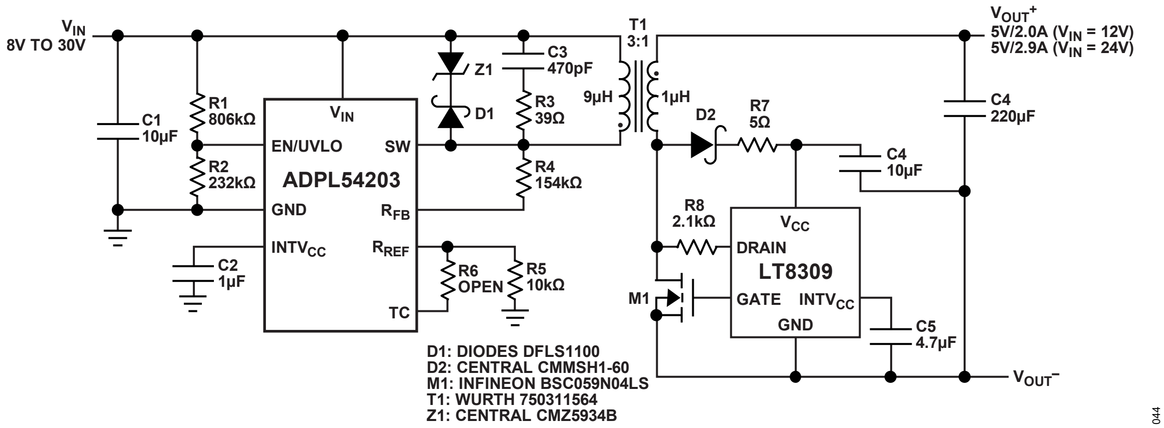

Figure 40. 8V to 30V_{IN}/5V_{OUT} Isolated Flyback Converter with LT8309

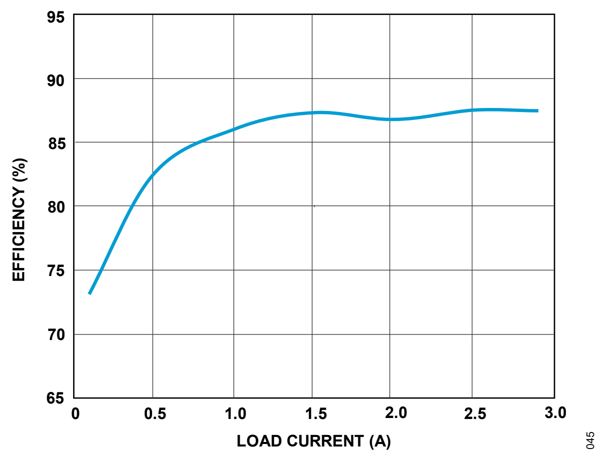

Figure 41. Efficiency vs. Load Current

OUTLINE DIMENSIONS

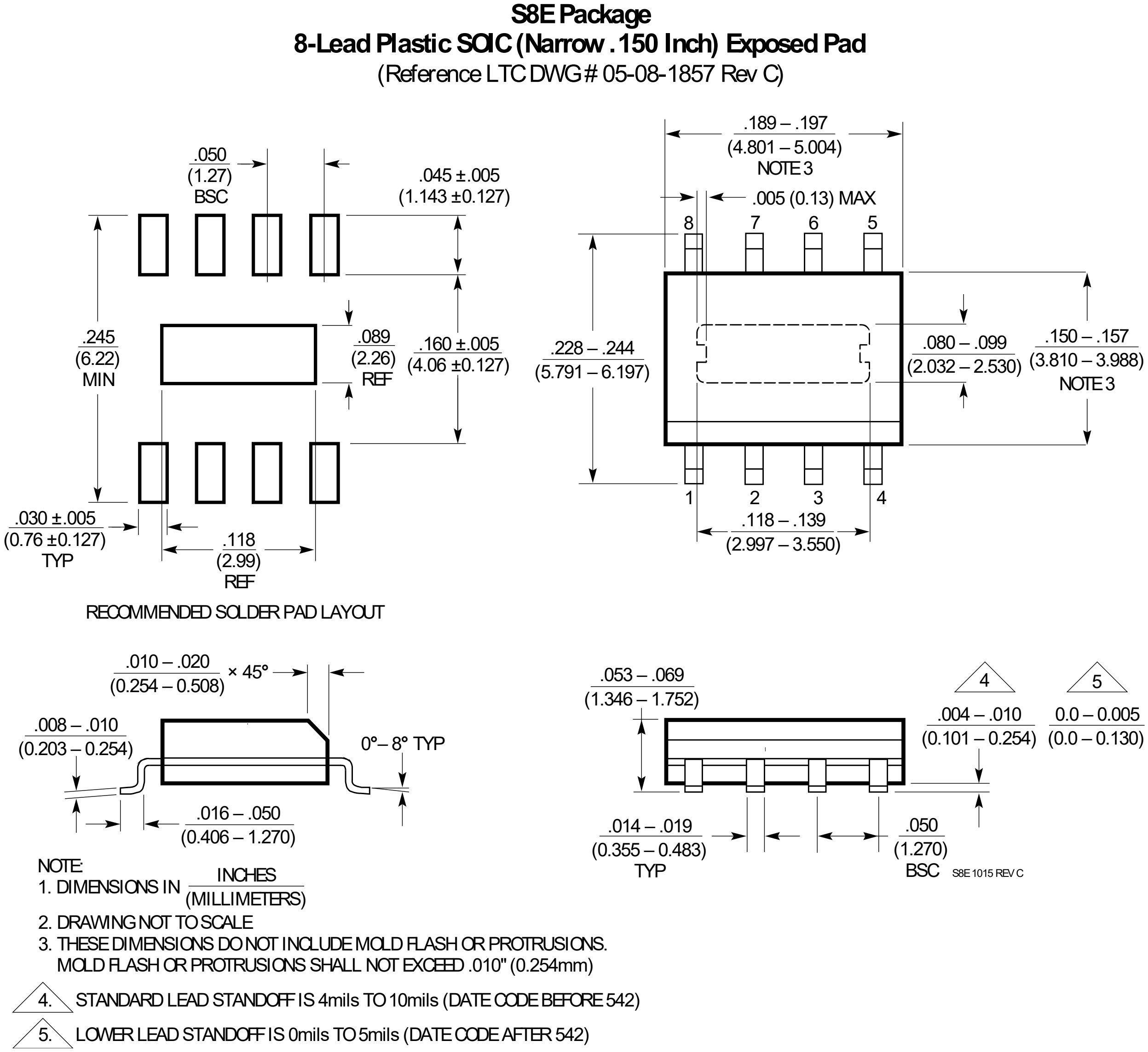

Figure 42. 8-Lead Plastic SO

ORDERING GUIDE

Table 6. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL*	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
ADPL54203ES8E#PBF	ADPL54203ES8E#TRPBF	54203	8-Lead Plastic SO	–40°C to 125°C

*For more information on tape and reel specifications, refer to the *Tape and Reel Specifications*.