Data Sheet

ADPL42005

20V, 500mA, Low Noise, CMOS LDO

FEATURES

- Input voltage range: 4V to 20V
- Maximum output current: 500mA
- Low noise: 32µVrms for fixed output versions
- PSRR performance of 58dB at 10kHz, V_{OUT} = 3.3V
- Reverse current protection
- Low dropout voltage: 400mV at 500mA
- Initial accuracy: ±0.8%
- Accuracy over line, load, and temperature
  - −2% to +1%, T_J = −40°C to +125°C
- Low quiescent current (V_{IN} = 10V), I_{GND} = 900µA with 500 mA load
- Low shutdown current: <40µA at V_{IN} = 12V, stable with small 1µF ceramic output capacitor
- Six fixed output voltage options: 1.5V, 1.8V, 2.5V, 3V, 3.3V, and 5V
- Adjustable output from 1.22V to V_{IN} − V_{DO}
- Foldback current limit and thermal overload protection
- User programmable precision UVLO/enable
- Power-good indicator
- 8-lead LFCSP and 8-lead SOIC packages

APPLICATIONS

- Regulation to noise-sensitive applications: ADC, DAC circuits, precision amplifiers, high-frequency oscillators, clocks, and PLLs
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation

GENERAL DESCRIPTION

The ADPL42005 is a complementary metal-oxide semiconductor (CMOS), low dropout linear regulator that operates from 4V to 20V and provides up to 500mA of output current. This high input voltage LDO is ideal for the regulation of high-performance analog and mixed-signal circuits operating from 19V to 1.22V rails. Using an advanced proprietary architecture, it provides high power supply rejection, low noise, and achieves excellent line and load transient response with just a small 1µF ceramic output capacitor.

The ADPL42005 is available in six fixed output voltage options and an adjustable version, which allows output voltages that range from 1.22V to V_{IN} − V_{DO} through an external feedback divider.

The ADPL42005 output noise voltage is 32µVrms and is independent of the output voltage. A digital power-good output allows power system monitors to check the health of the output voltage. A user programmable precision undervoltage lockout function facilitates sequencing of multiple power supplies.

The ADPL42005 is available in 8-lead, 3 mm × 3 mm LFCSP and 8-lead SOIC packages (*Figure 51* and *Figure 52*). The LFCSP offers a very compact solution and also provides excellent thermal performance for applications requiring up to 500mA of output current in a small, low-profile footprint.

SIMPLIFIED APPLICATION DIAGRAMS

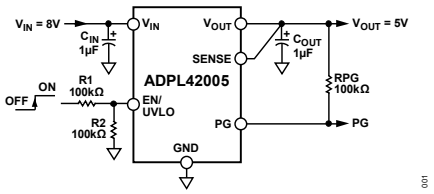

Figure 1. ADPL42005 with Fixed Output Voltage, 5V

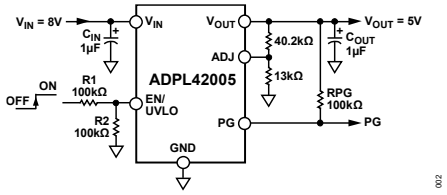

Figure 2. ADPL42005 with Adjustable Output Voltage, 5V

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SPECIFICATIONS

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(V_{IN} = (V_{OUT} + 1V) or 4V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE RANGE	V_{IN}		4		20	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 100µA, V_{IN} = 10V		440	900	µA
		I_{OUT} = 10mA, V_{IN} = 10V		450	1050	µA
		I_{OUT} = 300mA, V_{IN} = 10V		750	1400	µA
		I_{OUT} = 500mA, V_{IN} = 10V		900	1600	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND, V_{IN} = 12V		40	75	µA
INPUT REVERSE CURRENT	$I_{REV-INPUT}$	EN = GND, V_{IN} = 0V, V_{OUT} = 20V		0.3	5	µA
OUTPUT VOLTAGE						
FIXED OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 10mA	−0.8		+0.8	%
		1mA < I_{OUT} < 500mA, V_{IN} = (V_{OUT} + 1V) to 20V	−2		+1	%
ADJUSTABLE OUTPUT VOLTAGE ACCURACY	V_{ADJ}	I_{OUT} = 10mA	1.21	1.22	1.23	V
		1mA < I_{OUT} < 500mA, V_{IN} = (V_{OUT} + 1V) to 20V	1.196		1.232	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 1V) to 20V	−0.015		+0.015	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1mA to 500mA		0.2	0.75	%/A
ADJ INPUT BIAS CURRENT	ADJ_{I-BIAS}	1mA < I_{OUT} < 500mA, V_{IN} = (V_{OUT} + 1V) to 20V, ADJ connected to V_{OUT}		10		nA
SENSE INPUT BIAS CURRENT	$SENSE_{I-BIAS}$	1mA < I_{OUT} < 500mA, V_{IN} = (V_{OUT} + 1V) to 20V, SENSE connected to V_{OUT}, V_{OUT} = 1.5V		1		µA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10mA		20	40	mV
		I_{OUT} = 150mA		100	175	mV
		I_{OUT} = 300mA		200	325	mV
		I_{OUT} = 500mA		400	600	mV
CURRENT-LIMIT THRESHOLD3[3]	I_{LIMIT}		625	775	1000	mA
PG OUTPUT LOGIC LEVEL						
PG OUTPUT LOGIC HIGH	PG_{HIGH}	I_{OH} < 1µA	1.0			V
PG OUTPUT LOGIC LOW	PG_{LOW}	I_{OL} < 2mA			0.4	V
PG OUTPUT THRESHOLD						
PG OUTPUT VOLTAGE FALLING	PG_{FALL}			−9.2		%
PG OUTPUT VOLTAGE RISING	PG_{RISE}			−6.5		%
THERMAL SHUTDOWN						
THERMAL SHUTDOWN THRESHOLD	TS_{SD}	T_J rising		150		°C
THERMAL SHUTDOWN HYSTERESIS	TS_{SD-HYS}			15		°C
PROGRAMMABLE EN/UVLO						
UVLO THRESHOLD RISING	$UVLO_{RISE}$	3.3V ≤ V_{IN} ≤ 20V	1.18	1.22	1.28	V

(V_{IN} = (V_{OUT} + 1V) or 4V (whichever is greater), EN = V_{IN}, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO THRESHOLD FALLING	$UVLO_{FALL}$	3.3V ≤ V_{IN} ≤ 20V, 10kΩ in series with the enable pin		1.13		V
UVLO HYSTERESIS CURRENT	$UVLO_{HYS}$	V_{EN} > 1.25V	7.5	9.8	12	µA
ENABLE PULL-DOWN CURRENT	I_{EN-IN}	EN = V_{IN}		500		nA
START THRESHOLD	V_{START}				3.2	V
SHUTDOWN THRESHOLD	$V_{SHUTDOWN}$		2.45			V
HYSTERESIS				250		mV
OUTPUT NOISE	OUT_{NOISE}	10Hz to 100kHz, V_{IN} = 6.3V, V_{OUT} = 3.3V		32		µV rms
		10Hz to 100kHz, V_{IN} = 5.5V, V_{OUT} = 1.5V, adjustable mode		18		µV rms
		10Hz to 100kHz, V_{IN} = 12V, V_{OUT} = 5V, adjustable mode		30		µV rms
		10Hz to 100kHz, V_{IN} = 20V, V_{OUT} = 15V, adjustable mode		65		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V		50		dB
		10kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V		58		dB
		100kHz, V_{IN} = 3.3V, V_{OUT} = 1.8V, adjustable mode		50		dB
		10kHz, V_{IN} = 3.3V, V_{OUT} = 1.8V, adjustable mode		60		dB

1 Based on an end-point calculation using 1mA and 500mA loads. See *Figure 6* for typical load regulation performance for loads less than 1mA.

2 Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 3.0V.

3 Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0V, or 4.5V.

Table 2. Input and Output Capacitor, Recommended Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	0.7			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.2	Ω

1 The minimum input and output capacitance must be greater than 0.7µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to GND	−0.3V to +22V
V_{OUT} to GND	−0.3V to +20V
EN/UVLO to GND	−0.3V to V_{IN}
PG to GND	−0.3V to V_{IN}
SENSE/ADJ to GND	−0.3V to V_{OUT}
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Data

Absolute maximum ratings apply individually only, not in combination. The ADPL42005 can be damaged when the junction temperature limit is exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), power dissipation of the device (P_D), and junction-to-ambient thermal resistance of the package (θ_{JA}).

The maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a four-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a four-layer, 4 in. × 3 in. circuit board. Refer to JESD51-7 and JESD51-9 for detailed information on the board construction. For additional information, refer to the *AN-617* application note.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The package's Ψ_{JB} is based on modeling and calculation using a four-layer board. The JESD51-12, Guidelines for Reporting and Using Electronic Package Thermal Information, states that thermal characterization parameters are not the same as thermal

resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. The maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula:

$$T_J = T_B + (P_D \times \psi_{JB}) \quad (2)$$

Refer to JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

Thermal Resistance

θ_{JA} and Ψ_{JB} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages. θ_{JC} is a parameter for surface-mount packages with top mounted heat sinks. θ_{JC} is presented here for reference only.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
8-Lead LFCSP	40.1	27.1	17.2	°C/W
8-Lead SOIC	48.5	58.4	31.3	°C/W

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

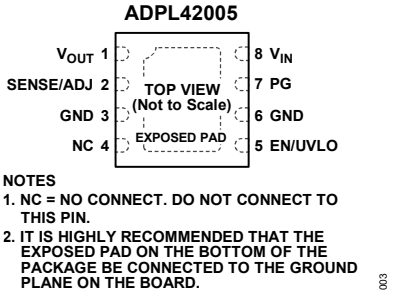

Figure 3. LFCSP Package

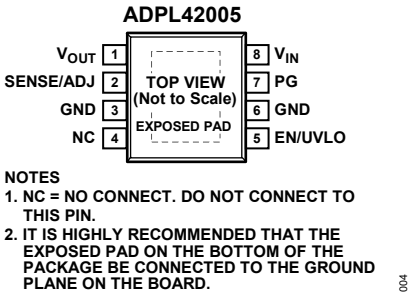

Figure 4. Narrow Body SOIC Package

Pin Descriptions

Table 5. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
1	V_{OUT}	Regulated Output Voltage. Bypass V_{OUT} to GND with a 1µF or greater capacitor.
2	SENSE/ADJ	Sense (SENSE). Measures the actual output voltage at the load and feeds it to the error amplifier. Connect SENSE as close as possible to the load to minimize the effect of IR drop between the regulator output and the load. This function applies to fixed voltages only. Adjust Input (ADJ). An external resistor divider sets the output voltage. This function applies to adjustable voltages only.
3	GND	Ground
4	NC	Do Not Connect to This Pin.
5	EN/UVLO	Enable Input (EN). Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to V_{IN}. Programmable Undervoltage Lockout (UVLO). When the programmable UVLO function is used, the upper and lower thresholds are determined by the programming resistors.
6	GND	Ground
7	PG	Power Good. This open-drain output requires an external pull-up resistor to V_{IN} or V_{OUT}. If the part is in shutdown, current limit, thermal shutdown, or falls below 90% of the nominal output voltage, PG immediately transitions low. If the power-good function is not used, the pin may be left open or connected to ground.
8	V_{IN}	Regulator Input Supply. Bypass V_{IN} to GND with a 1µF or greater capacitor.
	EPAD	Exposed Pad. Exposed paddle on the bottom of the package. The EPAD enhances thermal performance and is electrically connected to GND inside the package. It is highly recommended that the EPAD be connected to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7.5V, V_{OUT} = 5V, I_{OUT} = 10mA, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise noted.

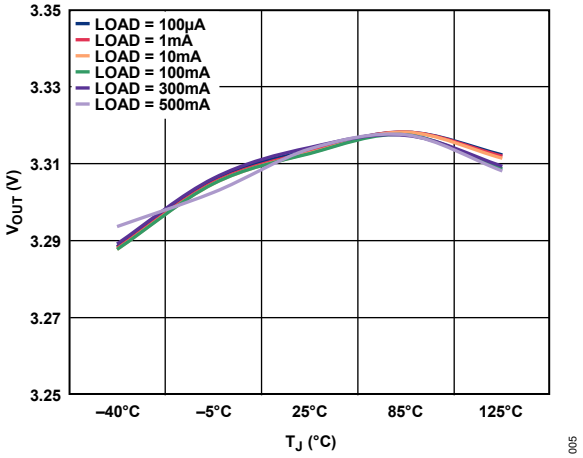

Figure 5. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = 3.3V

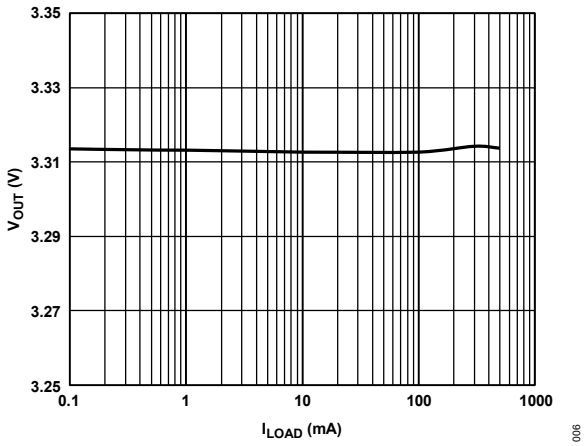

Figure 6. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3V

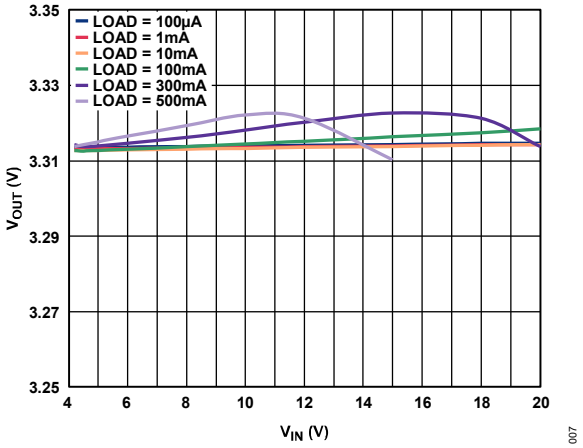

Figure 7. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 3.3V

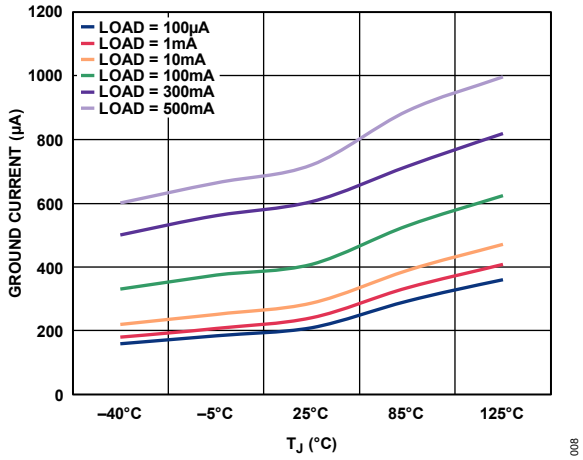

Figure 8. Ground Current (I_{GND}) vs. Junction Temperature (T_J), V_{OUT} = 3.3V

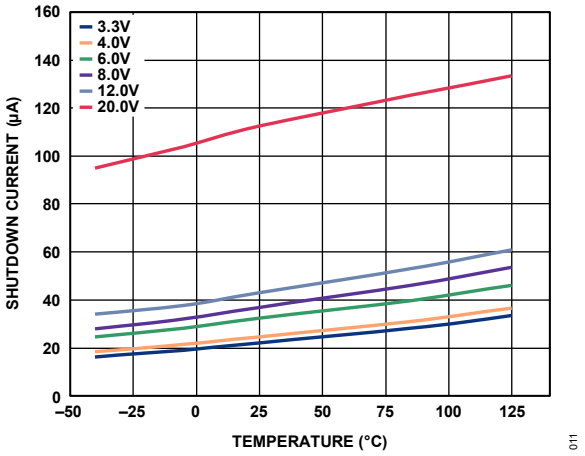

Figure 9. Shutdown Current (I_{GND-SD}) vs. Temperature (T_J) at Various Input Voltages, V_{OUT} = 3.3V

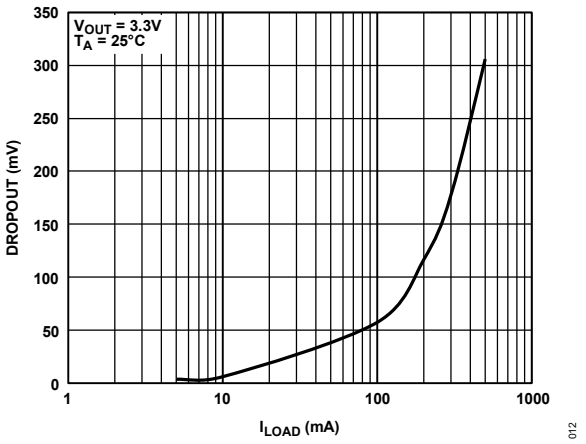

Figure 10. Dropout Voltage ($V_{DROPOUT}$) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3V

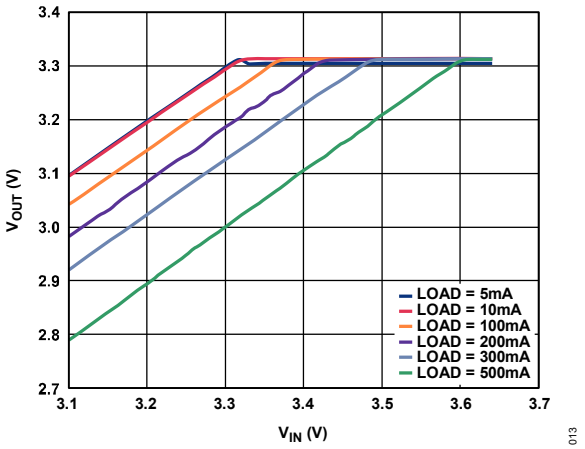

Figure 11. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (in Dropout), V_{OUT} = 3.3V

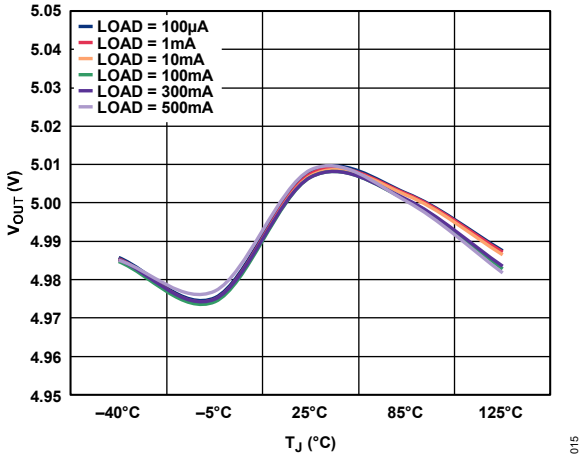

Figure 12. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = 5V

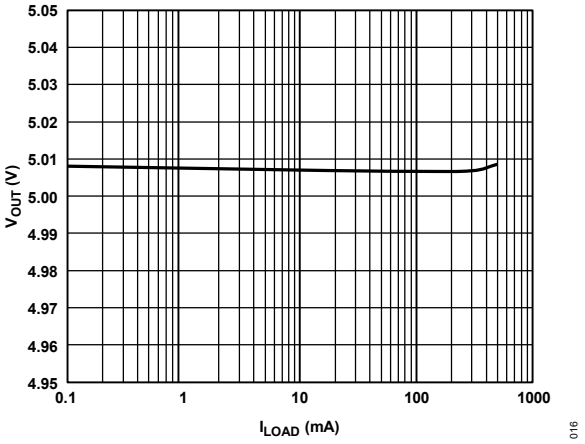

Figure 13. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 5V

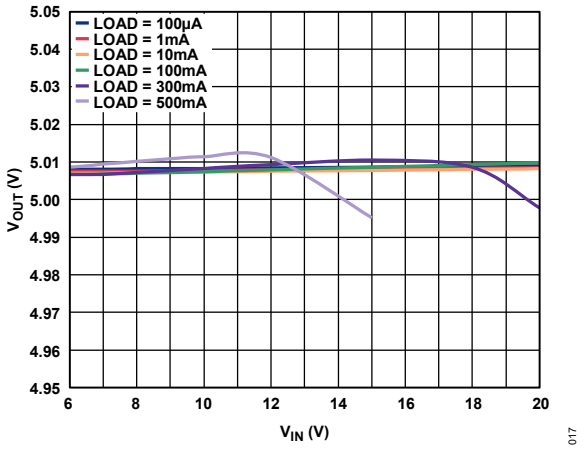

Figure 14. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 5V

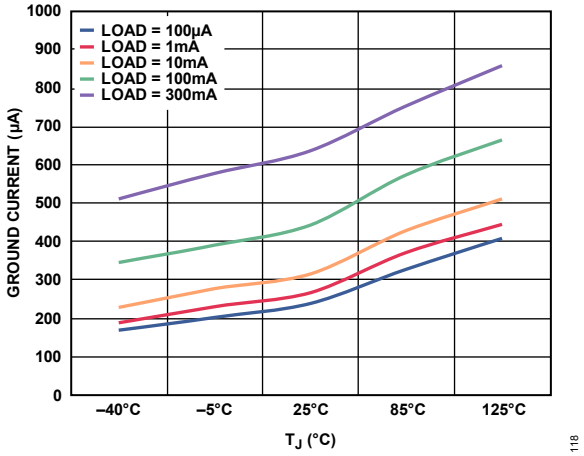

Figure 15. Ground Current (I_{GND}) vs. Junction Temperature (T_J), V_{OUT} = 5V

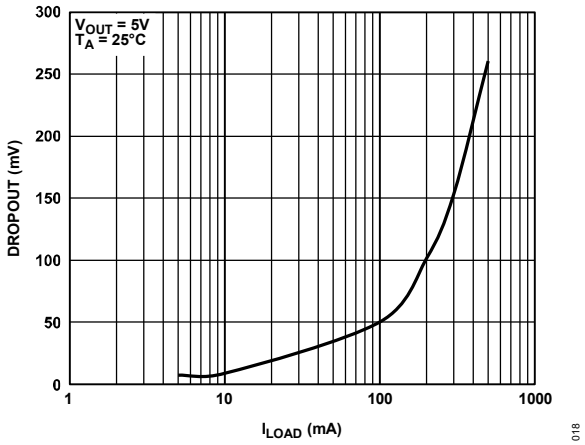

Figure 16. Dropout Voltage ($V_{DROPOUT}$) vs. Load Current (I_{LOAD}), V_{OUT} = 5V

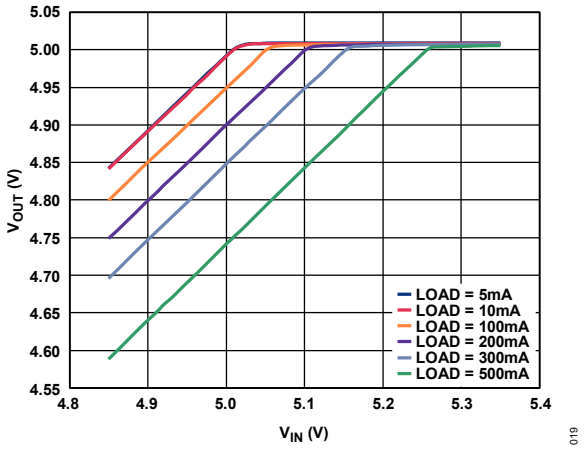

Figure 17. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (in Dropout), V_{OUT} = 5V

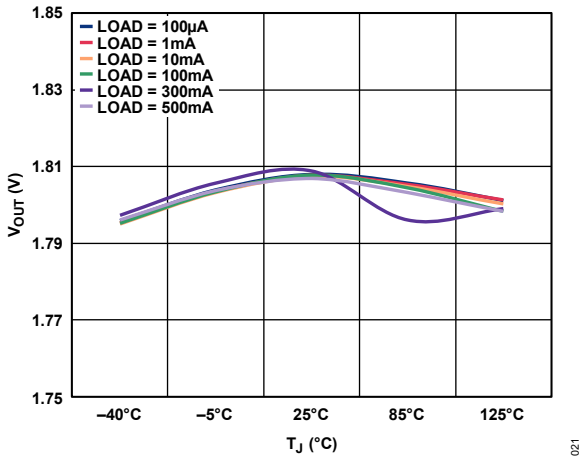

Figure 18. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = 1.8V

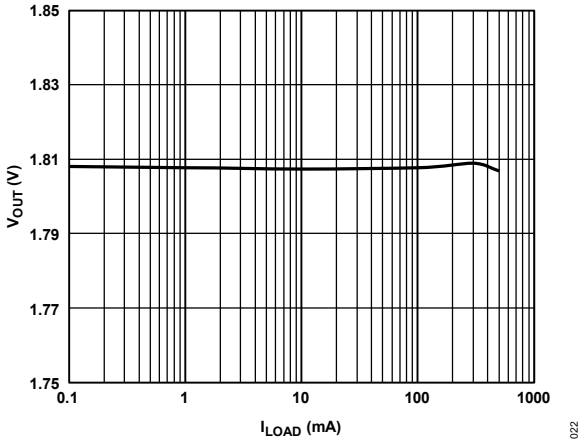

Figure 19. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 1.8V

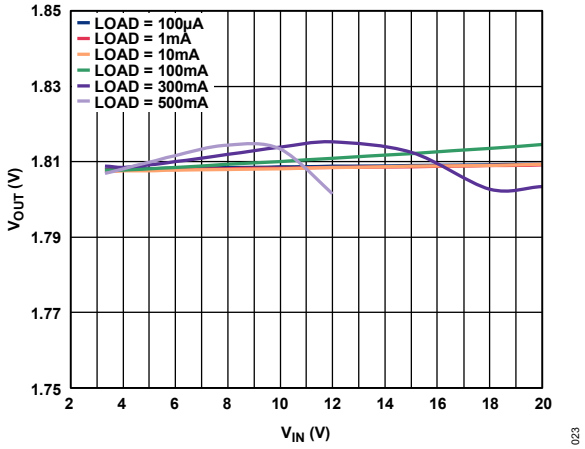

Figure 20. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 1.8V

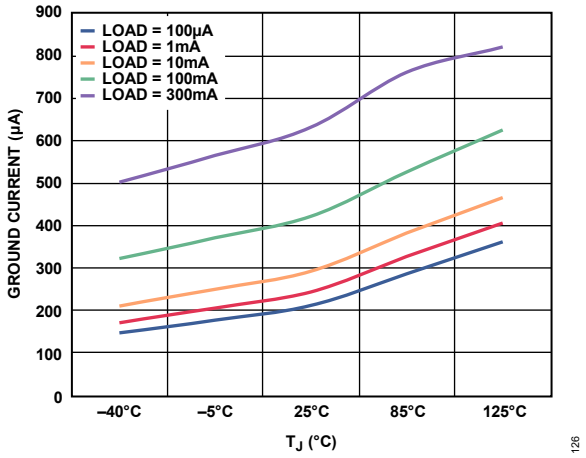

Figure 21. Ground Current (IGND) vs. Junction Temperature (T_J), V_{OUT} = 1.8V

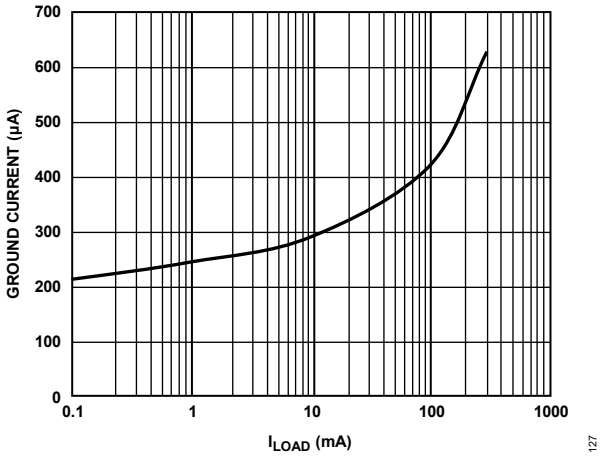

Figure 22. Ground Current (IGND) vs. Load Current (I_{LOAD}), V_{OUT} = 1.8V

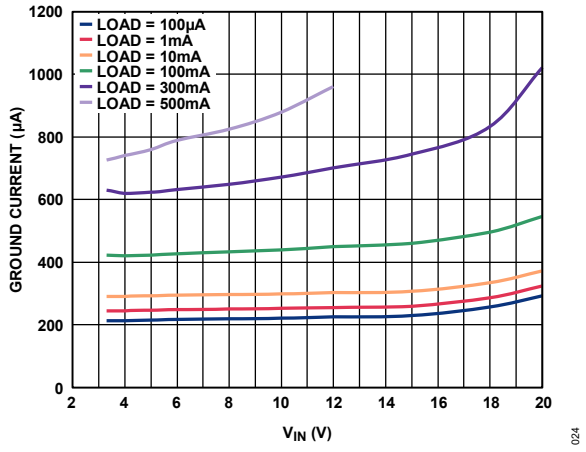

Figure 23. Ground Current (I_{GND}) vs. Input Voltage (V_{IN}), V_{OUT} = 1.8V

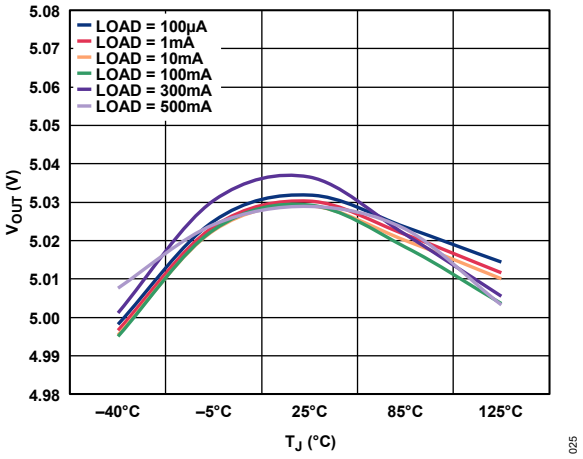

Figure 24. Output Voltage (V_{OUT}) vs. Junction Temperature (T_J), V_{OUT} = 5V, Adjustable

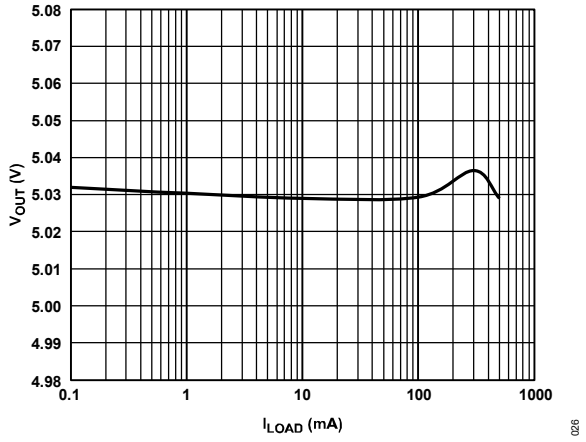

Figure 25. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 5V, Adjustable

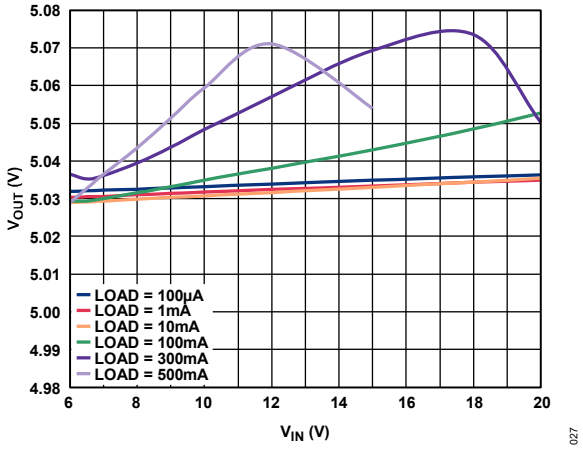

Figure 26. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 5V, Adjustable

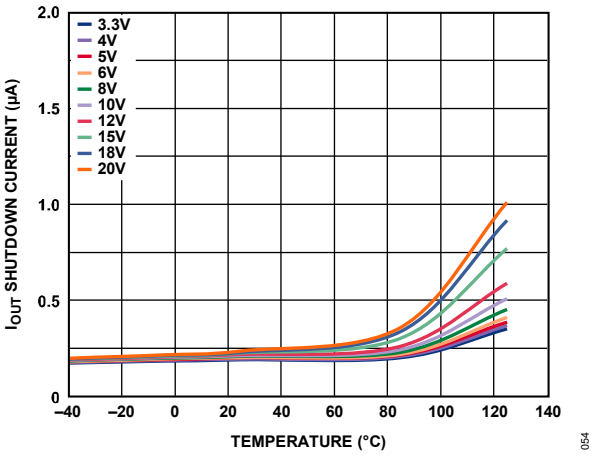

Figure 27. Reverse Input Current ($I_{REV-INPUT}$) vs. Temperature (T_J), V_{IN} = 0V, Different Voltages on V_{OUT}

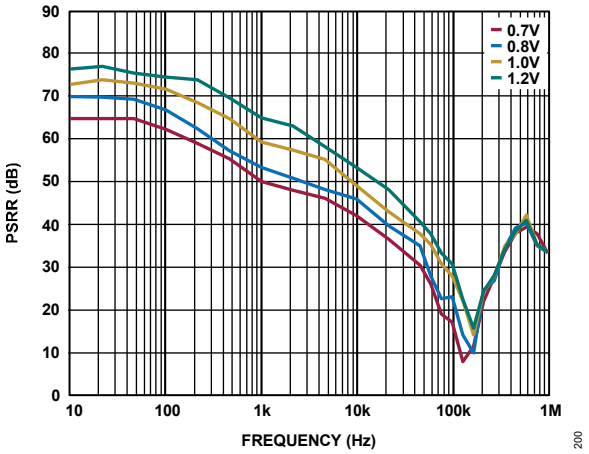

Figure 28. PSRR vs. Frequency, V_{OUT} = 5V, for Various Headroom Voltages

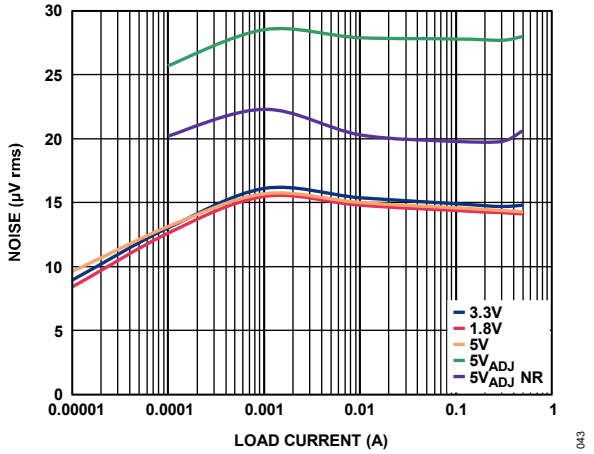

Figure 29.Output Noise vs. Load Current and Output Voltage, C_{OUT} = 1µF

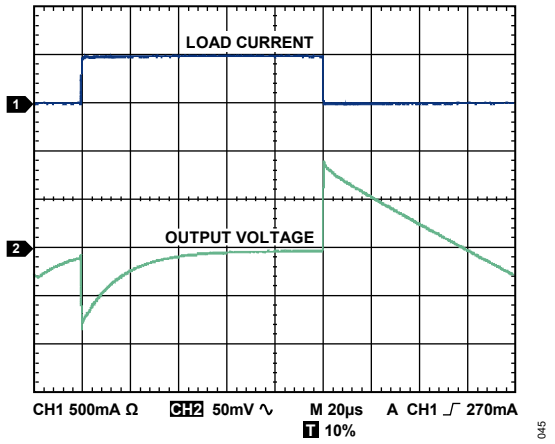

Figure 30. Load Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA to 500mA, V_{OUT} = 1.8V, V_{IN} = 5V

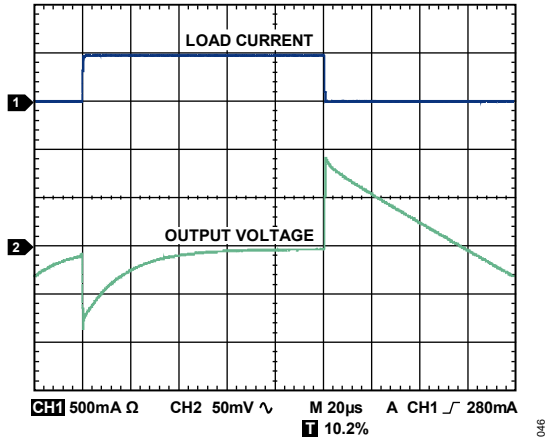

Figure 31. Load Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA to 500mA, V_{OUT} = 3.3V, V_{IN} = 5V

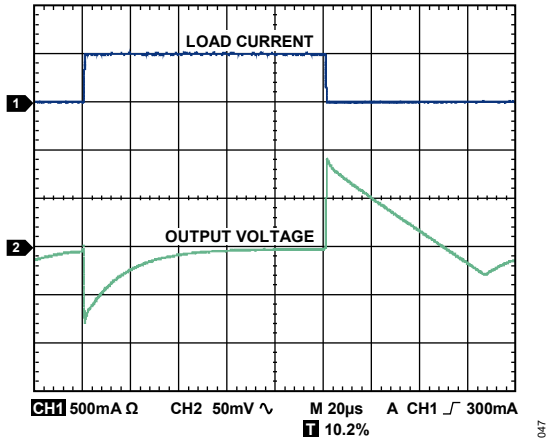

Figure 32. Load Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA to 500mA, V_{OUT} = 5V, V_{IN} = 7V

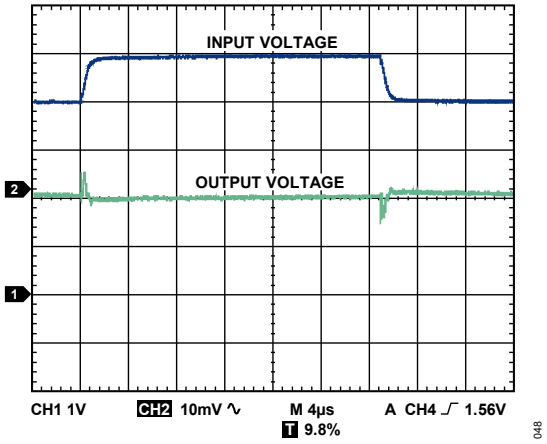

Figure 33. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 500mA, V_{OUT} = 1.8V

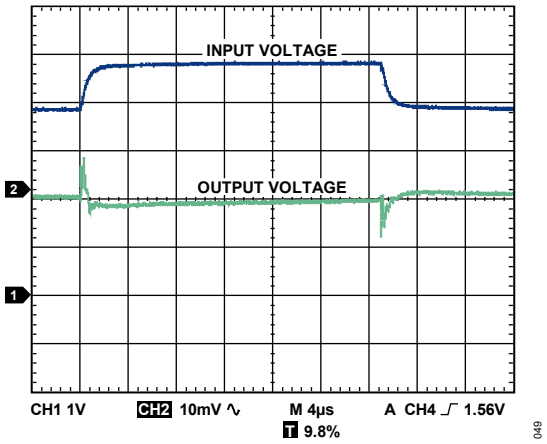

Figure 34. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 500mA, V_{OUT} = 3.3V

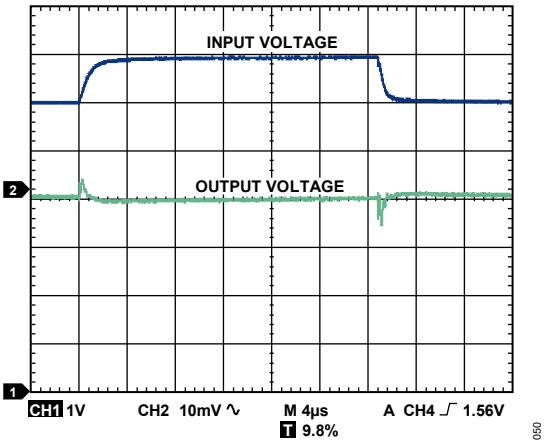

Figure 35. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 500mA, V_{OUT} = 5V

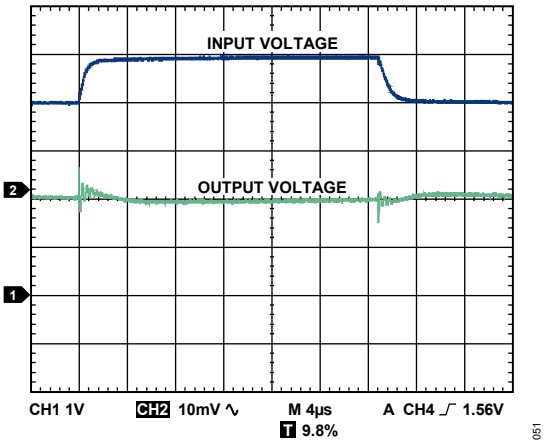

Figure 36. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA, V_{OUT} = 1.8V

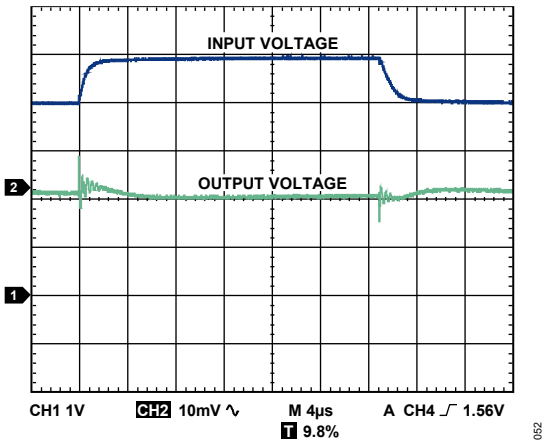

Figure 37. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA, V_{OUT} = 3.3V

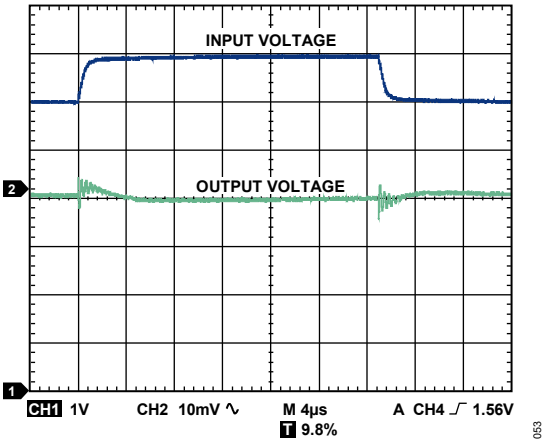

Figure 38. Line Transient Response, C_{IN} = C_{OUT} = 1µF, I_{LOAD} = 1mA, V_{OUT} = 5V

THEORY OF OPERATION

The ADPL42005 is a low quiescent current, low-dropout linear regulator that operates from 4V to 20V and provides up to 500mA of output current. Drawing a low 1mA of quiescent current (typical) at full load makes the ADPL42005 ideal for battery-operated portable equipment. Typical shutdown current consumption is 40µA at room temperature.

Optimized for use with small 1µF ceramic capacitors, the ADPL42005 provides excellent transient performance.

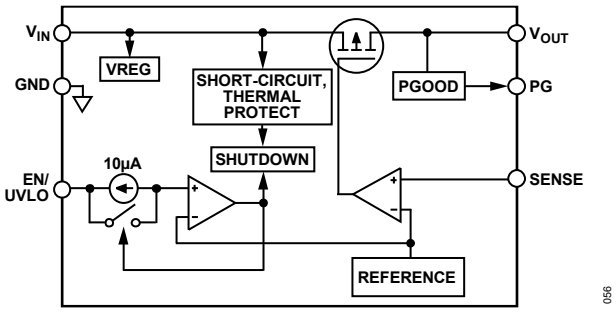

Figure 39. Fixed Output Voltage Internal Block Diagram

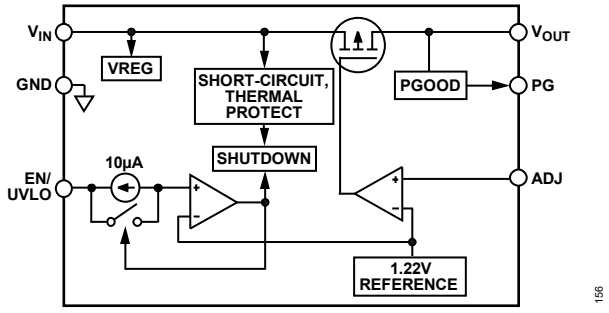

Figure 40. Adjustable Output Voltage Internal Block Diagram

Internally, the ADPL42005 consists of a reference, an error amplifier, and a PMOS pass transistor. Output current is delivered through the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADPL42005 is available in six fixed output voltage options, ranging from 1.5V to 5.0V and in an adjustable version with an output voltage that can be set to between 1.22V and 19V by an external voltage divider. The output voltage can be set according to the following Equation 3:

$$V_{OUT} = 1.22V\left(1 + \frac{R1}{R2}\right) \quad (3)$$

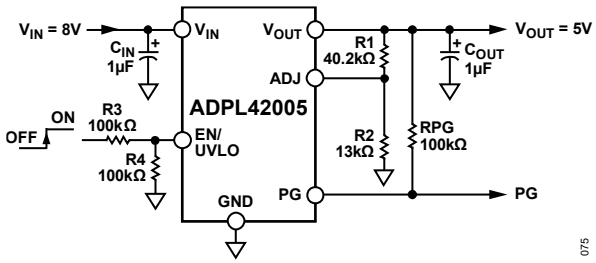

Figure 41. Typical Adjustable Output Voltage Application Schematic

The value of R2 must be less than 200kΩ to minimize errors in the output voltage caused by the ADJ pin input current. For example, when R1 and R2 each equal 200kΩ, the output voltage is 2.44V. The output voltage error introduced by the ADJ pin input current is 2mV or 0.08%, assuming a typical ADJ pin input current of 10nA at 25°C.

The ADPL42005 uses the EN/UVLO pin to enable and disable the V_{OUT} pin under normal operating conditions. When EN/UVLO is high, V_{OUT} turns on, and when EN is low, V_{OUT} turns off. For automatic startup, EN/UVLO can be tied to V_{IN}.

The ADPL42005 incorporates reverse current protections circuitry that prevents current flow backwards through the pass element when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 55mV, the body of the PFET is switched to V_{OUT} and turned off or opened. In other words, the gate is connected to V_{OUT}.

APPLICATIONS INFORMATION

Design Tools

The ADPL42005 is supported by the LTpowerCAD® and LTspice® design tools to produce complete power designs and simulations. For more information on design tools, visit the *ADPL42005 product page*.

Capacitor Selection

Output Capacitor

The ADPL42005 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1µF capacitance with an ESR of 1Ω or less is recommended to ensure the stability of the ADPL42005. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADPL42005 to large changes in load current. *Figure 42* shows the transient responses for an output capacitance value of 1µF.

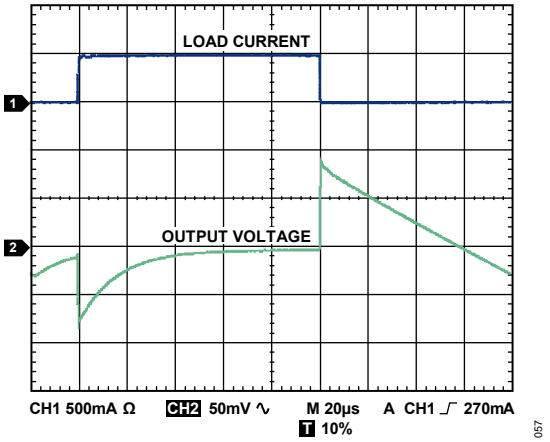

Figure 42. Output Transient Response, V_{OUT} = 1.8V, C_{OUT} = 1µF

Input Bypass Capacitor

Connecting a 1µF capacitor from V_{IN} to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1µF of output capacitance is required, the input capacitor should be increased to match it.

Programmable Undervoltage Lockout(UVLO)

The ADPL42005 uses the EN/UVLO pin to enable and disable the V_{OUT} pin under normal operating conditions. As shown in *Figure 43*, when a rising voltage on EN crosses the upper threshold, V_{OUT} turns on. When a falling voltage on EN/UVLO crosses the lower threshold, V_{OUT} turns off. The hysteresis of the EN/UVLO threshold is determined by the Thevenin equivalent resistance in series with the EN/UVLO pin.

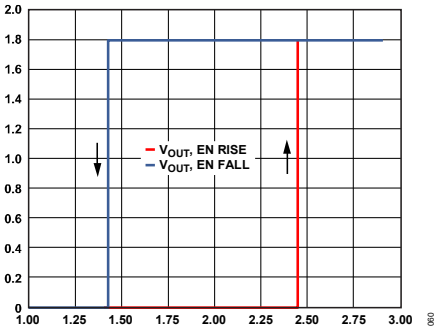

Figure 43. Typical V_{OUT} Response to EN Pin Operation

The upper and lower thresholds are user programmable and can be set using two resistors. When the EN/UVLO pin voltage is below 1.22V, the LDO is disabled. When the EN/UVLO pin voltage transitions above 1.22V, the LDO is enabled and 10µA hysteresis current is sourced out from the pin raising the voltage, thus providing threshold hysteresis. Typically, two external resistors program the minimum operational voltage for the LDO. The resistance values, R1 and R2, can be determined from:

$$R1 = V_{HYS}/10\mu A$$

$$R2 = 1.22V \times R1/(V_{IN} - 1.22V)$$

where:

V_{IN} is the desired turn-on voltage.

V_{HYS} is the desired EN/UVLO hysteresis level.

Hysteresis can also be achieved by connecting a resistor in series with the EN/UVLO pin. For the example shown in *Figure 44*, the enable threshold is 2.44V with a hysteresis of 1V.

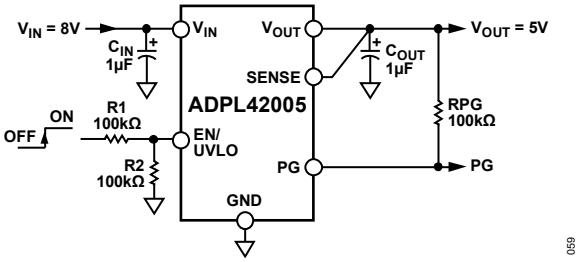

Figure 44. Typical EN Pin Voltage Divider

Figure 43 shows the typical hysteresis of the EN/UVLO pin. This prevents on/off oscillations that can occur because of noise on the EN pin as it passes through the threshold points.

The ADPL42005 uses an internal soft-start to limit the inrush current when the output is enabled. The startup time for the 3.3V option is approximately 580µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in *Figure 45*, the startup time is dependent on the output voltage setting.

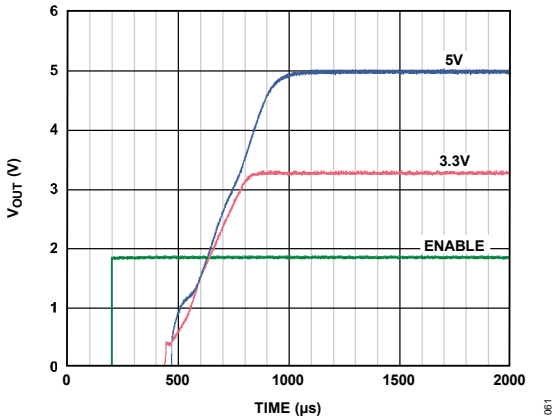

Figure 45. Typical Startup Behavior

Power-Good Feature

The ADPL42005 provides a power-good pin (PG) to indicate the status of the output. This open-drain output requires an external pull-up resistor to V_{IN} or V_{OUT}. If the part is in shutdown mode, current-limit mode, or thermal shutdown, or if it falls below 90% of the nominal output voltage, the power-good pin (PG) immediately transitions low. During soft-start, the rising threshold of the powergood signal is 93.5% of the nominal output voltage.

The open-drain output is held low when the ADPL42005 has sufficient input voltage to turn on the internal PG transistor. The PG transistor is terminated through a pull-up resistor to V_{OUT} or V_{IN}.

Power-good accuracy is 93.5% of the nominal regulator output voltage when this voltage is rising, with a 90% trip point when this voltage is falling. Regulator input voltage brownouts or glitches trigger power no good signals if V_{OUT} falls below 90%.

A normal power-down causes the power-good signal to go low when V_{OUT} drops below 90%.

Figure 46 and *Figure 47* show the typical power-good rising and falling threshold over temperature.

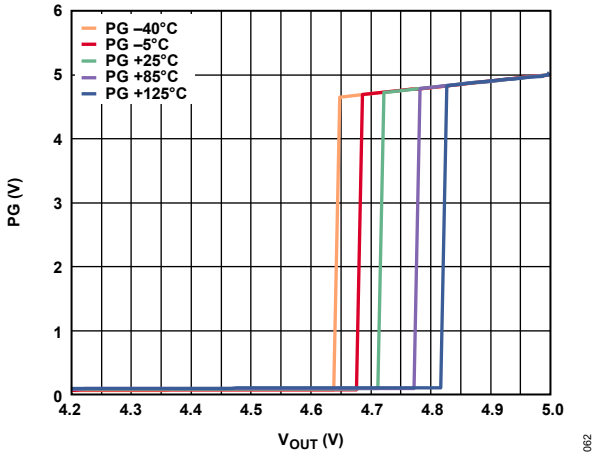

Figure 46. Typical Power-Good Threshold vs. Temperature, V_{OUT} Rising

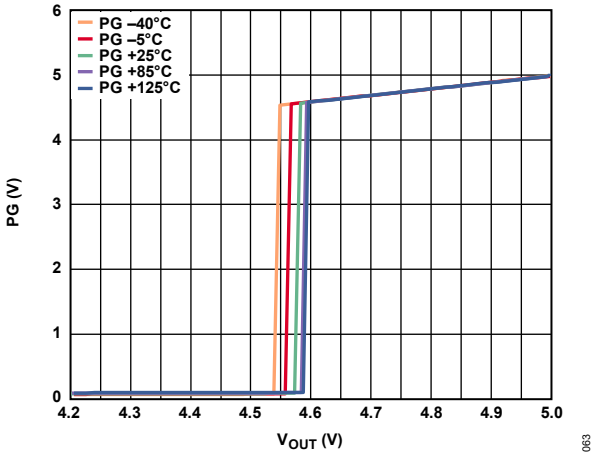

Figure 47. Typical Power-Good Threshold vs. Temperature, V_{OUT} Falling

Noise Reduction of the ADPL42005 in Adjustable Mode

The ultralow output noise of the fixed output ADPL42005 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO. The adjustable output ADPL42005 uses the more conventional architecture, where the reference voltage is fixed and the error amplifier gain is a function of the output voltage. The disadvantage of the conventional LDO architecture is that the output voltage noise is proportional to the output voltage.

The adjustable LDO circuit can be modified slightly to reduce the output voltage noise to levels close to that of the fixed output ADPL42005. The circuit shown in *Figure 48* adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the ac gain of the error amplifier. R_{NR} is chosen to be equal to R_{FB2}. This limits the AC gain of the error amplifier to approximately 6dB. The actual gain is the parallel combination of R_{NR} and R_{FB1} divided by R_{FB2}. This ensures the error amplifier always operates at greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to $R_{FB1} - R_{NR}$ at a frequency between 50Hz and 100Hz. This sets the frequency where the AC gain of the error amplifier is 3dB down from its DC gain.

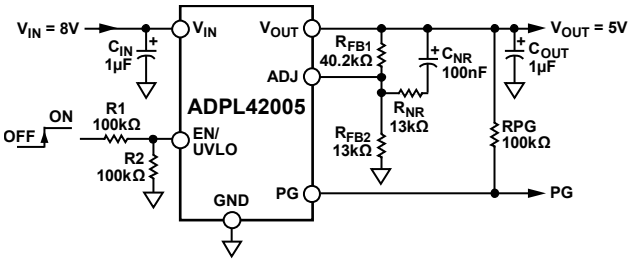

Figure 48. Noise Reduction Modification to Adjustable LDO

Current Limit and Thermal Overload Protection

The ADPL42005 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADPL42005 is designed to current limit when the output load reaches 775mA (typical). When the output load exceeds 775mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the

junction temperature drops below 135°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from V_{OUT} to ground occurs. At first, the ADPL42005 current limits, so that only 775mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 775mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 775mA and 0mA, which continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so the junction temperature does not exceed 125°C.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADPL42005. However, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the V_{IN} and GND pins. Place the output capacitor as close as possible to the V_{OUT} and GND pins. Use of 0805 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

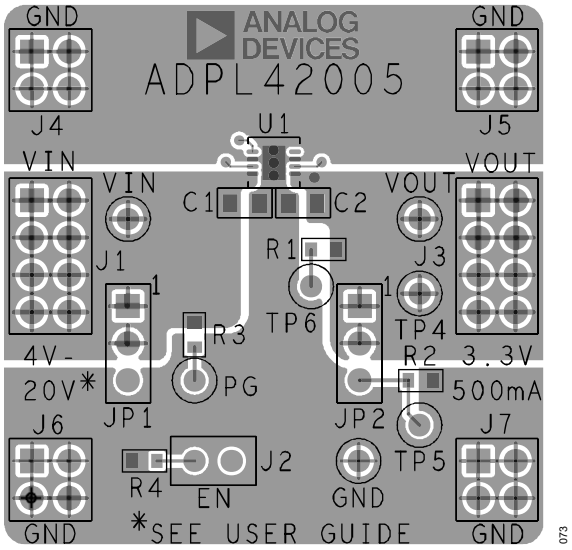

Figure 49. Example LFCSP PCB Layout

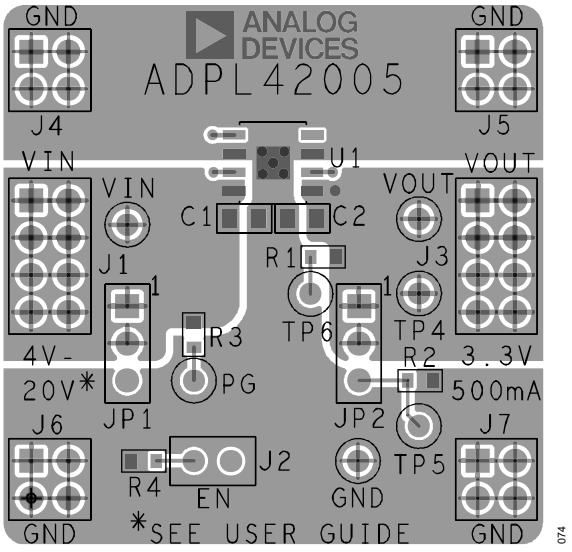

Figure 50. Example SOIC PCB Layout

OUTLINE DIMENSIONS

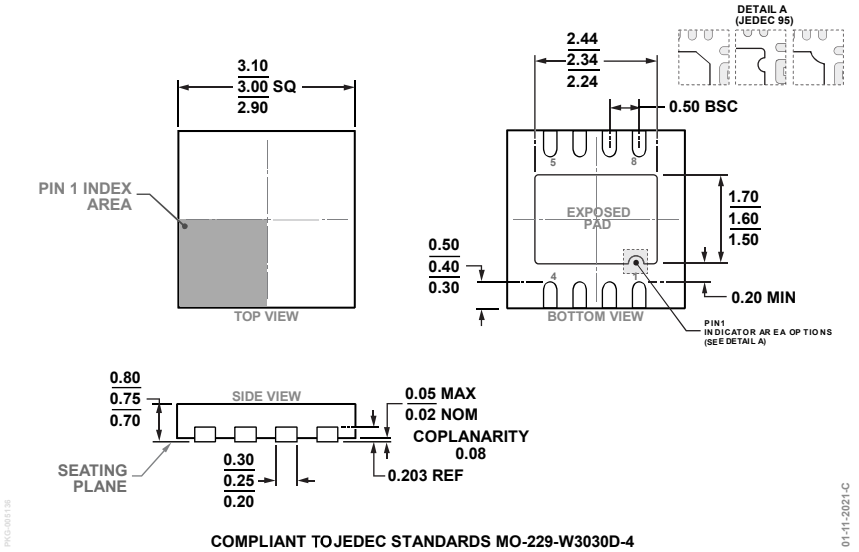

Figure 51. 8-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm × 3 mm Body and 0.75 mm Package Height (CP-8-11) Dimensions shown in millimeters

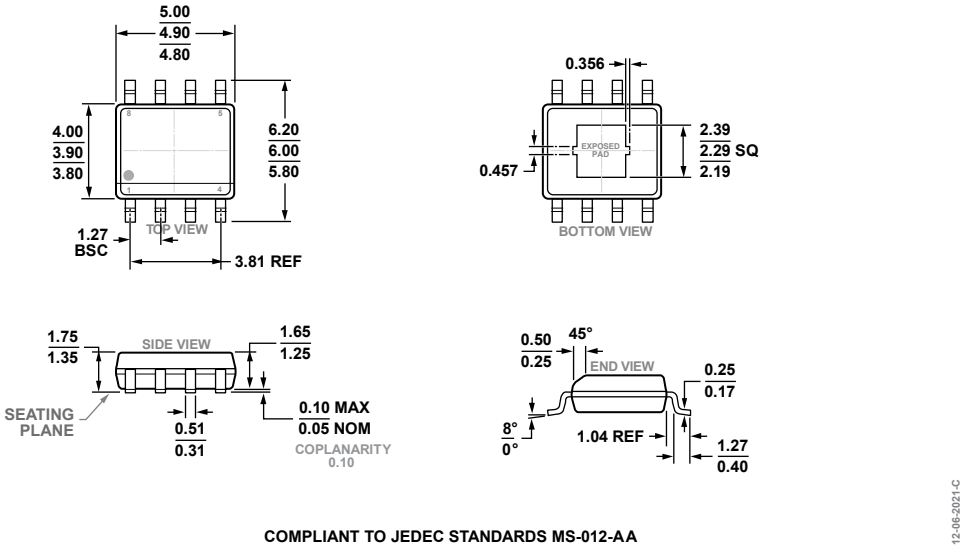

Figure 52. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP] Narrow Body (RD-8-1). Dimensions shown in millimeters

ORDERING GUIDE

Table 6. Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKING QUANTITY	PACKAGE OPTION	MARKING CODE
ADPL42005ACPZ-1.5-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LXX
ADPL42005ACPZ-1.8-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LXY
ADPL42005ACPZ-2.5-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LXZ
ADPL42005ACPZ-3.0-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LY0
ADPL42005ACPZ-3.3-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LY1
ADPL42005ACPZ-5.0-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LY2
ADPL42005ACPZ-R7	-40°C to +125°C	8-Lead LFCSP (3mm x 3mm w/ EP)	Reel, 1500	CP-8-11	LY3
ADPL42005ARDZ-1.5-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	200515
ADPL42005ARDZ-1.8-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	200518
ADPL42005ARDZ-2.5-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	200525
ADPL42005ARDZ-3.0-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	200530
ADPL42005ARDZ-3.3-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	200533
ADPL42005ARDZ-5.0-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	420055
ADPL42005ARDZ-R7	-40°C to +125°C	8-Lead SOIC w/ EP	Reel, 1000	RD-8-1	42005

[1] Z = RoHS compliant part

Output Voltage Options

MODEL[1]	OUTPUT VOLTAGE (V)[2]
ADPL42005ACPZ-1.5-R7	1.5
ADPL42005ACPZ-1.8-R7	1.8
ADPL42005ACPZ-2.5-R7	2.5
ADPL42005ACPZ-3.0-R7	3.0
ADPL42005ACPZ-3.3-R7	3.3
ADPL42005ACPZ-5.0-R7	5
ADPL42005ACPZ-R7	Adjustable
ADPL42005ARDZ-1.5-R7	1.5
ADPL42005ARDZ-1.8-R7	1.8
ADPL42005ARDZ-2.5-R7	2.5
ADPL42005ARDZ-3.0-R7	3.0
ADPL42005ARDZ-3.3-R7	3.3
ADPL42005ARDZ-5.0-R7	5
ADPL42005ARDZ-R7	Adjustable

[1] Z = RoHS compliant part

[2] For additional voltage options, contact a local Analog Devices sales or distribution representative.

Evaluation Boards

MODEL[1]	PACKAGE DESCRIPTION
EVAL-ADPL42005CP-AZ	LFCSP Evaluation Board
EVAL-ADPL42005RD-AZ	SOIC Evaluation Board
ADPL42005CPZ-REDYKIT	LFCSP REDYKIT
ADPL42005RDZ-REDYKIT	SOIC REDYKIT

[1] Z = RoHS compliant part

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	02/25	Initial release	—