17.7GHz to 55GHz, Wideband, Microwave Downconverter

FEATURES

- Wideband RF input frequency range: 17.7GHz to 55GHz
- Integrated RF chain features
  - Tunable image rejection filters
  - Gain control DSAs
- Integrated LO chain features
  - Input frequency range: 8.85GHz to 27.5GHz
  - Internal 2× multiplier
  - Tunable LO harmonic rejection filters
  - I/Q phase correction
- Two frequency translation modes
  - IF single-ended output (2GHz to 12GHz)
  - Baseband I/Q differential output (DC to 8GHz)
- I/Q baseband mode programmable features
  - Imbalance optimization
  - Common-mode voltages
  - DC offset correction
  - Gain selection
    - High gain (50Ω differential, DC to 8GHz)
    - Low gain (100Ω differential, DC to 4GHz)
- IF mode programmable features
  - Image rejection optimization
  - Tunable band-pass filter
  - Gain control DSAs
- Internal power detectors with programmable automatic power-down overload protection
- NVM factory calibration to minimize part to part variations
- Simple SPI: 3-wire or 4-wire
- General-purpose logic outputs for integration with other chips in a system
- LUT logic address inputs for fast frequency hopping applications
- 120-ball, 6mm × 6.5mm, CSP_BGA package

APPLICATIONS

- Satellite payload[1] and ground stations (SATCOM)
- Wideband radar and electronic warfare systems (EW)
- Instrumentation and automatic test equipment (ATE)
- Millimeter-wave 5G and 6G testers

[1]For information regarding commercial space low (CSL) or commercial space high (CSH) qualified versions of the ADMV1455, contact space@analog.com.

GENERAL DESCRIPTION

The ADMV1455 is a highly integrated microwave downconverter optimized for wideband radio designs operating in the 17.7GHz to 55GHz RF frequency range. Provides a compact alternative to traditional multichip solutions, significantly reducing system size, weight, and power consumption.

The integrated local oscillator (LO) signal chain accepts LO input signals in the 8.85GHz to 27.5GHz range. In the LO signal chain, there are internal amplifiers, a 2× frequency multiplier, programmable harmonic-rejection filters, and phase-adjust circuitry that generates the necessary 17.7GHz to 55GHz signal to drive the in-phase/quadrature (I/Q) mixer.

The ADMV1455 has two, switch selectable, RF signal chains. One chain operates within the 17.7GHz to 34GHz range, and the other chain operates in the 30GHz to 55GHz range. Each chain has multiple stages of low noise amplifiers (LNAs), signal level control, and filtering. A power detector is provided to allow monitoring of the power levels at the I/Q mixer inputs.

The two frequency translation modes available are: a single-ended output intermediate frequency (IF) and a differential I/Q baseband. The single-ended output IF mode operates in the 2GHz to 12GHz frequency range and includes an on-chip 90° IF hybrid, a tunable filter, and two adjustable stages of gain control. The differential I/Q baseband mode operates from DC to 8GHz and includes a programmable internal common-mode voltage, programmable offset voltages, and programmable gain select. The differential output impedance is centered about 75Ω, which allows the baseband outputs to interface with either a 50Ω or 100Ω differential load impedance.

The RF input, LO input, and IF output are all single-ended and matched to 50Ω impedance. No external matching circuitry is required.

Integrated gain and frequency look-up tables (LUT) are provided and can be addressed through the serial peripheral interface (SPI) or directly using the ADD_Fx and ADD_Gx ball connections to allow fast switching for frequency hopping applications.

Incorporated is a simple SPI that can operate in either a 3-wire or 4-wire implementation. The SPI allows programming all on-chip functions, such as gain control, image rejection optimization, tunable filters, general-purpose logic outputs, and the LUT.

The ADMV1455 downconverter is offered in a BGA package that supports heat sinking either from the top of the package or through the bottom of the printed circuit board (PCB). Either method of heat sinking has similar thermal performance and is acceptable to efficiently control the T_C. The ADMV1455 operates over the −40°C to +95°C temperature range.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.935.5565 |

TABLE OF CONTENTS

REVISION HISTORY

12/2025—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

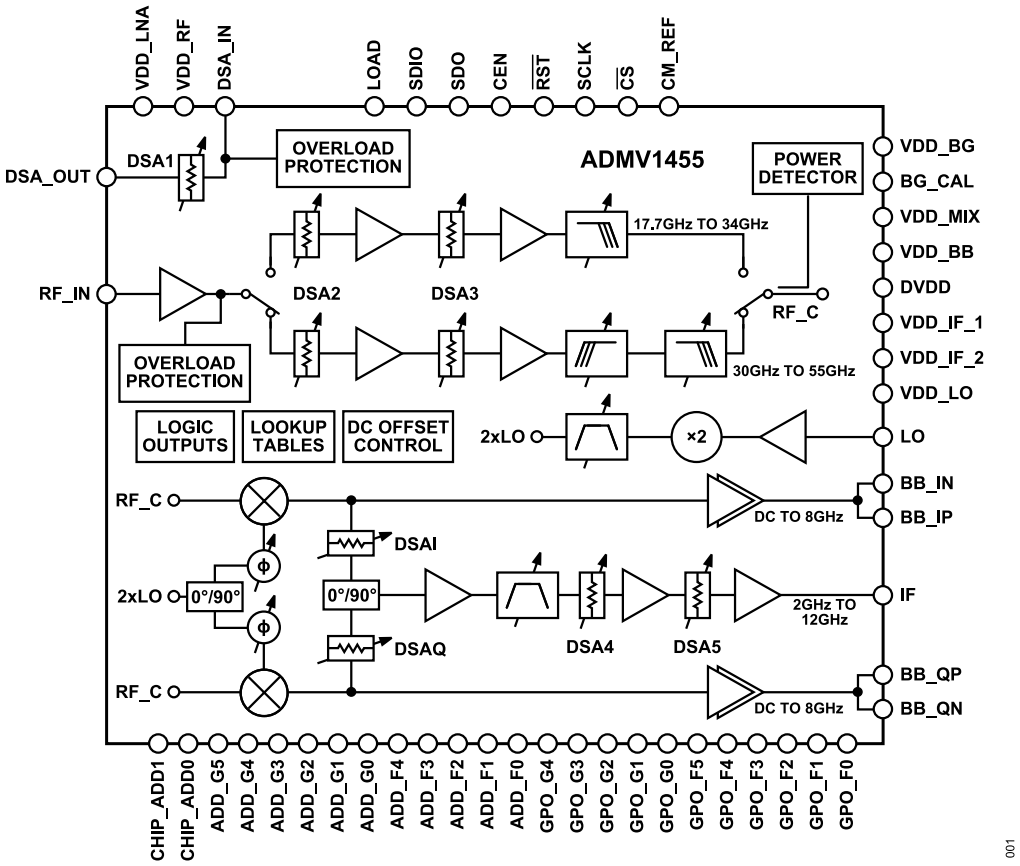

Figure 1. Functional Block Diagram

SPECIFICATIONS

T_C = 25°C, VDD_BB = 2.5V, and all other supplies = 1.8V, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGES					
RF Input (f_{RF})					
Low Band Signal Chain		17.7		34	GHz
High Band Signal Chain		30		55	GHz
LO Input (f_{LO})		8.85		27.5	GHz
2× LO Multiplier (2× f_{LO})		17.7		55	GHz
IF Single-Ended Output		2		12	GHz
Baseband I/Q Differential Output		DC		8	GHz
LO AMPLITUDE RANGE					
f_{LO} < 25GHz		−7		−3	dBm
f_{LO} ≥ 25GHz		−3		0	dBm
OPERATING TEMPERATURE RANGE		−40		+95	°C
IMAGE REJECTION CONTROL					
LO Phase Adjustment			±20		Degrees
LO Phase Step			0.6		Degrees
IF Amplitude Step Size			0.1		dB
BASEBAND OUTPUT COMMON-MODE VOLTAGE (V_{OCM})	Internally generated, digitally controlled				
VDD_BB = 1.8V		0.8		1.1	V
VDD_BB = 2.5V		0.8		1.5	V
POWER DETECTOR PERFORMANCE					
Input Range	Power at RF_IN and output measured digitally via the on-chip analog-to-digital converter (ADC)	−40		−17	dBm
RETURN LOSS					
RF_IN Input	50Ω single-ended				
Low Band	17GHz to 34GHz		−10		dB
High Band	30GHz to 55GHz		−8		dB
DSA_IN Input and DSA1 = 0dB	50Ω single-ended				
Low Band	17GHz to 50GHz		−14		dB
High Band	50GHz to 55GHz		−6		dB
DSA_IN Input and DSA1 = 15dB	50Ω single-ended				
Low Band	17GHz to 50GHz		−11		dB
High Band	50GHz to 55GHz		−6		dB
DSA_OUT Output and DSA1 = 0dB	50Ω single-ended				
Low Band	17GHz to 50GHz		−12		dB
High Band	50GHz to 55GHz		−6		dB
DSA_OUT Output and DSA1 = 15dB	50Ω single-ended				
Low Band	17GHz to 50GHz		−15		dB
High Band	50GHz to 55GHz		−8		dB
LO Input	50Ω single-ended		−8		dB
IF Output	50Ω single-ended				dB
2GHz to 6GHz			−7		dB
4GHz to 8GHz			−9		dB
6GHz to 10GHz			−9		dB
8GHz to 12GHz			−15		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input High Voltage (V_{INH})		1.2		1.8	V
Input Low Voltage (V_{INL})			0	0.63	V
High and Low Input Current (I_{INH}/I_{INL})			7		µA
Input Capacitance (C_{IN})			0.4		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	Output high current (I_{OH}) = 8mA	1.35			V
Output Low Voltage (V_{OL})	Output low current (I_{OL}) = 8mA			0.45	V
Minimum Hysteresis Window			160		mV
POWER SUPPLIES					
DVDD		1.6	1.8	2	V
VDD_LNA		1.6	1.8	2	V
VDD_RF		1.6	1.8	2	V
VDD_MIX		1.6	1.8	2	V
VDD_LO		1.6	1.8	2	V
VDD_IF		1.6	1.8	2	V
VDD_BG		1.6	1.8	2	V
VDD_IF_2		1.6	1.8	2	V
VDD_BB		1.6	1.8 or 2.5	2.75	V
Supply Current					
IF Mode					
1.8V Supplies	CEN high and RF Band 0		570		mA
	CEN high and RF Band 1		550		mA
	CEN low		65		mA
Baseband Mode					
1.8V Supplies	CEN high and RF Band 0		465		mA
2.5V Supply			125		mA

SPECIFICATIONS

IF MODE

RF_IN Input, High Band

T_C = 25°C, all supply voltages = 1.8V, RF power (P_{RF}) = −45dBm, LO power (P_{LO}) = −5dBm, f_{RF} = 49GHz, IF frequency (f_{IF}) = 8GHz, f_{LO} = 41GHz (upper sideband), maximum gain, RF low-pass filter (LPF) setting = 0x00 (highest cutoff), and RF high-pass filter (HPF) setting = 0x3F (lowest cutoff), unless otherwise noted.

Table 2. RF_IN Input, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL STEP ATTENUATOR (DSA) PERFORMANCE					
Full Attenuation Range	Set DSA2 to DSA5 maximum attenuation		50		dB
Attenuation Step Size	DSA2		6		dB
	DSA3, DSA4, and DSA5		1		dB
Attenuation Step Error	DSA2		±0.2		dB
	DSA3, DSA4, and DSA5		±0.2		dB
RX IF MODE, HIGH BAND, RF_IN PERFORMANCE	RF_IN input pin and IF_OUT output pin				
Conversion Gain			41		dB
Single Sideband Noise Figure			6.2		dB
Input 1 dB Compression (P1dB)			−27		dBm
Input Third-Order Intercept (IP3)	100 MHz tone spacing		−16		dBm
Image Rejection (IMRR)	Uncalibrated		−28		dBc
	Calibrated		−52		dBc

RF_IN Input, Low Band

T_C = 25°C, all supply voltages = 1.8V, P_{RF} = −50dBm, P_{LO} = −5dBm, f_{RF} = 26GHz, f_{IF} = 8GHz, f_{LO} = 34GHz (lower sideband), maximum gain, and RF LPF setting = 0x00 (highest cutoff), unless otherwise noted.

Table 3. RF_IN Input, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA PERFORMANCE					
Full Attenuation Range	Set DSA2 to DSA5 maximum attenuation		52		dB
Attenuation Step Size	DSA2		6		dB
	DSA3, DSA4, and DSA5		1		dB
Attenuation Step Error	DSA2		±0.2		dB
	DSA3, DSA4, and DSA5		±0.2		dB
RX IF MODE, LOW BAND, RF_IN PERFORMANCE	RF_IN input pin and IF_OUT output pin				
Conversion Gain			48		dB
Single Sideband Noise Figure			4.0		dB
Input P1dB			−34		dBm
IP3	100MHz tone spacing		−24		dBm
IMRR	Uncalibrated		−55		dBc
	Calibrated		−80		dBc

SPECIFICATIONS

DSA_IN Input, High Band

T_C = 25°C, all supply voltages = 1.8V, P_{RF} = −40dBm, P_{LO} = −5dBm, f_{RF} = 49GHz, f_{IF} = 8GHz, f_{LO} = 41GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), and RF HPF setting = 0x3F (lowest cutoff), unless otherwise noted.

Table 4. DSA_IN Input, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA PERFORMANCE					
Full Attenuation Range	Set DSA1 to DSA5 maximum attenuation		66		dB
Attenuation Step Size	DSA1		1		dB
	DSA2		6		dB
	DSA3, DSA4, and DSA5		1		dB
Attenuation Step Error	DSA1		±0.2		dB
	DSA2		±0.2		dB
	DSA3, DSA4, and DSA5		±0.2		dB
RX IF MODE, HIGH BAND, DSA_IN PERFORMANCE	DSA_IN input pin, IF_OUT output pin, and DSA_OUT connected by short 50Ω line to RF_IN on PCB				
Conversion Gain			36		dB
Single Sideband Noise Figure			12.0		dB
Input P1dB			−21		dBm
IP3	100 MHz tone spacing		−11		dBm
IMRR	Uncalibrated		−28		dBc
	Calibrated		−52		dBc

DSA_IN Input, Low Band

T_C = 25°C, all supply voltages = 1.8V, P_{RF} = −50dBm, P_{LO} = −5dBm, f_{RF} = 26GHz, f_{IF} = 8GHz, f_{LO} = 34GHz (lower sideband), maximum gain, and RF LPF setting = 0x00 (highest cutoff), unless otherwise noted.

Table 5. DSA_IN Input, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA PERFORMANCE					
Full Attenuation Range	Set DSA1 to DSA5 maximum attenuation		64		dB
Attenuation Step Size	DSA1		1		dB
	DSA2		6		dB
	DSA3, DSA4, and DSA5		1		dB
Attenuation Step Error	DSA1		±0.2		dB
	DSA2		±0.2		dB
	DSA3, DSA4, and DSA5		±0.2		dB
RX IF MODE, LOW BAND, DSA_IN PERFORMANCE	DSA_IN input pin, IF_OUT output pin, and DSA_OUT connected by short 50Ω line to RF_IN on PCB				
Conversion Gain			45		dB
Single Sideband Noise Figure			9.0		dB
Input P1dB			−30		dBm
IP3	100MHz tone spacing		−19		dBm
IMRR	Uncalibrated		−55		dBc
	Calibrated		−80		dBc

SPECIFICATIONS

I/Q BASEBAND MODE

DSA_IN Input, High Band

T_C = 25°C, VDD_BB = 2.5V, all other supply voltages = 1.8V, P_{RF} = −40dBm, P_{LO} = −5dBm, f_{RF} = 49GHz, baseband frequency (f_{BB}) = 100MHz, f_{LO} = 48.9GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), and V_{OCM} setting = 0x0C, unless otherwise noted.

Measurements performed with high gain settings (Register 0x194, Bits[1:0], = 0b'11) with on-board matching network, unless otherwise noted. Measurements performed as single-ended measurements on BB_IP output only, with other outputs BB_IN, BB_QP, and BB_QN terminated in 50Ω loads, unless otherwise noted. Data is corrected for 8.15dB of output matching-network loss and 3dB of differential loss, unless otherwise noted.

Table 6. DSA_IN Input, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA PERFORMANCE					
Full Attenuation Range	Set DSA1 to DSA3 maximum attenuation		36		dB
Attenuation Step Size	DSA1		1		dB
	DSA2		6		dB
	DSA3		1		dB
Attenuation Step Error	DSA1		±0.2		dB
	DSA2		±0.2		dB
	DSA3		±0.2		dB
RX I/Q BASEBAND MODE, HIGH BAND, DSA_IN PERFORMANCE	DSA_IN input pin, BB_IP output pin with other baseband outputs terminated, and DSA_OUT connected by short 50Ω line to RF_IN on PCB				
Conversion Gain					
Gain Setting High	For 50Ω operation		12		dB
Gain Stetting Low	For 100Ω operation		6		dB
Noise Figure, Single Sideband	Measured with output balun combining BB_IP and BB_IN, corrected −3dB for single sideband				
f_{BB} > 1GHz	Thermal noise floor		12.3		dB
f_{BB} < 100MHz	1/f noise corner		15.3		dB
Input P1dB			−7.5		dBm
IP3	100MHz tone spacing		0		dBm
Baseband Quadrature Imbalance	0GHz to 8GHz				
Amplitude			±0.8		dB
Phase			±5		Degrees

SPECIFICATIONS

DSA_IN Input, Low Band

T_C = 25°C, VDD_BB = 2.5V, all other supply voltages = 1.8V, P_{RF} = −45dBm, P_{LO} = −5dBm, f_{RF} = 29GHz, f_{BB} = 100MHz, f_{LO} = 29.1GHz (lower sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), and V_{OCM} setting = 0x0C, unless otherwise noted.

Measurements performed with high gain settings (Register 0x194, Bits[1:0] = 0b'11) with on-board matching network, unless otherwise noted. Measurements performed as single-ended measurements on BB_IP output only, with other outputs BB_IN, BB_QP, and BB_QN terminated in 50Ω loads, unless otherwise noted. Data is corrected for 8.15dB of output matching-network loss and 3dB of differential loss, unless otherwise noted.

Table 7. DSA_IN Input, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DSA PERFORMANCE					
Full Attenuation Range	Set DSA1 to DSA3 maximum attenuation		37		dB
Attenuation Step Size	DSA1		1		dB
	DSA2		6		dB
	DSA3		1		dB
Attenuation Step Error	DSA1		±0.2		dB
	DSA2		±0.2		dB
	DSA3		±0.2		dB
RX I/Q BASEBAND MODE, HIGH BAND, DSA_IN PERFORMANCE	DSA_IN input pin, BB_IP output pin with other baseband outputs terminated, and DSA_OUT connected by short 50Ω line to RF_IN on PCB				
Conversion Gain					
Gain Setting High	For 50Ω operation		22.5		dB
Gain Setting Low	For 100Ω operation		17		dB
Input P1dB			−15		dBm
IP3	100MHz tone spacing		−6.5		dBm
Baseband Quadrature Imbalance	0GHz to 8GHz				
Amplitude			±0.8		dB
Phase			5		Degrees

SPECIFICATIONS

TIMING SPECIFICATIONS

See the Timing Diagrams Overview section, the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional information.

Table 8. Timing Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_1	1		100	ms	Power supplies 10% to 90% rise time.
t_2	10			ns	Power supplies 90% level to valid digital input time ($t_{DIGITAL}$). Do not set any logic input levels high prior to $t_{DIGITAL}$. The $\overline{RST}$ and $\overline{CS}$ can go high together after t_2 has transpired. If CHIP_ADD0 and CHIP_ADD1 are to be set externally, then set them to the desired logic levels after t_2 and prior to any SPI instructions.
t_3	10			ns	$\overline{RST}$ rising edge to $\overline{CS}$ falling edge (first SPI instruction after reset). Waiting t_3 ensures that the digital logic has reset to the default values.
t_4	5			ns	$\overline{CS}$ falling edge to $\overline{SCLK}$ rising edge setup time.
t_5	10			ns	SCLK cycle time (write).
t_5	20			ns	SCLK cycle time (read).
t_6	2.5			ns	SCLK high time.
t_7	2.5			ns	SCLK low time.
t_8	3			ns	SDI data setup time.
t_9	2			ns	SDI data hold time.
t_{10}	5			ns	SCLK rising edge to $\overline{CS}$ hold time.
t_{11}	5			ns	Minimum $\overline{CS}$ high time for latching in data (for multiple SPI transactions).
t_{12}	5			ns	$\overline{CS}$ rising edge to next SCLK rising edge ignore.
t_{13}		4		ns	SCLK falling edge to SDO valid (load capacitance (C_L) = 10pF).
t_{14}		5		ns	SDO rise and fall time (C_L = 10pF).
t_{15}		4		ns	$\overline{CS}$ rising edge to SDO tristate (C_L = 10pF).
t_{16}	10			ns	Time from final initialization SPI instruction to entering the operational time ($t_{OPERATIONAL}$). Set CEN to logic high at this time.
t_{17}	5			ns	$\overline{CS}$ rising edge to LOAD pin first rising edge time for loading filter contents.
t_{18}	10			ns	LOAD pin high time for loading the filter and DSA contents.
t_{19}	10			ns	LOAD pin low time for preparing to load the DSA offsets.
t_{20}	10			ns	LOAD pin high time for loading the DSA offsets.
t_{21}	0			ns	$\overline{CS}$ falling edge to LOAD pin falling edge time. Both can be set low at the same time after a load operation has been completed (after t_{18} or t_{20}) and another SPI instruction is desired.
t_{22}	10			ns	Time from the last SPI instruction when the chip is operational ($t_{CONTINUE}$) to the disable time ($t_{DISABLE}$). After t_{22} has transpired, set CEN to logic low to disable the chip.
t_{23}	3			µs	CEN falling edge to $\overline{RST}$ falling edge. Waiting t_{23} ensures that the RF portions of the chip have been allowed to power down prior to chip reset.
t_{24}	10			ns	$\overline{RST}$ low time to perform reset.
t_{25}	3			µs	CEN falling edge to the power-down time ($t_{POWER-DOWN}$). Waiting t_{25} ensures that the RF portions of the chip have been allowed to power down prior to shutting down the chip power.
t_{26}			10	µs	Logic inputs fall time. The logic inputs and power supplies can be turned off at the same time.
t_{27}	1		100	ms	Power supplies 90% to 10% fall time.

ABSOLUTE MAXIMUM RATINGS

Table 9. Absolute Maximum Ratings for 10 Year Lifetime

Parameter	Rating
Supply Voltage	
2.5V Supply	2.75V
1.8V Supply	2V
Digital Input and Output Voltages	
1.8V Supply	2V
LO Input Power	0dBm
RF Input Power[1]	See Table 10, Table 11, Table 12, and Table 13 for additional information
Temperature	
Maximum Junction (T_J)	125°C
Maximum Storage Range	−65°C to +150°C
Operating T_C Range	−40°C to +95°C
Maximum Power Dissipation	1.4W
Moisture Sensitivity Level (MSL) Rating[2]	MSL3

[1] The RF input power rating assumes a peak to average ratio of 10dB.

[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Table 10. RF Input Power Ratings, IF Mode, 10 Year Lifetime

	RF Band	
Parameter	Low (dBm)	High (dBm)
CEN = Low		
RF_IN	+4	+4
DSA_IN at DSA1 ≤ 13	+8 + DSA1 Value	+8 + DSA1 Value
DSA_IN at DSA1 ≥ 14	+22	+22
CEN = High		
RF_IN for All DSAs Combined		
At Maximum Gain	−41	−34
At Minimum Gain	−9	−9
RF_IN for Each DSA Set to Its Maximum Attenuation		
DSA2	−35	−28
DSA3	−26	−19
DSA4	−26	−19
DSA5	−26	−19
DSA_IN for All DSAs Combined		
At Maximum Gain	−37	−30
At Minimum Gain	−5	−5
DSA_IN for Each DSA Set to Its Maximum Attenuation		
DSA1	−22	−15
DSA2	−32	−24
DSA3	−22	−15
DSA4	−22	−15
DSA5	−22	−15

Table 11. RF Input Power Ratings, I/Q Baseband Mode, 10 Year Lifetime

	RF Band	
Parameter	Low (dBm)	High (dBm)
CEN = Low		
RF_IN	+4	+4
DSA_IN at DSA1 ≤ 13	+8 + DSA1 Value	+8 + DSA1 Value
DSA_IN at DSA1 ≥ 14	+22	+22
CEN = High		
RF_IN for All DSAs Combined		
At Maximum Gain	−26	−16
At Minimum Gain	−9	−9
RF_IN for Each DSA Set to Its Maximum Attenuation		
DSA2	−21	−11
DSA3	−21	−11
DSA_IN for All DSAs Combined		
At Maximum Gain	−22	−12
At Minimum Gain	−5	−5
DSA_IN for Each DSA Set to Its Maximum Attenuation		
DSA1	−7	−2
DSA2	−17	−7
DSA3	−17	−7

ABSOLUTE MAXIMUM RATINGS

Table 12. RF Input Power Ratings, IF Mode, 2 Hour Lifetime

	RF Band	
Parameter	**Low (dBm)**	**High (dBm)**
CEN = Low		
RF_IN	+7	+7
DSA_IN at DSA1 ≤ 10	+11 + DSA1 Value	+11 + DSA1 Value
DSA_IN at DSA1 ≥ 11	+22	+22
CEN = High		
RF_IN for All DSAs Combined		
At Maximum Gain	−35	−28
At Minimum Gain	0	0
RF_IN for Each DSA Set to Its Maximum Attenuation		
DSA2	−29	−22
DSA3	−20	−13
DSA4	−20	−13
DSA5	−20	−13
DSA_IN for All DSAs Combined		
At Maximum Gain	−31	−24
At Minimum Gain	+4	+4
DSA_IN for Each DSA Set to Its Maximum Attenuation		
DSA1	−16	−16
DSA2	−25	−18
DSA3	−16	−9
DSA4	−16	−9
DSA5	−16	−9

Table 13. RF Input Power Ratings, I/Q Baseband Mode, 2 Hour Lifetime

	RF Band	
Parameter	**Low (dBm)**	**High (dBm)**
CEN = Low		
RF_IN	+7	+7
DSA_IN at DSA1 ≤ 13	+11 + DSA1 Value	+11 + DSA1 Value
DSA_IN at DSA1 ≥ 11	+22	+22
CEN = High		
RF_IN for All DSAs Combined		
At Maximum Gain	−20	−10
At Minimum Gain	0	0
RF_IN for Each DSA Set to Its Maximum Attenuation		
DSA2	−15	−5
DSA3	−15	−5
DSA_IN for All DSAs Combined		
At Maximum Gain	−16	−6
At Minimum Gain	+4	+4
DSA_IN for Each DSA Set to Its Maximum Attenuation		
DSA1	−1	+4
DSA2	−11	−1
DSA3	−11	−1

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ABSOLUTE MAXIMUM RATINGS

THERMAL RESISTANCE

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC_TOP} is thermal resistance, junction to case (°C/W).

Only use θ_{JC_TOP} to compare the thermal performance of different packages when all test conditions listed are similar to JEDEC specifications. Otherwise, use Ψ_{JT} and Ψ_{JB} to calculate the device junction temperature using the following equations:

$$T_J = (P \times \Psi_{JT}) + T_{TOP}$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JT} is the junction to top thermal characterization number.
T_{TOP} is the package top temperature (°C). T_{TOP} is measured at the top center of the package.

$$T_J = (P \times \Psi_{JB}) + T_{BOARD}$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JB} is the junction to board thermal characterization number.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package, no more than 1 mm from the edge of the package body (°C).

As stated in JEDEC51-12, only use the previous equations when no heat sink or a heat spreader is present. When a heat sink or heat spreader is added, use θ_{JC_TOP} to estimate or calculate the junction temperature.

Table 14 shows the temperature rise from case to junction (T_{RISE_JC}) based on a power map based on a JEDEC (JESD51-2) board, as opposed to a JEDEC standard of uniform power dissipation across the ADMV1455 package. T_{RISE_JC} applies to all conditions of operation and results in a higher calculated junction temperature. However, T_{RISE_JC} results in a more accurate calculation of the junction temperature on a JEDEC board with the ADMV1455.

To calculate $T_{BOARD,max}$ (maximum case temperature referred to the bottom of the package or the nearest point on the board to the package), use the following equations and refer to Figure 2:

$$T_{BOARD,\,MAX} = T_{J,\,MAX} - T_{RISE\_JC} - P \times \theta_{JC\_BOT} \quad (1)$$

If the bottom side is applied to the PCB bottom surface then the following:

$$T_{BOARD} = T_{BASE\_PLATE} + P \times \theta_{BOARD} + P \times \theta_{TIM} \quad (2)$$

where:
P is the total power dissipation in the chip (W).
$T_{J,\,MAX}$ is the maximum junction temperature (°C) in Table 9.
$T_{BOARD,\,MAX}$ is the maximum board temperature measured on the midpoint of the longest side of the package no more than 1 mm from the edge of the package body (°C).
T_{RISE_JC} is the highest temperature rise (°C) from case to junction in Table 14.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package no more than 1 mm from the edge of the package body (°C).
T_{BASE_PLATE} is the temperature of the base plate of the heatsink.
θ_{TIM} is the thermal resistance (°C/W) of the TIM.
θ_{BOARD} is the thermal resistance (°C/W) of the board.
θ_{JC_BOT} is the junction to top case thermal resistance (°C/W) in Table 15.

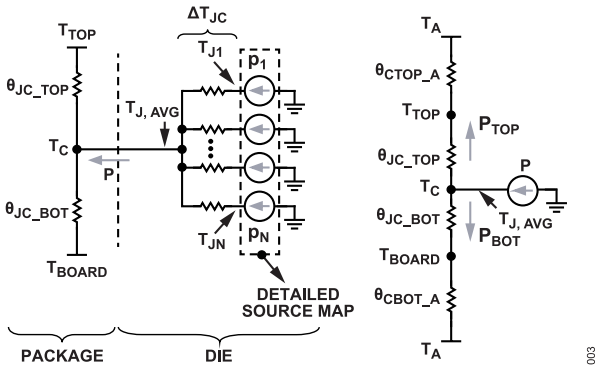

Figure 2. Circuit Level Description of Power Map (Left) and Uniform Power Dissipation Methods (Right)

Table 14. Temperature Rise Based on a Power Map

Package Type[1]	T_{RISE_JC}	Unit
BC-120-4	20	°C

[1] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

The thermal resistance of the ADMV1455 assuming the JEDEC standard of uniform power dissipation based on a JEDEC (JESD51-2) board is shown in Table 15. Thermal resistance based on a uniform power dissipation is useful to compare the performance of the ADMV1455 to other similar ICs.

Table 15. Thermal Resistance Based on Uniform Power Dissipation

Package Type	θ_{JC_BOT}[1]	θ_{JC_TOP}[2]	Ψ_{JT}	Ψ_{JB}	θ_{JA}	Unit
BC-120-4	2.3	3.0	0.1	7.3	24.3	°C/W

[1] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

[2] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADMV1455

Table 16. ADMV1455, 120-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	750	1B
FICDM	500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

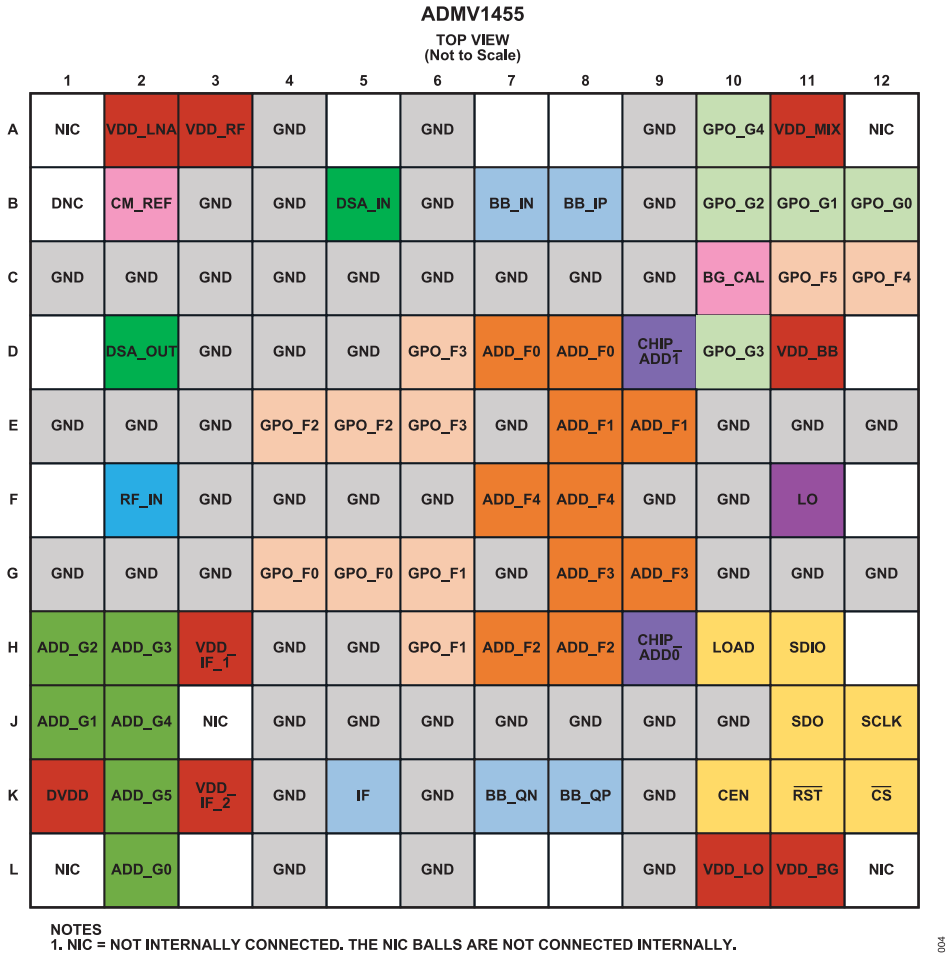

Figure 3. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A12, J3, L1, L12	NIC	Not Internally Connected. The NIC balls are not connected internally. It is acceptable to ground these balls if the application or implementation requires it.
A2	VDD_LNA	LNA Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_LNA.
A3	VDD_RF	RF Amplifier Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_RF.
A4, A6, A9, B3, B4, B6, B9, C1 to C9, D3 to D5, E1 to E3, E7, E10 to E12, F3 to F6, F9, F10, G1 to G3, G7, G10 to G12, H4, H5, J4 to J10, K4, K6, K9, L4, L6, L9	GND	Ground. Tie all GND balls together to a low impedance plane on the PCB.
A10	GPO_G4	General-Purpose Digital Output Ball Gain 4. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
A11	VDD_MIX	Mixer Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_MIX.
B1	DNC	Do Not Connect. Do not connect to or ground the DNC ball.
B2	CM_REF	I/Q Baseband Common-Mode Reference Voltage Input. When the internal common-mode voltage reference is used, the CM_REF ball can float. When setting the common-mode voltage externally, use the CM_REF ball and place a 0.01µF decoupling capacitor close to CM_REF. Do not ground CM_REF.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
B5	DSA_IN	DSA1 RF Input. The DSA_IN ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to DSA_IN. If required, place a DC-blocking capacitor in series with DSA_IN and ensure that any capacitor parasitic attributes are acceptable for the operating frequency range. If DSA1 is not used, the DSA_IN can float.
B7, B8	BB_IN, BB_IP	Differential Baseband I Outputs. The outputs are internally DC-coupled with a 75Ω differential output impedance, which allows the outputs to interface with either a 50Ω or 100Ω differential load impedance. The common-mode voltage range is from 0.8V to 1.5V when VDD_BB = 2.5V and from 0.8V to 1.1V when VDD_BB = 1.8V. When operating in the IF mode, BB_IN and BB_IP can float.
B10	GPO_G2	General-Purpose Digital Output Ball Gain 2. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
B11	GPO_G1	General-Purpose Digital Output Ball Gain 1. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
B12	GPO_G0	General-Purpose Digital Output Ball Gain 0. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
C10	BG_CAL	Band-Gap Reference Calibration. BG_CAL is used for factory and debug purposes. This ball can be left floating or be tied to a 3.48kΩ, 1%, resistor. Do not ground this ball.
C11	GPO_F5	General-Purpose Digital Output Ball Filter 5. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
C12	GPO_F4	General-Purpose Digital Output Ball Filter 4. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
D2	DSA_OUT	DSA1 RF output pin. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to DSA_OUT. If needed, place a DC-blocking capacitor in series with DSA_OUT, and be sure any capacitor parasitic attributes are acceptable for the operating frequency range. If DSA1 is not used, the DSA_OUT can float.
D6, E6	GPO_F3	General-Purpose Digital Output Ball Filter 3. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
D7, D8	ADD_F0	Frequency LUT Address Bit 0. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie to logic output from a microcontroller or field-programmable gate array (FPGA); do not float. If ADDF0 is not used to set the look-up table address pointer, then please ground this ball.
D9	CHIP_ADD1	Chip Address Bit 1. Active high, 1.8V logic. CHIP_ADD1 is internally pulled high through 15kΩ. This ball can be dynamically set by logic output from a microcontroller or FPGA. For fixed addressing implementations, set high by leave this ball floating, and set low by ground this ball. For single chip implementations, always ground this ball.
D10	GPO_G3	General-Purpose Digital Output Ball Gain 3. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
D11	VDD_BB	Baseband Supply Voltage. For I/Q baseband mode, the nominal voltage is 2.5V, but this voltage can be set to 1.8V if a lower gain is acceptable. The maximum P1dB performance is obtained by using 2.5V. For the IF mode, the voltage can be 1.8V or 2.5 V, with no change in performance. Place 0.01µF and 1µF decoupling capacitors close to VDD_BB.
E4, E5	GPO_F2	General-Purpose Digital Output Ball Filter 2. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
E8, E9	ADD_F1	Frequency LUT Address Bit 1. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie to logic output from a microcontroller or FPGA; do not float. If ADDF1 is not used to set the look-up table address pointer, then please ground this ball.
F2	RF_IN	RF input. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to RF_IN. If needed, place a DC-blocking capacitor in series with RF_IN, and be sure any capacitor parasitic attributes are acceptable for the operating frequency range. When using DSA1, connect RF_IN directly to DSA_OUT.
F7, F8	ADD_F4	Frequency LUT Address Bit 4. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie to logic output from a microcontroller or FPGA; do not float. If ADDF4 is not used to set the look-up table address pointer, then please ground this ball.
F11	LO	LO input. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to LO. If needed, place a DC-blocking capacitor in series with LO, and be sure any capacitor parasitic attributes are acceptable for the operating frequency range.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
G4, G5	GPO_F0	General-Purpose Digital Output Ball Filter 0. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
G6, H6	GPO_F1	General-Purpose Digital Output Ball Filter 1. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
G8, G9	ADD_F3	Frequency LUT Address Bit 3. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F3 to the logic output from a microcontroller or FPGA; do not float. If ADD_F3 is not used to set the LUT address pointer, ground this ball.
H1	ADD_G2	Gain LUT Address Bit 2. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G2 to the logic output from a microcontroller or FPGA; do not float. If ADD_G2 is not used to set the LUT address pointer, ground this ball.
H2	ADD_G3	Gain LUT Address Bit 3. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G2 to the logic output from a microcontroller or FPGA; do not float. If ADD_G3 is not used to set the LUT address pointer, ground this ball.
H3	VDD_IF_1	IF Chain Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_IF.
H7, H8	ADD_F2	Frequency LUT Address Bit 2. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F2 to the logic output from a microcontroller or FPGA; do not float. If ADD_F2 is not used to set the LUT address pointer, ground this ball.
H9	CHIP_ADD0	Chip Address Bit 0. Active high, 1.8V logic. CHIP_ADD0 is internally pulled high through 15kΩ. This ball can be dynamically set by the logic output from a microcontroller or FPGA. For fixed addressing implementations, set high by leaving this ball floating and set low by grounding this ball. For single chip implementations, always ground this ball.
H10	LOAD	Load Synchronous Toggle. Active high, 1.8V logic. When the LOAD feature is enabled, transitioning the LOAD ball from a logic low to logic high causes content in the filter and gain registers to be sent to the working registers. Return the LOAD ball to logic low when the loading operation completes, see Figure 168 for more information. No internal pull-up or pull-down resistance. Tie LOAD to the logic output from a microcontroller or FPGA; do not float. If LOAD feature is not used, ground this ball.
H11	SDIO	SPI Data Input and Output. Active high, 1.8V logic. For 3-wire SPI implementation, SDIO is bidirectional. For 4-wire SPI implementation, SDIO is only used for data input.
J1	ADD_G1	Gain LUT Address Bit 1. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G1 to the logic output from a microcontroller or FPGA; do not float. If ADD_G1 is not used to set the LUT address pointer, ground this ball.
J2	ADD_G4	Gain LUT Address Bit 4. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G4 to the logic output from a microcontroller or FPGA; do not float. If ADD_G4 is not used to set the LUT address pointer, ground this ball.
J11	SDO	SPI Data Output. Active high, 1.8V logic. For 4-wire SPI implementations, SPI data is read using the SDO ball. If SDO is not used, float this ball.
J12	SCLK	SPI Clock Input. Active high, 1.8V logic. During SPI write transactions, data is sampled on the rising edge of SCLK. During SPI read transactions, output data changes at the falling edge of SCLK.
K1	DVDD	Digital Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to DVDD.
K2	ADD_G5	Gain LUT Address Bit 5. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G5 to the logic output from a microcontroller or FPGA; do not float. If ADD_G5 is not used to set the LUT address pointer, ground this ball.
K3	VDD_IF_2	IF Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_IF_2.
K5	IF	IF Output. The IF ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to the IF ball. If required, place a DC-blocking capacitor in series with IF and ensure that any capacitor parasitic attributes are acceptable for the operating frequency range.
K7, K8	BB_QN, BB_QP	Differential Baseband Q Outputs. The outputs are internally DC-coupled with a 75Ω differential output impedance, which allows the outputs to interface with either a 50Ω or 100Ω differential load impedance. The common-mode voltage range is from 0.8V to 1.5V when VDD_BB = 2.5V and from 0.8V to 1.1V when VDD_BB = 1.8V. When operating in IF mode, BB_QN and BB_QP can float.
K10	CEN	Chip Enable. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie CEN to the logic output from a microcontroller, FPGA, or power sequencer; do not float. The CEN pin must be held low until all supply voltages have been turned on and $\overline{\text{RST}}$ has been set high.
K11	$\overline{\text{RST}}$	Chip Reset. Active low, 1.8V logic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 17. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
K12	$\overline{CS}$	SPI Chip Select. Active low, 1.8V logic. Bring $\overline{CS}$ low to begin a SPI transaction, see Figure 167 and Figure 168 for more information.
L2	ADD_G0	Gain LUT Address Bit 0. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G0 to the logic output from a microcontroller or FPGA; do not float. If ADD_G0 is not used to set the LUT address pointer, ground this ball.
L10	VDD_LO	LO Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_LO.
L11	VDD_BG	Band-Gap Reference Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_BG. Ideally for proper NVM load operation, apply the VDD_BG voltage after all other supplies have been turned on and $\overline{RST}$ has been set high. If this is not possible, as is the case if all supply voltages are applied together, ensure to set $\overline{RST}$ high and run the NVM refresh commands.

TYPICAL PERFORMANCE CHARACTERISTICS

IF MODE, RF_IN, HIGH BAND

All measurements use RF_IN as an input and IF as an output, with the RF high-band settings. The supply voltage = 1.8V (all supplies) and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{RF} = −45dBm, P_{LO} = −5dBm, f_{RF} = 49GHz, f_{IF} = 8GHz, f_{LO} = 41GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), IF band-pass filter (BPF) settings = 8GHz (see Table 24), and LO tunable filter wideband high settings (see Table 22), unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the RF and IF input and output pins in Figure 3).

Conversion Gain

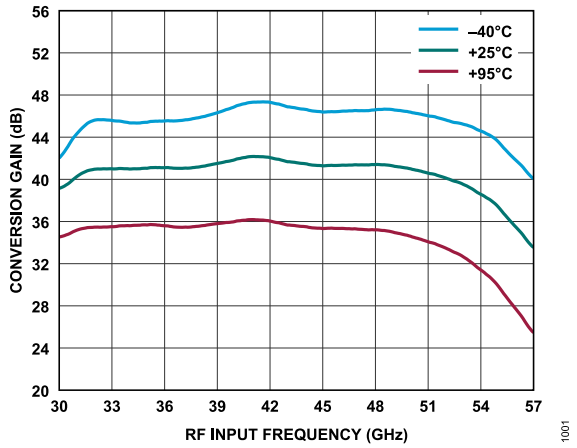

Figure 4. Conversion Gain vs. RF Input Frequency at Various Temperatures

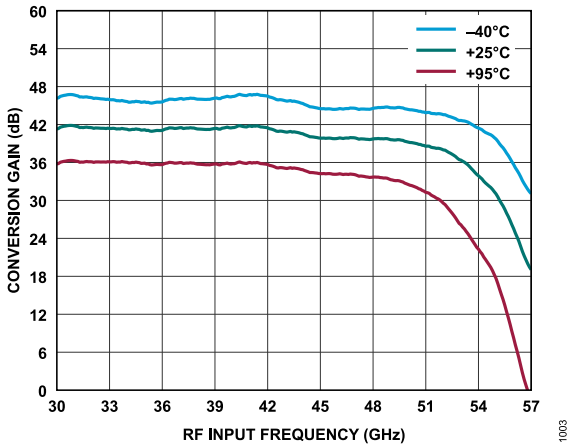

Figure 6. Conversion Gain vs. RF Input Frequency at Various Temperatures, LO Filter Wideband Low Setting

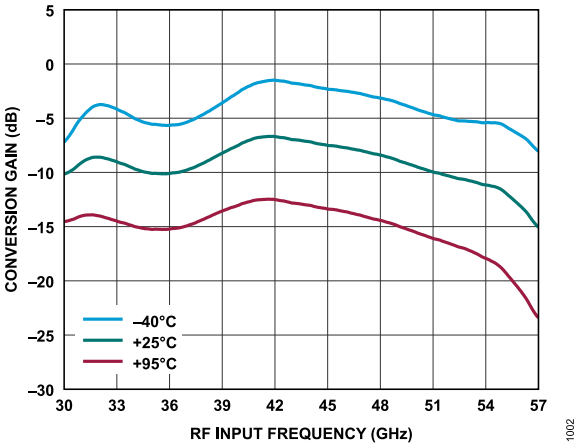

Figure 5. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

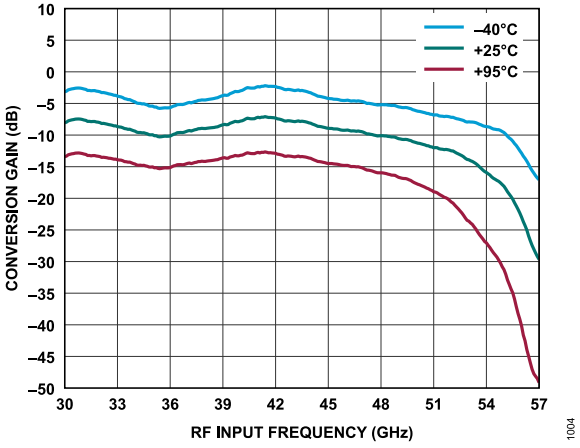

Figure 7. Conversion Gain vs. RF Input Frequency at Various Temperatures, LO Filter Wideband Low Setting, Minimum Gain

TYPICAL PERFORMANCE CHARACTERISTICS

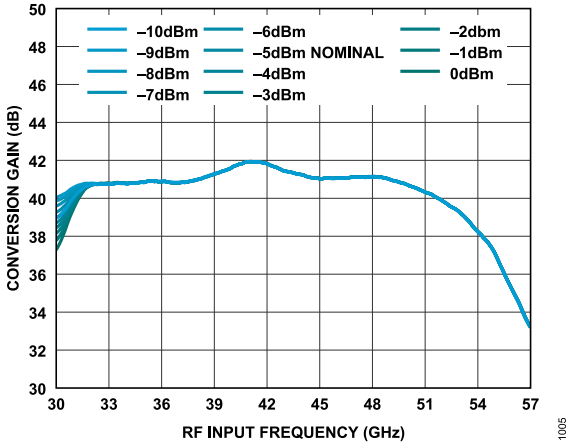

Figure 8. Conversion Gain vs. RF Input Frequency at Various LO Powers

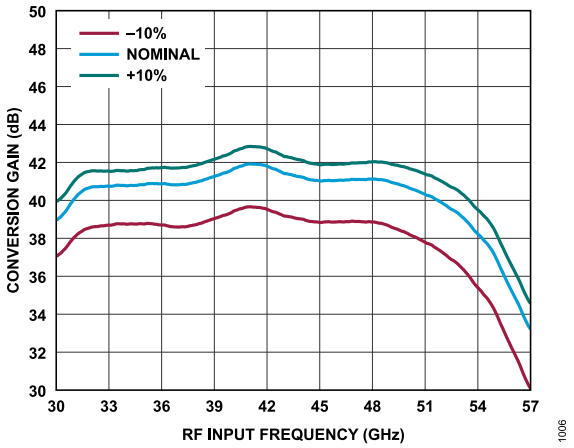

Figure 9. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

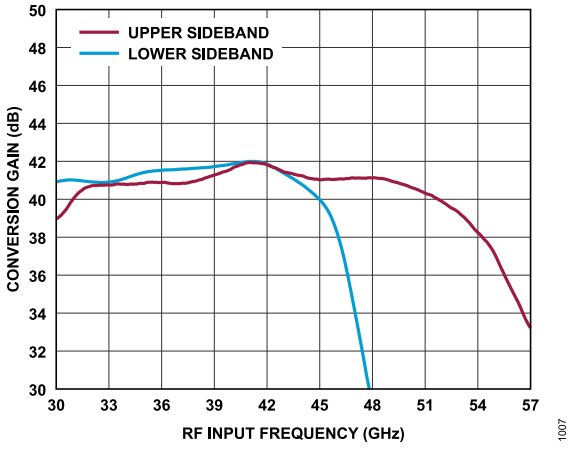

Figure 10. Conversion Gain vs. RF Input Frequency, Upper Sideband and Lower Sideband

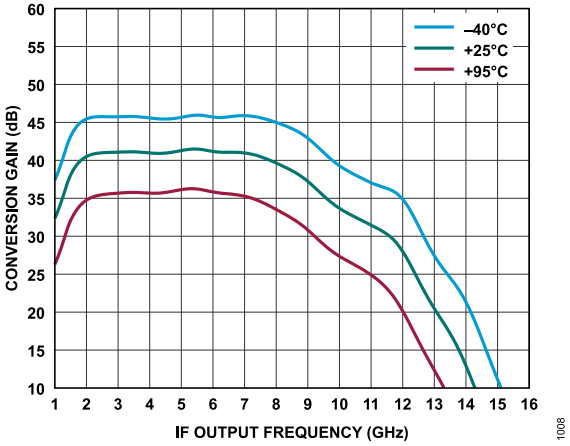

Figure 11. Conversion Gain vs. IF Output Frequency at Various Temperatures, 4GHz IF Filter

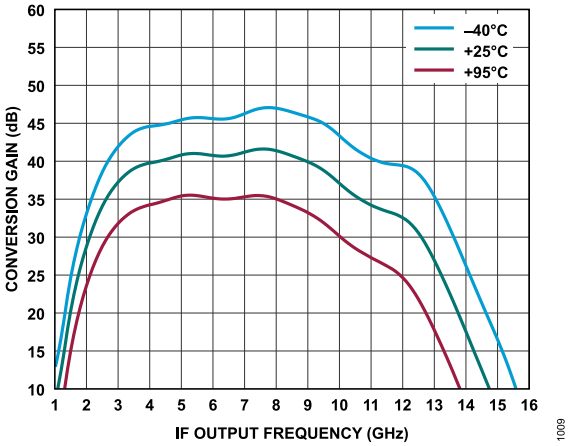

Figure 12. Conversion Gain vs. IF Output Frequency at Various Temperatures, 6GHz IF Filter

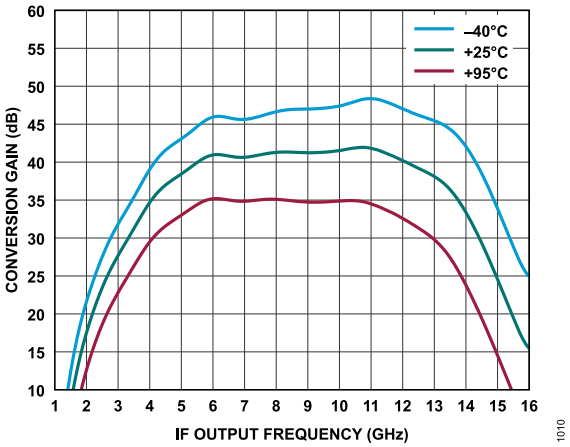

Figure 13. Conversion Gain vs. IF Output Frequency at Various Temperatures, 8GHz IF Filter

TYPICAL PERFORMANCE CHARACTERISTICS

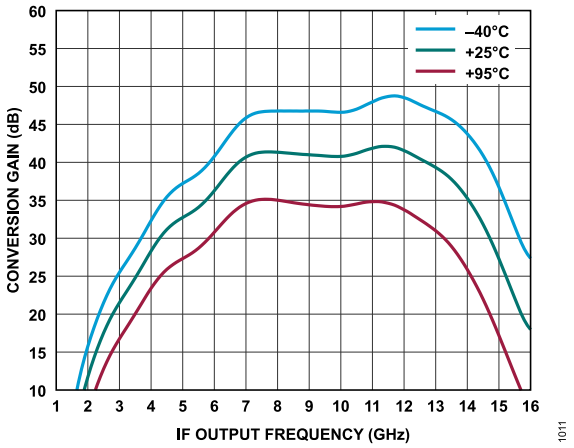

Figure 14. Conversion Gain vs. IF Output Frequency at Various Temperatures, 10GHz IF Filter

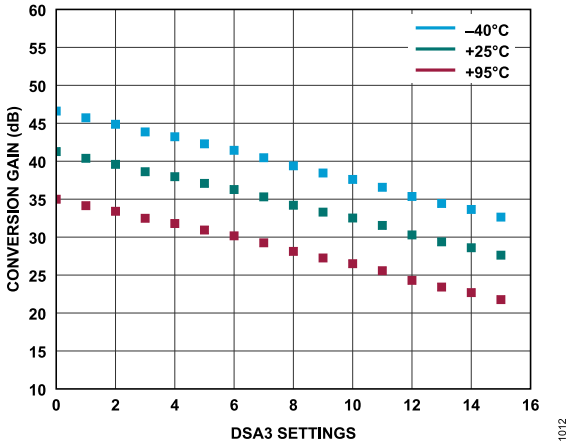

Figure 15. Conversion Gain vs. DSA3 Settings at Various Temperatures, Single f_{RF} = 49GHz

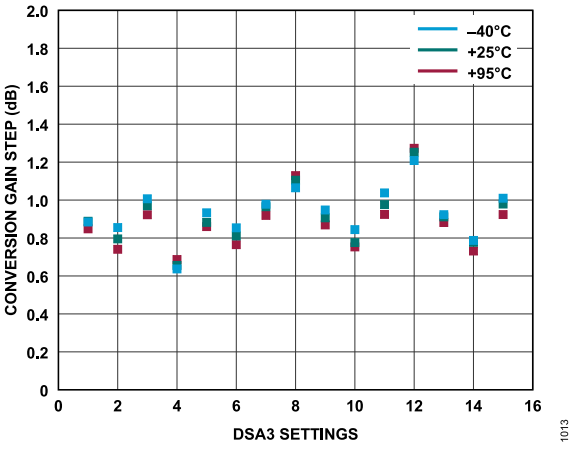

Figure 16. Conversion Gain Step vs. DSA3 Settings at Various Temperatures, Single f_{RF} = 49GHz

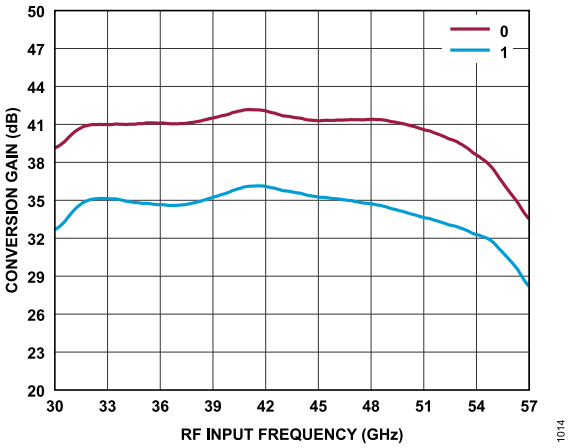

Figure 17. Conversion Gain vs. RF Input Frequency at Various DSA2 Settings

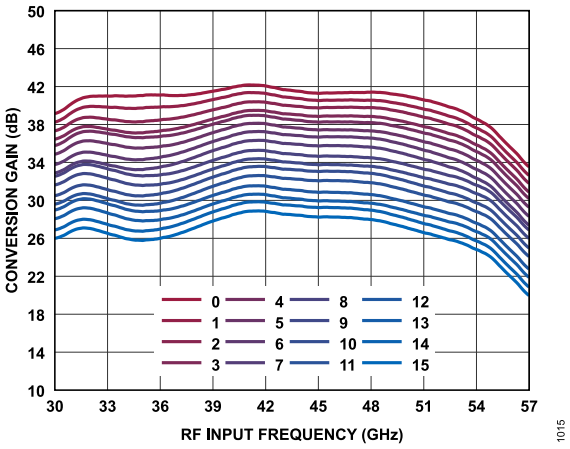

Figure 18. Conversion Gain vs. RF Input Frequency at Various DSA3 Settings

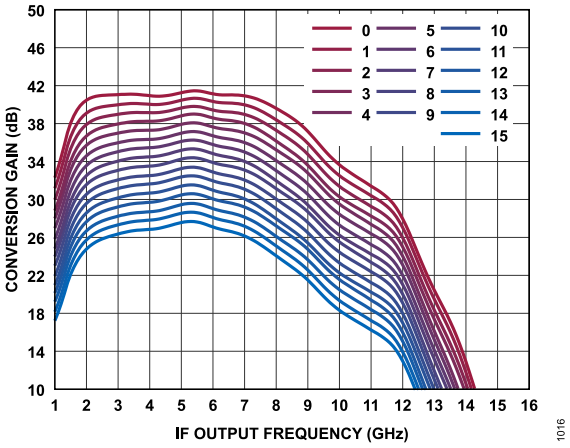

Figure 19. Conversion Gain vs. IF Output Frequency at Various DSA4 Settings, 4GHz IF Filter

TYPICAL PERFORMANCE CHARACTERISTICS

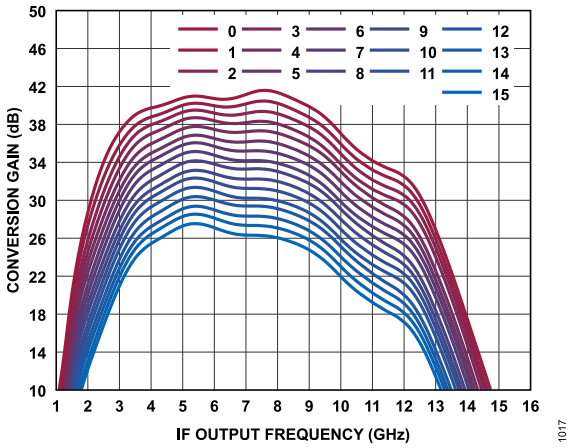

Figure 20. Conversion Gain vs. IF Output Frequency at Various DSA4 Settings, 6GHz IF Filter

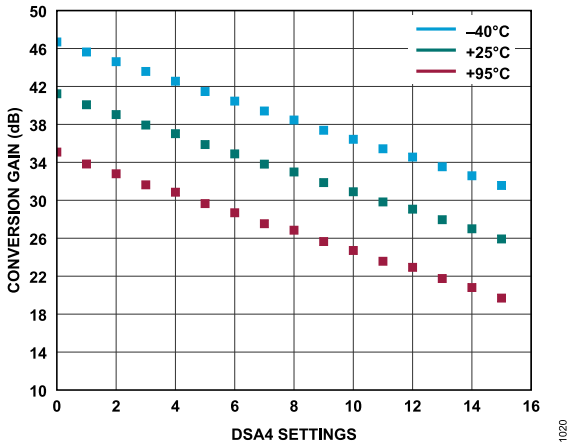

Figure 23. Conversion Gain vs. DSA4 Settings at Various Temperatures, Single f_{RF} = 49GHz

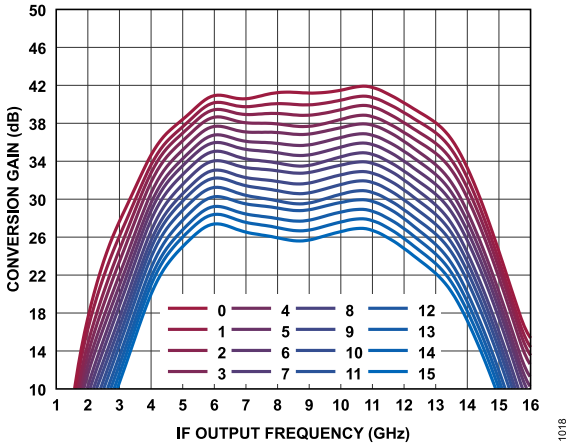

Figure 21. Conversion Gain vs. IF Output Frequency at Various DSA4 Settings, 8GHz IF Filter

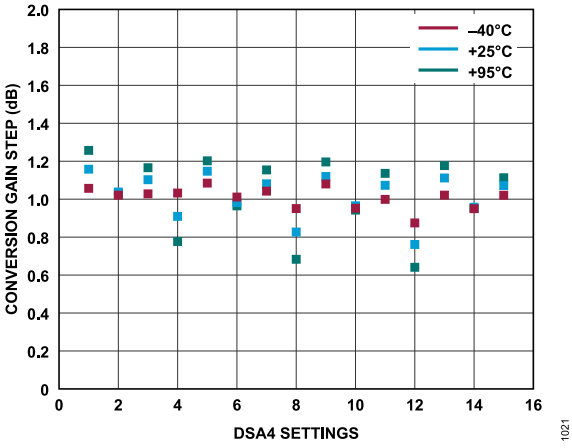

Figure 24. Conversion Gain Step vs. DSA4 Settings at Various Temperatures, Single f_{RF} = 49GHz

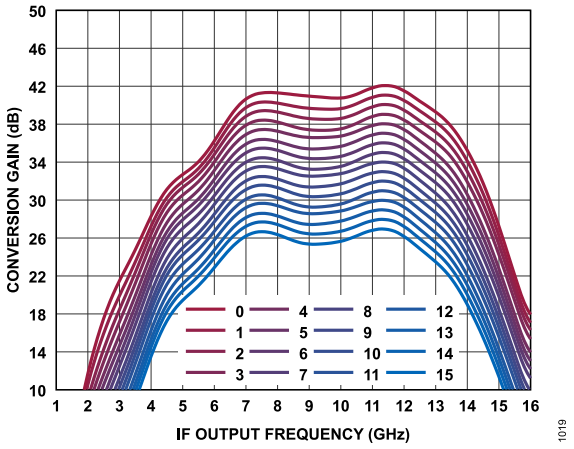

Figure 22. Conversion Gain vs. IF Output Frequency at Various DSA4 Settings, 10GHz IF Filter

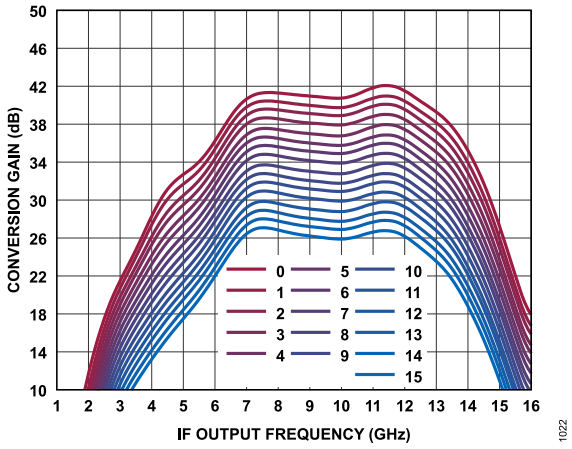

Figure 25. Conversion Gain vs. IF Output Frequency at Various DSA5 Settings, 10GHz IF Filter

TYPICAL PERFORMANCE CHARACTERISTICS

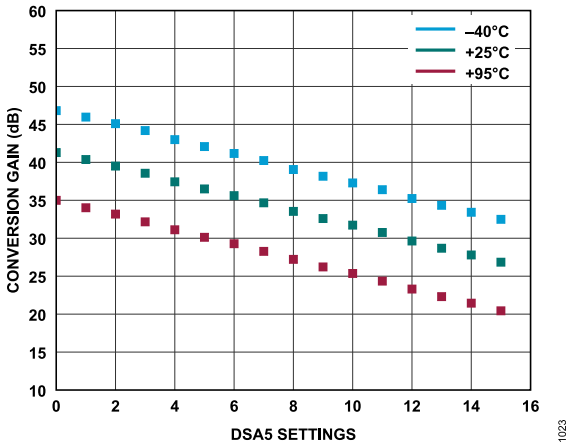

Figure 26. Conversion Gain vs. DSA5 Settings at Various Temperatures, Single f_{RF} = 49GHz, Single f_{IF} = 10GHz

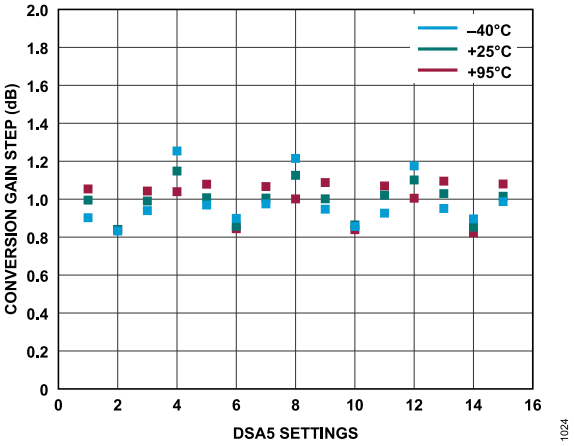

Figure 27. Conversion Gain Step vs. DSA5 Settings at Various Temperatures, Single f_{RF} = 49GHz, Single f_{IF} = 10GHz

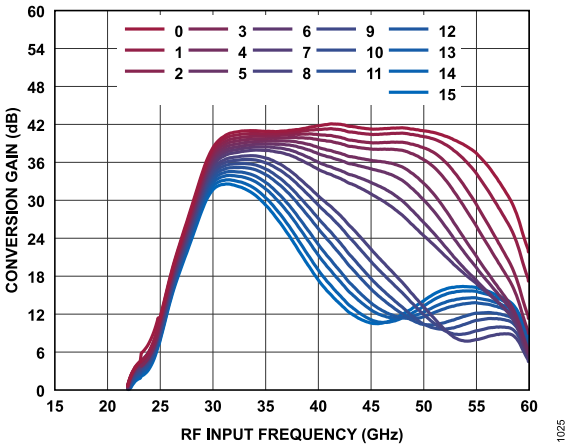

Figure 28. Conversion Gain vs. RF Input Frequency at Various RF Low-Pass Filter Settings

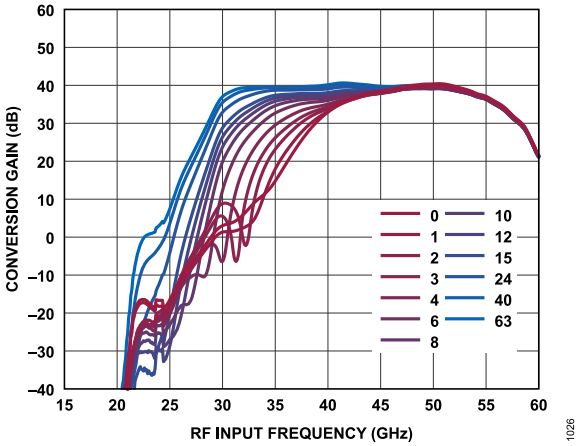

Figure 29. Conversion Gain vs. RF Input Frequency at Various RF High-Pass Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

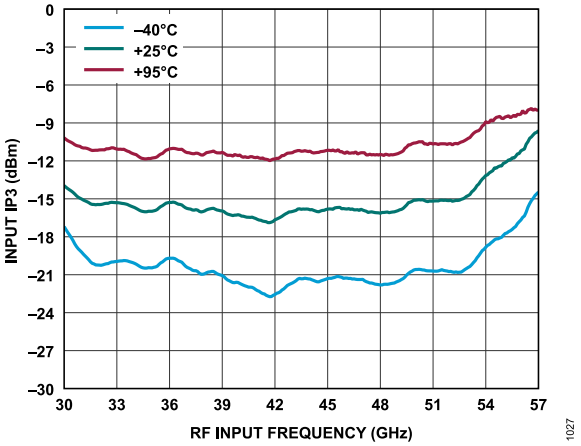

Figure 30. Input IP3 vs. RF Input Frequency at Various Temperatures

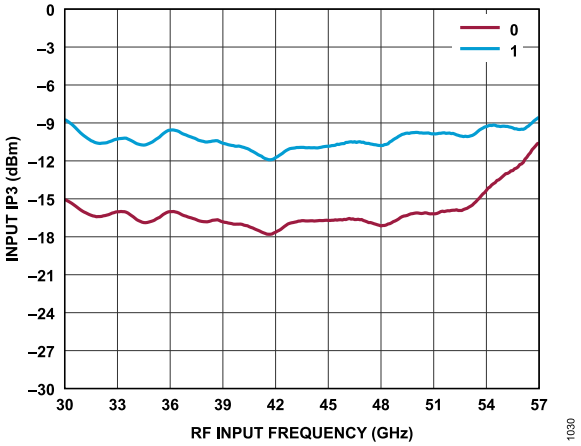

Figure 33. Input IP3 vs. RF Input Frequency at Various DSA2 Settings

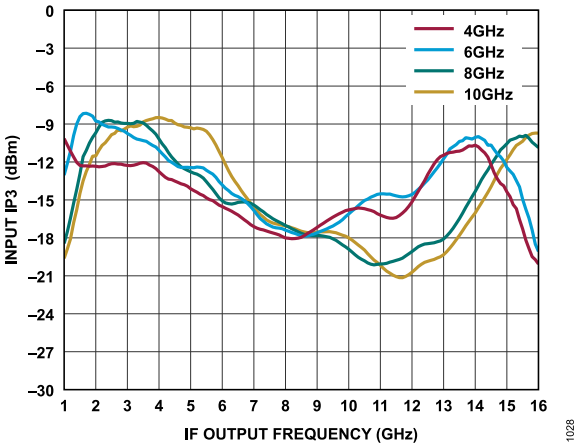

Figure 31. Input IP3 vs. IF Output Frequency at Various IF Filter Settings

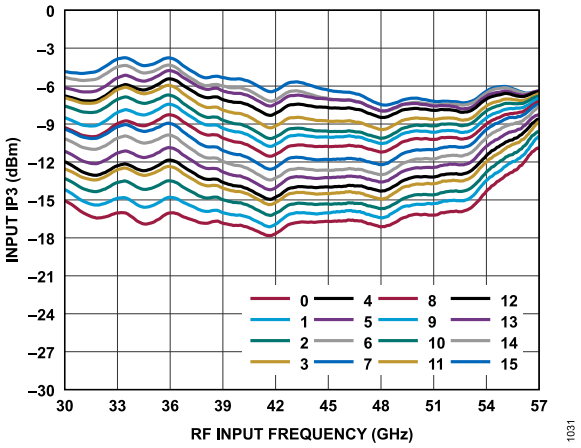

Figure 34. Input IP3 vs. RF Input Frequency at Various DSA3 Settings

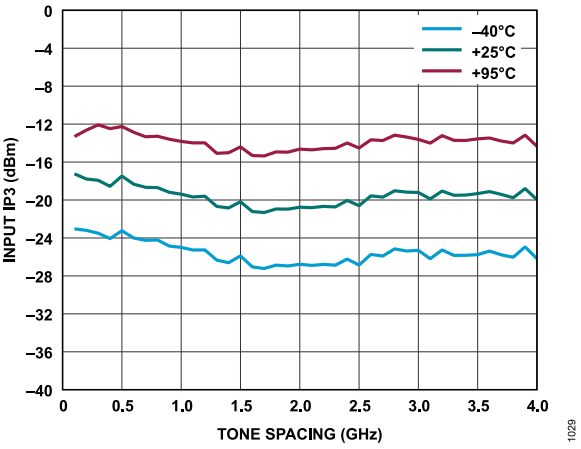

Figure 32. Input IP3 vs. Tone Spacing over Temperature

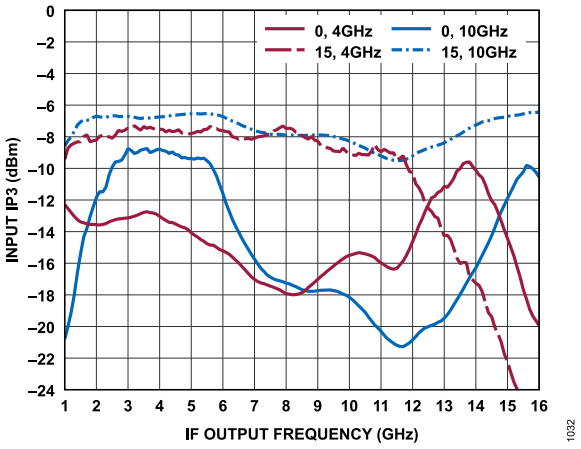

Figure 35. Input IP3 vs. IF Output Frequency at Various DSA4 Settings and IF Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

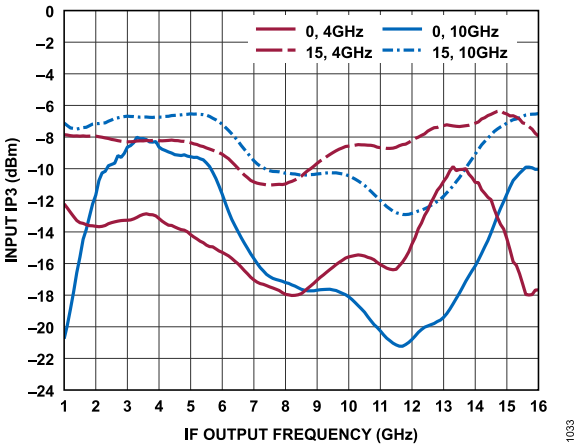

Figure 36. Input IP3 vs. IF Output Frequency at Various DSA5 Settings and IF Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

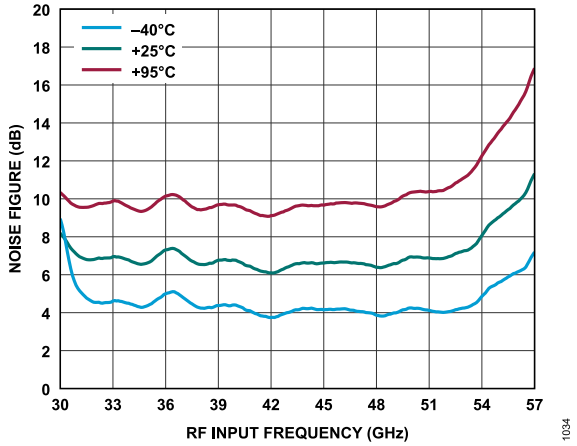

Figure 37. Noise Figure vs. RF Input Frequency at Various Temperatures

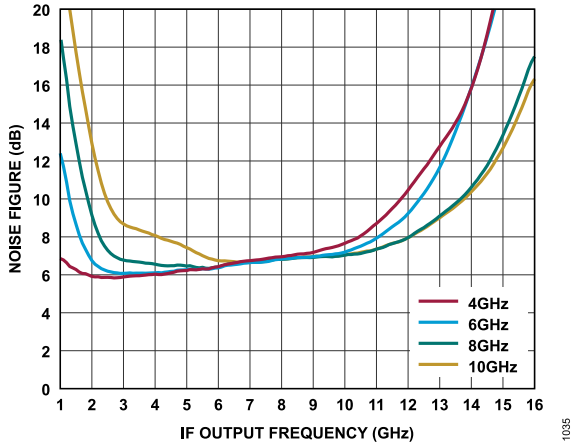

Figure 38. Noise Figure vs. IF Output Frequency at Various IF Filter Settings

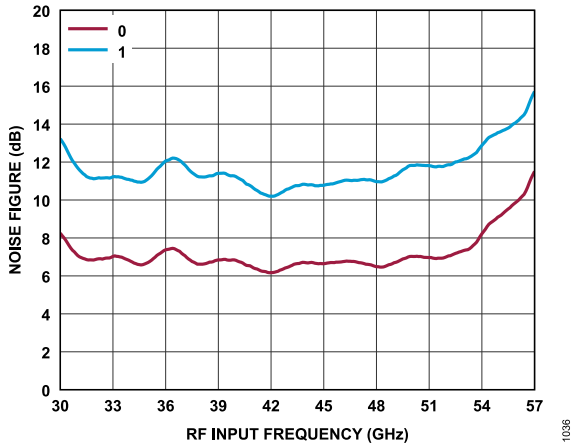

Figure 39. Noise Figure vs. RF Input Frequency at Various DSA2 Settings

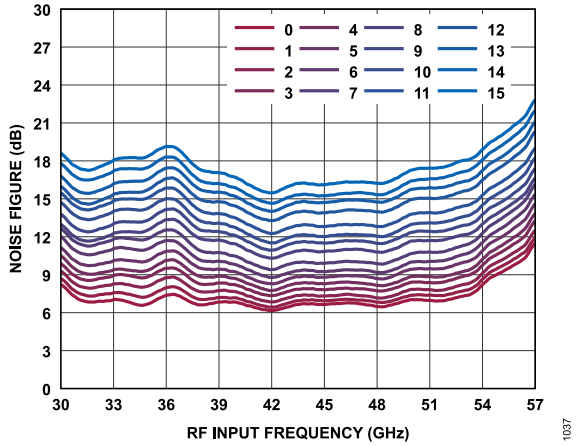

Figure 40. Noise Figure vs. RF Input Frequency at Various DSA3 Settings

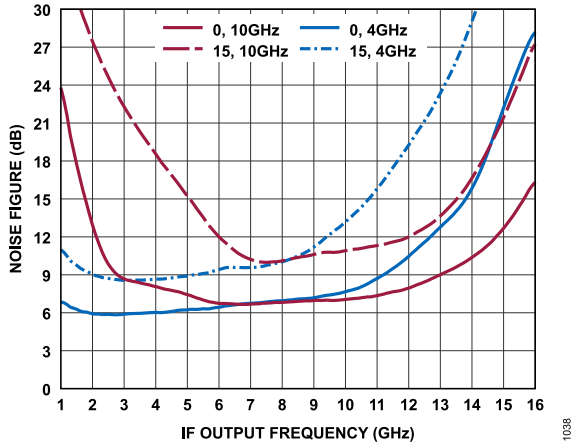

Figure 41. Noise Figure vs. IF Output Frequency at Various DSA4 Settings and IF Filter Settings

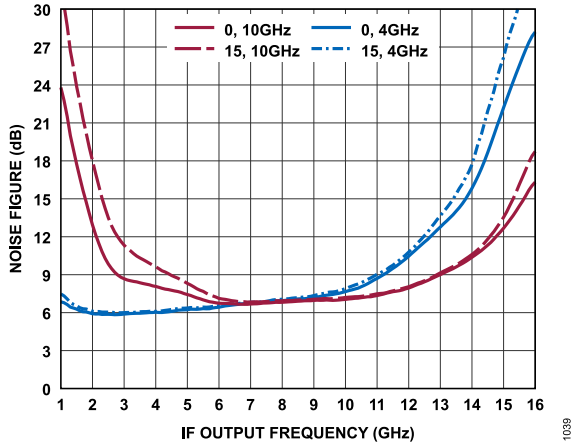

Figure 42. Noise Figure vs. IF Output Frequency at Various DSA5 Settings and IF Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

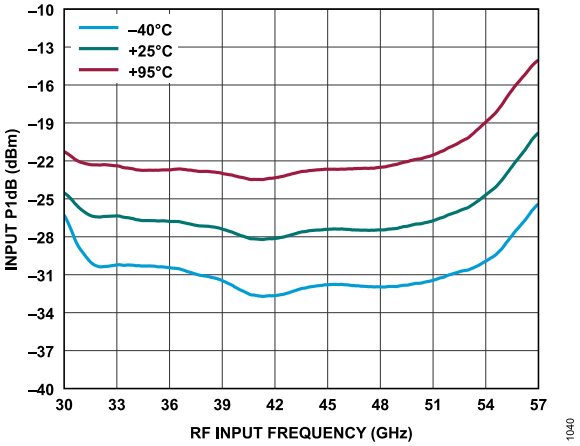

Figure 43. Input P1dB vs. RF Input Frequency at Various Temperatures

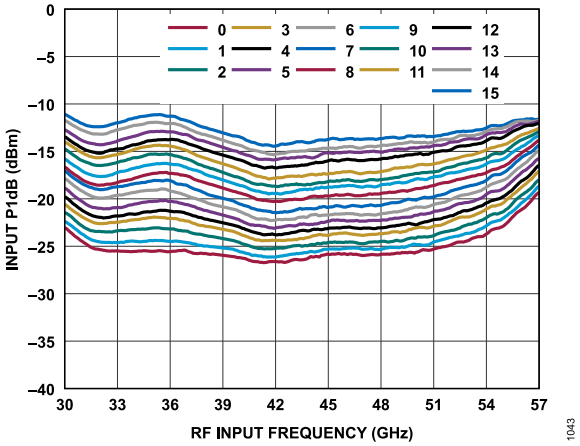

Figure 46. Input P1dB vs. RF Input Frequency at Various RF_DSA3 Settings

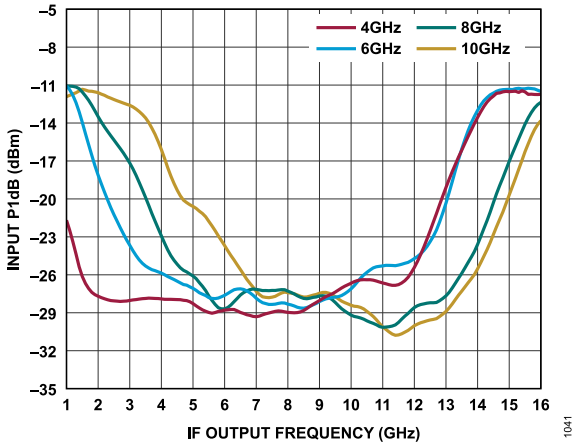

Figure 44. Input P1dB vs. IF Output Frequency over IF Filter Settings

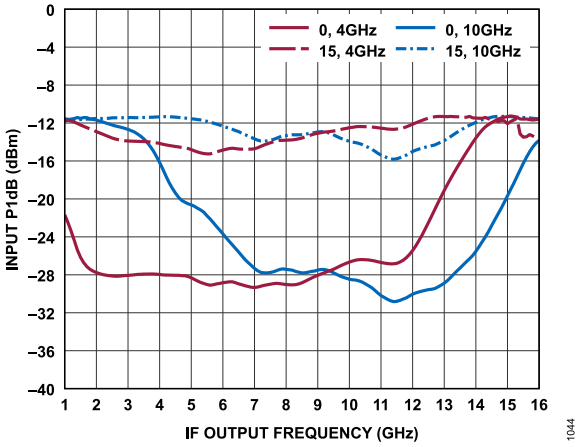

Figure 47. Input P1dB vs. IF Output Frequency at Various RF_DSA4 Settings and IF Filter Settings

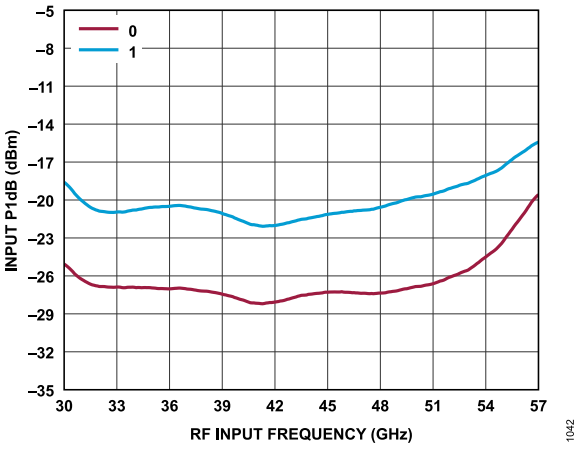

Figure 45. Input P1dB vs. RF Input Frequency at Various RF_DSA2 Settings

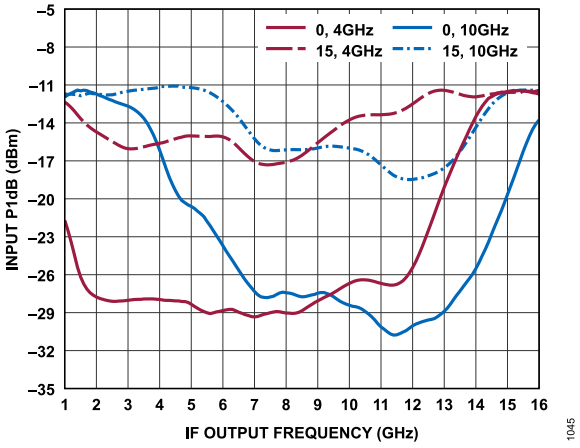

Figure 48. Input P1dB vs. IF Output Frequency at Various RF_DSA5 Settings and IF Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Image Rejection

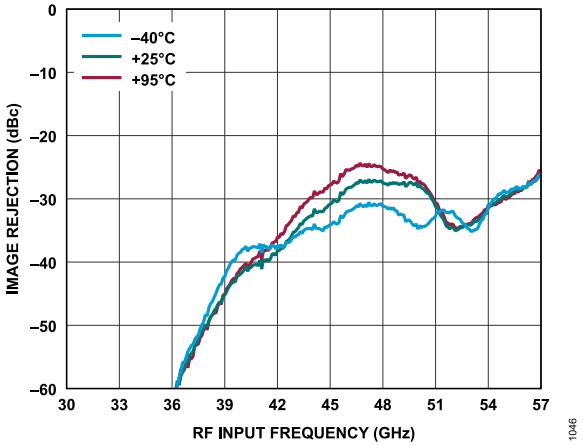

Figure 49. Image Rejection vs. RF Input Frequency at Various Temperatures, No Calibration, Wideband RF Filters

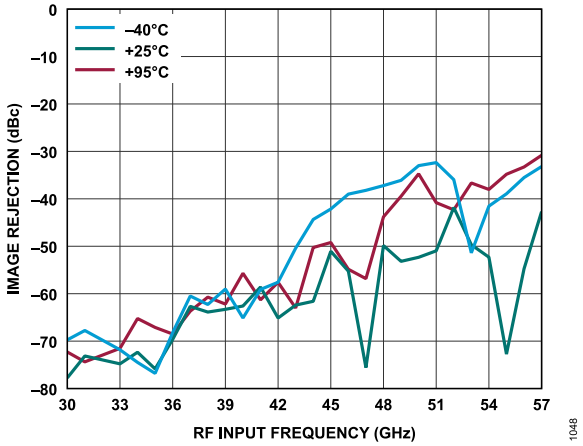

Figure 51. Image Rejection vs. RF Input Frequency at Various Temperatures, with Optimization at 25°C, Wideband RF Filters

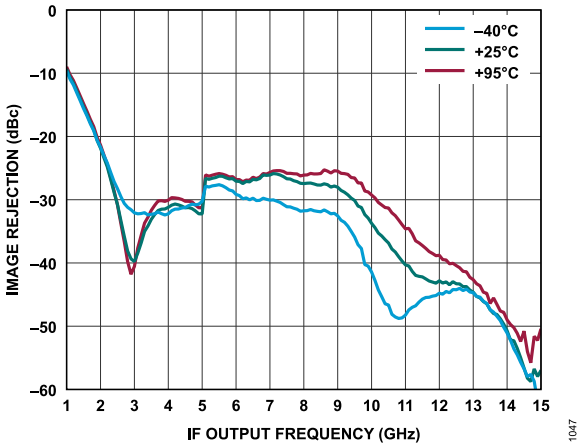

Figure 50. Image Rejection vs. IF Output Frequency at Various Temperatures, No Calibration, Wideband RF Filters, IF Filter Settings Adjusted with Sweeping Frequency

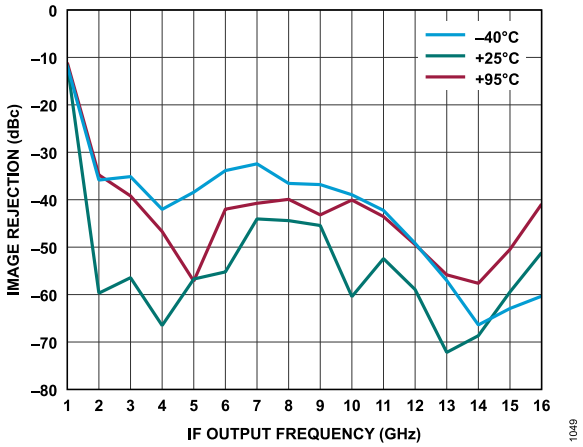

Figure 52. Image Rejection vs. IF Output Frequency at Various Temperatures, with Optimization at 25°C, Wideband RF Filters, IF Filters Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

Power Detector

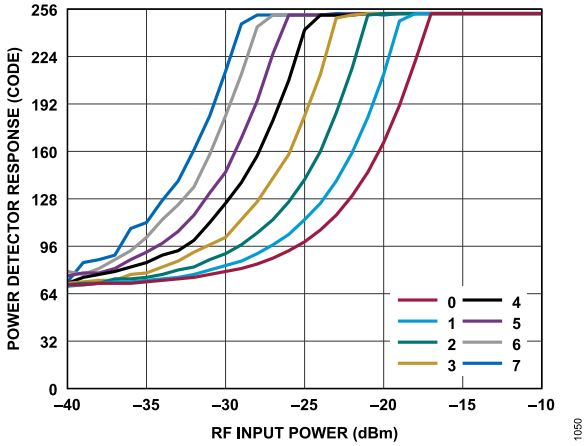

Figure 53. Power Detector Response vs. RF Input Power at Various Detector Resistor Control Settings

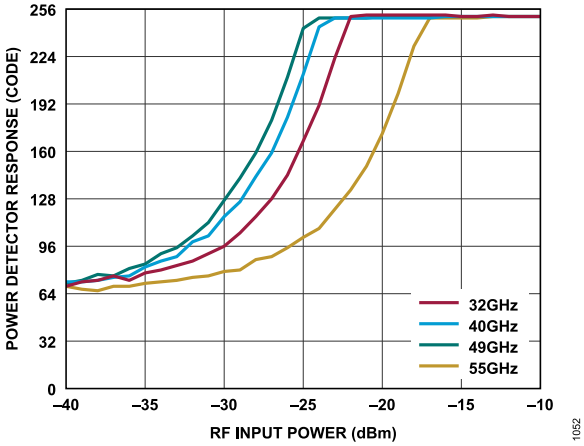

Figure 55. Power Detector Response vs. RF Input Power at Various RF Input Frequencies, Detector Resistor Control Setting = 4

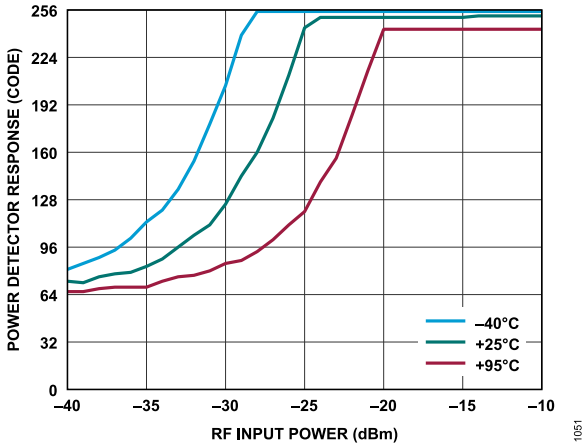

Figure 54. Power Detector Response vs. RF Input Power at Various Temperatures, Detector Resistor Control Setting = 4

TYPICAL PERFORMANCE CHARACTERISTICS

RETURN LOSS

The supply voltage = 1.8V (all supplies) and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{RF} = −45dBm, P_{LO} = −5dBm, P_{IF} = −15dBm, maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), and IF BPF settings = 8GHz, unless otherwise noted.

Probe measurements, where applicable, were performed by probing the trace terminated out of the device.

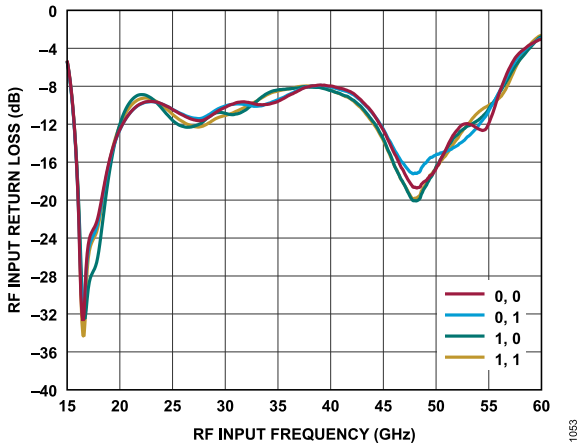

Figure 56. RF Input Return Loss vs. RF Input Frequency at Various RF Bands and DSA2 Settings, at 25°C

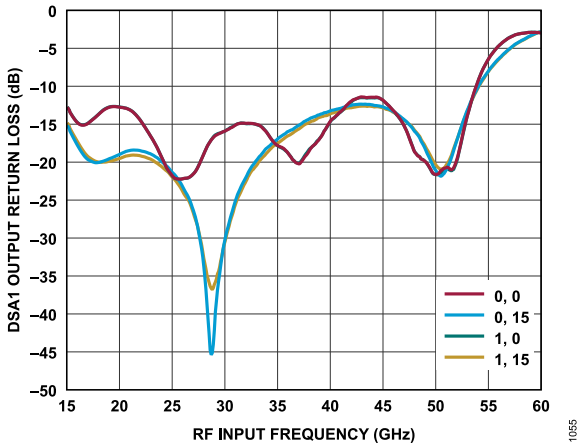

Figure 58. DSA1 Output Return Loss vs. RF Input Frequency at Various RF Bands and DSA1 Settings, at 25°C

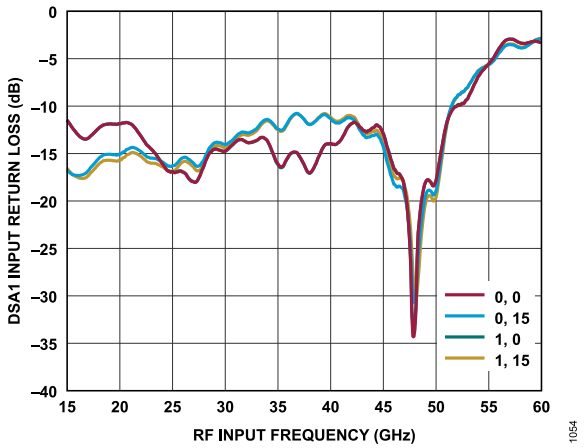

Figure 57. DSA1 Input Return Loss vs. RF Input Frequency at Various RF Bands and DSA1 Settings, at 25°C

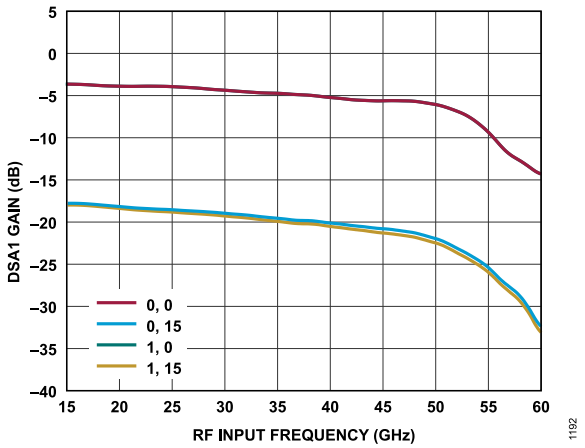

Figure 59. DSA1 Gain vs. RF Input Frequency at Various RF Bands and DSA1 Settings, at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

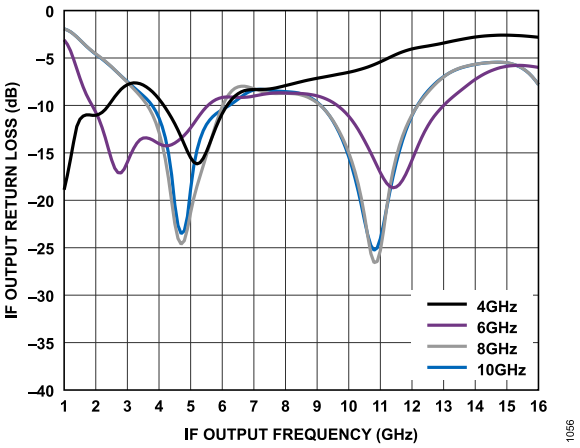

Figure 60. IF Output Return Loss vs. IF Output Frequency at Various IF Filter Settings, at 25°C

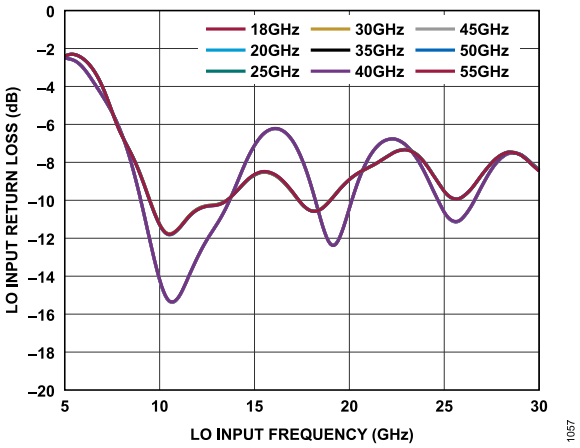

Figure 61. LO Input Return Loss vs. LO Input Frequency at Various LO Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

LO LEAKAGE

Digital 1.8V voltage supplies = 1.8V, DC 1.8V voltage supplies = 1.8V, and T_{TOP} (referenced to topside of package) = 25°C, unless otherwise noted. Measurements are de-embedded to the RF pins (see the RF and IF input and output pins in Figure 3).

All measurements taken at RF amplitude = −45dBm, IF = 8GHz, LO power = −5dBm, RF Band 1, upper sideband, maximum gain, LO tunable filter wideband high settings, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), IF filter = 8GHz, and T_C = 25°C, unless otherwise noted. All temperatures specified are T_C. All measurements taken at IF output unless otherwise noted. Trace and connector loss are de-embeded.

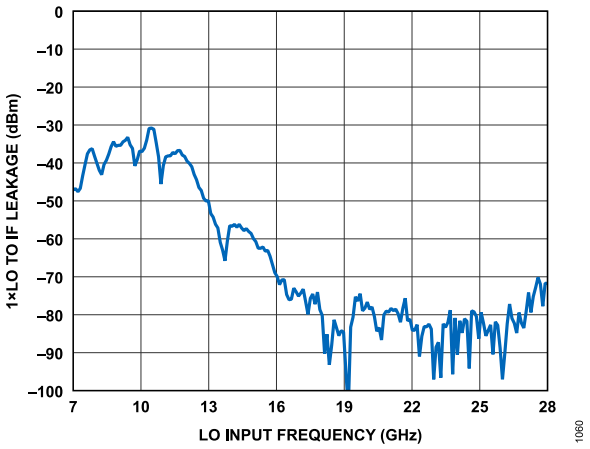

Figure 62. 1×LO to IF Leakage vs. LO Input Frequency, RF High Band at 25°C

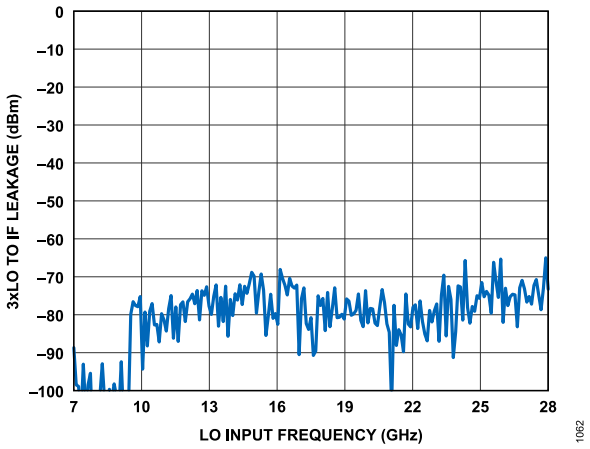

Figure 64. 3×LO to IF Leakage vs. LO Input Frequency, RF High Band at 25°C

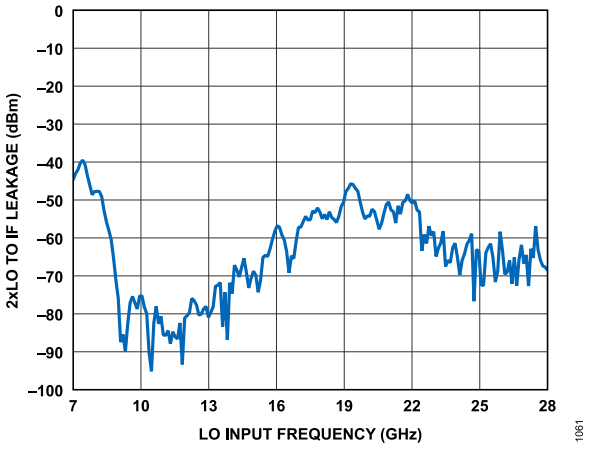

Figure 63. 2×LO to IF Leakage vs. LO Input Frequency, RF High Band at 25°C

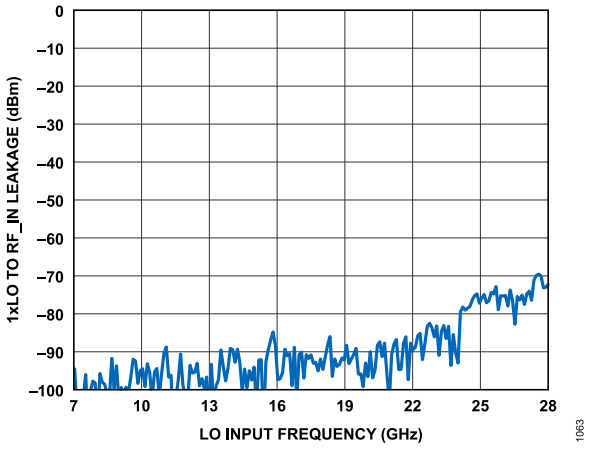

Figure 65. 1×LO to RF_IN Leakage vs. LO Input Frequency, RF High Band at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

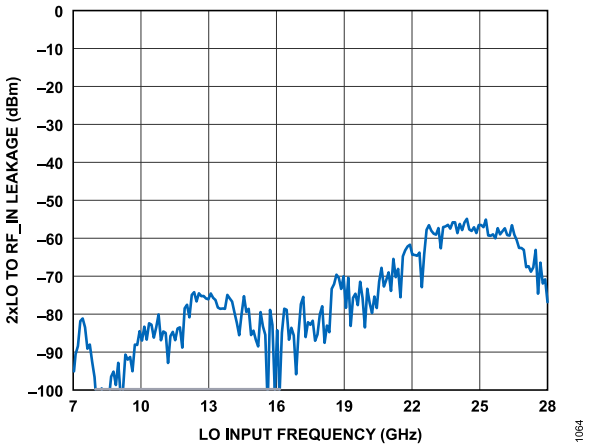

Figure 66. 2×LO to RF_IN Leakage vs. LO Input Frequency, RF High Band at 25°C

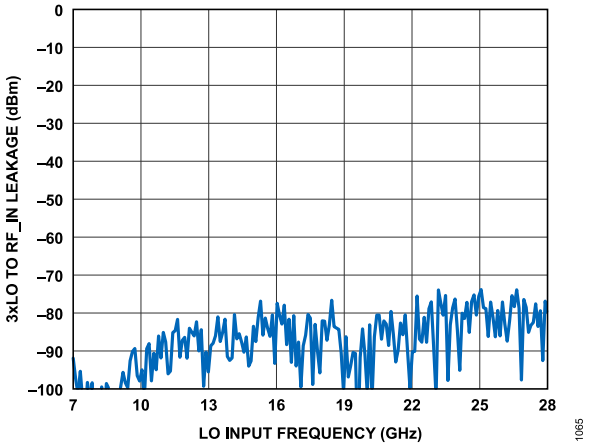

Figure 67. 3×LO to RF_IN Leakage vs. LO Input Frequency, RF High Band at 25°C

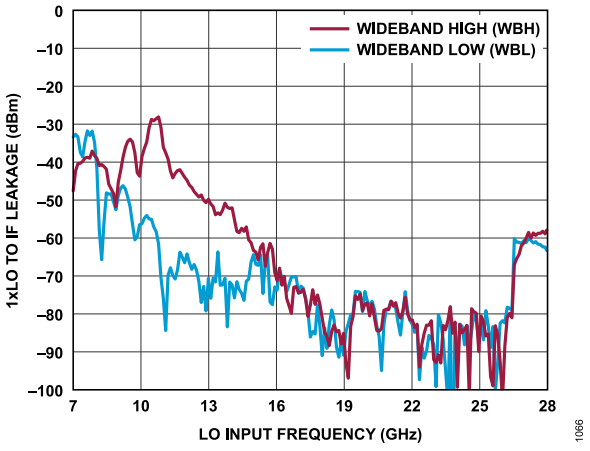

Figure 68. 1×LO to IF Leakage vs. LO Input Frequency, RF Low Band at 25°C

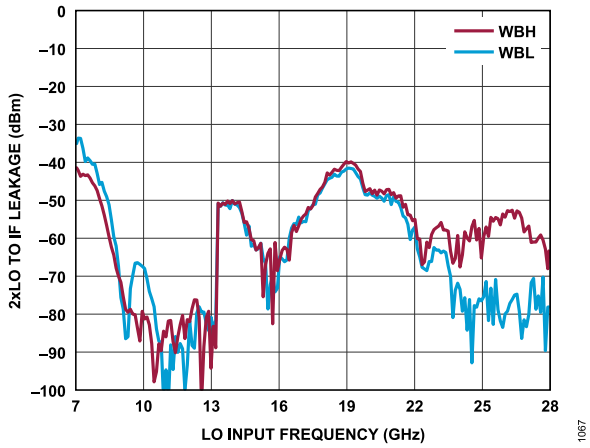

Figure 69. 2×LO to IF Leakage vs. LO Input Frequency, RF Low Band at 25°C

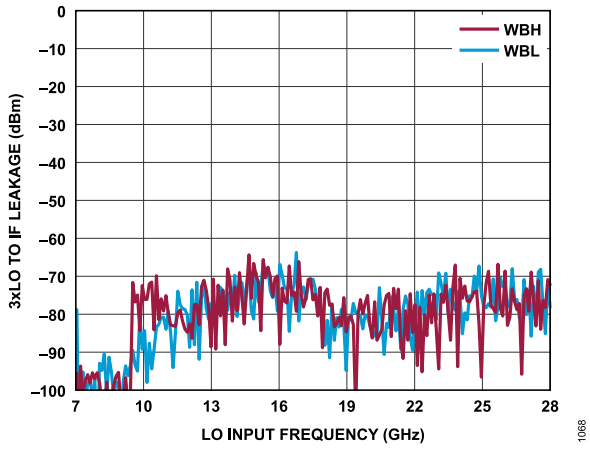

Figure 70. 3×LO to IF Leakage vs. LO Input Frequency, RF Low Band at 25°C

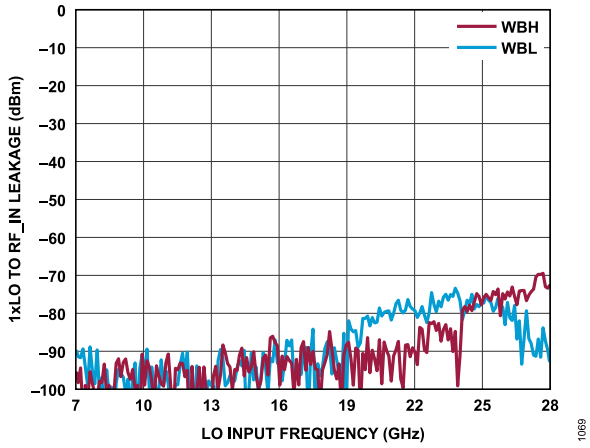

Figure 71. 1×LO to RF_IN Leakage vs. LO Input Frequency, RF Low Band at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

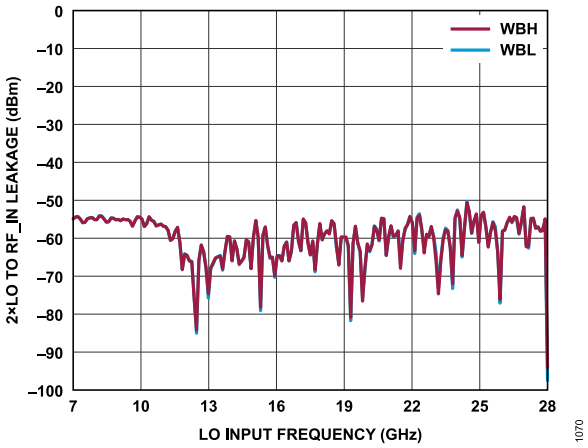

Figure 72. 2×LO to RF_IN Leakage vs. LO Input Frequency, RF Low Band at 25°C

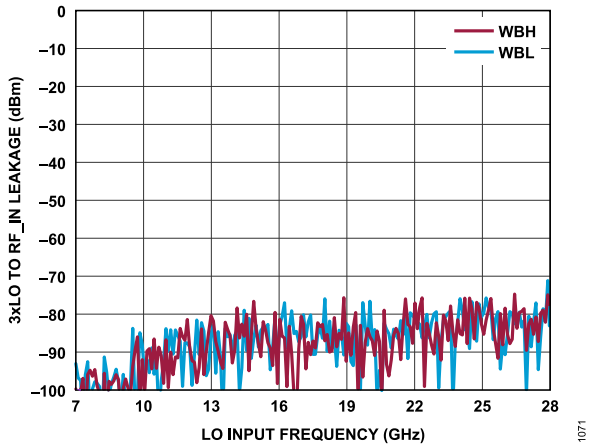

Figure 73. 3×LO to RF_IN Leakage vs. LO Input Frequency, RF Low Band at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

IF MODE, RF_IN, LOW BAND

All measurements use RF_IN as an input and IF as an output, with the RF low-band settings. The supply voltage = 1.8V (all supplies) and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{RF} = −55dBm, P_{LO} = −5dBm, f_{RF} = 29GHz, f_{IF} = 8GHz, f_{LO} = 37GHz (lower sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), LO tunable filter wideband high settings, and IF BPF settings = 8GHz, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the RF and IF input and output pins in Figure 3).

Conversion Gain

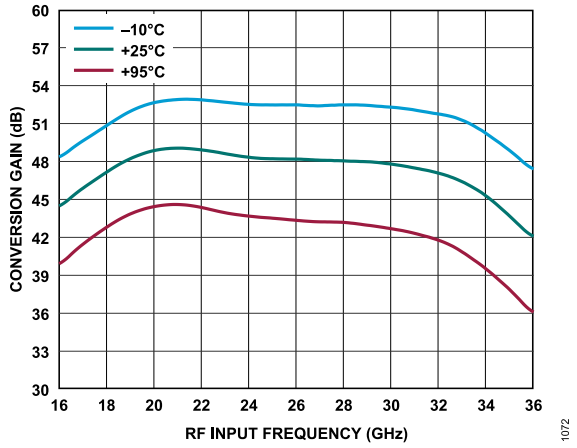

Figure 74. Conversion Gain vs. RF Input Frequency at Various Temperatures

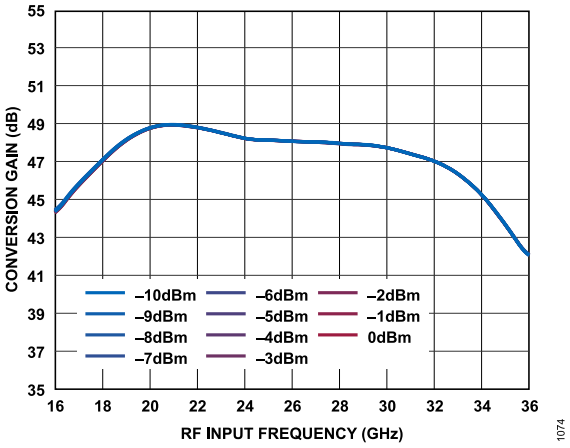

Figure 76. Conversion Gain vs. RF Input Frequency at Various LO Powers

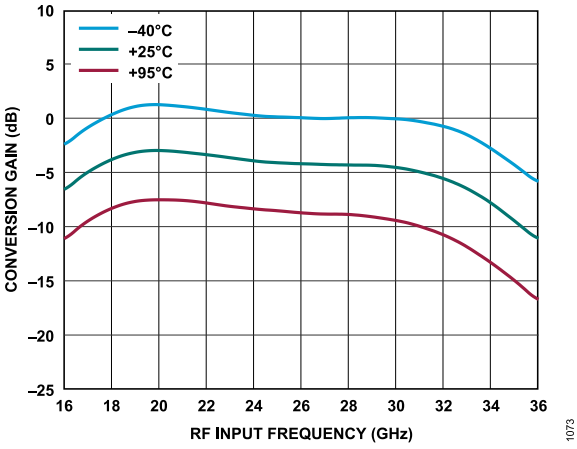

Figure 75. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

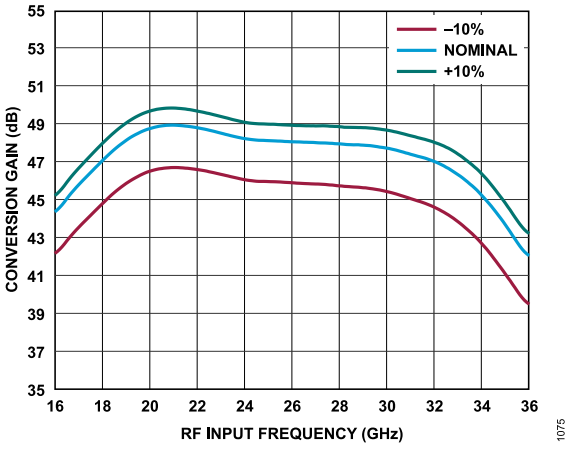

Figure 77. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

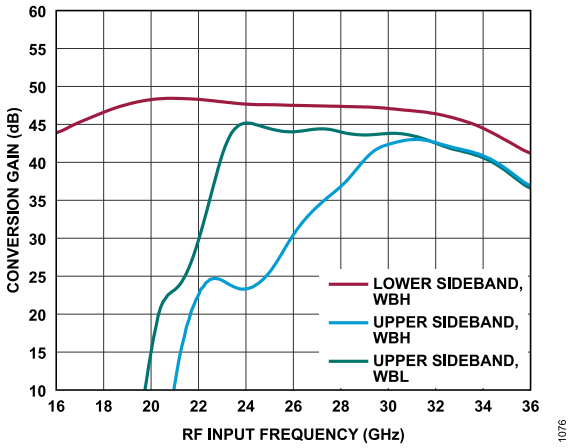

Figure 78. Conversion Gain vs. RF Input Frequency, Upper Sideband and Lower Sideband at Various LO Tunable Filter Settings

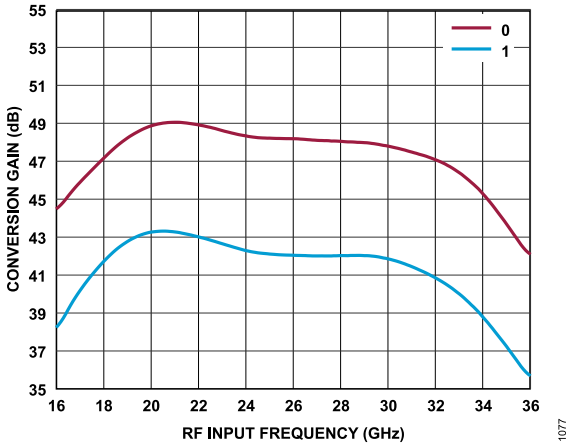

Figure 79. Conversion Gain vs. RF Input Frequency at Various DSA2 Settings

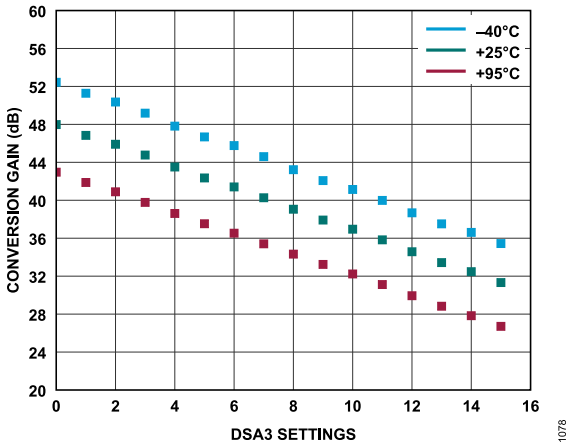

Figure 80. Conversion Gain vs. DSA3 Settings at Various Temperatures, Single f_{RF} = 29GHz

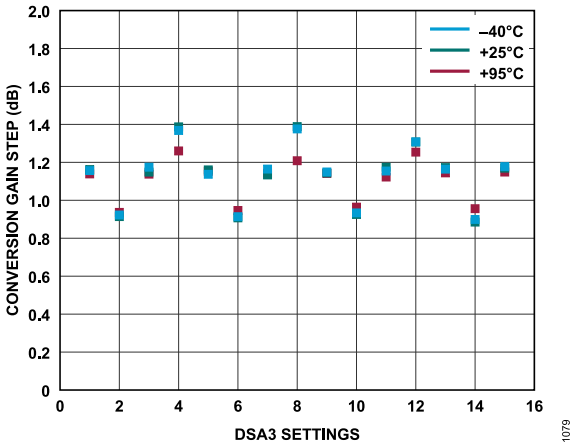

Figure 81. Conversion Gain Step vs. DSA3 Settings at Various Temperatures, Single f_{RF} = 29GHz

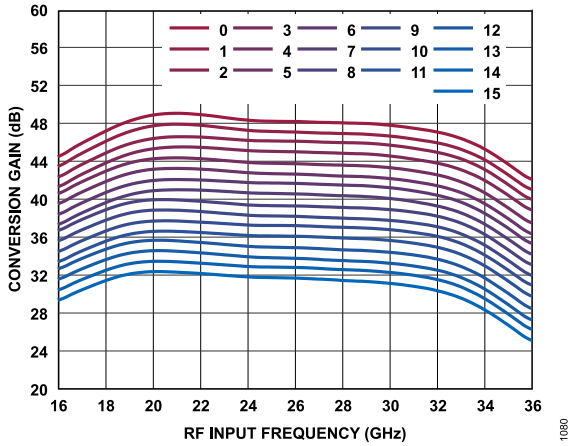

Figure 82. Conversion Gain vs. RF Input Frequency at Various DSA3 Settings

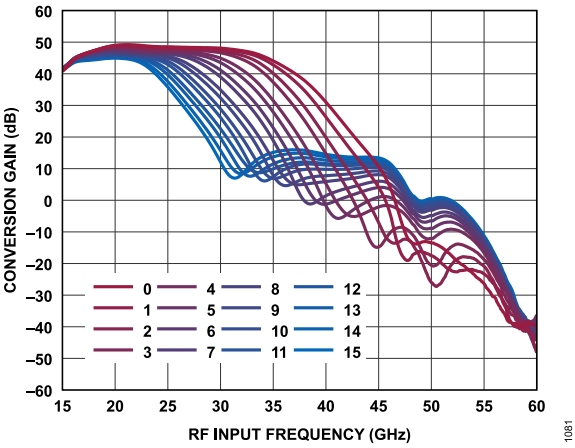

Figure 83. Conversion Gain vs. RF Input Frequency at Various RF Low-Pass Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

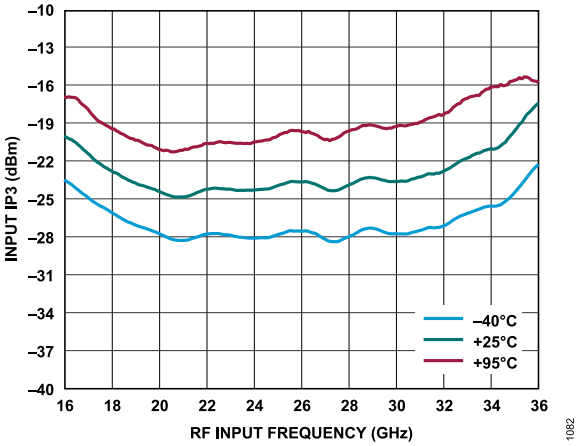

Figure 84. Input IP3 vs. RF Input Frequency at Various Temperatures

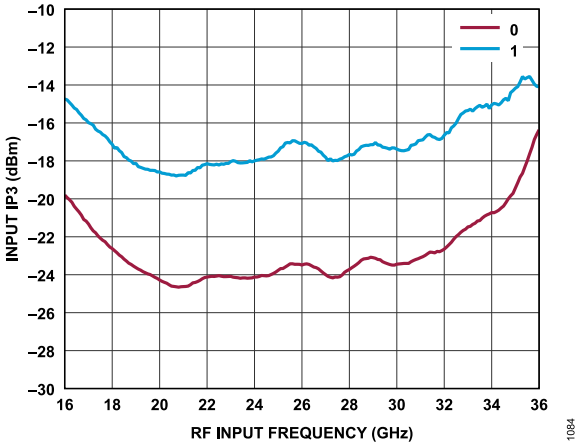

Figure 86. Input IP3 vs. RF Input Frequency at Various DSA2 Settings

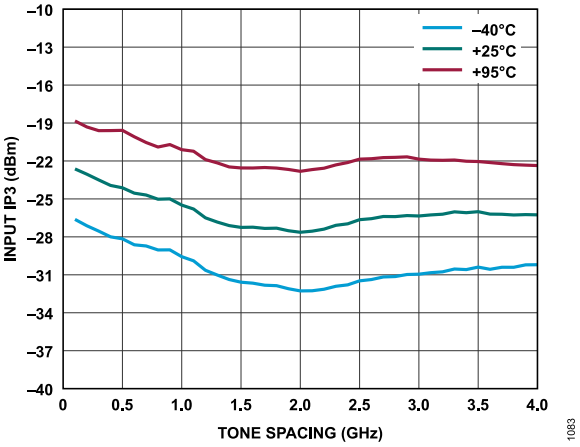

Figure 85. Input IP3 vs. Tone Spacing at Various Temperatures

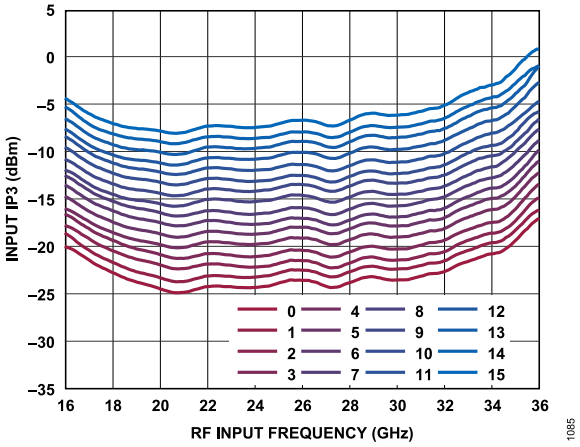

Figure 87. Input IP3 vs. RF Input Frequency at Various DSA3 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

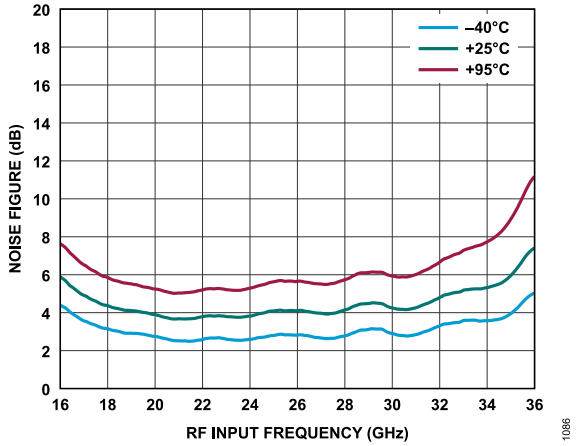

Figure 88. Noise Figure vs. RF Input Frequency at Various Temperatures

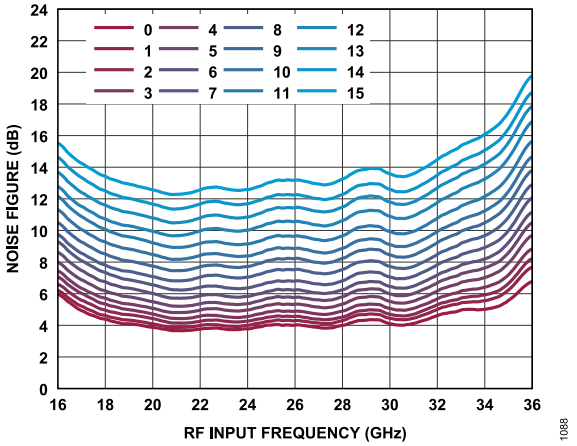

Figure 90. Noise Figure vs. RF Input Frequency at Various DSA3 Settings

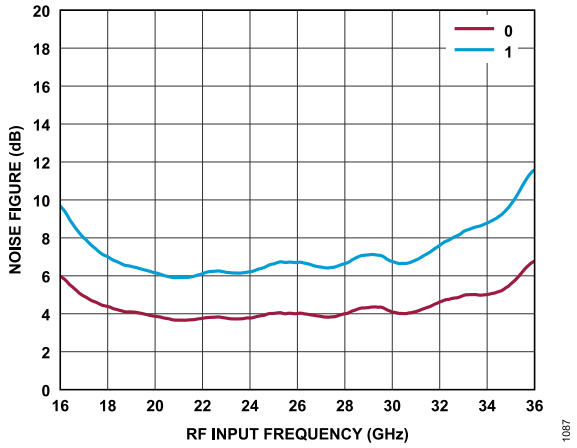

Figure 89. Noise Figure vs. RF Input Frequency at Various DSA2 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

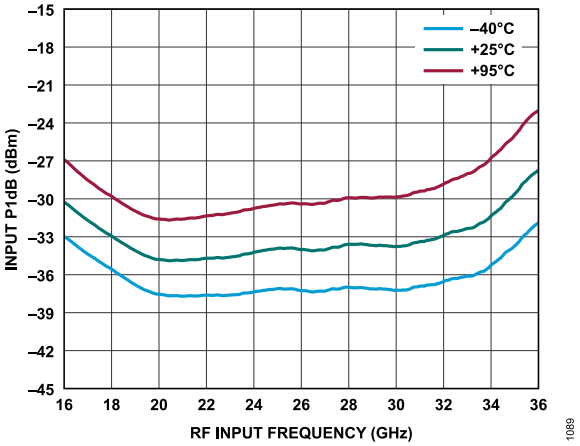

Figure 91. Input P1dB vs. RF Input Frequency at Various Temperatures

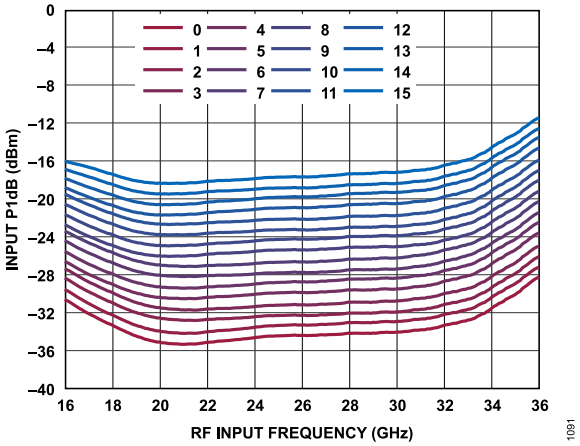

Figure 93. Input P1dB vs. RF Input Frequency at Various RF_DSA3 Settings

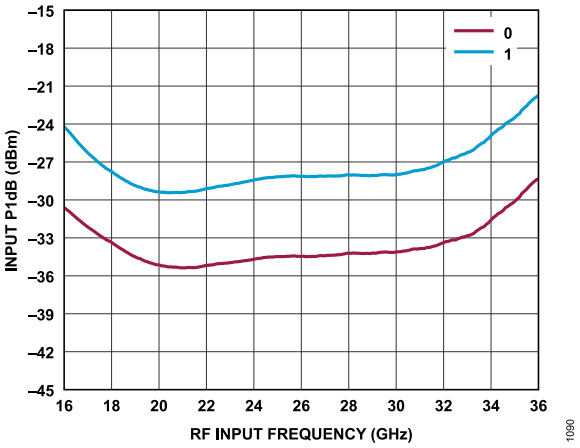

Figure 92. Input P1dB vs. RF Input Frequency at Various RF_DSA2 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Image Rejection

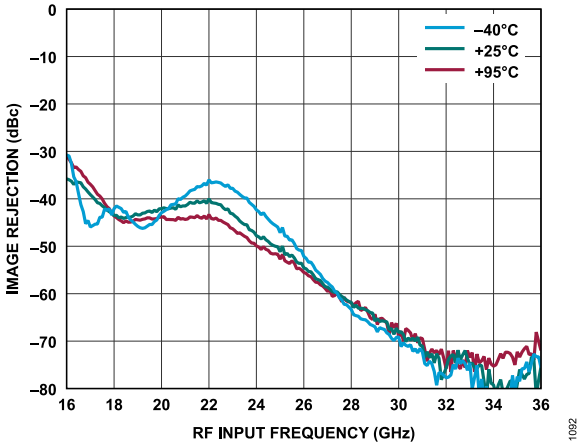

Figure 94. Image Rejection vs. RF Input Frequency at Various Temperatures, No Calibration

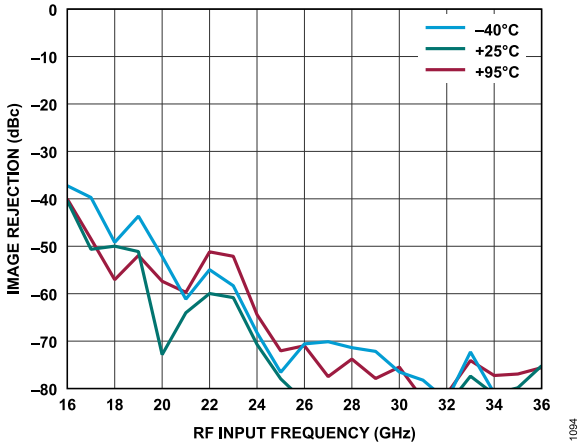

Figure 95. Image Rejection vs. RF Input Frequency at Various Temperatures, with Optimization at 25°C

TYPICAL PERFORMANCE CHARACTERISTICS

Power Detector

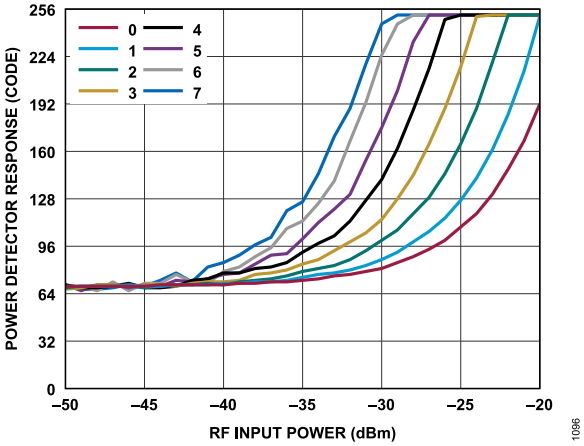

Figure 96. Power Detector Response vs. RF Input Power at Various Detector Resistor Control Settings

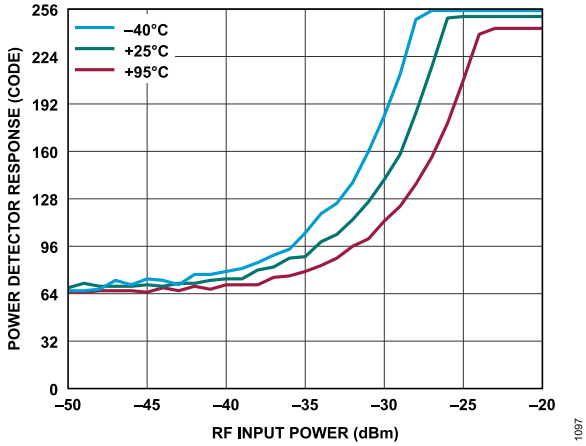

Figure 97. Power Detector Response vs. RF Input Power at Various Temperatures, Detector Resistor Control Setting = 4

TYPICAL PERFORMANCE CHARACTERISTICS

IF MODE, DSA_IN, LOW BAND

All measurements use DSA_IN as an input and IF as an output, with the RF low-band settings. DSA_OUT is connected to RF_IN on-board with a short 50Ω trace. Supply voltage = 1.8V (all supplies), and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{RF} = −55dBm, P_{LO} = −5dBm, f_{RF} = 29GHz, f_{IF} = 8GHz, f_{LO} = 37GHz (lower sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), LO tunable filter wideband high settings, and IF BPF settings = 8GHz, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the RF and IF input and output pins in Figure 3).

Conversion Gain

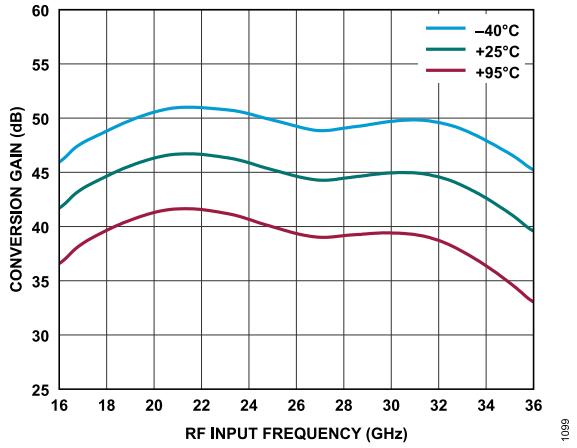

Figure 98. Conversion Gain vs. RF Input Frequency at Various Temperatures

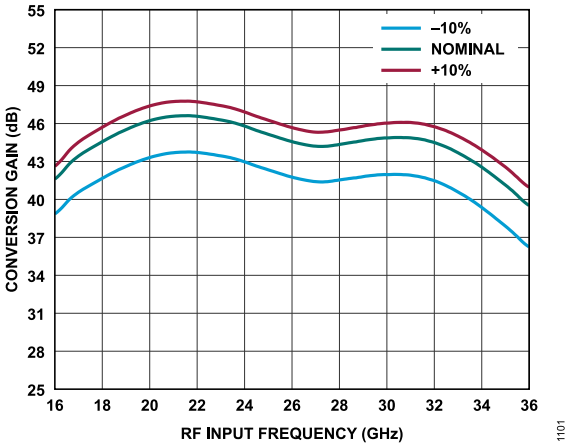

Figure 100. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

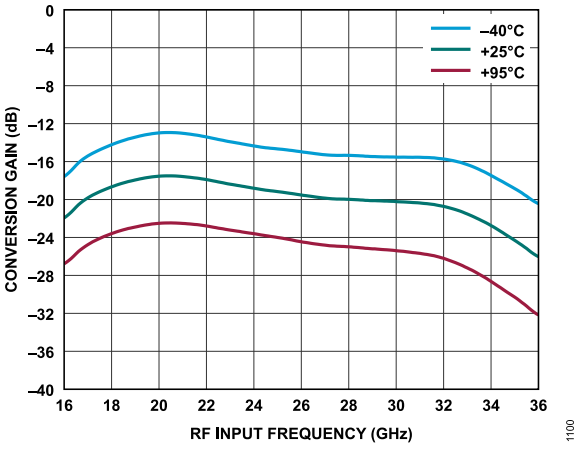

Figure 99. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

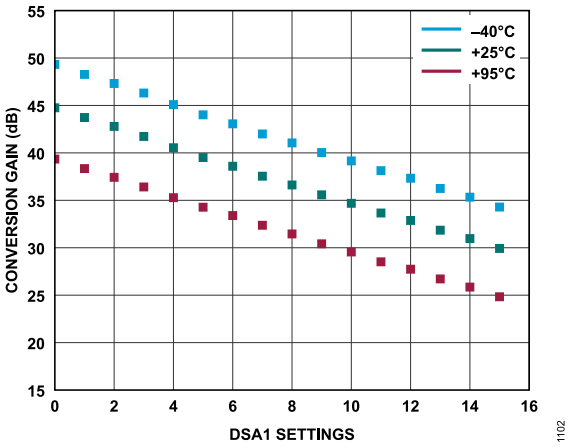

Figure 101. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

TYPICAL PERFORMANCE CHARACTERISTICS

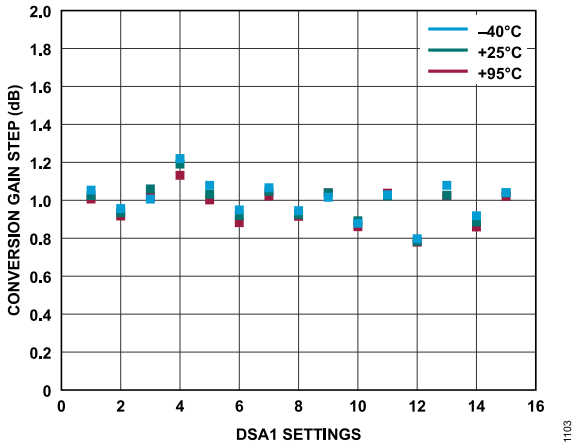

Figure 102. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

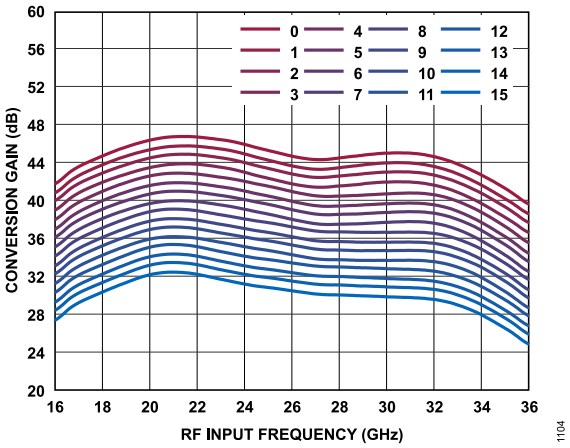

Figure 103. Conversion Gain vs RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

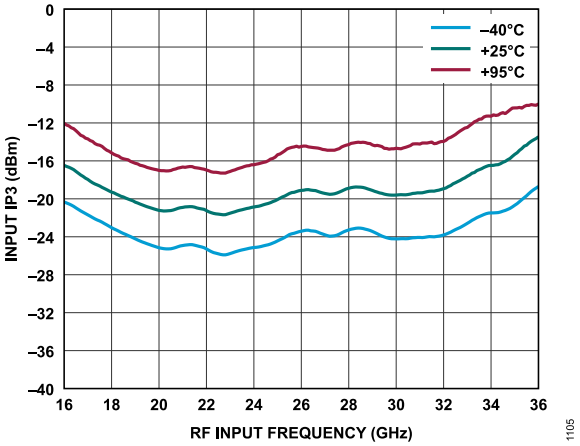

Figure 104. Input IP3 vs. RF Input Frequency at Various Temperatures

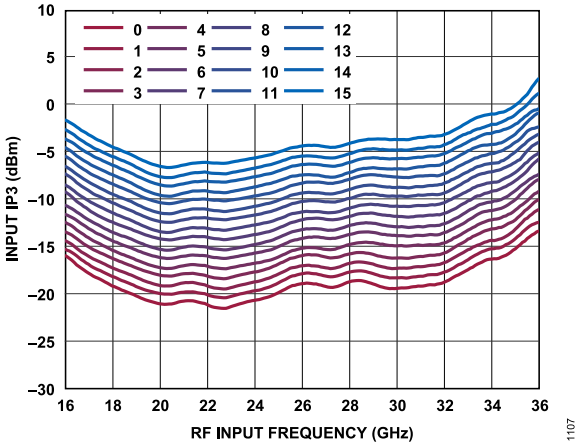

Figure 106. Input IP3 vs. RF Input Frequency at Various DSA1 Settings

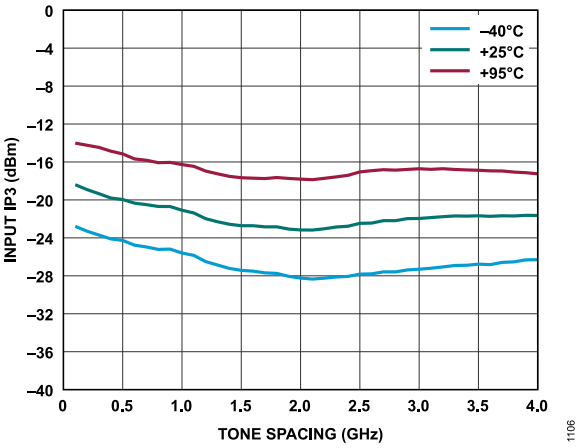

Figure 105. Input IP3 vs. Tone Spacing at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

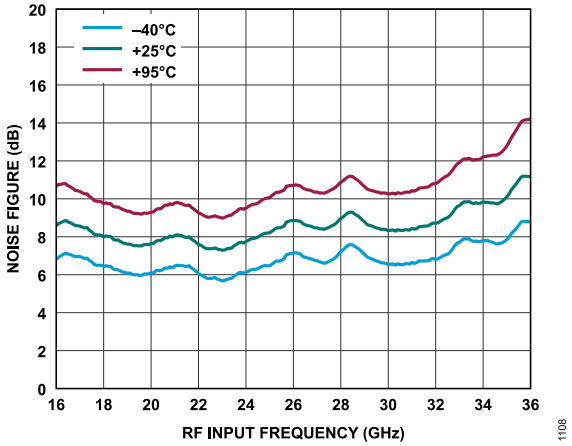

Figure 107. Noise Figure vs. RF Input Frequency at Various Temperatures

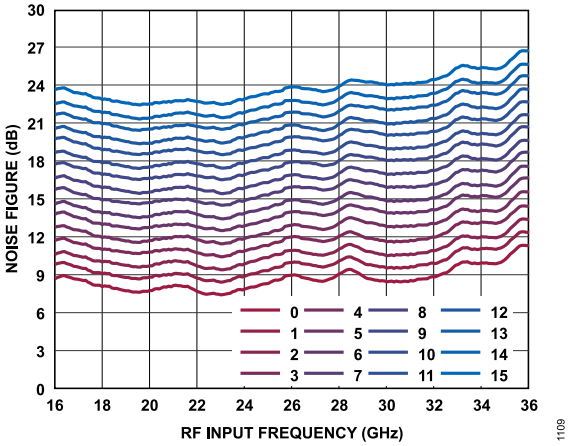

Figure 108. Noise Figure vs. RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

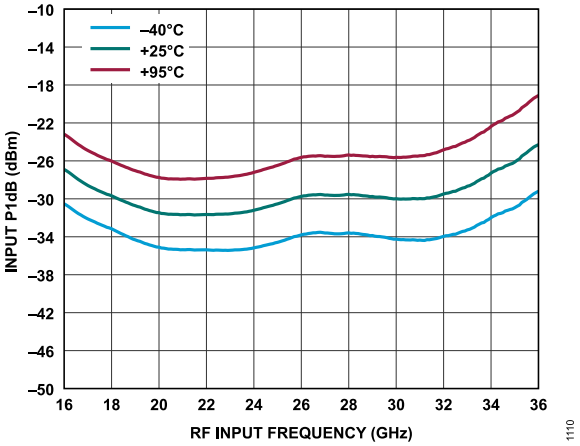

Figure 109. Input P1dB vs. RF Input Frequency at Various Temperatures

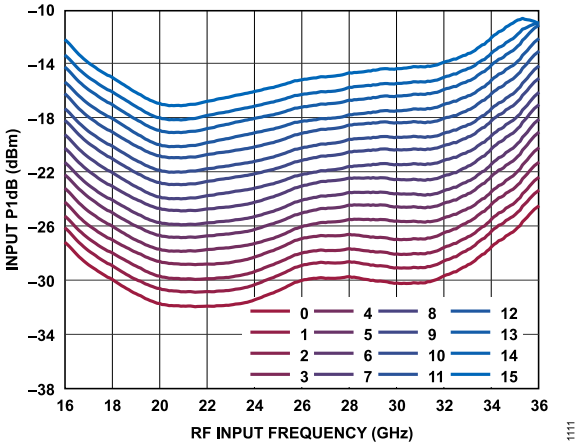

Figure 110. Input P1dB vs. RF Input Frequency at Various RF_DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

IF MODE, DSA_IN, HIGH BAND

All measurements use DSA_IN as an input and IF as an output, with the RF high-band settings. DSA_OUT is connected to RF_IN on-board with a short 50Ω trace. The supply voltage = 1.8V (all supplies) and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{RF} = −45dBm, P_{LO} = −5dBm, f_{RF} = 49GHz, f_{IF} = 8GHz, f_{LO} = 41GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), LO tunable filter wideband high settings, and IF BPF settings = 8GHz, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the RF and IF input and output pins in Figure 3).

Conversion Gain

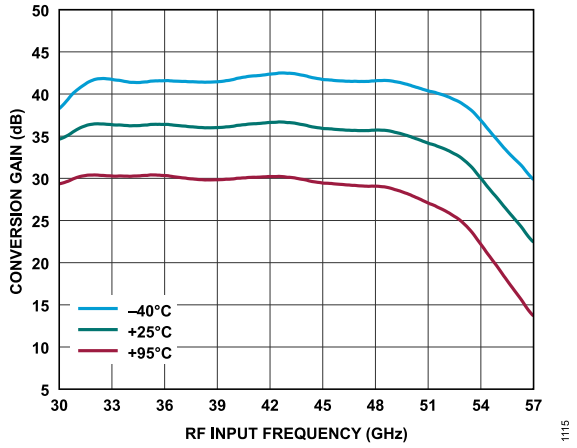

Figure 111. Conversion Gain vs. RF Input Frequency at Various Temperatures

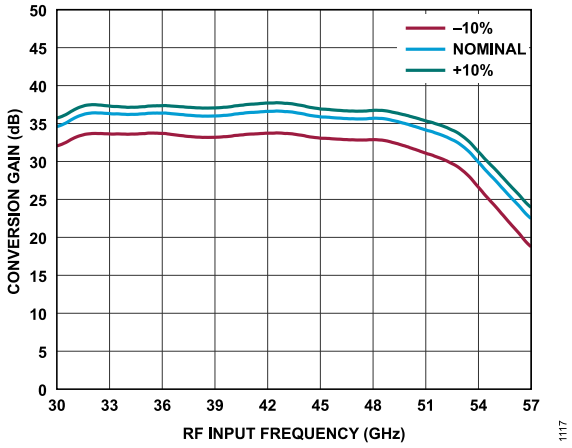

Figure 113. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

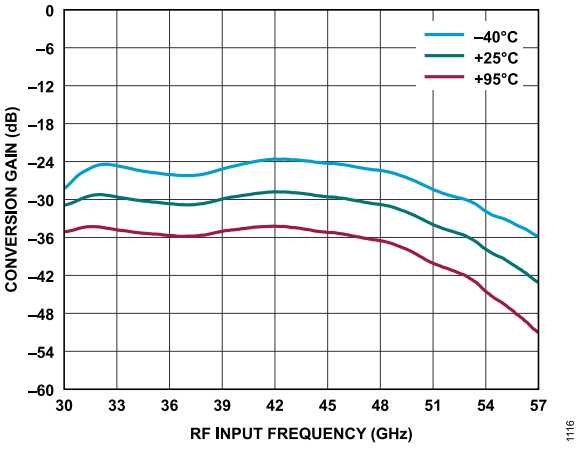

Figure 112. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

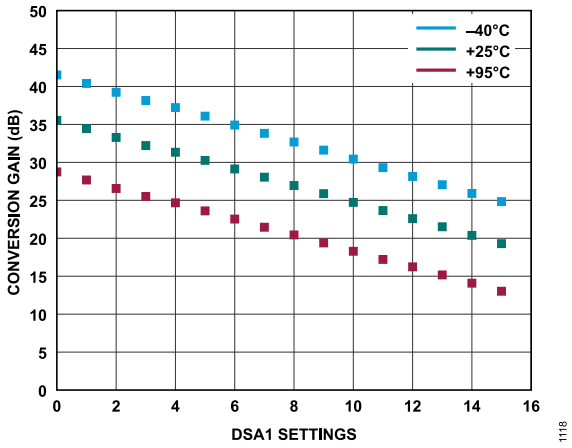

Figure 114. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

TYPICAL PERFORMANCE CHARACTERISTICS

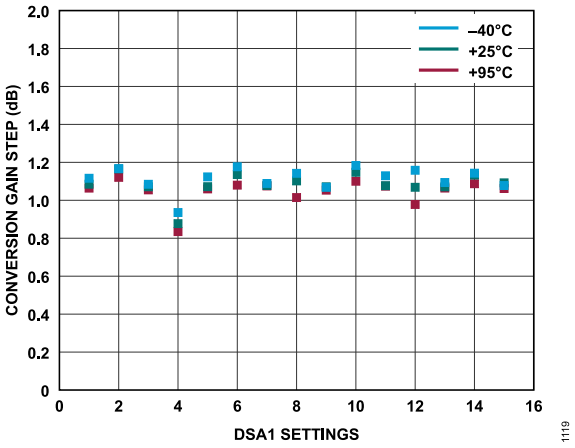

Figure 115. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

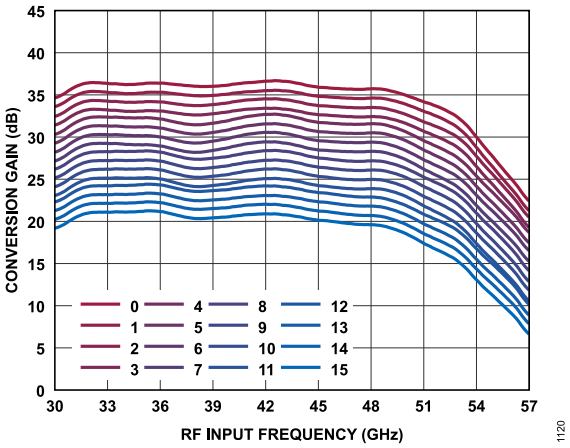

Figure 116. Conversion Gain vs RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

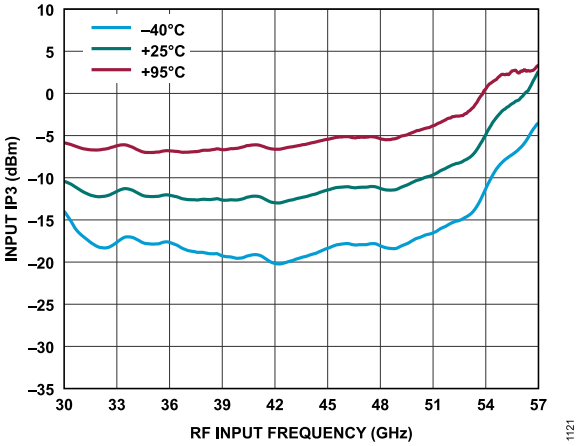

Figure 117. Input IP3 vs. RF Input Frequency at Various Temperatures

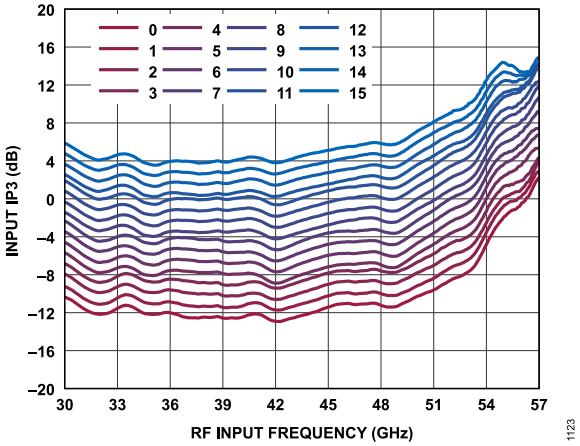

Figure 119. Input IP3 vs. RF Input Frequency at Various DSA1 Settings

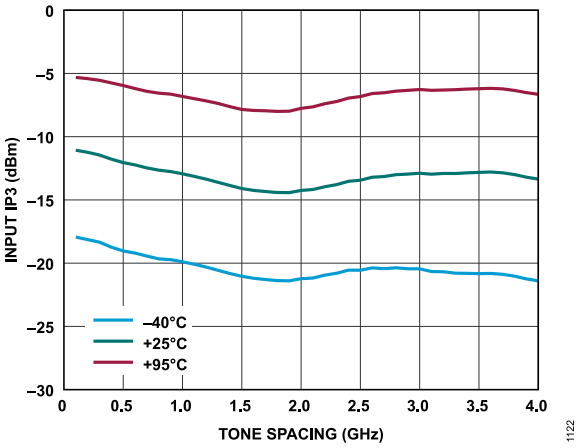

Figure 118. Input IP3 vs. Tone Spacing at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

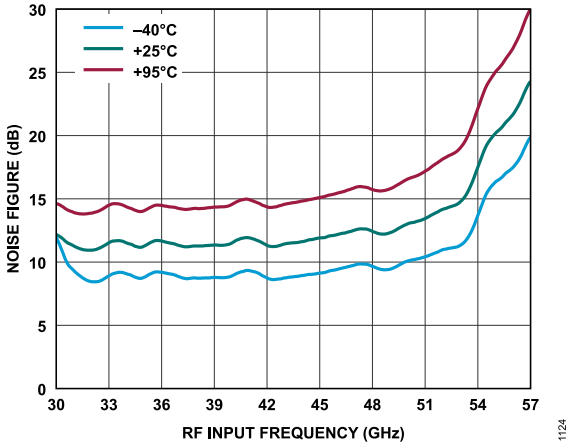

Figure 120. Noise Figure vs. RF Input Frequency at Various Temperatures

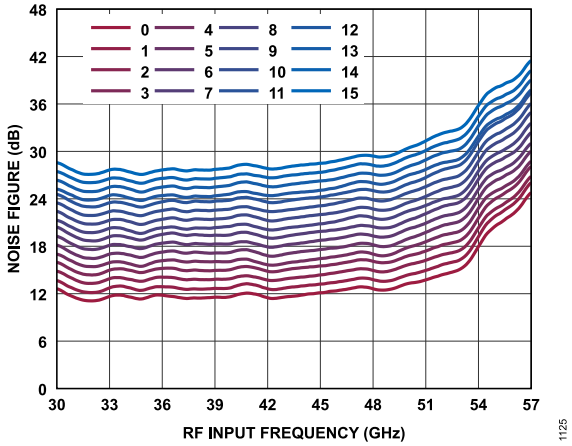

Figure 121. Noise Figure vs. RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

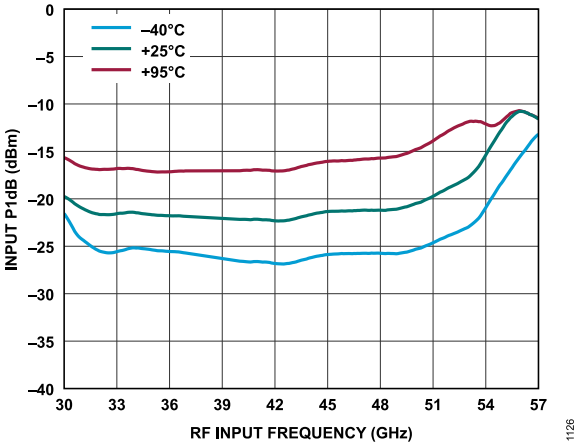

Figure 122. Input P1dB vs. RF Input Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

BASEBAND MODE, DSA_IN, LOW BAND

All measurements use DSA_IN as an input and baseband IQ as an output, with the RF low-band settings. DSA_OUT is connected to RF_IN on-board with a short 50Ω trace.

VDD_BB = 2.5V, all other supplies = 1.8V, and T_C = 25°C, unless otherwise noted.

Measurements performed with P_{RF} = −55dBm, P_{LO} = −5dBm, f_{RF} = 29GHz, f_{BB} = 100MHz, f_{LO} = 29.1GHz (lower sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), LO tunable filter wideband low settings, and V_{OCM} setting = 0x0C, unless otherwise noted.

Measurements performed with high gain settings (Register 0x194, Bits[1:0] = 0b'11) with on-board matching network, unless otherwise noted. Measurements performed as single-ended measurements on BB_IP output only, with other outputs BB_IN, BB_QP, and BB_QN terminated in 50Ω loads, unless otherwise noted. Data is corrected for 8.15dB of output matching-network loss and 3dB of differential loss, unless otherwise noted.

Conversion Gain

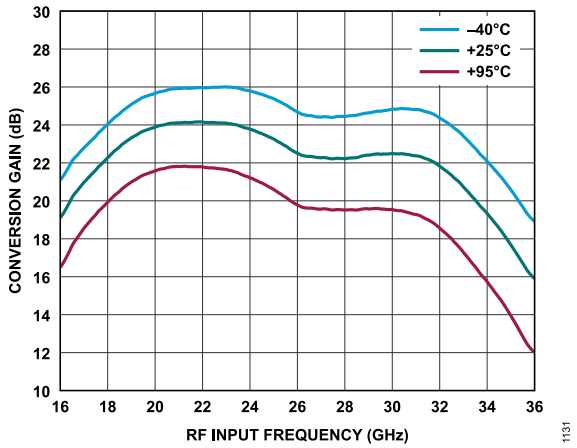

Figure 123. Conversion Gain vs. RF Input Frequency at Various Temperatures

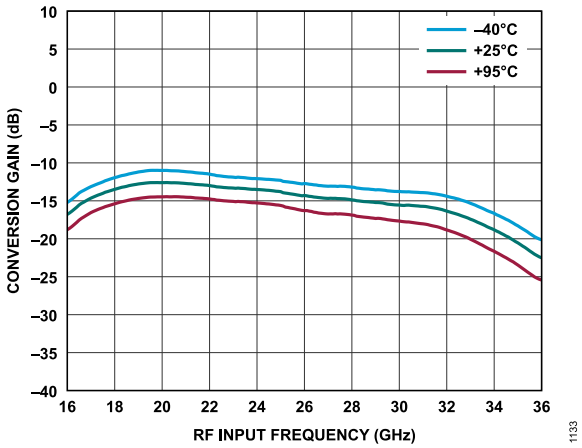

Figure 125. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

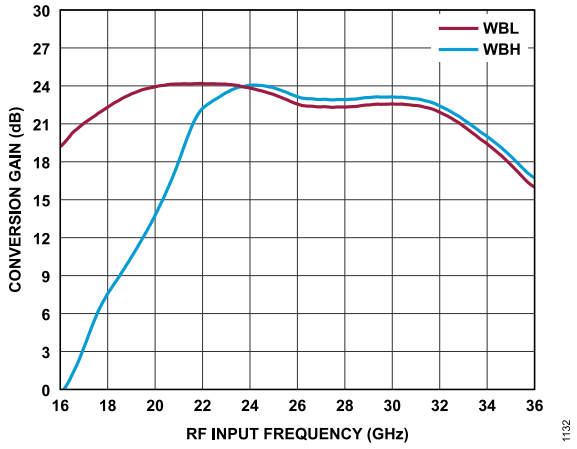

Figure 124. Conversion Gain vs. RF Input Frequency at Various LO Filter Settings

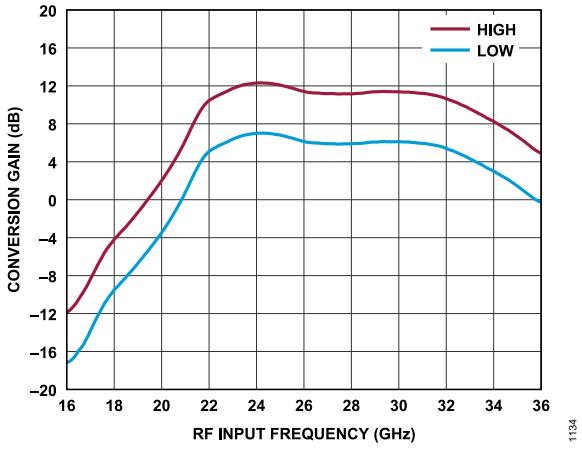

Figure 126. Conversion Gain vs. RF Input Frequency at Various Gain Settings

TYPICAL PERFORMANCE CHARACTERISTICS

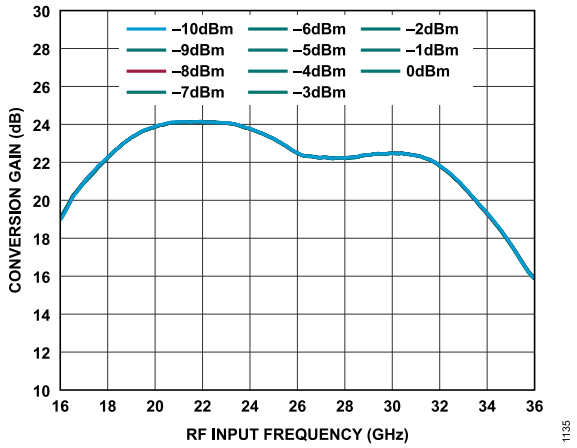

Figure 127. Conversion Gain vs. RF Input Frequency at Various LO Powers

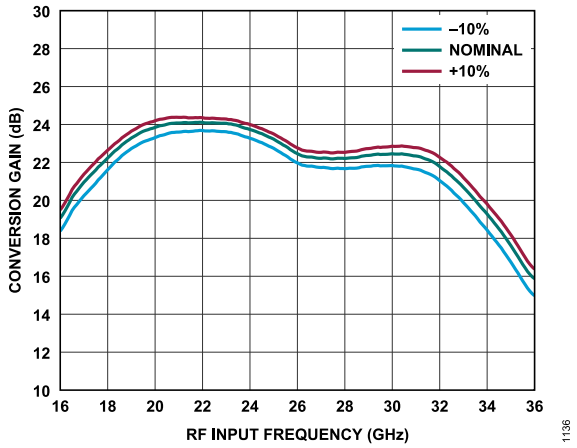

Figure 128. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

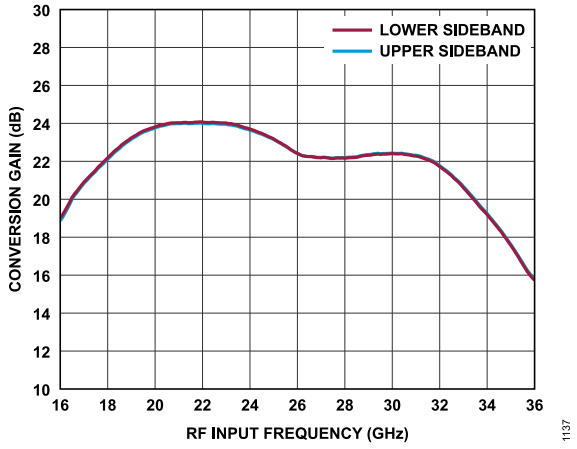

Figure 129. Conversion Gain vs. RF Input Frequency, Upper Sideband and Lower Sideband

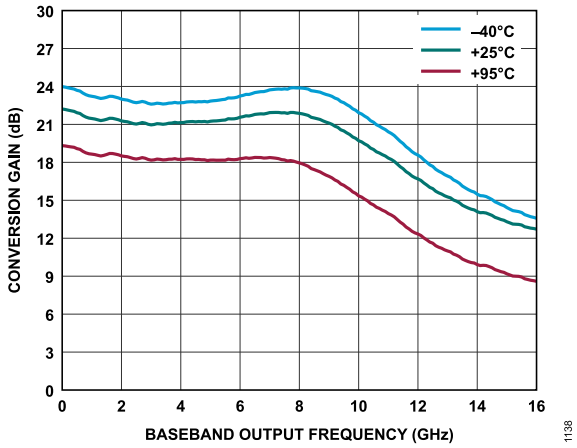

Figure 130. Conversion Gain vs. Baseband Output Frequency at Various Temperatures

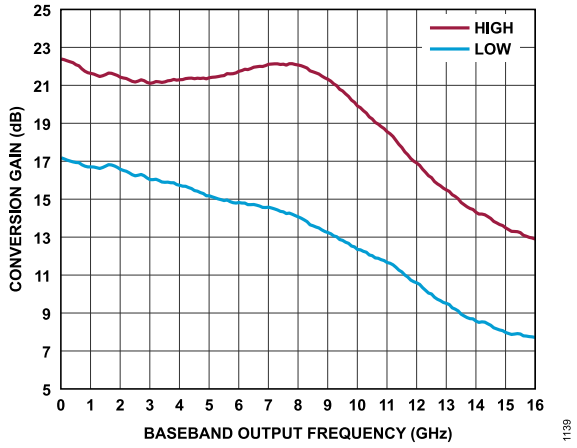

Figure 131. Conversion Gain vs. Baseband Output Frequency at Various Gain Settings

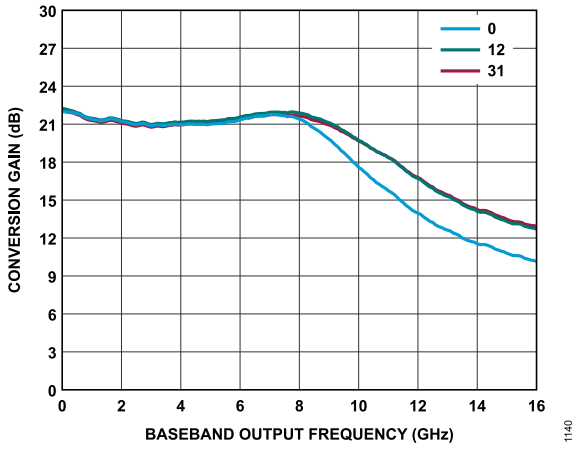

Figure 132. Conversion Gain vs. Baseband Output Frequency at Various Common-Mode Voltage Settings

TYPICAL PERFORMANCE CHARACTERISTICS

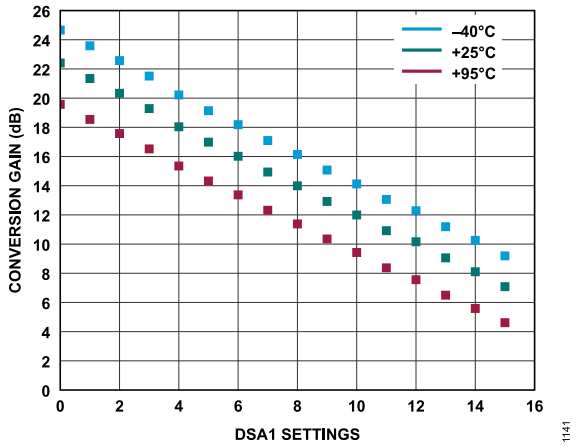

Figure 133. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

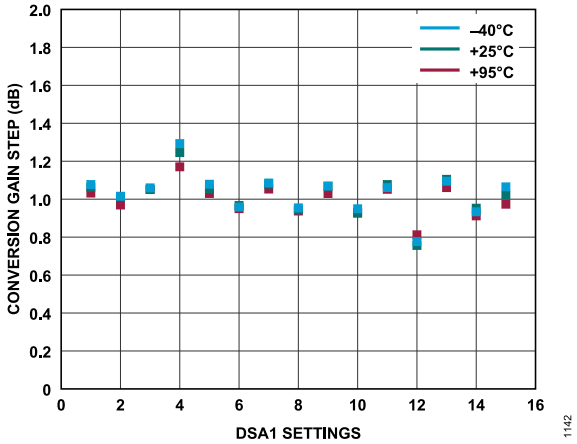

Figure 134. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

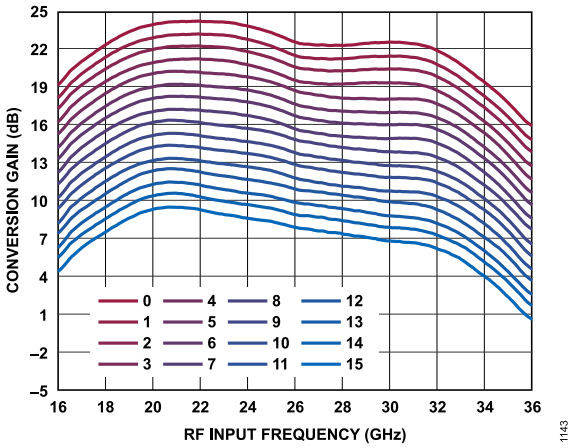

Figure 135. Conversion Gain vs. RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

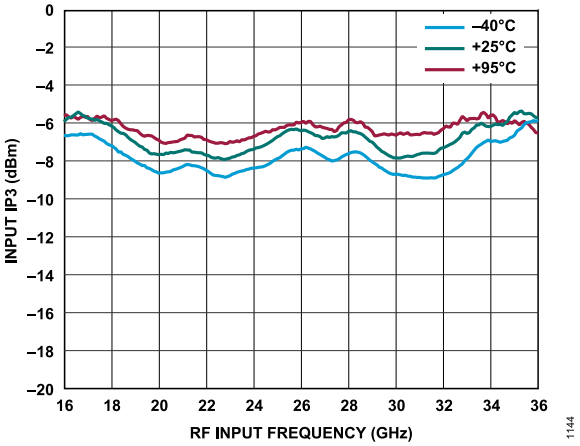

Figure 136. Input IP3 vs. RF Input Frequency at Various Temperatures

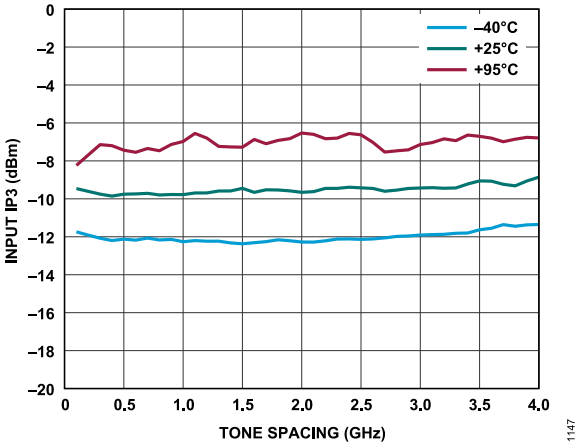

Figure 138. Input IP3 vs. Tone Spacing at Various Temperatures

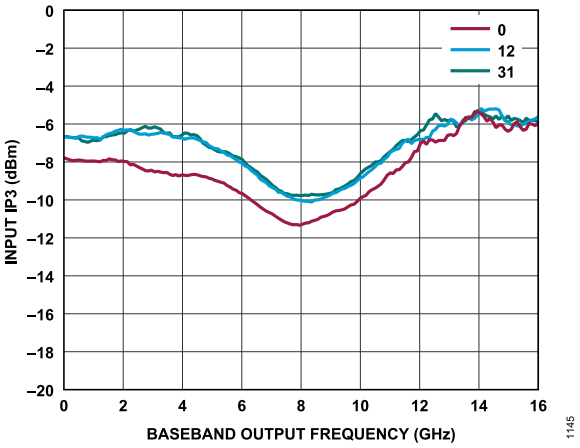

Figure 137. Input IP3 vs. Baseband Output Frequency at Various Common-Mode Voltage Settings

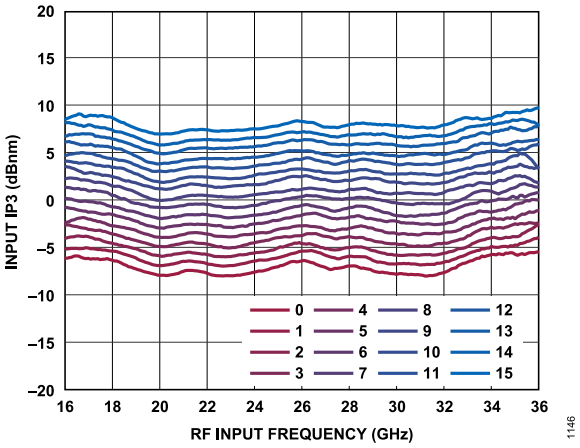

Figure 139. Input IP3 vs. RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

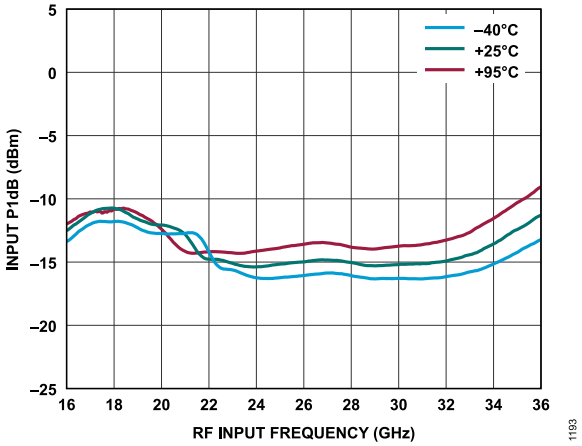

Figure 140. Input P1dB vs. RF Input Frequency at Various Temperatures

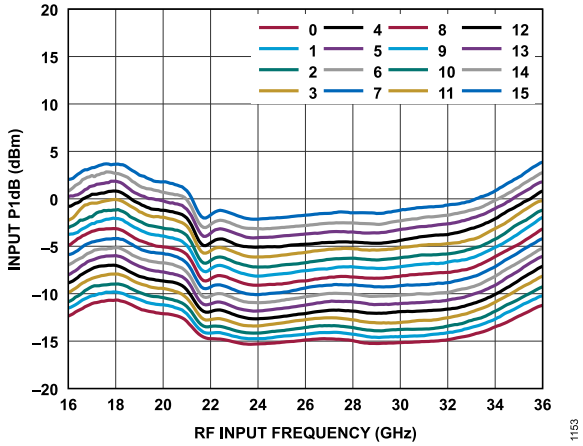

Figure 141. Input P1dB vs. RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

BASEBAND MODE, DSA_IN, HIGH BAND

All measurements use DSA_IN as an input and baseband IQ as an output, with the RF high-band settings. DSA_OUT is connected to RF_IN on-board with a short 50Ω trace.

VDD_BB = 2.5V, all other supplies = 1.8V, and T_C = 25°C, unless otherwise noted.

Measurements performed with P_{RF} = −40dBm, P_{LO} = −5dBm, f_{RF} = 49GHz, f_{BB} = 100MHz, f_{LO} = 48.9GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), LO tunable filter wideband high settings, and V_{OCM} setting = 0x0C, unless otherwise noted.

Measurements performed with high gain settings (Register 0x194, Bits[1:0] = 0b'11) with on-board matching network, unless otherwise noted. Measurements performed as single-ended measurements on BB_IP output only, with other outputs BB_IN, BB_QP, and BB_QN terminated in 50Ω loads, unless otherwise noted. Data is corrected for 8.15dB of output matching-network loss and 3dB of differential loss, unless otherwise noted.

Conversion Gain

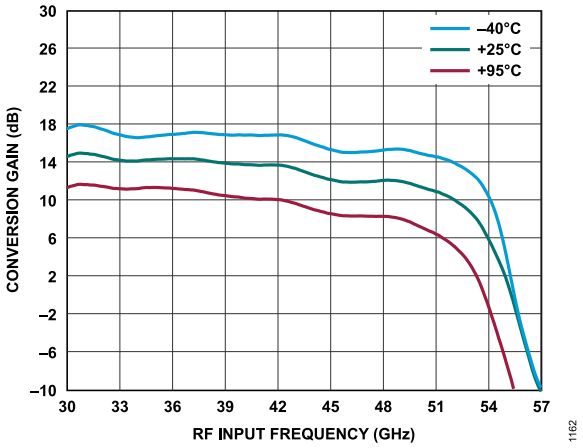

Figure 142. Conversion Gain vs. RF Input Frequency at Various Temperatures

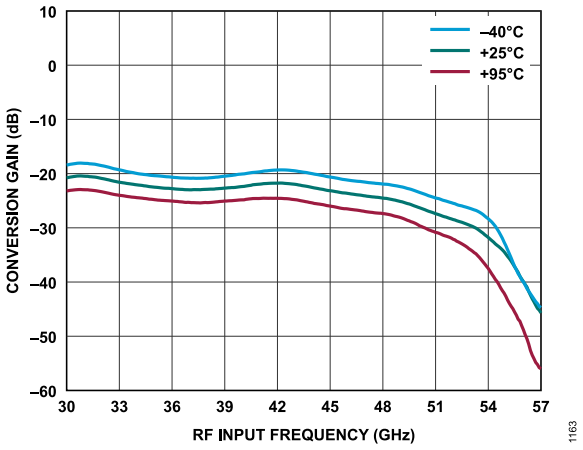

Figure 143. Conversion Gain vs. RF Input Frequency at Various Temperatures, Minimum Gain

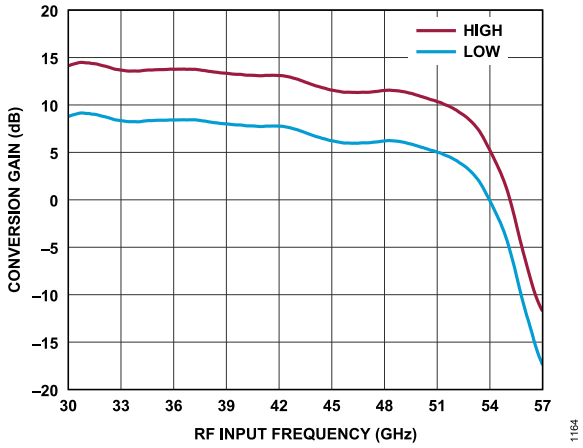

Figure 144. Conversion Gain vs. RF Input Frequency at Various Gain Settings

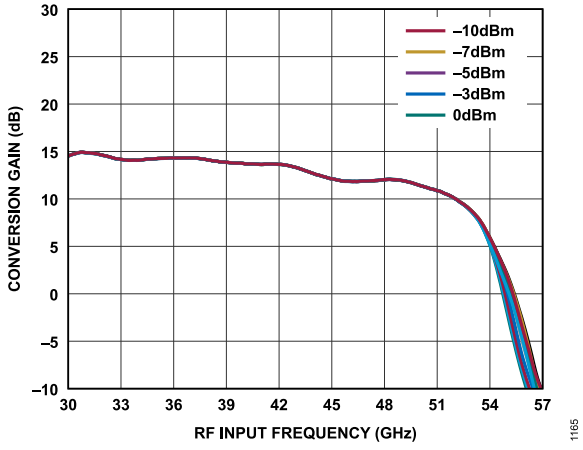

Figure 145. Conversion Gain vs. RF Input Frequency at Various LO Powers

TYPICAL PERFORMANCE CHARACTERISTICS

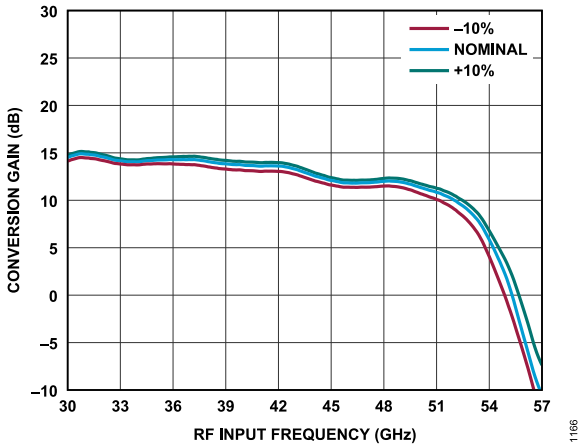

Figure 146. Conversion Gain vs. RF Input Frequency at Various Supply Voltages

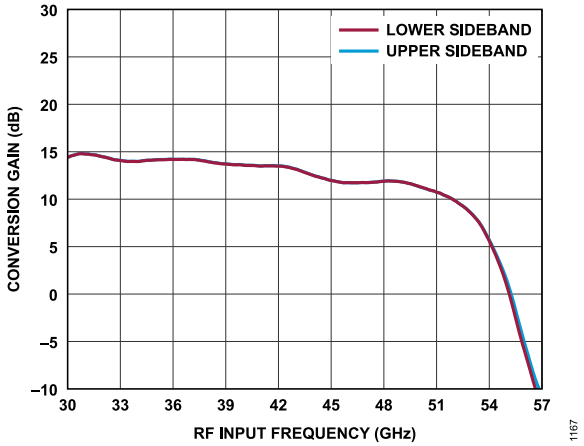

Figure 147. Conversion Gain vs. RF Input Frequency, Upper Sideband and Lower Sideband

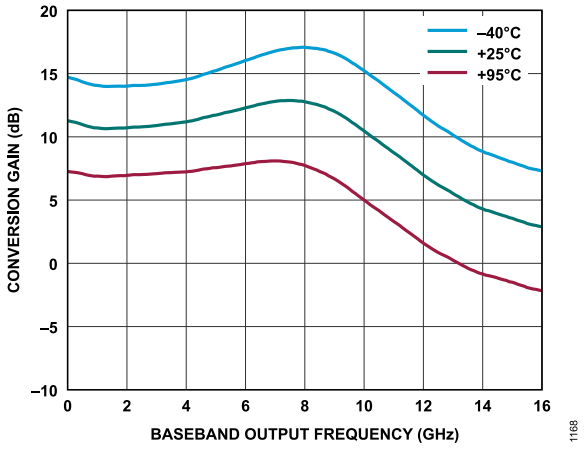

Figure 148. Conversion Gain vs. Baseband Output Frequency at Various Temperatures, Single f_{RF} = 49GHz

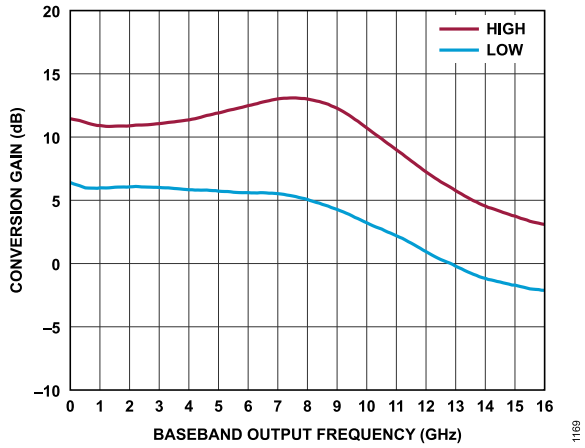

Figure 149. Conversion Gain vs. Baseband Output Frequency at Various Gain Settings

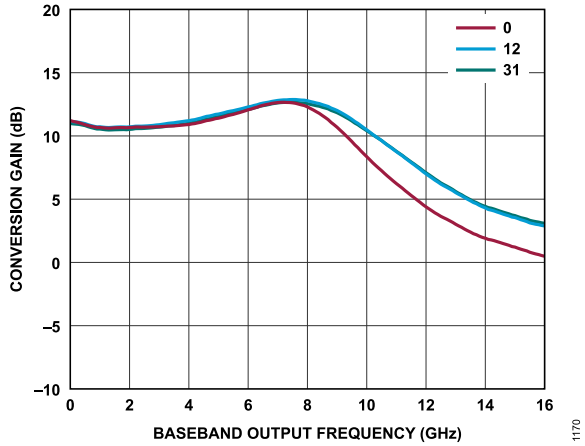

Figure 150. Conversion Gain vs. Baseband Output Frequency at Various Common-Mode Voltage Settings

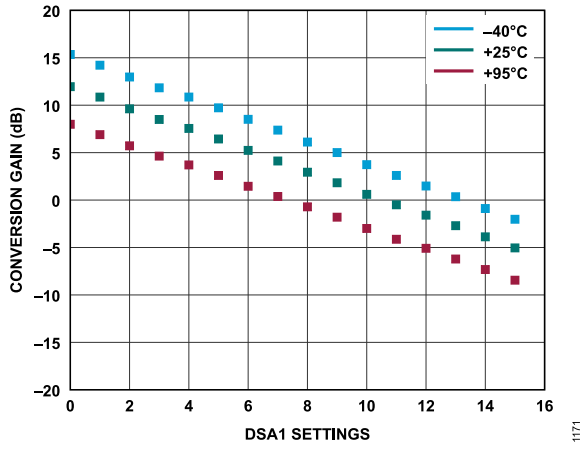

Figure 151. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

TYPICAL PERFORMANCE CHARACTERISTICS

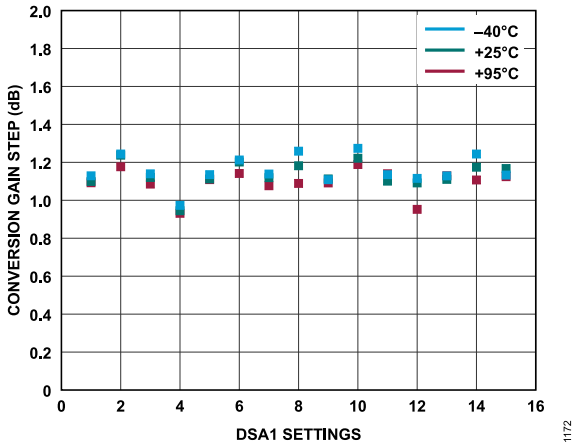

Figure 152. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

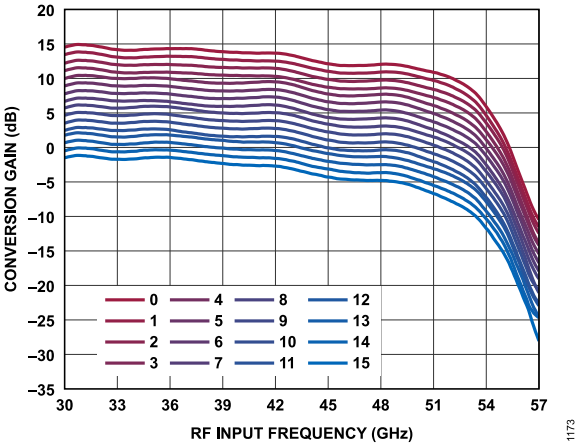

Figure 153. Conversion Gain vs RF Input Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Input IP3

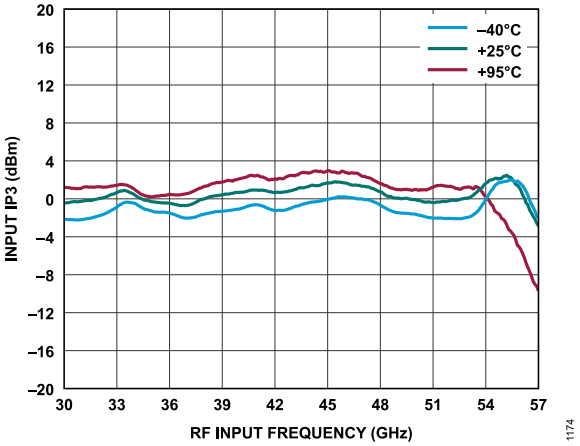

Figure 154. Input IP3 vs. RF Input Frequency at Various Temperatures

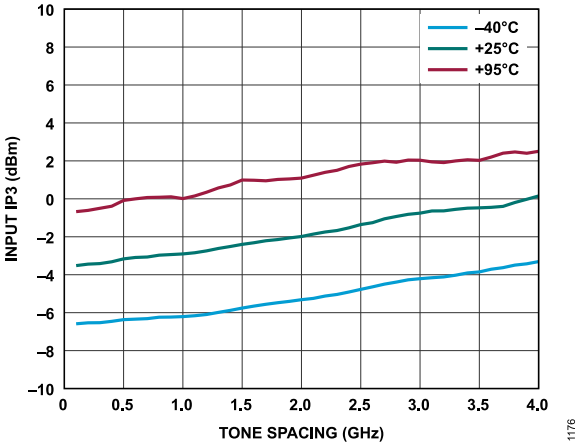

Figure 156. Input IP3 vs. Tone Spacing at Various Temperatures

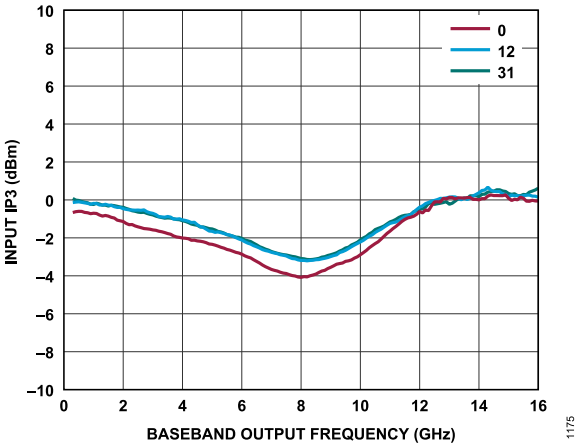

Figure 155. Input IP3 vs. Baseband Output Frequency at Various Common-Mode Voltage Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

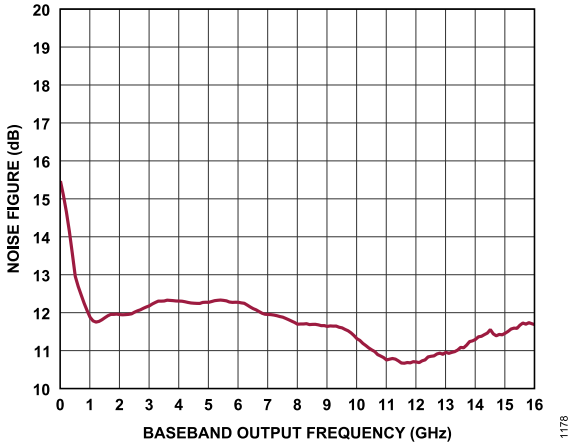

Figure 157. Noise Figure vs. Baseband Output Frequency, Measured with Output Balun Combining BB_IP and BB_IN Differentially, Corrected by −3dB for Single Sideband

TYPICAL PERFORMANCE CHARACTERISTICS

Input P1dB

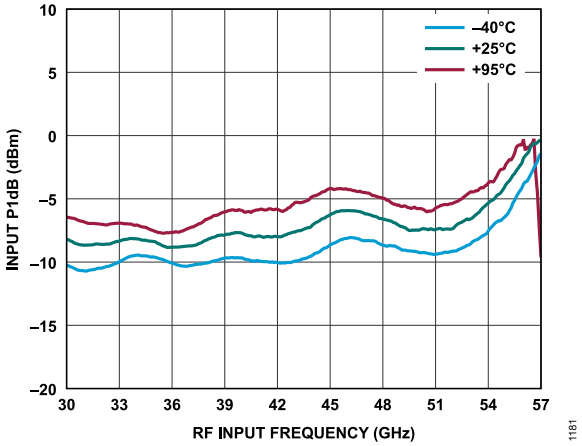

Figure 158. Input P1dB vs. RF Input Frequency at Various Temperatures

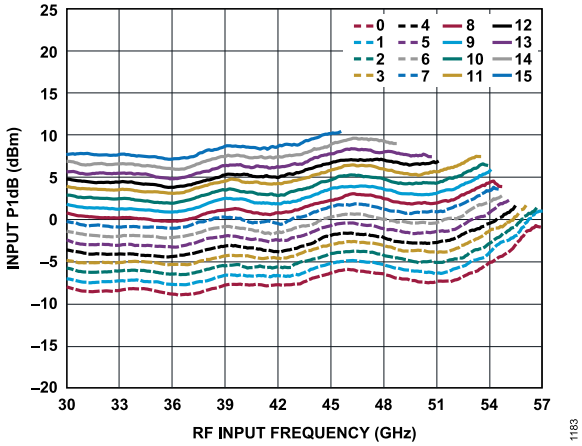

Figure 160. Input P1dB vs. RF Input Frequency at Various DSA1 Settings

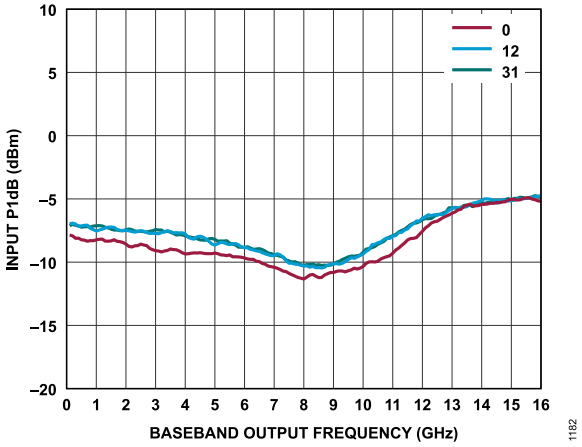

Figure 159. Input P1dB vs. Baseband Output Frequency at Various Common-Mode Voltage Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Signal Balance

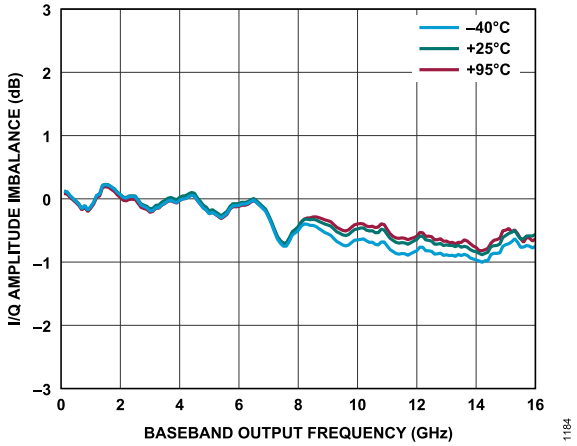

Figure 161. I/Q Amplitude Imbalance vs. Baseband Output Frequency at Various Temperatures, Baseband Gain High, No Calibration, Single f_{LO} = 42GHz, Baluns Used on I/Q Outputs

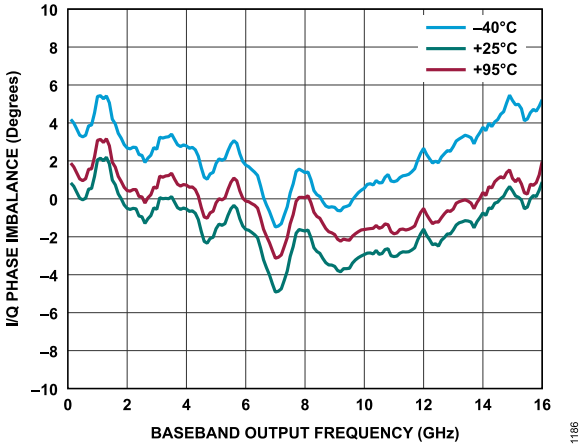

Figure 163. I/Q Phase Imbalance vs. Baseband Output Frequency at Various Temperatures, Baseband Gain High, No Calibration, Single f_{LO} = 42GHz, Baluns Used on I/Q Outputs

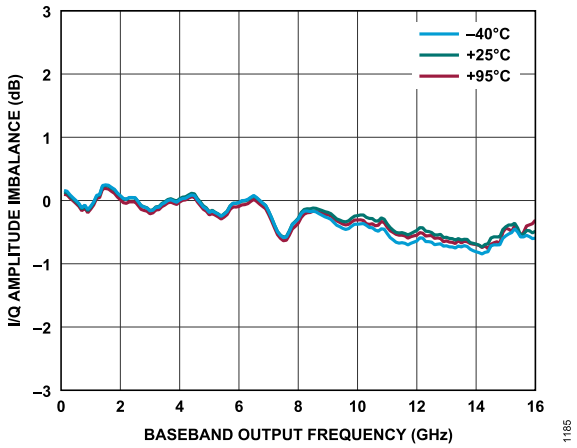

Figure 162. I/Q Amplitude Imbalance vs. Baseband Output Frequency at Various Temperatures, Baseband Gain Low, No Calibration, Single f_{LO} = 42GHz, Baluns Used on I/Q Outputs

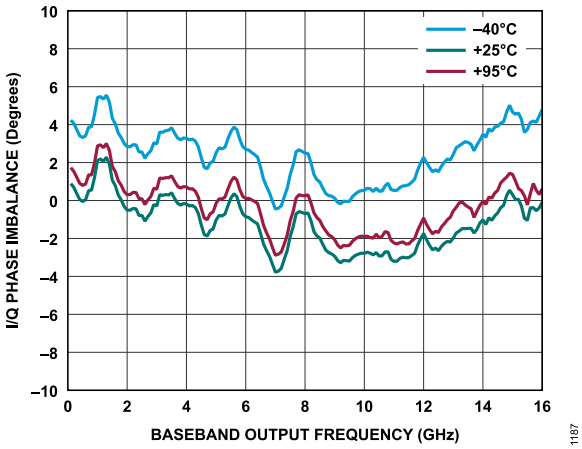

Figure 164. I/Q Phase Imbalance vs. Baseband Output Frequency at Various Temperatures, Baseband Gain Low, No Calibration, Single f_{LO} = 42GHz, Baluns Used on I/Q Outputs

TYPICAL PERFORMANCE CHARACTERISTICS

Output Common-Mode Voltage (V_{OCM})

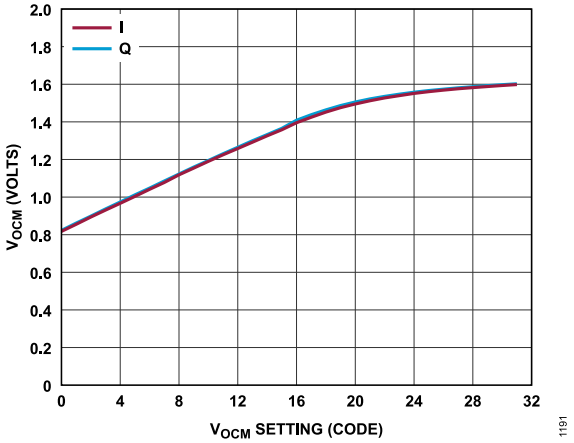

Figure 165. V_{OCM} vs. V_{OCM} Setting

THEORY OF OPERATION

CHIP OVERVIEW

The ADMV1455 is a highly integrated microwave downconverter designed for wideband radio systems operating across a broad RF frequency range of 17.7GHz to 55GHz. The device supports IF outputs up to 12GHz, enabling seamless integration with modern high-speed data converters and extending their effective frequency coverage well into the millimeter-wave spectrum.

The chip incorporates a fully configurable architecture that includes an I/Q mixer, a LO signal chain, two RF signal chains, an IF signal chain, and baseband I/Q amplifiers, all of which are configurable via a simple SPI. This level of integration minimizes the external component count while offering maximum design flexibility.

With its compact 6mm × 6.5mm footprint, wideband capability, and configurable signal chains, the ADMV1455 is ideally suited for next generation, high data rate systems requiring low size, weight, and power (SWaP) without compromising on system performance.

POWER-UP AND INITIALIZATION SEQUENCE

To power up and initialize the ADMV1455, take the following steps and refer to the Timing Diagrams Overview section and Figure 167 for more information:

1. Ensure that all digital logic inputs are logic level low.
2. Power on all supply voltages simultaneously, with a rise time of 1ms or longer.
3. Once the supplies are stable, set $\overline{\text{RST}}$ to logic level high.
4. Program the NVM load instructions.
5. Program the necessary registers for the intended chip operation.
6. Set CEN to logic level high.

POWER-DOWN SEQUENCE

There are two possible power-down options available for the ADMV1455. One power-down option removes all power from the chip, and the other power-down option disables the chip, causing it to enter a low power mode.

Full Power-Down

To fully power down the chip in an ordered fashion, take the following steps and refer to Figure 170 for more information:

1. Set CEN to logic level low.
2. Set all other logic inputs to logic level low.
3. Power off all supply voltages.

Chip Disable with CEN

To disable the chip and enter low power mode while the supply voltages are still powered on, bring CEN to logic level low. Bringing CEN to logic level low causes the chip to power off most of the RF circuits within the chip. Refer to Figure 169 for more information.

THEORY OF OPERATION

SPI

The ADMV1455 utilizes the SPI for communication to configure the chip settings. The SPI can be implemented in either 3-wire or 4-wire configurations, supports 1.8V logic levels, and SCLK frequencies up to 125MHz.

The SPI consists of digital inputs and outputs. CHIP_ADD0, CHIP_ADD1, SCLK, and $\overline{CS}$ are the digital inputs. SDIO is bidirectional and can be an input or output, depending upon the type of SPI operation being performed, and SDO is a digital output that remains in a high impedance state unless a read operation is being performed. $\overline{CS}$ is an active low digital input and must be asserted low during a SPI instruction. Be sure to deasserted $\overline{CS}$ at the end of a SPI instruction.

The chip address inputs, CHIP_ADD0 and CHIP_ADD1, can be used in multichip systems to assign an address to a particular chip. This feature allows up to four chips to share SCLK, SDIO, SDO, and $\overline{CS}$ connections. To set a chip address input to 0, ground the ball or add a 0Ω pull-down resistor. To set a chip address input to 1, leave it floating, and the internal 15kΩ resistor will set it to a logic level high. The assigned chip address modifies the SPI Communications Frame Bits[21:20].

For single SPI instructions, the communications frame is 24-bits wide and consists of a 16-bit header and 8 bits of data. The header contains a R/W bit, a broadcast (BR) bit, two chip address bits, and 12 register address bits. Both the header and data are organized MSB first and must be shifted in on SDIO with the chip sampling the logic level on the rising edge of SCLK. See Figure 166 for the SPI communications frame.

Set the R/W bit to 0 for a write operation and set the R/W to 1 for a read operation. Set the BR bit to 0 for single chip SPI instructions and set this bit to 1 to have all chips, regardless of their chip address, respond to a SPI instruction. For read operations, the BR bit must only be set to 0.

For a read operation when using a 3-wire SPI, the SDIO changes from an input to an output after the last header SCLK rising edge. The data is then shifted out on SDIO, with the logic level changing on the falling edge of SCLK, so that it can be sampled on the next rising edge of SCLK. When $\overline{CS}$ is deasserted, SDIO changes back to a digital input.

For a read operation when using a 4-wire SPI, the SDO transitions from a high impedance state to an active output, after the last header SCLK rising edge. The data is then shifted out on SDO, with the logic level changing on the falling edge of SCLK, so that it can be sampled on the next rising edge of SCLK. When $\overline{CS}$ is deasserted, SDO returns to a high impedance state.

The ADMV1455 supports SPI streaming that minimizes the SPI instruction time. During a SPI streaming instruction, $\overline{CS}$ is asserted low, a single 16-bit header instruction is given, followed by multiple bytes of data, and then $\overline{CS}$ is deasserted to end the instruction. Sequential register addresses are assumed in ascending or descending order based on how Register 0x000, Bit 5 and Bit 2 are set. Note that the default order is descending addresses.

If $\overline{CS}$ is deasserted during any header portion of a SPI instruction, the operation is ignored. If $\overline{CS}$ is deasserted during a data portion of a SPI instruction, then that data is ignored. For SPI streaming operations, any complete bytes (8 bits) of data are accepted by the chip, but a partial byte is ignored.

See the Timing Diagrams Overview section, the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional timing information and refer to the ADI-SPI, Serial Control Interface Standard (Rev 1.0) for more information on SPI and communications protocol.

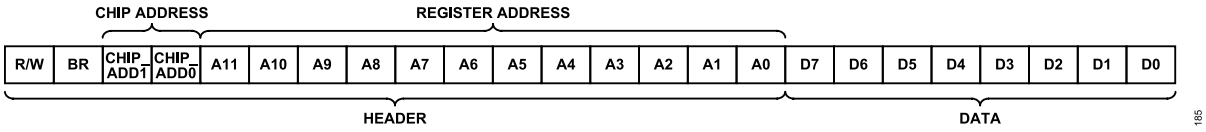

Figure 166. Single SPI Frame Timing Diagram

THEORY OF OPERATION

TIMING DIAGRAMS OVERVIEW

The timing diagrams shown in Figure 167, Figure 168, Figure 169, and Figure 170 help with visualizing the various programming and power sequences of operation for the ADMV1455. These timing diagrams utilize the timing specifications detailed in Table 8.

Contained within this guidance are limitations to prevent possible damage to the ADMV1455, such as keeping the digital inputs low during power up and removing the digital inputs before or at the same time as power down. Additionally, the timing diagrams contain best practices for operation, such as programming the necessary SPI instructions prior to enabling the RF portions of the chip using the CEN input.

See the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional details regarding these timing diagrams.

Power-Up and Apply the Digital Inputs

The power-up and initialization timing diagram (see Figure 167) shows the power supplies rising by t_1, starting from the start time, t_{START}. After the power supply voltages have been brought to 90% of their nominal values, valid digital inputs can be applied after waiting a minimum time of t_2 at $t_{DIGITAL}$. To prevent possible damage to the chip, do not apply digital inputs before $t_{DIGITAL}$.

Generally, at $t_{DIGITAL}$, the $\overline{RST}$ and $\overline{CS}$ inputs go high together. If applicable, the CHIP_ADD0 and CHIP_ADD1 are also set at this time in preparation for the SPI instructions. Wait a minimum of t_3 to allow the chip to reset before beginning the SPI instructions at the initialization time, $t_{INITIALIZE}$.

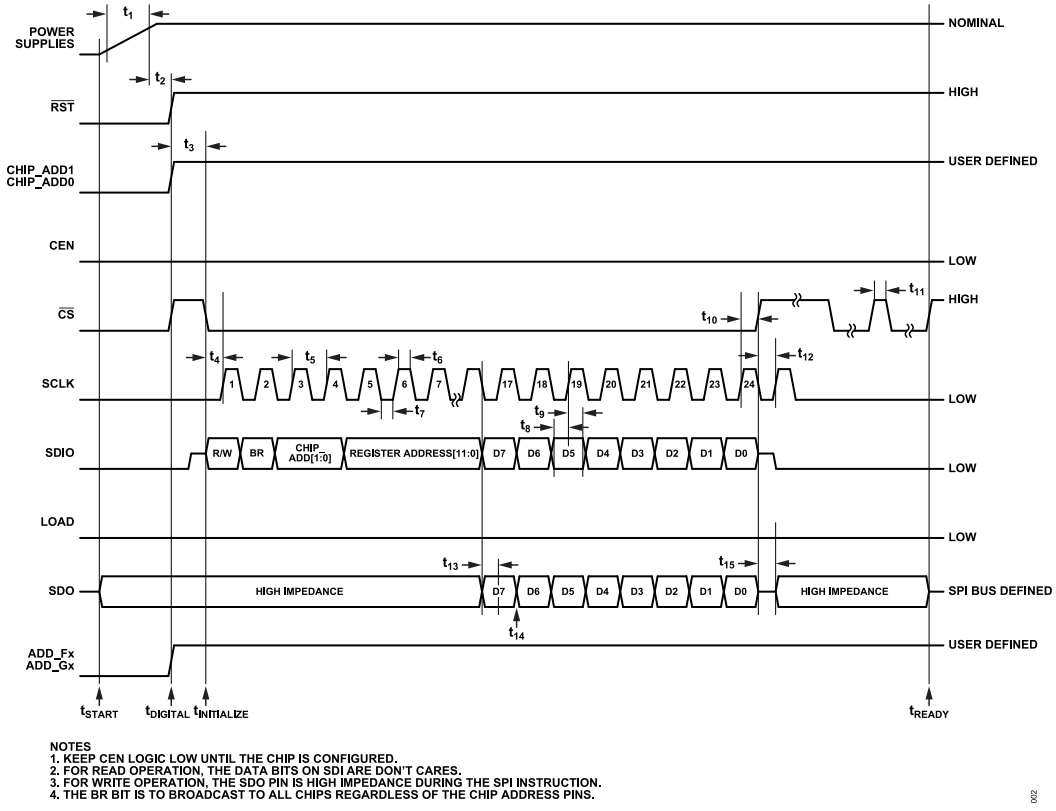

Figure 167. Power-Up and Initialization Timing Diagram

THEORY OF OPERATION

Initialization SPI Instructions

Starting at $t_{INITIALIZE}$ (see Figure 167), configure the chip by using the SPI instructions for its intended operation. Give all the necessary SPI instructions to configure the chip, looping from $t_{INITIALIZE}$ to the ready time, t_{READY} for each instruction. Keep the CEN input low during the initialization SPI instructions, and complete the initialization at t_{READY}.

Chip Enable and Operation

After all the initialization SPI instructions have been completed, wait a minimum of t_{16} to ensure that the digital logic has processed the instructions prior to setting the CEN input high at $t_{OPERATIONAL}$ to enable chip operation. At $t_{OPERATIONAL}$, the RF portions of the chip are enabled. See Figure 168 for more information.

During chip operation, any necessary SPI instructions can be given, along with the LOAD input toggles, and any changes to the ADD_Fx and ADD_Gx inputs. Continue operating, looping from $t_{OPERATIONAL}$ to $t_{CONTINUE}$ until it is desired to either disable the chip, reset the chip, or power down the chip.

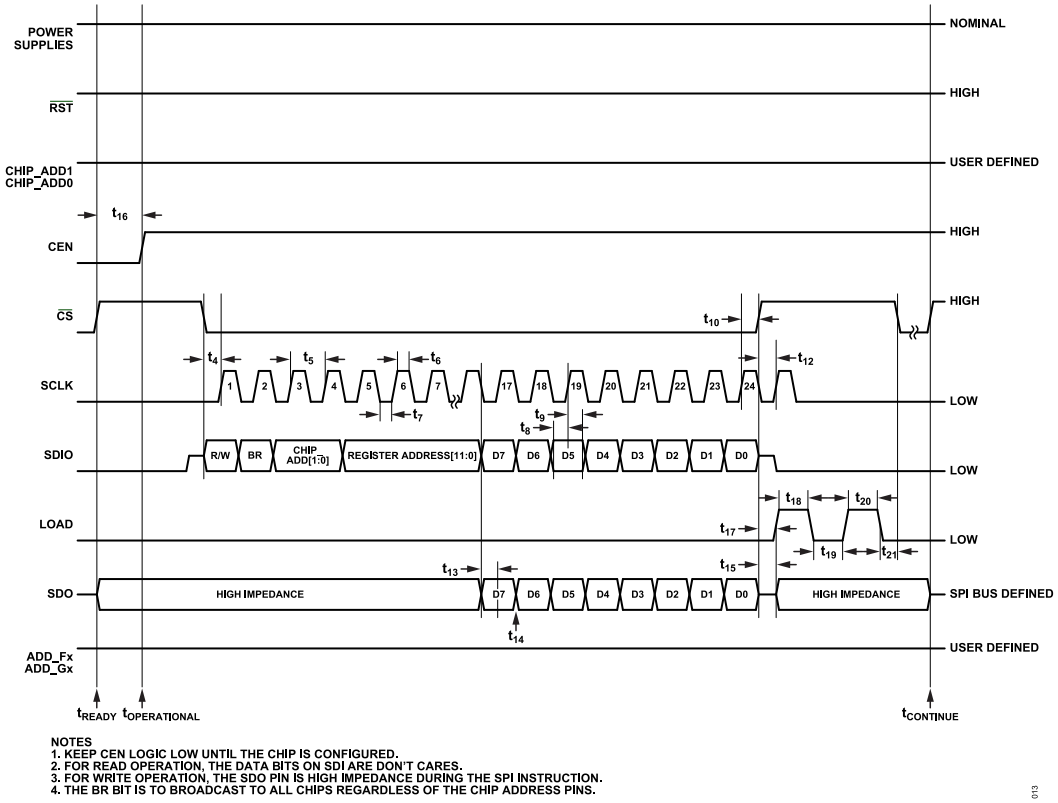

Figure 168. Operational Timing Diagram

THEORY OF OPERATION

Chip Disable and Reset

When it is desired to either disable the chip or reset the chip, follow Figure 169 starting at $t_{CONTINUE}$. Wait a minimum of t_{22} from the last SPI instruction before disabling the chip by setting the CEN input low at $t_{DISABLE}$.

After setting the CEN input low, wait a minimum of t_{23} to allow the RF portions of the chip to power down. The $\overline{RST}$ input can then be set low for a minimum of t_{24} before the $\overline{RST}$ input can be set high again. Wait a minimum of t_3 before looping back to $t_{INITIALIZE}$, which is shown in Figure 167.

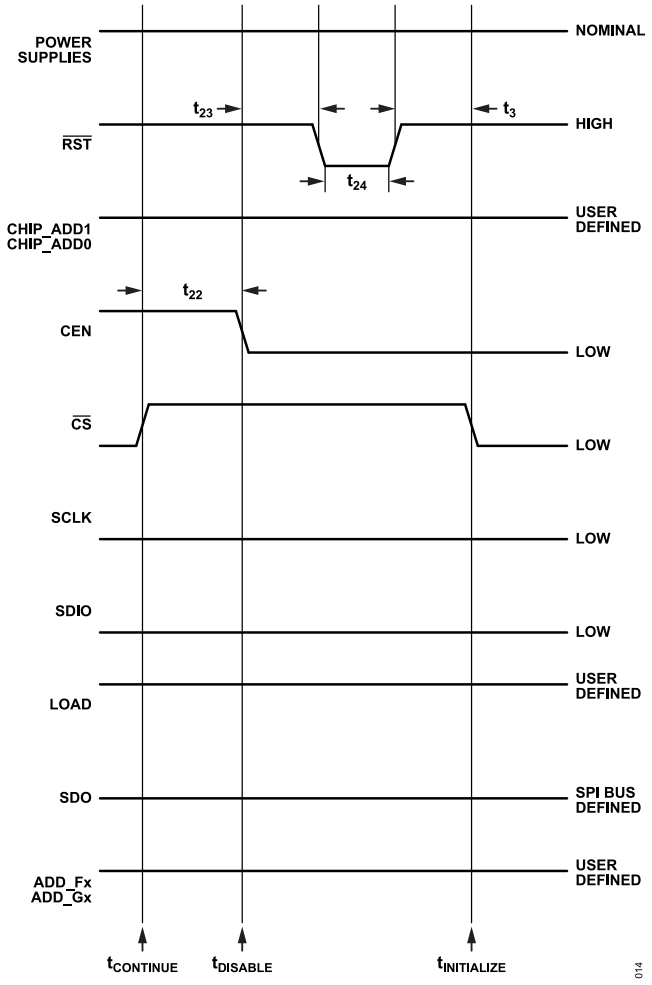

Figure 169. Chip Disable and Reset Timing Diagram

Chip Disable and Power-Down

When it is desired to disable and power down the chip, follow Figure 170 starting at $t_{CONTINUE}$. Wait a minimum of t_{22} from the last SPI instruction before disabling the chip by setting the CEN input low at $t_{DISABLE}$.

After setting the CEN input low, wait a minimum of t_{25} to allow the RF portions of the chip to power down before starting the chip power down at $t_{POWER-DOWN}$. At $t_{POWER-DOWN}$, all other logic inputs must be set low with a fall time of t_{26}, and the power supply voltages can be turned off with a fall time of t_{27}. Ideally, the logic inputs are removed prior to the power supply ramp down, but they can occur simultaneously provided that the logic inputs fall time does not exceed the t_{26} maximum time. Note that the time units for t_{26} are in microseconds, and the time units for t_{27} are milliseconds.

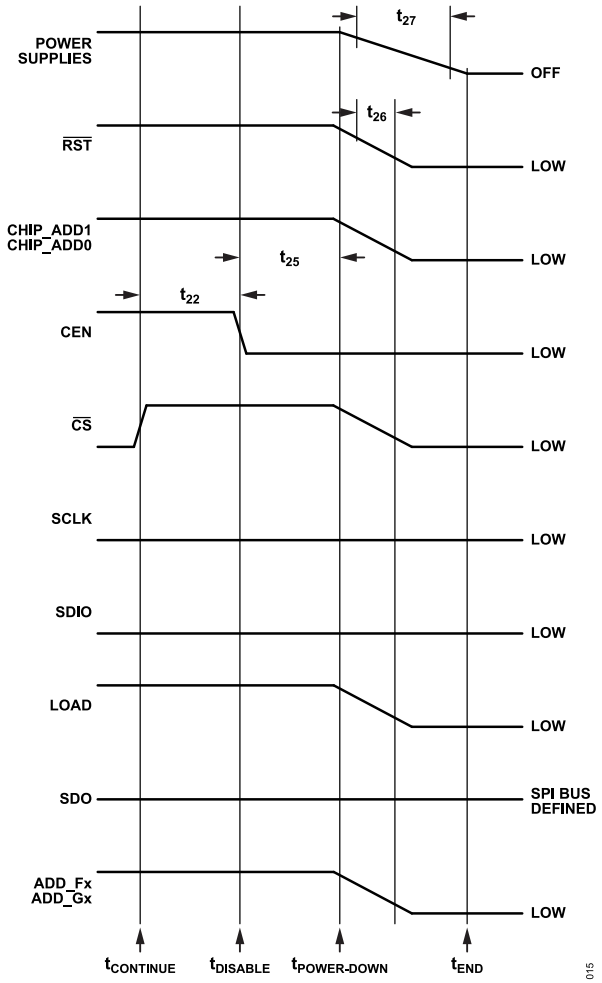

Figure 170. Chip Disable and Power-Down Timing Diagram

THEORY OF OPERATION

NONVOLATILE MEMORY

The ADMV1455 contains a simple nonvolatile memory (NVM) that is used to store factory calibration values to minimize part to part variation. The values in the NVM set the chip bias current, trim the internal ADC, and trim the internal temperature sensor. At chip power-up, it is recommended to ensure that this NVM has loaded its values into their correct shadow registers. The NVM is static and can not be modified by the user.

NVM Health Check

To confirm the NVM values have loaded, use the following NVM health check instructions:

1. Shadow Register 0x033 by doing the following:
   - Set Register 0x07B to Value 0x33.
   - Read Register 0x07B, it should return 0x33.
   - Read Register 0x07C, it should return a nonzero value, typically 0x20.
2. Shadow Register 0x034 by doing the following:
   - Set Register 0x07B to Value 0x34.
   - Read Register 0x07B, it should return 0x34.
   - Read Register 0x07C, it should return a nonzero value, typically 0x20.
3. Shadow Register 0x037 by doing the following:
   - Set Register 0x07B to Value 0x37.
   - Read Register 0x07B, it should return 0x37.
   - Read Register 0x07C, it should return a nonzero value, typically 0x0D.
4. Shadow Register 0x038 by doing the following:
   - Set Register 0x07B to Value 0x38.
   - Read Register 0x07B, it should return 0x38.
   - Read Register 0x07C, it should return a nonzero value, typically 0x0D.

If any of the return values are zero, follow the instructions detailed in the NVM Load Instructions section.

NVM Load Instructions

If any of the return values from Register 0x07C are zero, run the following NVM load instructions:

1. Set Register 0x078 to Value 0x08.
2. Pause 1ms.
3. Set Register 0x07E to Value 0x40.
4. Pause 1ms.
5. Set Register 0x07E to Value 0x54.
6. Pause 1ms.
7. Set Register 0x078 to Value 0x09.

DIGITAL OVERVIEW

The ADMV1455 contains advanced digital logic that allows for various methods of configuring each circuit block within the chip. These methods include simple register configurations, a synchronous LOAD feature, look-up tables (LUTs), logic state machines, parallel input logic pointers, and general-purpose logic outputs.

The digital logic can be partitioned into two subsections, one for frequency control (filters) and the other for gain control (attenuators). See Figure 171 and Figure 172 for representative diagrams for each subsection. When reviewing these diagrams, it may be helpful to follow from right to left, starting from the items being controlled, then deciding the input control method.

For the frequency control subsection, the most simplistic way of configuring the filters and GPO_Fx logic outputs is by using Register 0x800 to Register 0x80C. Register 0x2A0 is a bypass register that allows setting the RF chain LPF value, and this register gives more resolution than the LPF value in Register 0x802. Similarly, Register 0x2A1 is the bypass register for the RF chain HPF value, and this register gives more resolution than the HPF value in Register 0x804. Register 0x2A2 is a necessary register that trims the IF chain BPF corner frequencies. See Table 24 for the recommended values.

When evaluating the ADMV1455, if there is a plan to implement the chip to use the LUT to set the filters, then it is recommended to use Register 0x802 and Register 0x804. However, if there is no plan to use the LUT, then it is advantageous to use Register 0x2A0 and Register 0x2A1 because these registers provide more resolution.

For the gain control subsection, the most simplistic way of configuring the attenuators and GPO_Gx logic outputs is by using Register 0x28B to Register 0x28E. Register 0x600 to Register 0x603 can also be used when it is desired to use the LOAD feature.

THEORY OF OPERATION

Digital Diagrams

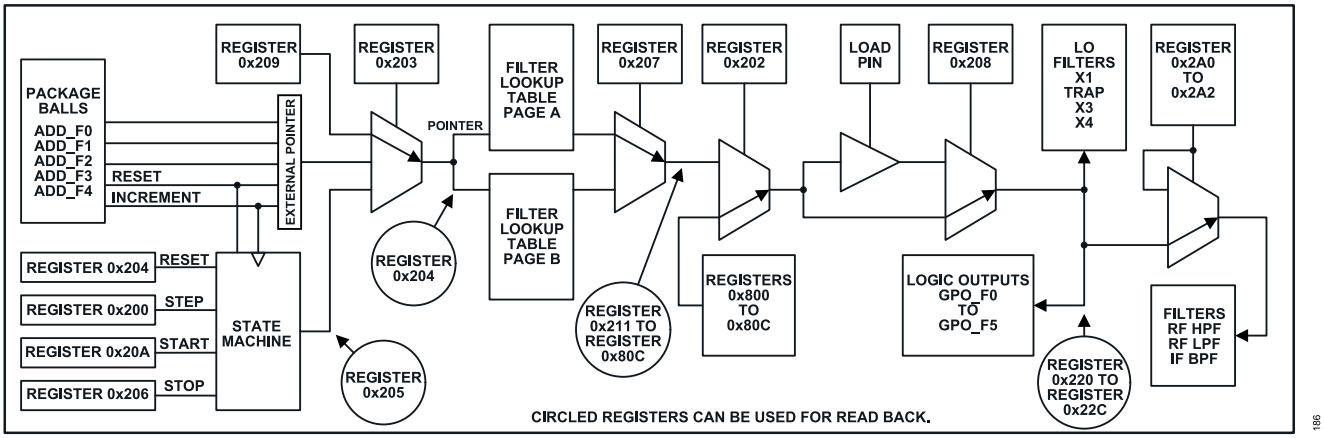

Figure 171. Filter Diagram

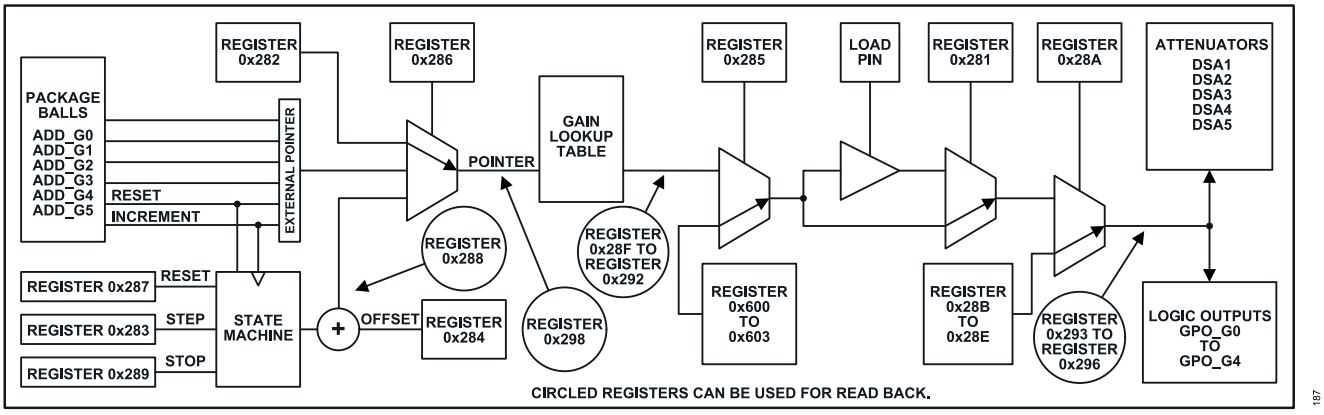

Figure 172. Gain Diagram

SYNCHRONOUS LOAD FEATURE

The ADMV1455 includes a synchronous load feature that allows the filter settings and gain settings to be applied at specific trigger rising edge events on the LOAD ball. See Figure 168 for the LOAD feature timing. To enable the load feature for the filter settings, set Register 0x208 to 1. To enable the load feature for the gain settings, set Register 0x281 to 1.

FILTER LUT

The digital logic contains a filter LUT that can be used to determine the state of the LO tunable filters, RF tunable filters, and GPO_F logic outputs. This LUT can be beneficial for fast frequency hopping applications, where it may be necessary to quickly change chip configuration states.

To use the LUT, set Register 0x202 to 1 and setup the LUT from Register 0x900 to Register 0xC3F.

The LUT contains two pages that have 32 indices each, or 64 total. To select Page A, set Register 0x207 to 0. To select Page B, set Register 0x207 to 1.

There are three potential sources for the LUT index (pointer), as determined by Register 0x203. The pointer can be set by using the parallel logic input ADD_F balls, by using Register 0x209, or by using the internal state machine. Set Register 0x203 to 0 to use ADD_F balls as the pointer, set Register 0x203 to 1 to use Register 0x209 as the pointer, and Register 0x203 set to 2 to use the internal state machine.

Regardless of the LUT pointer source, use Register 0x240 to read back the pointer value.

The LUT output values can be read from Register 0x211 to Register 0x21D. The values in these registers represent the filter values prior to the mux controlled by Register 0x202 and the LOAD feature.

THEORY OF OPERATION

Filter State Machine

The internal state machine can be used to sequence through many states, using the ADD_F4 input to advance and the ADD_F3 to reset. The state machine has several input parameters from the SPI, such as start value, stop value, step size, wrap setting, and reset.

At power up, the state machine output is zero, and it can be reset to zero using either the ADD_F3 ball or Register 0x204. Set ADD_F3 to logic high to hold the state machine in reset and then bring to logic low to re-enter normal operation. Alternatively, set Register 0x204 to 0 to hold the state machine in reset and then set it back to 1 to re-enter normal operation.

To ensure the state machine is well behaved, it is recommended to set the stop value greater than the start value. The step size is a 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF. A step size of zero is invalid.

Use Register 0x205 to read back the current value of the state machine.

When the wrap setting is disabled, incremental sequencing starts at zero, incrementing by the step size. If the state machine has reached the stop value, then the next state is the start value. If the step size increments to more than the stop value, then the start value is used.

When the wrap setting is disabled, decremental sequencing starts at zero, then decrements by the step size. If the state machine has reached zero, then the next state is the stop value. If the step size decrements to less than zero, then the stop value is used. The start value is ignored during this sequence.

When the wrap setting is enabled, incremental sequencing starts at zero, then increments by the step size. If the step size increments to more than the stop value, then the sequence rolls over and continues the remaining count from zero. The start value is ignored during this sequence.

When the wrap setting is enabled, decremental sequencing starts at zero, then decrements by the step size. If the step size decrements to less than zero, then the sequence rolls over and continues the remaining count from the stop value. The start value is ignored during this sequence.

Refer to Table 18 for the applicable registers and example state machine behavior. The sequences shown in Table 18 continue indefinitely for each rising edge on ADD_F4.

Table 18. Filter State Machine Example Behavior

Example	Step[1]	Start[2]	Stop[3]	Wrap[4]	State Machine Sequence
1	+1	3	6	0	0, 1, 2, 3, 4, 5, 6, 3, 4, 5, 6, 3, 4, 5, 6...
2	+2	3	6	0	0, 2, 4, 6, 3, 5, 3, 5, 3, 5, 3, 5, 3, 5, 3...
3	+3	3	6	0	0, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6...
4	+4	3	6	0	0, 4, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3...
5	−1	3	6	0	0, 6, 5, 4, 3, 2, 1, 0, 6, 5, 4, 3, 2, 1, 0...
6	−2	3	6	0	0, 6, 4, 2, 0, 6, 4, 2, 0, 6, 4, 2, 0, 6, 4...
7	−3	3	6	0	0, 6, 3, 0, 6, 3, 0, 6, 3, 0, 6, 3, 0, 6, 3...
8	−4	3	6	0	0, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2...
9	+1	3	6	1	0, 1, 2, 3, 4, 5, 6, 0, 1, 2, 3, 4, 5, 6, 0...
10	+2	3	6	1	0, 2, 4, 6, 1, 3, 5, 0, 2, 4, 6, 1, 3, 5, 0...
11	+3	3	6	1	0, 3, 6, 2, 5, 1, 4, 0, 3, 6, 2, 5, 1, 4, 0...
12	+4	3	6	1	0, 4, 1, 5, 2, 6, 3, 0, 4, 1, 5, 2, 6, 3, 0...
13	−1	3	6	1	0, 6, 5, 4, 3, 2, 1, 0, 6, 5, 4, 3, 2, 1, 0...
14	−2	3	6	1	0, 5, 3, 1, 6, 4, 2, 0, 5, 3, 1, 6, 4, 2, 0...
15	−3	3	6	1	0, 4, 1, 5, 2, 6, 3, 0, 4, 1, 5, 2, 6, 3, 0...
16	−4	3	6	1	0, 3, 6, 2, 5, 1, 4, 0, 3, 6, 2, 5, 1, 4, 0...

[1] The step size is determined by Register 0x200, Bits[7:0].

[2] The start is determined by Register 0x20A, Bits[4:0].

[3] The stop is determined by Register 0x206, Bits[4:0].

[4] The wrap setting is determined by Register 0x20A, Bit 5.

THEORY OF OPERATION

GAIN LUT

The digital logic contains a gain LUT with 67 indices that can be used to determine the state of the DSAs and the GPO_G logic outputs. This LUT can be beneficial for fast frequency hopping applications, where it may be necessary to quickly change the chip configuration states.

To use the LUT, set Register 0x285 to 1 and setup the LUT from Register 0xE00 to Register 0xF0B.

There are three potential sources for the LUT index (pointer), as determined by Register 0x286. The pointer can be set by using the parallel logic input ADD_G balls, by using Register 0x282, or by using the internal state machine. Set Register 0x286 to 0 to use ADD_G balls as the pointer, set Register 0x286 to 1 to use Register 0x282 as the pointer, and set Register 0x286 to 2 to use the internal state machine.

Regardless of LUT pointer source, use Register 0x298 to read back the pointer value.

The LUT output values can be read from Register 0x28F to Register 0x290. The values in these registers represent the DSA values prior to the mux controlled by Register 0x285 and the LOAD feature.

Gain State Machine

The internal state machine can be used to sequence through many states, using the ADD_G5 input to advance and ADD_G4 to reset. The state machine has several input parameters from the SPI, such as offset value, stop value, step size, and reset.

At power up, the state machine output is zero, and it can be reset to zero using either the ADD_G4 ball or Register 0x287. Set ADD_G4 to logic high to hold the state machine in reset and then bring to logic low to re-enter normal operation. Alternatively, set Register 0x287 to 0 to hold the state machine in reset and then set it back to 1 to re-enter normal operation.

The step size is a 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF. A step size of zero is invalid.

The state machine increments or decrements on each rising edge of ADD_G5 based upon the step size value programmed. The state machine is always bound by zero and the stop value. Once it has reached one of these bounds, it remains there. When the state machine value is equal to the stop value, changing the step size from a positive number to a negative number allows the state machine to be decremented back to zero.

The offset value is a 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF.

The pointer value is equal to the state machine value plus the offset value. Use Register 0x288 to read back the current value of the pointer.

Both the state machine value and the pointer value are bound by zero and the stop value. If the state machine is left at a particular value and the stop value or offset value is changed, then the pointer may update provided it is within these bounds. The minimum pointer value is bound by the offset value or zero, which ever is greater.

Refer to Table 19 for the applicable registers and example state machine behavior. The sequences shown in Table 19 continue do not continue indefinitely for each rising edge on ADD_G5. The state machine must be reset, the step size changed, or the stop value changed to allow additional sequencing after it has reached the end of a sequence.

Table 19. Gain State Machine Example Behavior

Example	Step[1]	Offset[2]	Stop[3]	State Machine Sequence
1	1	0	6	0, 1, 2, 3, 4, 5, 6
2	2	0	6	0, 2, 4, 6
3	4	0	6	0, 4, 6
4	6	0	6	0, 6
5	1	1	6	1, 2, 3, 4, 5, 6
6	2	1	6	1, 3, 5, 6
7	3	1	6	1, 4, 6
8	-1	0	6	6, 5, 4, 3, 2, 1, 0

[1] The step size is determined by Register 0x283, Bits[7:0].

[2] The offset is determined by Register 0x284, Bits[7:0].

[3] The stop is determined by Register 0x289, Bits[6:0].

THEORY OF OPERATION

GENERAL-PURPOSE OUTPUTS

The ADMV1455 includes 11 genera- purpose outputs that can be used to set logic levels of other components within a system, such as standalone tunable filters or standalone DSAs. These outputs support 1.8V logic levels and can be defined by either the SPI or by the LUTs.

Before using any of the general-purpose outputs, it is necessary to set the output enable bit to 1 for that output by using Register 0x780 and Register 0x781. The output state, logic high or logic low, is then determined by the values programmed into Register 0x603 and Register 0x805. Refer to Table 20 table for more details.

Table 20. GPO Registers

	Output Enable		Output State	
Output	Register	Bit	Register	Bit
GPO_F0	0x780	0	0x805	0
GPO_F1	0x780	1	0x805	1
GPO_F2	0x780	2	0x805	2
GPO_F3	0x780	3	0x805	3
GPO_F4	0x780	4	0x805	4
GPO_F5	0x780	5	0x805	5
GPO_G0	0x780	6	0x603	0
GPO_G1	0x780	7	0x603	1
GPO_G2	0x781	0	0x603	2
GPO_G3	0x781	1	0x603	3
GPO_G4	0x781	2	0x603	4

RF CONNECTIONS

The RF connections of the ADMV1455 are considered DC-coupled. If a DC voltage is present on the connections from other components within the system, it is recommended to place DC blocking capacitors in series with these pins. The DC blocking capacitors must be selected based on the operating frequency of the filter. Generally, a value greater than 100pF is sufficient to minimize insertion loss at the lower frequencies of operation. At higher frequencies of operation, it may be necessary to consider the parasitic elements of the selected capacitor. Figure 173 shows a general model of a capacitor with the parasitic elements. The parasitic series inductance (L_{ESL}) is typically of most concern given that its impedance can become dominant at frequencies of more than 10GHz. The other parasitic elements, including the leakage resistance (R_L), dielectric absorption resistance (R_{DA}), dielectric absorption capacitance (C_{DA}), and electrical series resistance (R_{ESR}) are less critical elements for consideration but are shown here for completeness.

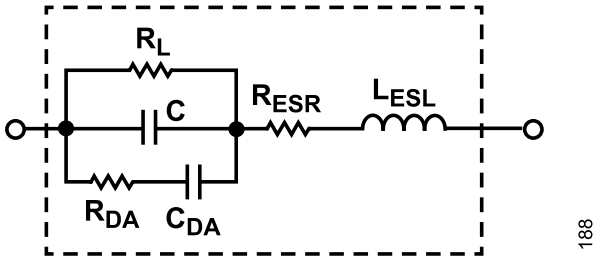

Figure 173. General Model of a Capacitor

LO SIGNAL CHAIN

The LO signal chain of the ADMV1455 accepts an input signal from the LO ball. The LO input signal is buffered with an amplifier, doubled using a 2× multiplier, before being fed into tunable filters, a wideband 90° hybrid, and two adjustable phase shifters. Figure 174 shows the LO signal chain. The LO signal chain is specified to operate with input frequencies from 8.85GHz to 27.5GHz.

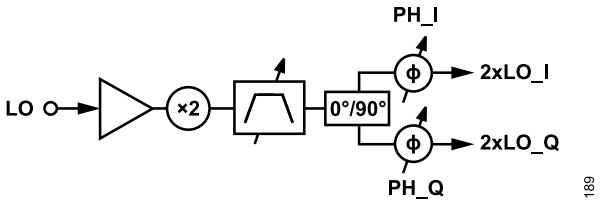

Figure 174. LO Chain Diagram

For input frequencies less than 25GHz, the specified input power levels are from −7dBm to −3dBm. Functional, but degraded performance, is possible with input power levels from −10dBm to −7dBm and from −3dBm to 0dBm.

For input frequencies greater than or equal to 25GHz, the specified input levels are from −3dBm to 0dBm. Functional, but degraded performance, is possible with input power levels from −10dBm to −3dBm.

Minimize the harmonic content of the LO input signal to prevent unwanted spurious mixer products. It is recommended to keep all LO input harmonic signals −40dBc less than the fundamental LO signal.

To help reduce spurious mixer products, the LO tunable filters are used to optimize any LO harmonic content that may be present after the 2× multiplier. Refer to the LO Tunable Filters section for more recommendations on setting these tunable filters.

The wideband 90° hybrid and adjustable phase shifters generate the necessary mixer LO signals, 2×LO_I and 2×LO_Q. The mixer LO signals operate from 17.7GHz to 55GHz. The adjustable phase shifters allow for trimming the quadrature phase of the mixer LO signals, which can be used in conjunction with the fine adjust attenuators, DSAI and DSAQ, to optimize the image rejection capability of the ADMV1455. Refer to Image Rejection Optimization section for more information on how to perform this optimization.

THEORY OF OPERATION

LO TUNABLE FILTERS

The LO tunable filters are set using Register 0x800, Register 0x801, Register 0x802, Register 0x803, Register 0x804, and Register 0x80C. See Table 21 for guidance on setting these filters based upon the LO input frequency.

For wideband applications, where the LO input frequency is continuously changing, it can be beneficial to set the LO tunable filters for wideband operation. Setting the filters to wideband operation allows the mixer to be driven with healthy input power level, at the expense of spurious mixer products. See Table 22 for guidance on setting these filters based upon the wideband LO input frequencies.

Table 21. LO Tunable Filter Narrow-Band Recommended Settings

LO Frequency		1×LO	3×LO	4×LO	LO Trap		LO Band	LO Doubler
Minimum	Maximum	Register 0x800, Bits[4:0]	Register 0x801, Bits[4:0]	Register 0x802, Bits[3:0]	Register 0x803, Bits[7:0]	Register 0x804, Bits[1:0]	Register 0x80A, Bit 5	Register 0x80C, Bits[7:0]
8.85	9.99	0x1F	0x1C	0x08	0x18	0x03	0x00	0x1F
10	11.99	0x1F	0x1C	0x00	0x18	0x03	0x00	0x1D
12	12.49	0x0A	0x07	0x00	0xAA	0x03	0x00	0x04
12.5	12.99	0x0A	0x07	0x00	0xAA	0x03	0x00	0x04
13	13.99	0x0A	0x07	0x00	0xAA	0x03	0x01	0x04
14	14.49	0x0A	0x07	0x05	0xAA	0x03	0x01	0x08
14.5	14.99	0x0A	0x07	0x05	0xA3	0x01	0x01	0x08
15	16.99	0x05	0x05	0x05	0xA3	0x01	0x01	0x08
17	17.99	0x01	0x04	0x05	0xA3	0x01	0x01	0x08
18	18.49	0x01	0x04	0x07	0xA3	0x01	0x01	0x80
18.5	18.99	0x01	0x04	0x07	0xA7	0x01	0x01	0x80
19	20.99	0x01	0x03	0x07	0xA7	0x01	0x01	0x80
21	23.99	0x00	0x02	0x07	0xE7	0x01	0x01	0x80
24	27.5	0x00	0x00	0x07	0xE7	0x01	0x01	0xC0

Table 22. LO Tunable Filter Wideband Recommended Settings

LO Frequency		1×LO	3×LO	4×LO	LO Trap		LO Band	LO Doubler
Minimum	Maximum	Register 0x800, Bits[4:0]	Register 0x801, Bits[4:0]	Register 0x802, Bits[3:0]	Register 0x803, Bits[7:0]	Register 0x804, Bits[1:0]	Register 0x80A, Bit 5	Register 0x80C, Bits[7:0]
8.85	12.99	0x1F	0x00	0x05	0x18	0x03	0x00	0x08
13	27.5	0x1F	0x00	0x05	0xA7	0x01	0x01	0x80

THEORY OF OPERATION

DSA1

The ADMV1455 includes a wideband, standalone, digital step attenuator, DSA1. This attenuator is intended for use in systems where more dynamic range control is required at the expense of the system noise figure. The device includes 15dB of attenuation control, with steps of 1dB. The attenuation is proportional to the value programmed.

When using the bypass registers (Register 0x28A set to 1), use Register 0x28B, Bits[3:0] to set the DSA1 state. When not using the bypass registers (Register 0x28A set to 0), use Register 0x600, Bits[3:0] to set the DSA1 state.

To use DSA1, the output of the previous stage in a system line up must be connected to DSA_IN and, then, DSA_OUT must be connected to RF_IN through a short PCB trace. If DSA1 is not used, both DSA_IN and DSA_OUT can be left floating.

RF SIGNAL CHAINS

The RF_IN ball of the ADMV1455 is connected directly to a LNA, followed by two switch selectable, wideband, RF signal chains. The low band, RF signal chain operates from 17.7GHz to 34GHz, and the high band, RF signal chain operates from 30GHz to 55GHz. Each signal chain includes multiple DSAs and tunable filters. Figure 175 shows the RF signal chains. Note that the RF signal chains output (RF_C) is fed into the I/Q mixer.

To select the low band, RF signal chain, set Register 0x800, Bit 7, to 0 and set Register 0x801, Bits [6:5] both to 0. To select the high band, RF signal chain, set Register 0x800, Bit 7, to 1 and set Register 0x801, Bits[6:5] both to 1.

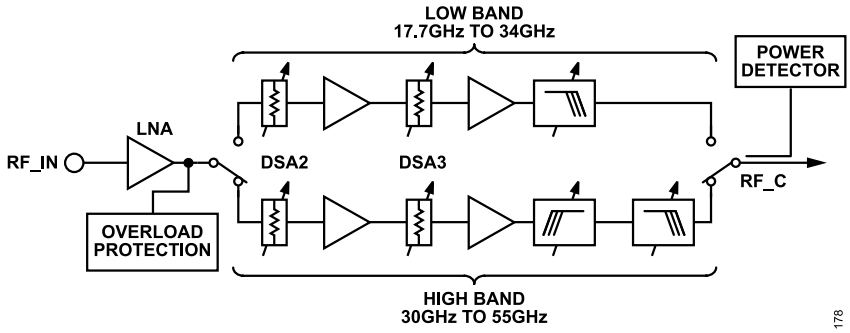

Figure 175. RF Signal Chain Diagram

THEORY OF OPERATION

DSA2

The DSA directly after the LNA in the RF signal chains is DSA2. This attenuator offers two states, 0dB and 6dB. When using the bypass registers (Register 0x28A set to 1), use Register 0x28B, Bit 4, to set the DSA2 state. When not using the bypass registers (Register 0x28A set to 0), use Register 0x600, Bit 4, to set the DSA2 state. Set Bit 4 to 0 for the 0dB state and 1 for the 6dB state.

DSA3

The DSA directly after DSA2 in the RF signal chains is DSA3. This attenuator offers 16 states, 0dB to 15dB, with steps of 1dB. The attenuation is proportional to the value programmed. When using the bypass registers (Register 0x28A set to 1), use Register 0x28C, Bits[3:0] to set the DSA3 state. When not using the bypass registers (Register 0x28A set to 0), use Register 0x601, Bits[3:0] to set the DSA3 state.

RF TUNABLE LPFS

Both the low band and the high band RF signal chains contain a tunable LPF to help reject image frequencies. Each tunable LPF contains 4 bits, or 16 states, that control the cutoff frequency. The cutoff frequency is inversely proportional to the LPF value programmed.

When using the bypass register (Register 0x2A0), set Bit 4 to 1, and then program the intended LPF value into Bits[3:0]. When not using the bypass register (Register 0x2A0), set Bit 4 to 0, then use Register 0x802, Bits[7:4], or the frequency LUT.

When using either Register 0x802 or the frequency LUT, the low band tunable LPF has three control bits (0 to 7), and the value programmed is multiplied by 2 (shift left by one position). For example, when Register 0x802, Bits[7:4] are set to 7, the effective LPF value is 14.

When using either Register 0x802 or the frequency LUT, the high band tunable LPF retains the full 4 control bits.

RF TUNABLE HPF

The high band RF signal chains contain a tunable HPF to help reject image frequencies. The tunable HPF contains 6 bits, or 64 states, that control the cutoff frequency. The cutoff frequency is inversely proportional to the HPF value programmed.

When using the bypass register (Register 0x2A1), set Bit 7 to 1, and then program the intended HPF value into Bits[5:0]. When not using the bypass register (Register 0x2A1), set Bit 7 to 0, then use Register 0x804, Bits[7:4], or the frequency LUT.

When using either Register 0x804 or the frequency LUT, the tunable HPF has four control bits, and the value programmed is multiplied by 4 (shift left by two positions). For example, when Register 0x804, Bits[7:4] are set to 15, the effective LPF value is 60.

THEORY OF OPERATION

MIXER OVERVIEW

The ADMV1455 contains an image rejection down converting I/Q mixer with excellent linearity and noise figure. The necessary LO signals, 2×LO_I and 2×LO_Q, to drive the mixer come from the LO signal chain. The output from the RF signal chains, RF_C, also feeds into the mixer. The mixer supports RF and LO input frequencies up to 55GHz. The quadrature outputs of the mixer, IF_I and IF_Q, are then used to drive the IF signal chain and I/Q baseband signal chain. Figure 176 shows the mixer.

The mixer contains a gate selection bit field in Register 0x17D. For I/Q baseband mode, set this register to 0, and for IF mode, set this register to 1.

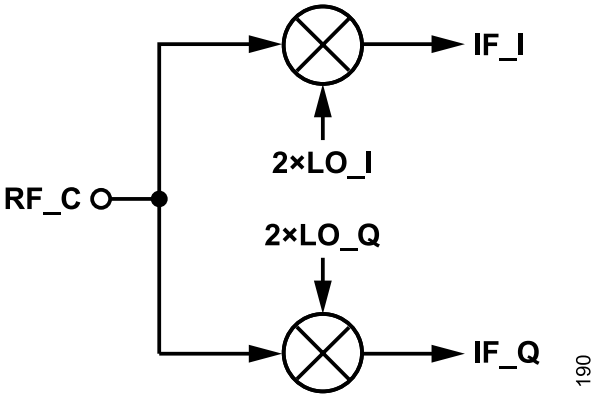

Figure 176. Mixer Diagram

MIXER SIDEBAND SELECTION

The ADMV1455 mixer sideband can be selected by swapping the mixer LO inputs, 2×LO_I and 2×LO_Q. To swap these inputs, use Register 0x801, Bit 7. Set this bit to 0 for the upper sideband, which is for cases where the RF frequency > the 2×LO frequency. Set this bit to 1 for the lower sideband, which is for cases where the RF frequency < the 2×LO frequency.

I/Q BASEBAND SIGNAL CHAINS

The I/Q baseband signal chains of the ADMV1455 support frequencies from DC to 8GHz and consist of baseband amplifiers. The baseband amplifiers include V_{OCM} adjustment and DC offset corrections. Figure 177 shows the I/Q baseband signal chains.

To use the I/Q baseband signal chains, set Register 0x184 to 0. Set Register 0x107, Bits[3:0] to 0 to power up the baseband amplifiers. If not using the I/Q baseband signal chains, set Register 0x107, Bits[3:0], to 1 to power down the baseband amplifiers.

The I/Q baseband outputs are internally DC-coupled with a 75Ω differential output impedance, which allows the outputs to interface with either 50Ω or 100Ω differential load impedance. When these outputs are not used, they can be left floating.

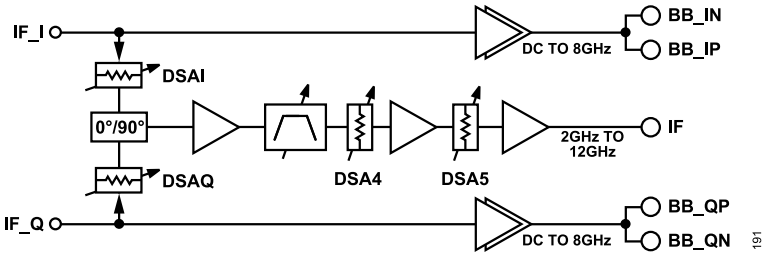

Figure 177. IF and I/Q Baseband Signal Chains

THEORY OF OPERATION

I/Q BASEBAND GAIN SELECTION

The baseband amplifiers include two gain selection bits from Register 0x194. Select the high gain setting for 50Ω differential load impedance operating from DC to 8GHz, and select the low gain setting for 100Ω differential load impedance operating from DC to 4GHz. For high gain selection, set the register to 3, and for low gain selection, set the register to 0. The delta gain between the two states is typically 6dB.

I/Q BASEBAND COMMON-MODE VOLTAGE (V_{OCM})

The are two ways to set the I/Q baseband output V_{OCM}, one is through an internally generated voltage that is adjustable via the SPI, and the other is through the CM_REF input. The acceptable V_{OCM} range is from 0.8V to 1.1V when the VDD_BB is 1.8V, and this range can be extended to 1.5V when the VDD_BB voltage is 2.5V.

Set Register 0x18A, Bit 0, to 1 to use the internally generated V_{OCM} and set it to 0 when applying an external voltage to the CM_REF ball. Ensure to include a shunt 0.01µF capacitor between the CM_REF ball and ground when applying the external voltage.

When using the internally generated V_{OCM} to adjust the voltage on the BB_IP and BB_IN balls, use Register 0x15C, Bits[4:0]. For adjusting the voltage of the BB_QP and BB_QN balls, use Register 0x165, Bits[4:0]. Figure 165 shows the typical V_{OCM} vs. the V_{OCM} settings. Regardless of the VDD_BB supply setting, 1.8V or 2.5V, the initial linear slope in the plot remains the same (for register settings less than 14).

I/Q BASEBAND DC OFFSETS

Offset DC voltages can be introduced to each I/Q baseband output. The offsets are controlled by eight registers, Register 0x18C to Register 0x193. Each register has a bitfield that is 6-bits wide, with approximately a 1.45mV step size, a 92mV range, and is across 64 states.

The eight registers are grouped into pairs, with the first register in a pair setting the offset value and direction (positive or negative) applied to the positive output ball, and then the second register in a pair setting the opposite offset value and direction to the negative output ball. Within a pair, the second register value must be set to 63 minus the value programmed into the first register.

The register pairs help maintain an average common-mode voltage between BB_IP and BB_IN, as well as between BB_QP and BB_QN. For example, Register 0x18C introduces a positive offset to the BB_IP ball, and Register 0x18D introduces a negative offset to the BB_IN ball.

Only use a single register pair for BB_IP and BB_IN at a time. Similarly, only use a single register pair for BB_QP and BB_QN at a time. The unused register pairs must retain their default register values. Refer to Table 23 for details on the registers, the corresponding output ball, as well as the offset direction.

Table 23. I/Q Baseband DC Offset Register Pairs

Pair	Register	Bits	Output	Offset Direction	Value
1	0x18C	[5:0]	BB_IP	Positive	User determined
	0x18D	[5:0]	BB_IN	Negative	63, Register 0x18C, Bits[5:0]
2	0x18E	[5:0]	BB_IP	Negative	User determined
	0x18F	[5:0]	BB_IN	Positive	63, Register 0x18E, Bits[5:0]
3	0x190	[5:0]	BB_QP	Positive	User determined
	0x191	[5:0]	BB_QN	Negative	63, Register 0x190, Bits[5:0]
4	0x192	[5:0]	BB_QP	Negative	User determined
	0x193	[5:0]	BB_QN	Positive	63, Register 0x192, Bits[5:0]

IF SIGNAL CHAIN

The IF signal of the ADMV1455 supports frequencies from 2GHz to 12GHz and consists of a 90° hybrid with fine adjust attenuators, a tunable BPF with 4GHz of bandwidth, and two 15dB DSAs. The IF_I and IF_Q quadrature outputs from the mixer feed into two fine adjust attenuators that are then fed into the 90° hybrid. The single-ended 90° hybrid output then drives the IF BPF, which subsequently drives the DSAs. See Figure 177 for the IF signal chain.

To use the IF signal chain, set Register 0x184 to 1. Power down the baseband amplifiers by setting Register 0x107, Bits[3:0] to 1.

The IF signal chain output is internally DC-coupled with a 50Ω single-ended impedance. When the IF signal chain is not used, the IF ball can be left floating.

THEORY OF OPERATION

IMAGE REJECTION OPTIMIZATION

The image rejection capability of a mixer is defined as the ability to have no gain, or a rejected output signal, for a given RF input frequency that would otherwise provide the same IF output frequency. For example, if the intended RF input frequency is 30GHz, the 2×LO_I and 2×LO_Q mixer LO frequencies are 28GHz, and the desired IF output frequency is 2GHz, then the RF input image frequency is 26GHz.

Imperfections in the quadrature phase imbalance of the mixer LO signals (ideal 90°), imperfections in the mixer output amplitude imbalance (ideal 0dB), as well as the imbalance characteristics of the IF hybrid output may cause an IF output signal to be present when applying this RF image frequency. To overcome these imperfections and help optimize the image rejection capability of the ADMV1455, the phase of the mixer LO signals and amplitudes of the mixer outputs can be adjusted.

The adjustable phase shifters, PH_I and PH_Q, in LO signal chain allow correcting of the quadrature phase imbalance between the 2×LO_I and 2×LO_Q signals. Each phase shifter has a typical 0.6° step size, 20° of range, across 32 states. Use Register 0x80A, Bits[4:0] to adjust the phase of 2×LO_I, and use Register 0x809, Bits[4:0] to adjust the phase of 2×LO_Q.

The IF_I and IF_Q signals from the mixer feed into fine adjust attenuators, DSAI and DSAQ. These attenuators allow for small 0.1dB steps and 1.5dB of total amplitude control for these signals to optimize the image rejection capability of the ADMV1455. Use Register 0x80B to adjust these attenuators. Bits[3:0] set DSAI and Bits[7:4] set DSAQ.

When applying an RF image frequency and observing the IF output power level, there are various options to perform image rejection optimization. See the Sensitivity Guided Optimization section and the Coarse and Fine Sweep Optimization section for two possible options.

Sensitivity Guided Optimization

The first option for performing image rejection optimization uses sensitivity analysis to assist in making decisions to narrow the scope of possible optimization values. To perform this optimization, apply an RF image frequency and take the following steps while measuring the IF output power:

1. Set both PH_I and PH_Q to 15.
2. Set both DSAI and DSAQ to 0.
3. Step through the DSAI values starting from 0. Stop sweeping when a local minima for the IF output power has been achieved and retain the DSAI value that provides the local minima.
4. Repeat Step 3 for DSAQ.
5. Set PH_I to 14 and then 16 to determine the optimum direction to step through. If PH_I = 14 provides a better result than PH_I = 16, then step through the values from 13 to 0; otherwise, step through values 17 to 31. Stop sweeping when a local minima for the IF output power has been achieved and retain the PH_I value that provides the local minima.
6. Repeat Step 5 for PH_Q.
7. With the values determined in Step 3 to Step 6 for DSAI, DSAQ, PH_I, and PH_Q, further optimization may be possible by adjusting each ±1 value.

Coarse and Fine Sweep Optimization

The second option for performing image rejection optimization uses a coarse sweep followed by a fine sweep to determine the optimization values. To perform this optimization, apply an RF image frequency and take the following steps while measuring the IF output power:

1. Set both PH_I and PH_Q to 0.
2. Set DSAQ to 0. Step through the DSAI values starting from 0 to 15. Record the IF output power for each value.
3. Set DSAI to 0. Step through the DSAQ values starting from 0 to 15. Record the IF output power for each value.
4. Pick the combination of values from Step 2 and Step 3 that provide the lowest IF output power. Note, that one fine step DSA value will be zero.
5. Perform a nested coarse sweep of PH_I and PH_Q for values 0, 4, 8, 12, 16, 20, 24, and 28. There are 64 combinations of those values for both phase shifters that are tested. Record the combination of values that provides the lowest IF output power.
6. Use the combination of values determined in Step 5 to then determine the fine sweep range by adding and subtracting 4 from each value. Perform a nested fine sweep of PH_I and PH_Q for these values. For example, if Step 5 yielded PH_I = 16 and PH_Q = 12, then the fine sweep range for PH_I is 12 to 20 and the fine sweep range for PH_Q is 8 to 16. Excluding the coarse values from the fine sweep, there are an additional 80 combinations of fine sweep values. Pick the combination of values that provides the lowest IF output power.

THEORY OF OPERATION

IF TUNABLE BPF

The IF signal chain contains a tunable BPF to help reject unwanted IF frequencies and optimize IF output power flatness. The tunable BPF has a typical bandwidth of 4GHz and includes both coarse and fine adjustabilities.

Set Register 0x2A2, Bit 4, to 1 to enable the fine adjust of the tunable BPF. The fine adjust value is then set by Register 0x2A2, Bits[3:0]. The coarse adjust is set by either Register 0x804, Bits[3:2], or the frequency LUT.

There are two additional controls that impact the IF signal chain performance, the IF resistor calibration and the IF subband. The IF resistor calibration is enabled by Register 0x188, Bit 3, and the value is determined by Bits[2:0]. The IF subband is determined by Register 0x800, Bits[6:5]. These settings must be adjusted together with the BPF coarse adjust value based upon the desired IF center frequency.

Refer to Table 24 for guidance on setting the tunable BPF based upon the desired IF center frequency. Depending upon the application requirements for gain flatness and rejection, further small changes to the BPF fine adjust value can be beneficial.

Table 24. IF Tunable BPF Recommended Settings

	Register			
Frequency	IF Resistor Calibration, Register 0x188, Bits[3:0]	IF Subband, Register 0x800, Bits[6:5]	Coarse Adjust, Register 0x804, Bits[3:2]	Fine Adjust, Register 0x2A2, Bits[4:0]
4GHz	0xC	0x3	0x3	0x1F
6GHz	0xE	0x1	0x0	0x1D
8GHz	0xE	0x0	0x0	0x12
10GHz	0xE	0x0	0x0	0x10

THEORY OF OPERATION

DSA4

The DSA directly after the IF BPF in the IF signal chains is DSA4. This attenuator offers 16 states, 0dB to 15dB, with steps of 1dB. The attenuation is proportional to the value programmed. When using the bypass registers (Register 0x28A set to 1), use Register 0x28C, Bits[7:4], to set the DSA4 state. When not using the bypass registers (Register 0x28A set to 0), use Register 0x601, Bits[7:4], to set the DSA4 state.

DSA5

The DSA directly after DSA4 in the IF signal chains is DSA5. This attenuator offers 16 states, 0dB to 15dB, with steps of 1dB. The attenuation is proportional to the value programmed. When using the bypass registers (Register 0x28A set to 1), use Register 0x28D, Bits[3:0], to set the DSA5 state. When not using the bypass registers (Register 0x28A set to 0), use Register 0x602, Bits[3:0] to set the DSA5 state.

TOTAL GAIN CONTROL

Table 25 is the typical total available gain (attenuation) control for each configuration that can be implemented with the ADMV1455.

Table 25. Typical Total Available Gain (Attenuation) for Each Configuration

Configuration		
Input	**Output**	**Available Attenuation (dB)**
LNA (RF_IN)	IF	51
	I/Q baseband	21
DSA1 (DSA_IN)	IF	66
	I/Q baseband	36

RF GAIN POLICY

The RF gain (attenuation) policy to achieve the best noise figure performance is to keep all DSAs at their maximum gain state.

When it is necessary to reduce the gain and the noise figure is prioritized, it is then best to set the attenuation in reverse order. For IF mode, start by introducing attenuation in DSA5, followed by DSA4, DSA3, DSA2, and then DSA1. For I/Q baseband mode, it start by introducing attenuation in DSA3, DSA2, and then DSA1.

To optimize input P1dB and input IP3 performance, set the attenuation in normal order. For IF mode, start by introducing attenuation in DSA1, followed by DSA2, DSA3, DSA4, and then DSA5. Note that this gain policy significantly degrades noise figure performance.

To balance input P1dB, input IP3, and noise figure, set attenuation in DSA4 and then DSA5. This gain improves P1dB and IIP3 while having minimal impact on noise figure.

AUTOMATIC ADC CONFIGURATION

The ADMV1455 includes an on-chip, automatic ADC that can continuously capture the power detector and temperature sensor values. The values can then be read back using the SPI via Register 0x040 and Register 0x041.

The ADC also contains averaging that can be configured using Register 0x055 (ADC_FILTER_TAPS). The amount of averaging is determined by 2 raised to the power of the value in Register 0x055. The recommended value is 2^7, or 128 averages. The ADC capture time is inversely proportional to the number of averages.

To set up the automatic ADC configuration, take the following steps:

1. Set Register 0x107, Bit 7 and Bit 5 to value 0, which powers up the temperature sensor and the ADC.
2. Set Register 0x178 to the value desired, DETECTOR_RES_CTRL, typically 7.
3. Set Register 0x043 to 0x00 to disable the ADC_CLK.
4. Set Register 0x051 to 0x00 to set the ADC for automatic mode.
5. Set Register 0x055 to 0x07 to set ADC_FILTER_TAPS averaging to 2^7.
6. Set Register 0x052 to 0x21 for reading of both the power detector and temperature sensor, as well as set the ADC_CLK_FREQ to 3.5MHz.
7. Set Register 0x05F to 0x00 to ensure that the digital filter is not held in reset.
8. Set Register 0x043 to 0x01 to enable the ADC_CLK.

Perform read backs of the following registers for the power detector and temperature sensor values:

1. Read Register 0x041 for the power detector value.
2. Read Register 0x040 for the temperature sensor value.

THEORY OF OPERATION

POWER DETECTOR

The ADMV1455 contains a power detector after the RF signal chains (RF_C) and before the I/Q mixer that allows for estimating of the RF input power level. The power detector output can be sampled by using the on-chip ADC, and the value can then be read back via the SPI.

The internal termination resistor on the power detector can shift the RF input power level vs. the ADC code response. Refer to Figure 96 for an example response curve.

Use Register 0x178 (DETECTOR_RES_CTRL) to set the internal termination resistor. It is recommended to maintain a value of 7 for most applications, particularly when the chip is configured for maximum gain. If there is a requirement for lower gain (more attenuation), then it may be beneficial to use a lower value for the internal termination resistor.

It is useful to perform a factory calibration, where known RF input power levels are applied to RF_IN or DSA_IN, and then the corresponding ADC codes are read back via the SPI. Create a table in the system microcontroller for storing the factory calibration values.

Follow the instructions in the Automatic ADC Configuration section for information on setting up the ADC and reading back the power detector value.

TEMPERATURE SENSOR

The ADMV1455 contains an on-chip temperature sensor that allows monitoring of the chip temperature. The temperature sensor output can be sampled using the on-chip ADC, and the value can then be read back via the SPI.

Follow the instructions in the Automatic ADC Configuration section for information on setting up the ADC and reading back the temperature sensor value.

To estimate the T_C of the ADMV1455 use the following equation:

$$T_C = -\frac{5}{6} \times ADC\_CODE + 177 \quad (3)$$

THEORY OF OPERATION

OVERLOAD PROTECTION

The ADMV1455 contains overload protection circuits connected to DSA1 and the RF input LNA that allow the chip to automatically power down when the CEN input is high and excessive RF input power is detected. The overload protection helps prevent infrequent excessive RF input power from causing catastrophic damage to the ADMV1455.

Four different overload protection modes are available. Use Register 0x108 (OVERLOAD_PROTECTION_MODE) to set the overload protection mode.

When Register 0x108 is set to 0, automatic overload protection is disabled. The two overload signals can be read back from Register 0x0A0 (RX_DSA1_OVERLOAD and RX_LNA_OVERLOAD). External appropriate action must be taken, such as powering down the chip by using the CEN input.

When Register 0x108 is set to 1, automatic overload protection is enabled for DSA1. When DSA1 experiences excessive RF input power, the RX_DSA1_OVERLOAD bit is asserted high, and many of the RF portions of the chip are powered down until the excessive RF input power is removed.

When Register 0x108 is set to 2, automatic overload protection is enabled for the RF input LNA. When the RF input LNA experiences excessive RF input power, the RX_LNA_OVERLOAD bit is asserted high, and many of the RF portions of the chip are powered down until the excessive RF input power is removed.

When Register 0x108 is set to 3, automatic overload protection is enabled for the RF input LNA with latch. When the RF input LNA experiences excessive RF input power, the RX_LNA_OVERLOAD_LATCHED bit in Register 0x0A1 is asserted high, and many of the RF portions of the chip are powered down. When the excessive RF input power is removed, the many of the RF portions of the chip continue to power down. To power up the RF portions of the chip, the RX_LNA_OVERLOAD_LATCHED bit must be cleared, which can be accomplished by setting OVERLOAD_PROTECTION_MODE to any other value. Ensure to set OVERLOAD_PROTECTION_MODE back to the desired mode after performing the clear operation.

The DSA1 threshold value is determined by Register 0x173. It is recommended to use the 0 value, which corresponds with the DSA1 overload protection input power threshold of approximately 13dBm.

The RF input LNA threshold value is determined by Register 0x172. It is recommended to use the 0 value, which corresponds with the LNA overload protection input power threshold of approximately −6dBm.

Relationship to the Absolute Maximum Rating

The overload protection is intended for infrequent instances of excessive RF input power. Continuous operation of the ADMV1455 with excessive RF input power is discouraged because it can reduce chip lifetime.

Overload protection typically triggers at −6dBm for RF_IN (LNA) and +13dBm for DSA_IN (DSA1). These levels exceed most absolute maximum ratings when CEN = high.

When using automatic overload protection for the DSA1 mode or the RF input LNA with latch mode, and excessive RF input power has triggered the overload protection circuit, the expected chip lifetime aligns with the absolute maximum ratings for CEN = low. These two modes provide the highest level of protection.

When using the automatic overload protection for the RF input LNA mode (nonlatched), and excessive RF input power has triggered the overload protection circuit, the chip lifetime is approximately 2 hours with 0dBm applied.

Before overload protection activates, chip lifetime follows the absolute maximum ratings for CEN = high. The RF input power range between these ratings and the overload threshold is unprotected, and continuous operation in this range is discouraged.

In systems that need to support a wide range of RF input power levels, it may be advantageous to implement an external automatic gain control (AGC) loop with the ADMV1455. The AGC loop could monitor the RF input power and then make adjustments to DSAs on the ADMV1455 to ensure chip lifetime is maintained.

For systems requiring prolonged excessive RF input power, or to discuss possible AGC loop options, contact Analog Devices, Inc., Technical Support for guidance.

APPLICATIONS INFORMATION

RECOMMENDED SETTINGS

For wideband operation or to begin evaluating the ADMV1455, refer to Table 26 for the recommended settings. These recommended settings can be considered the minimum requirements for configuring the ADMV1455. Additional features can be configured, and all settings can be tailored for a particular end application. Refer to the Theory of Operation for more details.

Table 26. Recommended Settings

	IF Mode		I/Q Baseband Mode		
Register	RF Low Band	RF High Band	RF Low Band	RF High Band	Notes
0x000	0x18	0x18	0x18	0x18	Enables the SDO output.
0x104	0x00	0x00	0xB6	0xB6	Configures the power downs.
0x105	0x00	0x00	0x01	0x01	Configures the power downs.
0x107	0xAF	0xAF	0xA0	0xA0	Configures the power downs.
0x108	0x03	0x03	0x03	0x03	Automatic overload protection for the RF input LNA with latch.
0x172	0x00	0x00	0x00	0x00	RF input LNA threshold.
0x173	0x00	0x00	0x00	0x00	DSA1 threshold.
0x17D	0x01	0x01	0x00	0x00	Configures mixer mode.
0x184	0x01	0x01	0x00	0x00	Configures mixer mode.
0x188	0x0E	0x0E	Don't care	Don't care	Configures the IF BPF.
0x202	0x00	0x00	0x00	0x00	Disables the filter LUT.
0x285	0x00	0x00	0x00	0x00	Disables the gain LUT.
0x2A2	0x12	0x12	0x12	0x12	Configures the IF BPF.
0x600	0x00	0x00	0x00	0x00	Configure the maximum gain.
0x601	0x00	0x00	0x00	0x00	Configures the maximum gain.
0x602	0x00	0x00	Don't care	Don't care	Configure the maximum gain.
0x800	0x1F	0x9F	0x1F	0x9F	Configures the bands and filters.
0x801	0x80	0x60	0x80	0x60	Configures the bands and filters.
0x802	0x05	0x05	0x05	0x05	Configures the filters.
0x803	0xA7	0xA7	0xA7	0xA7	Configures the filters.
0x804	0xF1	0xF1	0xF1	0xF1	Configures the filters.
0x809	0x0F	0x0F	0x0F	0x0F	Configures the LO phase.
0x80A	0x2F	0x2F	0x2F	0x2F	Configures the LO band and LO phase.
0x80C	0x80	0x80	0x80	0x80	Configures the filters.

APPLICATIONS INFORMATION

RECOMMENDED PCB LAYOUT

The ADMV1455 package type is a ball grid array that allows for a high pin count in a small footprint. The exposed balls on the underside of the package are intended to be soldered to a low thermal and electrical impedance ground plane. Typically, the PCB contains a solder mask defined land pattern for each ball to ensure proper solder containment and attachment.

Care must be taken with the RF trace routing escape plan for a particular implementation. In order of precedence, it is recommended to prioritize the RF traces, followed by the power supply pins, and then the digital logic connections.

The RF connections into and out of the ADMV1455 are near the edge of the package to ease the escape plan. Inner layer trace stripline routing is encouraged, particularly for applications where RF isolation performance metrics are important. Regardless of the type of RF traces employed in a PCB design, it is generally recommended to have via stitching run parallel to either side of the RF traces. The via stitching can be either through-board type vias or blind layer-to-layer vias.

Ideally, the ground connection balls are connected to the through-board type vias to maximum the heat transfer from the package to the PCB thermal plane. Refer to the Thermal Resistance section for more information on ADMV1455 thermal performance metrics.

The ADMV1455 evaluation board utilizes the recommendations listed within this section, and this section is a good starting point for many applications. Refer to the ADMV1455-EVALZ user guide for more information regarding the evaluation board.

EVALUATION BOARD INFORMATION

See the ADMV1455-EVALZ evaluation board web page for additional information on the evaluation board for the ADMV1455.

REGISTER SUMMARY

Note: The Filter LUT A Index 1 to filter LUT B Index 31 bit fields functionality (Register 0x90D to Register 0xC3F) is identical to filter LUT A Index 0 bit fields functionality (Register 0x900 and Register 0x90C). The Gain LUT Index 1 to gain LUT Index 66 bit fields functionality (Register 0xE04 to Register 0xF0B) is identical to gain LUT_0 bit fields functionality (Register 0xE00 and Register 0xE03).

Table 27. ADMV1455 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x000	REG0000	[7:0]	SOFT_RESET_R	LSB_FIRST_R	ADDR_ASCN_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDR_ASCN	LSB_FIRST	SOFT_RESET	0x00	R/W
0x004	REG0004	[7:0]	PRODUCT_ID[7:0]								0x66	R
0x005	REG0005	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x00A	REG000A	[7:0]	SCRATCH_PAD								0x00	R/W
0x040	REG0040	[7:0]	ADC_TEMP_SENSOR_READBACK								0x00	R
0x041	REG0041	[7:0]	ADC_DETECTOR_READBACK								0x00	R
0x043	REG0043	[7:0]	RESERVED							ADC_CLK_EN	0x00	R/W
0x051	REG0051	[7:0]	MANUAL_ADC_MODE_EN	MANUAL_ADC_EN	RESERVED	MANUAL_ADC_MUX_SEL					0x00	R/W
0x052	REG0052	[7:0]	RESERVED		DETECTOR_SAMPLING_TRIG	DIGITAL_FILTER_RESET	ADC_RESET	RESERVED	ADC_CLK_FREQ		0x00	R/W
0x053	REG0053	[7:0]	ADC_OUT								0x00	R
0x054	REG0054	[7:0]	RESERVED							ADC_EOC	0x01	R
0x055	REG0055	[7:0]	RESERVED				ADC_FILTER_TAPS				0x00	R/W
0x05F	REG005F	[7:0]	RESERVED							HARD_RESET_DIGITAL_FILTER	0x00	R/W
0x078	REG0078	[7:0]	RESERVED			NVM_OSC_CFG					0x09	R/W
0x07B	REG007B	[7:0]	NVM_READ_ADDRESS								0x00	R/W
0x07C	REG007C	[7:0]	NVM_READ_DATA[7:0]								0x00	R
0x07D	REG007D	[7:0]	NVM_READ_DATA[15:8]								0x00	R
0x07E	REG007E	[7:0]	NVM_REFRESH								0x68	R/W
0x0A0	REG00A0	[7:0]	RESERVED						RX_LNA_OVERLOAD	RX_DSA1_OVERLOAD	0x00	R
0x0A1	REG00A1	[7:0]	RESERVED							RX_LNA_OVERLOAD_LATCHED	0x00	R
0x101	REG0101	[7:0]	RESERVED					RF_DSA_OVERLOAD_PD	RESERVED		0x00	R/W
0x102	REG0102	[7:0]	RESERVED		RF_LNA_OVERLOAD_PD	RESERVED					0x00	R/W
0x104	REG0104	[7:0]	IF_AMP3_BIAS_PD	RESERVED	IF_AMP2_PD	IF_AMP2_BIAS_PD	RESERVED	IF_AMP1_PD	IF_AMP1_BIAS_PD	RESERVED	0x00	R/W
0x105	REG0105	[7:0]	RESERVED							IF_AMP3_PD	0x00	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x107	REG0107	[7:0]	TEMP_ SENSOR_ PD	RE- SERVED	ADC_PD	RE- SERVED	BB_Q_ AMP_PD	BB_Q_ AMP_ BIAS_PD	BB_I_ AMP_PD	BB_I_ AMP_ BIAS_PD	0x0F	R/W
0x108	REG0108	[7:0]	RESERVED						OVERLOAD_ PROTECTION_ MODE		0x00	R/W
0x15C	REG015C	[7:0]	RESERVED			BB_I_VOCM					0x05	R/W
0x165	REG0165	[7:0]	RESERVED			BB_Q_VOCM					0x05	R/W
0x172	REG0172	[7:0]	RESERVED			LNA_OVERLOAD_THRESHOLD					0x0F	R/W
0x173	REG0173	[7:0]	RESERVED			DSA1_OVERLOAD_THRESHOLD					0x0F	R/W
0x178	REG0178	[7:0]	RESERVED					DETECTOR_RES_CTRL			0x07	R/W
0x17D	REG017D	[7:0]	RESERVED							MIXER_ GATE_ SELECT	0x01	R/W
0x184	REG0184	[7:0]	RESERVED							IF_BB_ SWITCH_ CTRL	0x01	R/W
0x188	REG0188	[7:0]	RESERVED				IF_RES_ CAL_ BYPASS_ EN	IF_RES_CAL			0x04	R/W
0x18A	REG018A	[7:0]	RESERVED							BB_ VOCM_ SEL	0x01	R/W
0x18C	REG018C	[7:0]	RESERVED		BB_IP_OFFSET_POS						0x00	R/W
0x18D	REG018D	[7:0]	RESERVED		BB_IN_OFFSET_NEG						0x3F	R/W
0x18E	REG018E	[7:0]	RESERVED		BB_IP_OFFSET_NEG						0x00	R/W
0x18F	REG018F	[7:0]	RESERVED		BB_IN_OFFSET_POS						0x3F	R/W
0x190	REG0190	[7:0]	RESERVED		BB_QP_OFFSET_POS						0x00	R/W
0x191	REG0191	[7:0]	RESERVED		BB_QN_OFFSET_NEG						0x3F	R/W
0x192	REG0192	[7:0]	RESERVED		BB_QP_OFFSET_NEG						0x00	R/W
0x193	REG0193	[7:0]	RESERVED		BB_QN_OFFSET_POS						0x3F	R/W
0x194	REG0194	[7:0]	RESERVED						BB_Q_ GAIN_SEL	BB_I_ GAIN_SEL	0x03	R/W
0x200	REG0200	[7:0]	FILTER_SM_STEP								0x01	R/W
0x202	REG0202	[7:0]	RESERVED							FILTER_ LUT_EN	0x01	R/W
0x203	REG0203	[7:0]	RESERVED						FILTER_LUT_MODE		0x00	R/W
0x204	REG0204	[7:0]	RESERVED							FILTER_ SM_ RESET	0x01	R/W
0x205	REG0205	[7:0]	FILTER_SM_POINTER								0x00	R
0x206	REG0206	[7:0]	RESERVED		FILTER_SM_STOP						0x1F	R/W
0x207	REG0207	[7:0]	RESERVED							FILTER_ LUT_ SELECT	0x00	R/W
0x208	REG0208	[7:0]	RESERVED							FILTER_ LOAD_ EN	0x00	R/W
0x209	REG0209	[7:0]	RESERVED		FILTER_SPI_POINTER						0x00	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x20A	REG020A	[7:0]	RESERVED		FILTER_SM_WRAP	FILTER_SM_START					0x00	R/W
0x210	REG0210	[7:0]	RESERVED			FILTER_ADD_F_READBACK					0x00	R
0x211	REG0211	[7:0]	FILTER_LUT_OUTPUT[7:0]								0x00	R
0x212	REG0212	[7:0]	FILTER_LUT_OUTPUT[15:8]								0x00	R
0x213	REG0213	[7:0]	FILTER_LUT_OUTPUT[23:16]								0x00	R
0x214	REG0214	[7:0]	FILTER_LUT_OUTPUT[31:24]								0x00	R
0x215	REG0215	[7:0]	FILTER_LUT_OUTPUT[39:32]								0x00	R
0x216	REG0216	[7:0]	FILTER_LUT_OUTPUT[47:40]								0x00	R
0x217	REG0217	[7:0]	FILTER_LUT_OUTPUT[55:48]								0x00	R
0x218	REG0218	[7:0]	FILTER_LUT_OUTPUT[63:56]								0x00	R
0x219	REG0219	[7:0]	FILTER_LUT_OUTPUT[71:64]								0x00	R
0x21A	REG021A	[7:0]	FILTER_LUT_OUTPUT[79:72]								0x00	R
0x21B	REG021B	[7:0]	FILTER_LUT_OUTPUT[87:80]								0x00	R
0x21C	REG021C	[7:0]	FILTER_LUT_OUTPUT[95:88]								0x00	R
0x21D	REG021D	[7:0]	FILTER_LUT_OUTPUT[103:96]								0x00	R
0x220	REG0220	[7:0]	FILTER_READBACK[7:0]								0x00	R
0x221	REG0221	[7:0]	FILTER_READBACK[15:8]								0x00	R
0x222	REG0222	[7:0]	FILTER_READBACK[23:16]								0x00	R
0x223	REG0223	[7:0]	FILTER_READBACK[31:24]								0x00	R
0x224	REG0224	[7:0]	FILTER_READBACK[39:32]								0x00	R
0x225	REG0225	[7:0]	FILTER_READBACK[47:40]								0x00	R
0x226	REG0226	[7:0]	FILTER_READBACK[55:48]								0x00	R
0x227	REG0227	[7:0]	FILTER_READBACK[63:56]								0x00	R
0x228	REG0228	[7:0]	FILTER_READBACK[71:64]								0x00	R
0x229	REG0229	[7:0]	FILTER_READBACK[79:72]								0x00	R
0x22A	REG022A	[7:0]	FILTER_READBACK[87:80]								0x00	R
0x22B	REG022B	[7:0]	FILTER_READBACK[95:88]								0x00	R
0x22C	REG022C	[7:0]	FILTER_READBACK[103:96]								0x00	R
0x240	REG0240	[7:0]	FILTER_LUT_POINTER								0x00	R
0x281	REG0281	[7:0]	RESERVED							GAIN_LOAD_EN	0x00	R/W
0x282	REG0282	[7:0]	RESERVED	GAIN_SPI_POINTER							0x00	R/W
0x283	REG0283	[7:0]	GAIN_SM_STEP								0x01	R/W
0x284	REG0284	[7:0]	GAIN_SM_OFFSET								0x00	R/W
0x285	REG0285	[7:0]	RESERVED							GAIN_LUT_EN	0x01	R/W
0x286	REG0286	[7:0]	RESERVED						GAIN_LUT_MODE		0x00	R/W
0x287	REG0287	[7:0]	RESERVED							GAIN_SM_RESET	0x01	R/W
0x288	REG0288	[7:0]	GAIN_SM_POINTER_PLUS_OFFSET								0x00	R
0x289	REG0289	[7:0]	RESERVED	GAIN_SM_STOP							0x42	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x28A	REG028A	[7:0]	RESERVED							GAIN_LUT_BYPASS_EN	0x00	R/W
0x28B	REG028B	[7:0]	RESERVED			DSA2_BYPASS_VALUE	DSA1_BYPASS_VALUE				0x00	R/W
0x28C	REG028C	[7:0]	DSA4_BYPASS_VALUE				DSA3_BYPASS_VALUE				0x00	R/W
0x28D	REG028D	[7:0]	RESERVED				DSA5_BYPASS_VALUE				0x00	R/W
0x28E	REG028E	[7:0]	RESERVED			GPO_G_BYPASS					0x00	R/W
0x28F	REG028F	[7:0]	RESERVED			GAIN_LUT_OUTPUT[4:0]					0x00	R
0x290	REG0290	[7:0]	GAIN_LUT_OUTPUT[12:5]								0x00	R
0x291	REG0291	[7:0]	RESERVED				GAIN_LUT_OUTPUT[16:13]				0x00	R
0x292	REG0292	[7:0]	RESERVED			GAIN_LUT_OUTPUT[21:17]					0x00	R
0x293	REG0293	[7:0]	RESERVED			GAIN_READBACK[4:0]					0x00	R
0x294	REG0294	[7:0]	GAIN_READBACK[12:5]								0x00	R
0x295	REG0295	[7:0]	RESERVED				GAIN_READBACK[16:13]				0x00	R
0x296	REG0296	[7:0]	RESERVED			GAIN_READBACK[21:17]					0x00	R
0x298	REG0298	[7:0]	GAIN_LUT_POINTER								0x00	R
0x29B	REG029B	[7:0]	GAIN_SM_POINTER_PRE_OFFSET								0x00	R
0x2A0	REG02A0	[7:0]	RESERVED			LPF_SELECT	LPF_BYPASS_VALUE				0x00	R/W
0x2A1	REG02A1	[7:0]	HPF_SELECT	RESERVED		HPF_BYPASS_VALUE					0x00	R/W
0x2A2	REG02A2	[7:0]	RESERVED			BPF_SELECT	BPF_FINE				0x00	R/W
0x2A3	REG02A3	[7:0]	RESERVED				LPF_READBACK				0x00	R
0x2A4	REG02A4	[7:0]	RESERVED			HPF_READBACK					0x00	R
0x2A5	REG02A5	[7:0]	RESERVED				BPF_READBACK				0x00	R
0x2B0	REG02B0	[7:0]	RESERVED			GAIN_ADD_G_READBACK					0x00	R
0x600	REG0600	[7:0]	RESERVED			RF_DSA2_GAIN	RF_DSA1_GAIN				0x00	R/W
0x601	REG0601	[7:0]	IF_DSA4_GAIN				RF_DSA3_GAIN				0x00	R/W
0x602	REG0602	[7:0]	RESERVED				IF_DSA5_GAIN				0x00	R/W
0x603	REG0603	[7:0]	RESERVED			GPO_G					0x00	R/W
0x780	REG0780	[7:0]	GPO_G_OE[1:0]			GPO_F_OE					0x00	R/W
0x781	REG0781	[7:0]	RESERVED						GPO_G_OE[4:2]		0x00	R/W
0x800	REG0800	[7:0]	RF_BAND_SELECT	IF_SUBBAND		LO_X1_FILTER					0x00	R/W
0x801	REG0801	[7:0]	LO_SIDEBAND	RF_SUBBAND		LO_X3_FILTER					0x80	R/W
0x802	REG0802	[7:0]	LPF_VALUE				LO_X4_FILTER				0x00	R/W
0x803	REG0803	[7:0]	LO_TRAP_FILTER[7:0]								0x00	R/W
0x804	REG0804	[7:0]	HPF_VALUE				BPF_COARSE		LO_TRAP_FILTER[9:8]		0x00	R/W
0x805	REG0805	[7:0]	RESERVED			GPO_F					0x00	R/W
0x806	REG0806	[7:0]	RESERVED		DSA2_OFFSET		DSA1_OFFSET				0x00	R/W
0x807	REG0807	[7:0]	DSA4_OFFSET				DSA3_OFFSET				0x00	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x808	REG0808	[7:0]	RESERVED				DSA5_OFFSET				0x00	R/W
0x809	REG0809	[7:0]	RESERVED			LO_PHASE_Q					0x00	R/W
0x80A	REG080A	[7:0]	RESERVED		LO_BAND	LO_PHASE_I					0x20	R/W
0x80B	REG080B	[7:0]	DSAQ_0P1DB				DSAI_0P1DB				0x00	R/W
0x80C	REG080C	[7:0]	LO_DOUBLER_BAND								0x00	R/W
0x900	REG0900	[7:0]	RF_BAND_SELECT_LUT_A_0	IF_SUBBAND_LUT_A_0		LO_X1_FILTER_LUT_A_0					0x00	R/W
0x901	REG0901	[7:0]	LO_SIDEBAND_LUT_A_0	RF_SUBBAND_LUT_A_0		LO_X3_FILTER_LUT_A_0					0x80	R/W
0x902	REG0902	[7:0]	LPF_VALUE_LUT_A_0				LO_X4_FILTER_LUT_A_0				0x00	R/W
0x903	REG0903	[7:0]	LO_TRAP_FILTER_LUT_A_0[7:0]								0x00	R/W
0x904	REG0904	[7:0]	HPF_VALUE_LUT_A_0				BPF_COARSE_LUT_A_0		LO_TRAP_FILTER_LUT_A_0[9:8]		0x00	R/W
0x905	REG0905	[7:0]	RESERVED		GPO_F_LUT_A_0						0x00	R/W
0x906	REG0906	[7:0]	RESERVED		DSA2_OFFSET_LUT_A_0		DSA1_OFFSET_LUT_A_0				0x00	R/W
0x907	REG0907	[7:0]	DSA4_OFFSET_LUT_A_0				DSA3_OFFSET_LUT_A_0				0x00	R/W
0x908	REG0908	[7:0]	RESERVED				DSA5_OFFSET_LUT_A_0				0x00	R/W
0x909	REG0909	[7:0]	RESERVED			LO_PHASE_Q_LUT_A_0					0x00	R/W
0x90A	REG090A	[7:0]	RESERVED		LO_BAND_LUT_A_0	LO_PHASE_I_LUT_A_0					0x20	R/W
0x90B	REG090B	[7:0]	DSAQ_0P1DB_LUT_A_0				DSAI_0P1DB_LUT_A_0				0x00	R/W
0x90C	REG090C	[7:0]	LO_DOUBLER_BAND_LUT_A_0								0x00	R/W
…	…	…	…								…	…
0xA93	REG0A93	[7:0]	RF_BAND_SELECT_LUT_A_31	IF_SUBBAND_LUT_A_31		LO_X1_FILTER_LUT_A_31					0x00	R/W
0xA94	REG0A94	[7:0]	LO_SIDEBAND_LUT_A_31	RF_SUBBAND_LUT_A_31		LO_X3_FILTER_LUT_A_31					0x00	R/W
0xA95	REG0A95	[7:0]	LPF_VALUE_LUT_A_31				LO_X4_FILTER_LUT_A_31				0x00	R/W
0xA96	REG0A96	[7:0]	LO_TRAP_FILTER_LUT_A_31[7:0]								0x00	R/W
0xA97	REG0A97	[7:0]	HPF_VALUE_LUT_A_31				BPF_COARSE_LUT_A_31		LO_TRAP_FILTER_LUT_A_31[9:8]		0x00	R/W
0xA98	REG0A98	[7:0]	RESERVED		GPO_F_LUT_A_31						0x00	R/W
0xA99	REG0A99	[7:0]	RESERVED		DSA2_OFFSET_LUT_A_31		DSA1_OFFSET_LUT_A_31				0x00	R/W
0xA9A	REG0A9A	[7:0]	DSA4_OFFSET_LUT_A_31				DSA3_OFFSET_LUT_A_31				0x00	R/W
0xA9B	REG0A9B	[7:0]	RESERVED				DSA5_OFFSET_LUT_A_31				0x00	R/W
0xA9C	REG0A9C	[7:0]	RESERVED			LO_PHASE_Q_LUT_A_31					0x00	R/W
0xA9D	REG0A9D	[7:0]	RESERVED		LO_BAND_LUT_A_31	LO_PHASE_I_LUT_A_31					0x00	R/W
0xA9E	REG0A9E	[7:0]	DSAQ_0P1DB_LUT_A_31				DSAI_0P1DB_LUT_A_31				0x00	R/W
0xA9F	REG0A9F	[7:0]	LO_DOUBLER_BAND_LUT_A_31								0x00	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xAA0	REG0AA0	[7:0]	RF_BAND_SELECT_LUT_B_0	IF_SUBBAND_LUT_B_0		LO_X1_FILTER_LUT_B_0					0x00	R/W
0xAA1	REG0AA1	[7:0]	LO_SIDEBAND_LUT_B_0	RF_SUBBAND_LUT_B_0		LO_X3_FILTER_LUT_B_0					0x00	R/W
0xAA2	REG0AA2	[7:0]	LPF_VALUE_LUT_B_0				LO_X4_FILTER_LUT_B_0				0x00	R/W
0xAA3	REG0AA3	[7:0]	LO_TRAP_FILTER_LUT_B_0[7:0]								0x00	R/W
0xAA4	REG0AA4	[7:0]	HPF_VALUE_LUT_B_0				BPF_COARSE_LUT_B_0		LO_TRAP_FILTER_LUT_B_0[9:8]		0x00	R/W
0xAA5	REG0AA5	[7:0]	RESERVED		GPO_F_LUT_B_0						0x00	R/W
0xAA6	REG0AA6	[7:0]	RESERVED		DSA2_OFFSET_LUT_B_0		DSA1_OFFSET_LUT_B_0				0x00	R/W
0xAA7	REG0AA7	[7:0]	DSA4_OFFSET_LUT_B_0				DSA3_OFFSET_LUT_B_0				0x00	R/W
0xAA8	REG0AA8	[7:0]	RESERVED				DSA5_OFFSET_LUT_B_0				0x00	R/W
0xAA9	REG0AA9	[7:0]	RESERVED			LO_PHASE_Q_LUT_B_0					0x00	R/W
0xAAA	REG0AAA	[7:0]	RESERVED		LO_BAND_LUT_B_0	LO_PHASE_I_LUT_B_0					0x00	R/W
0xAAB	REG0AAB	[7:0]	DSAQ_0P1DB_LUT_B_0				DSAI_0P1DB_LUT_B_0				0x00	R/W
0xAAC	REG0AAC	[7:0]	LO_DOUBLER_BAND_LUT_B_0								0x00	R/W
…	…	…	…								…	…
0xC33	REG0C33	[7:0]	RF_BAND_SELECT_LUT_B_31	IF_SUBBAND_LUT_B_31		LO_X1_FILTER_LUT_B_31					0x00	R/W
0xC34	REG0C34	[7:0]	LO_SIDEBAND_LUT_B_31	RF_SUBBAND_LUT_B_31		LO_X3_FILTER_LUT_B_31					0x00	R/W
0xC35	REG0C35	[7:0]	LPF_VALUE_LUT_B_31				LO_X4_FILTER_LUT_B_31				0x00	R/W
0xC36	REG0C36	[7:0]	LO_TRAP_FILTER_LUT_B_31[7:0]								0x00	R/W
0xC37	REG0C37	[7:0]	HPF_VALUE_LUT_B_31				BPF_COARSE_LUT_B_31		LO_TRAP_FILTER_LUT_B_31[9:8]		0x00	R/W
0xC38	REG0C38	[7:0]	RESERVED		GPO_F_LUT_B_31						0x00	R/W
0xC39	REG0C39	[7:0]	RESERVED		DSA2_OFFSET_LUT_B_31		DSA1_OFFSET_LUT_B_31				0x00	R/W
0xC3A	REG0C3A	[7:0]	DSA4_OFFSET_LUT_B_31				DSA3_OFFSET_LUT_B_31				0x00	R/W
0xC3B	REG0C3B	[7:0]	RESERVED				DSA5_OFFSET_LUT_B_31				0x00	R/W
0xC3C	REG0C3C	[7:0]	RESERVED			LO_PHASE_Q_LUT_B_31					0x00	R/W
0xC3D	REG0C3D	[7:0]	RESERVED		LO_BAND_LUT_B_31	LO_PHASE_I_LUT_B_31					0x00	R/W
0xC3E	REG0C3E	[7:0]	DSAQ_0P1DB_LUT_B_31				DSAI_0P1DB_LUT_B_31				0x00	R/W
0xC3F	REG0C3F	[7:0]	LO_DOUBLER_BAND_LUT_B_31								0x00	R/W
0xE00	REG0E00	[7:0]	RESERVED			RF_DSA2_GAIN_LUT_0	RF_DSA1_GAIN_LUT_0				0x00	R/W
0xE01	REG0E01	[7:0]	IF_DSA4_GAIN_LUT_0				RF_DSA3_GAIN_LUT_0				0x00	R/W
0xE02	REG0E02	[7:0]	RESERVED				IF_DSA5_GAIN_LUT_0				0x00	R/W

REGISTER SUMMARY

Table 27. ADMV1455 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xE03	REG0E03	[7:0]	RESERVED			GPO_G_LUT_0					0x00	R/W
…	…	…	…								…	…
0xF08	REG0F08	[7:0]	RESERVED			RF_DSA2_GAIN_LUT_66	RF_DSA1_GAIN_LUT_66				0x00	R/W
0xF09	REG0F09	[7:0]	IF_DSA4_GAIN_LUT_66				RF_DSA3_GAIN_LUT_66				0x00	R/W
0xF0A	REG0F0A	[7:0]	RESERVED				IF_DSA5_GAIN_LUT_66				0x00	R/W
0xF0B	REG0F0B	[7:0]	RESERVED			GPO_G_LUT_66					0x00	R/W

REGISTER DETAILS

REGISTER 0X000 TO REGISTER 0X0A1

Address: 0x000, Reset: 0x00, Name: REG0000

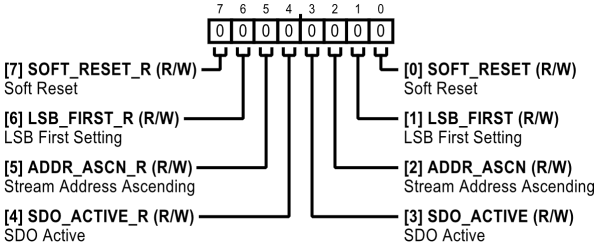

Figure 178.

Table 28. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Soft Reset. This bit field self resets to zero; no need to set to zero after initiating a reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W
6	LSB_FIRST_R	LSB First Setting. 0: MSB First. 1: LSB First.	0x0	R/W
5	ADDR_ASCN_R	Stream Address Ascending. 0: Disable. 1: Enable.	0x0	R/W
4	SDO_ACTIVE_R	SDO Active. 0: Enable 3-wire SPI. 1: Enable 4-wire SPI.	0x0	R/W
3	SDO_ACTIVE	SDO Active. 0: Enable 3-wire SPI. 1: Enable 4-wire SPI.	0x0	R/W
2	ADDR_ASCN	Stream Address Ascending. 0: Disable. 1: Enable.	0x0	R/W
1	LSB_FIRST	LSB First Setting. 0: MSB First. 1: LSB First.	0x0	R/W
0	SOFT_RESET	Soft Reset. This bit field self resets to zero; no need to set to zero after initiating a reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W

Address: 0x004, Reset: 0x66, Name: REG0004

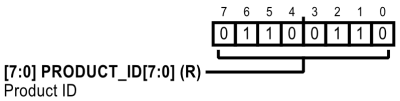

Figure 179.

Table 29. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID.	0x66	R

REGISTER DETAILS

Address: 0x005, Reset: 0x00, Name: REG0005

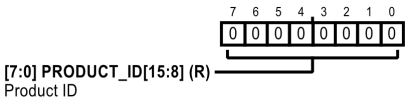

Figure 180.

Table 30. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID.	0x0	R

Address: 0x00A, Reset: 0x00, Name: REG000A

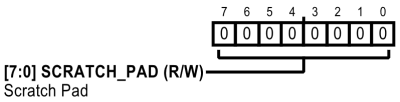

Figure 181.

Table 31. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_PAD	Scratch Pad.	0x0	R/W

Address: 0x040, Reset: 0x00, Name: REG0040

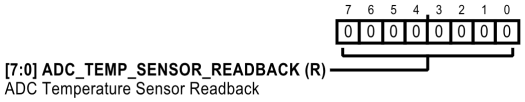

Figure 182.

Table 32. Bit Descriptions for REG0040

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_TEMP_SENSOR_READBACK	ADC Temperature Sensor Readback. Updated in automatic mode only.	0x0	R

Address: 0x041, Reset: 0x00, Name: REG0041

Figure 183.

Table 33. Bit Descriptions for REG0041

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_DETECTOR_READBACK	ADC Power Detector Readback.	0x0	R

Address: 0x043, Reset: 0x00, Name: REG0043

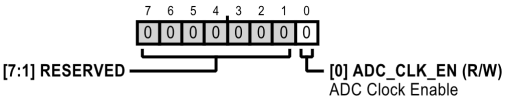

Figure 184.

REGISTER DETAILS

Table 34. Bit Descriptions for REG0043

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_CLK_EN	ADC Clock Enable. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x051, Reset: 0x00, Name: REG0051

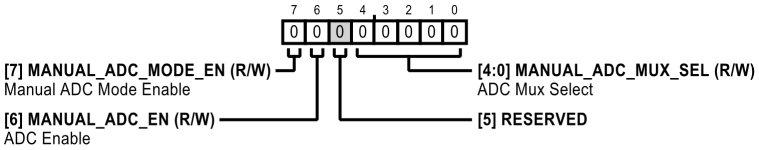

Figure 185.

Table 35. Bit Descriptions for REG0051

Bits	Bit Name	Description	Reset	Access
7	MANUAL_ADC_MODE_EN	Manual ADC Mode Enable. 0: Automatic. 1: Manual.	0x0	R/W
6	MANUAL_ADC_EN	ADC Enable. This bit is used in manual mode. In automatic mode, it is not required because the ADC is always enabled. 0: Disable. 1: Enable.	0x0	R/W
5	RESERVED	Reserved.	0x0	R/W
[4:0]	MANUAL_ADC_MUX_SEL	ADC Mux Select. 0: Read Temperature Sensor. 1: Read Power Detector.	0x0	R/W

Address: 0x052, Reset: 0x00, Name: REG0052

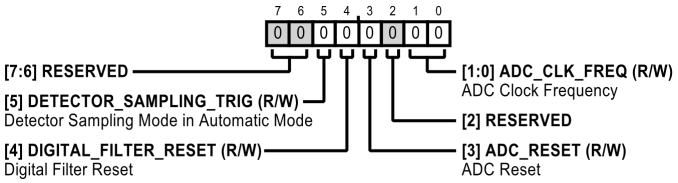

Figure 186.

Table 36. Bit Descriptions for REG0052

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	DETECTOR_SAMPLING_TRIG	Detector Sampling Mode in Automatic Mode. 0: Only the temperature reading is captured. 1: Detector and temperature readings are captured.	0x0	R/W
4	DIGITAL_FILTER_RESET	Digital Filter Reset. 0: To Disable Reset. 1: To Reset with the Next Rising Edge of DETECTOR_SAMPLING_TRIG.	0x0	R/W
3	ADC_RESET	ADC Reset.	0x0	R/W

REGISTER DETAILS

Table 36. Bit Descriptions for REG0052 (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Normal Operation. 1: Reset.		
2	RESERVED	Reserved.	0x0	R
[1:0]	ADC_CLK_FREQ	ADC Clock Frequency. 00: 7MHz. 01: 3.5MHz. 10: SPI SCLK Clock Frequency.	0x0	R/W

Address: 0x053, Reset: 0x00, Name: REG0053

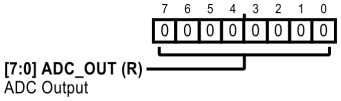

Figure 187.

Table 37. Bit Descriptions for REG0053

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_OUT	ADC Output. Power detector or temperature sensor reading in manual mode.	0x0	R

Address: 0x054, Reset: 0x01, Name: REG0054

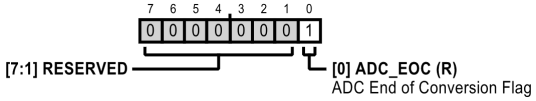

Figure 188.

Table 38. Bit Descriptions for REG0054

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	ADC_EOC	ADC End of Conversion Flag.	0x1	R

Address: 0x055, Reset: 0x00, Name: REG0055

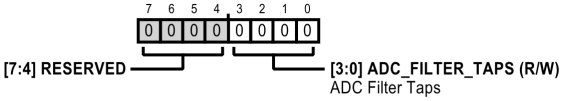

Figure 189.

Table 39. Bit Descriptions for REG0055

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	ADC_FILTER_TAPS	ADC Filter Taps. These bits defines the number of ADC filter taps. For any other bit field value besides 1 to 8, ADC averaging is zero. 0001: 2^1. 0010: 2^2. 0011: 2^3. 0100: 2^4. 0101: 2^5.	0x0	R/W

REGISTER DETAILS

Table 39. Bit Descriptions for REG0055 (Continued)

Bits	Bit Name	Description	Reset	Access
		0110: 2^6. 0111: 2^7. 1000: 2^8.		

Address: 0x05F, Reset: 0x00, Name: REG005F

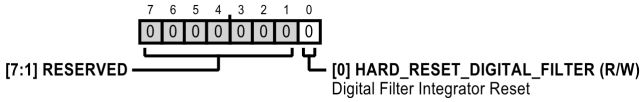

Figure 190.

Table 40. Bit Descriptions for REG005F

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	HARD_RESET_DIGITAL_FILTER	Digital Filter Integrator Reset. 0: Normal Operation. 1: Reset.	0x0	R/W

Address: 0x078, Reset: 0x09, Name: REG0078

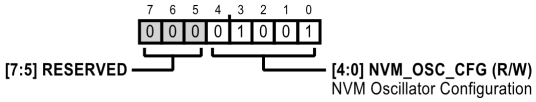

Figure 191.

Table 41. Bit Descriptions for REG0078

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	NVM_OSC_CFG	NVM Oscillator Configuration.	0x9	R/W

Address: 0x07B, Reset: 0x00, Name: REG007B

Figure 192.

Table 42. Bit Descriptions for REG007B

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_ADDRESS	NVM Read Address. This bit field defines a pointer to the NVM register address that is read back when performing a read operation of NVM_READ_DATA. Applicable NVM register addresses to read back from are 0x33 to 0x38.	0x0	R/W

Address: 0x07C, Reset: 0x00, Name: REG007C

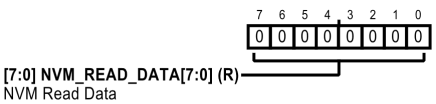

Figure 193.

REGISTER DETAILS

Table 43. Bit Descriptions for REG007C

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_DATA[7:0]	NVM Read Data. Set NVM_READ_ADDRESS to the NVM address to be read back, then perform a read operation of NVM_READ_DATA to retrieve the value.	0x0	R

Address: 0x07D, Reset: 0x00, Name: REG007D

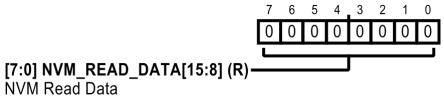

Figure 194.

Table 44. Bit Descriptions for REG007D

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_DATA[15:8]	NVM Read Data. Set NVM_READ_ADDRESS to the NVM address to be read back, then perform a read operation of NVM_READ_DATA to retrieve the value.	0x0	R

Address: 0x07E, Reset: 0x68, Name: REG007E

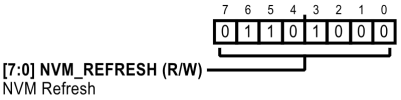

Figure 195.

Table 45. Bit Descriptions for REG007E

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_REFRESH	NVM Refresh.	0x68	R/W

Address: 0x0A0, Reset: 0x00, Name: REG00A0

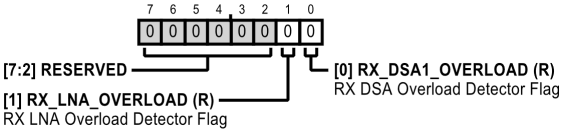

Figure 196.

Table 46. Bit Descriptions for REG00A0

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	RX_LNA_OVERLOAD	RX LNA Overload Detector Flag. 0: LNA Input Power Below Threshold Value. 1: LNA Input Power Above Threshold Value.	0x0	R
0	RX_DSA1_OVERLOAD	RX DSA Overload Detector Flag. 0: DSA1 Input Power Below Threshold Value. 1: DSA1 Input Power Above Threshold Value.	0x0	R

Address: 0x0A1, Reset: 0x00, Name: REG00A1

REGISTER DETAILS

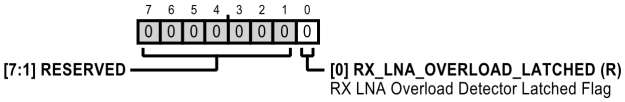

Figure 197.

Table 47. Bit Descriptions for REG00A1

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	RX_LNA_OVERLOAD_LATCHED	RX LNA Overload Detector Latched Flag. When OVERLOAD_PROTECTION_MODE is set to Mode 3 (b11) and the RF input LNA experiences excessive RF input power, the RX_LNA_OVERLOAD_LATCHED bit is asserted high and many of the RF portions of the chip are powered down. To power up the RF portions of the chip, the RX_LNA_OVERLOAD_LATCHED bit must be cleared, which can be accomplished by setting OVERLOAD_PROTECTION_MODE to any other value. Ensure to set OVERLOAD_PROTECTION_MODE back to the desired mode after performing the clear operation. 0: Normal Operation. 1: RF Input LNA Experienced Power Above Threshold Value.	0x0	R

REGISTER 0X101 TO REGISTER 0X194

Address: 0x101, Reset: 0x00, Name: REG0101

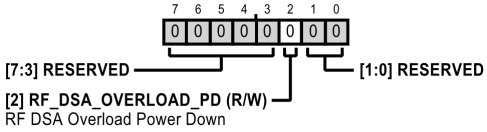

Figure 198.

Table 48. Bit Descriptions for REG0101

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	RF_DSA_OVERLOAD_PD	RF DSA Overload Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R/W

Address: 0x102, Reset: 0x00, Name: REG0102

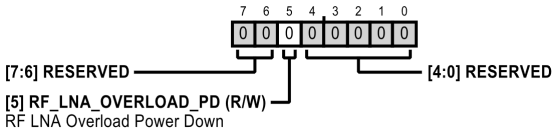

Figure 199.

Table 49. Bit Descriptions for REG0102

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	RF_LNA_OVERLOAD_PD	RF LNA Overload Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
[4:0]	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Address: 0x104, Reset: 0x00, Name: REG0104

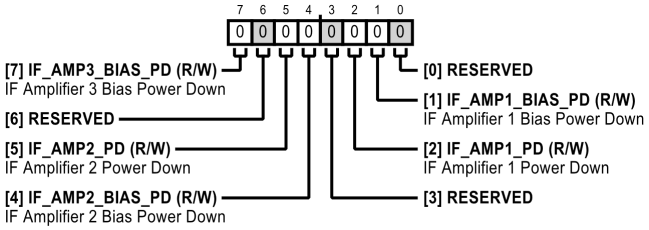

Figure 200.

Table 50. Bit Descriptions for REG0104

Bits	Bit Name	Description	Reset	Access
7	IF_AMP3_BIAS_PD	IF Amplifier 3 Bias Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	IF_AMP2_PD	IF Amplifier 2 Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
4	IF_AMP2_BIAS_PD	IF Amplifier 2 Bias Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
3	RESERVED	Reserved.	0x0	R/W
2	IF_AMP1_PD	IF Amplifier 1 Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
1	IF_AMP1_BIAS_PD	IF Amplifier 1 Bias Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

Address: 0x105, Reset: 0x00, Name: REG0105

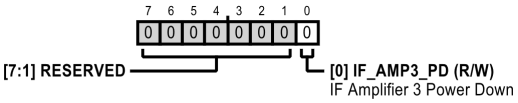

Figure 201.

Table 51. Bit Descriptions for REG0105

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	IF_AMP3_PD	IF Amplifier 3 Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W

Address: 0x107, Reset: 0x0F, Name: REG0107

REGISTER DETAILS

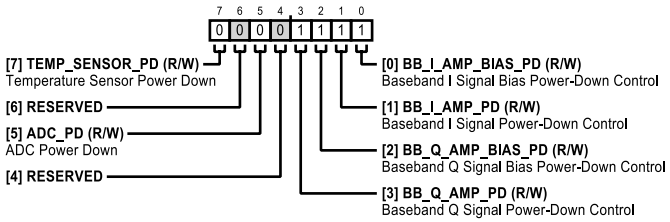

Figure 202.

Table 52. Bit Descriptions for REG0107

Bits	Bit Name	Description	Reset	Access
7	TEMP_SENSOR_PD	Temperature Sensor Power Down 0: Normal Operation. 1: Powered Down.	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
5	ADC_PD	ADC Power Down. 0: Normal Operation. 1: Powered Down.	0x0	R/W
4	RESERVED	Reserved.	0x0	R/W
3	BB_Q_AMP_PD	Baseband Q Signal Power-Down Control. 0: Normal Operation. 1: Powered Down.	0x1	R/W
2	BB_Q_AMP_BIAS_PD	Baseband Q Signal Bias Power-Down Control. 0: Normal Operation. 1: Powered Down.	0x1	R/W
1	BB_I_AMP_PD	Baseband I Signal Power-Down Control. 0: Normal Operation. 1: Powered Down.	0x1	R/W
0	BB_I_AMP_BIAS_PD	Baseband I Signal Bias Power-Down Control. 0: Normal Operation. 1: Powered Down.	0x1	R/W

Address: 0x108, Reset: 0x00, Name: REG0108

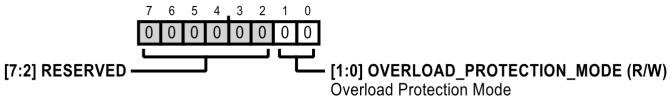

Figure 203.

Table 53. Bit Descriptions for REG0108

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	OVERLOAD_PROTECTION_MODE	Overload Protection Mode. 00: Disable automatic overload protection. The two overload signals, RX_DSA1_OVERLOAD and RX_LNA_OVERLOAD, can be read through SPI. External appropriate action must be taken, such as powering down the chip by using the CHIP_EN pin. 01: Monitor DSA1. When DSA1 experiences excessive RF input power, the RX_DSA1_OVERLOAD bit is asserted high, and many of the RF portions of the chip are powered down until the excessive RF input power is removed.	0x0	R/W

REGISTER DETAILS

Table 53. Bit Descriptions for REG0108 (Continued)

Bits	Bit Name	Description	Reset	Access
		10: Monitor RF Input LNA. When the RF input LNA experiences excessive RF input power, the RX_LNA_OVERLOAD bit is asserted high, and many of the RF portions of the chip are powered down until the excessive RF input power is removed. 11: Monitor RF Input LNA and Latch. When the RF input LNA experiences excessive RF input power, the RX_LNA_OVERLOAD_LATCHED bit is asserted high, and many of the RF portions of the chip are powered down. When the excessive RF input power is removed, the RF portions of the chip continue to be powered down. To power up the RF portions of the chip, the RX_LNA_OVERLOAD_LATCHED bit must be cleared, which can be accomplished by setting OVERLOAD_PROTECTION_MODE to any other value. Ensure to set OVERLOAD_PROTECTION_MODE back to the desired mode after performing the clear operation.		

Address: 0x15C, Reset: 0x05, Name: REG015C

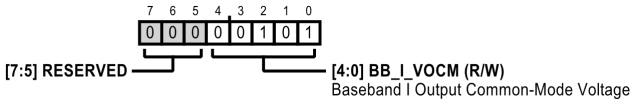

Figure 204.

Table 54. Bit Descriptions for REG015C

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	BB_I_VOCM	Baseband I Output Common-Mode Voltage.	0x5	R/W

Address: 0x165, Reset: 0x05, Name: REG0165

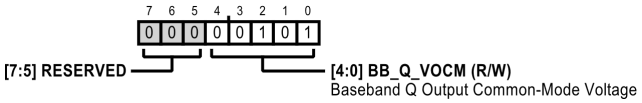

Figure 205.

Table 55. Bit Descriptions for REG0165

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	BB_Q_VOCM	Baseband Q Output Common-Mode Voltage.	0x5	R/W

Address: 0x172, Reset: 0x0F, Name: REG0172

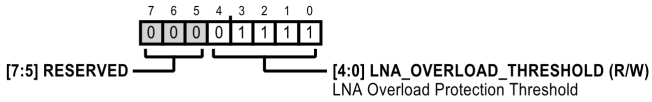

Figure 206.

Table 56. Bit Descriptions for REG0172

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LNA_OVERLOAD_THRESHOLD	LNA Overload Protection Threshold.	0xF	R/W

Address: 0x173, Reset: 0x0F, Name: REG0173

REGISTER DETAILS

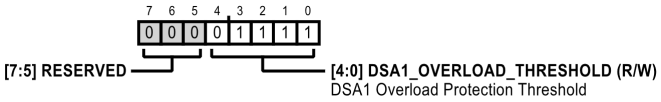

Figure 207.

Table 57. Bit Descriptions for REG0173

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	DSA1_OVERLOAD_THRESHOLD	DSA1 Overload Protection Threshold.	0xF	R/W

Address: 0x178, Reset: 0x07, Name: REG0178

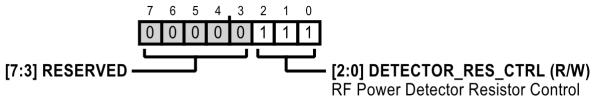

Figure 208.

Table 58. Bit Descriptions for REG0178

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	DETECTOR_RES_CTRL	RF Power Detector Resistor Control. Power detection dynamic range control. The RF input power sensing is inversely proportional to this value.	0x7	R/W

Address: 0x17D, Reset: 0x01, Name: REG017D

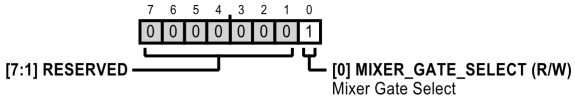

Figure 209.

Table 59. Bit Descriptions for REG017D

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	MIXER_GATE_SELECT	Mixer Gate Select. 0: I/Q Baseband Mode. 1: IF Mode.	0x1	R/W

Address: 0x184, Reset: 0x01, Name: REG0184

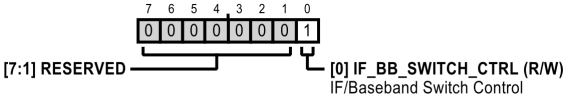

Figure 210.

Table 60. Bit Descriptions for REG0184

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	IF_BB_SWITCH_CTRL	IF/Baseband Switch Control. 0: I/Q Baseband Mode.	0x1	R/W

REGISTER DETAILS

Table 60. Bit Descriptions for REG0184 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: IF Mode.		

Address: 0x188, Reset: 0x04, Name: REG0188

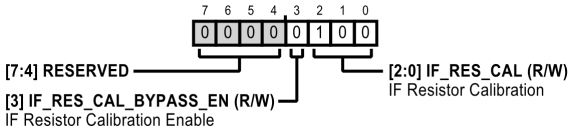

Figure 211.

Table 61. Bit Descriptions for REG0188

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	IF_RES_CAL_BYPASS_EN	IF Resistor Calibration Enable.	0x0	R/W
[2:0]	IF_RES_CAL	IF Resistor Calibration. 100: Low IF. 110: High IF.	0x4	R/W

Address: 0x18A, Reset: 0x01, Name: REG018A

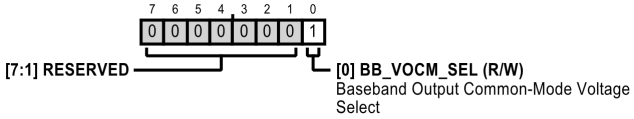

Figure 212.

Table 62. Bit Descriptions for REG018A

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	BB_VOCM_SEL	Baseband Output Common-Mode Voltage Select. 0: External Using CM_REF. 1: Internal Using Register 0x15C and Register 0x165.	0x1	R/W

Address: 0x18C, Reset: 0x00, Name: REG018C

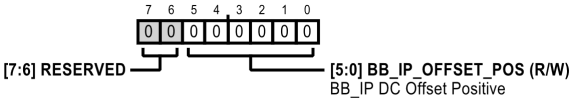

Figure 213.

Table 63. Bit Descriptions for REG018C

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_IP_OFFSET_POS	BB_IP DC Offset Positive.	0x0	R/W

Address: 0x18D, Reset: 0x3F, Name: REG018D

REGISTER DETAILS

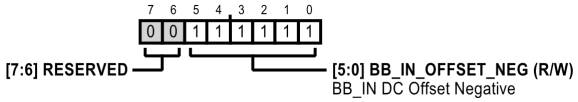

Figure 214.

Table 64. Bit Descriptions for REG018D

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_IN_OFFSET_NEG	BB_IN DC Offset Negative.	0x3F	R/W

Address: 0x18E, Reset: 0x00, Name: REG018E

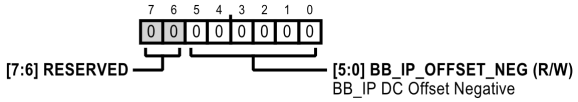

Figure 215.

Table 65. Bit Descriptions for REG018E

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_IP_OFFSET_NEG	BB_IP DC Offset Negative.	0x0	R/W

Address: 0x18F, Reset: 0x3F, Name: REG018F

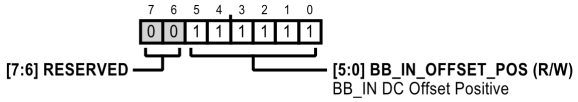

Figure 216.

Table 66. Bit Descriptions for REG018F

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_IN_OFFSET_POS	BB_IN DC Offset Positive.	0x3F	R/W

Address: 0x190, Reset: 0x00, Name: REG0190

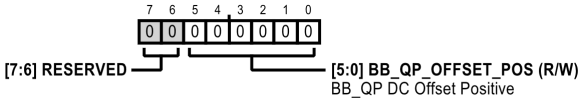

Figure 217.

Table 67. Bit Descriptions for REG0190

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_QP_OFFSET_POS	BB_QP DC Offset Positive.	0x0	R/W

Address: 0x191, Reset: 0x3F, Name: REG0191

REGISTER DETAILS

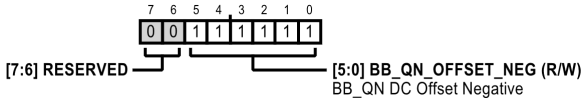

Figure 218.

Table 68. Bit Descriptions for REG0191

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_QN_OFFSET_NEG	BB_QN DC Offset Negative.	0x3F	R/W

Address: 0x192, Reset: 0x00, Name: REG0192

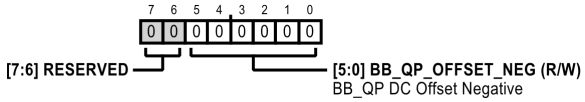

Figure 219.

Table 69. Bit Descriptions for REG0192

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_QP_OFFSET_NEG	BB_QP DC Offset Negative.	0x0	R/W

Address: 0x193, Reset: 0x3F, Name: REG0193

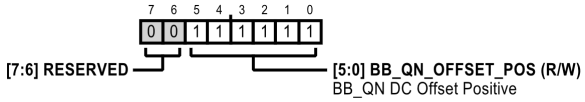

Figure 220.

Table 70. Bit Descriptions for REG0193

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	BB_QN_OFFSET_POS	BB_QN DC Offset Positive.	0x3F	R/W

Address: 0x194, Reset: 0x03, Name: REG0194

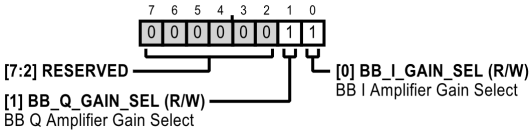

Figure 221.

Table 71. Bit Descriptions for REG0194

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	BB_Q_GAIN_SEL	BB Q Amplifier Gain Select. Use high gain for 50Ω differential impedance and low gain for 100Ω differential impedance implementations. 0: Low Gain. 1: High Gain.	0x1	R/W

REGISTER DETAILS

Table 71. Bit Descriptions for REG0194 (Continued)

Bits	Bit Name	Description	Reset	Access
0	BB_I_GAIN_SEL	BB I Amplifier Gain Select. Use high gain for 50Ω differential impedance and low gain for 100Ω differential impedance implementations. 0: Low Gain. 1: High Gain.	0x1	R/W

REGISTER 0X200 TO REGISTER 0X2B0

Address: 0x200, Reset: 0x01, Name: REG0200

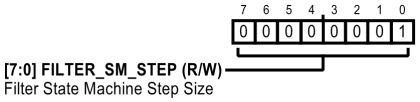

Figure 222.

Table 72. Bit Descriptions for REG0200

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_SM_STEP	Filter State Machine Step Size. This twos complement value determines how much the filter state machine is incremented or decremented. A step size of zero is invalid.	0x1	R/W

Address: 0x202, Reset: 0x01, Name: REG0202

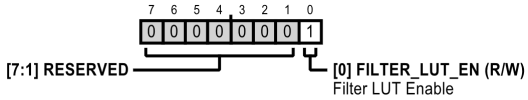

Figure 223.

Table 73. Bit Descriptions for REG0202

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LUT_EN	Filter LUT Enable. When disabled, filter settings defined using Register 0x800 to Register 0x80C. When enabled, filter settings are dependent upon the LUT, that is set using Register 0x900 to Register 0xC3F. 0: Disable. 1: Enable.	0x1	R/W

Address: 0x203, Reset: 0x00, Name: REG0203

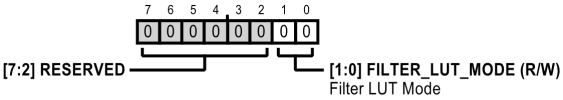

Figure 224.

Table 74. Bit Descriptions for REG0203

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	FILTER_LUT_MODE	Filter LUT Mode. 00: LUT pointer selected by using the ADD_F balls. 01: LUT pointer selected by using Register 0x209 (FILTER_SPI_POINTER). 10: LUT pointer is incremented or decremented on rising edge of ADD_F4.	0x0	R/W

REGISTER DETAILS

Address: 0x204, Reset: 0x01, Name: REG0204

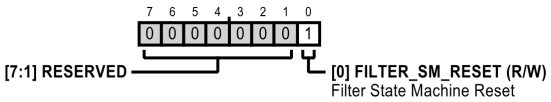

Figure 225.

Table 75. Bit Descriptions for REG0204

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_SM_RESET	Filter State Machine Reset. Active low reset. Set this bit field to 0 and then to 1 to reset the state machine to 0. When this bit field is kept at 0, the state machine remains at 0. 0: Reset Address Pointer to Zero. 1: Normal Operation.	0x1	R/W

Address: 0x205, Reset: 0x00, Name: REG0205

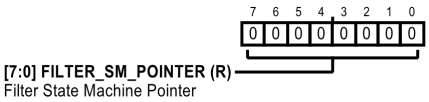

Figure 226.

Table 76. Bit Descriptions for REG0205

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_SM_POINTER	Filter State Machine Pointer.	0x0	R

Address: 0x206, Reset: 0x1F, Name: REG0206

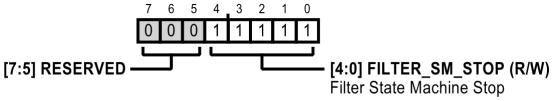

Figure 227.

Table 77. Bit Descriptions for REG0206

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_SM_STOP	Filter State Machine Stop.	0x1F	R/W

Address: 0x207, Reset: 0x00, Name: REG0207

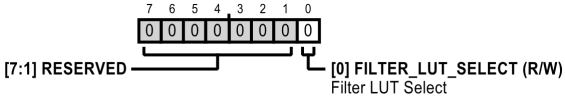

Figure 228.

Table 78. Bit Descriptions for REG0207

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LUT_SELECT	Filter LUT Select. 0: Table A.	0x0	R/W

REGISTER DETAILS

Table 78. Bit Descriptions for REG0207 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Table B.		

Address: 0x208, Reset: 0x00, Name: REG0208

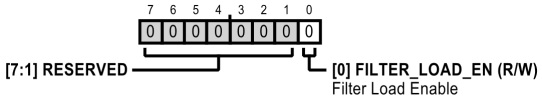

Figure 229.

Table 79. Bit Descriptions for REG0208

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LOAD_EN	Filter Load Enable. When disabled, the filter values are applied immediately. When enabled, the filter values are applied upon the rising edge of the LOAD ball. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x209, Reset: 0x00, Name: REG0209

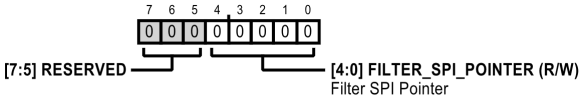

Figure 230.

Table 80. Bit Descriptions for REG0209

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_SPI_POINTER	Filter SPI Pointer.	0x0	R/W

Address: 0x20A, Reset: 0x00, Name: REG020A

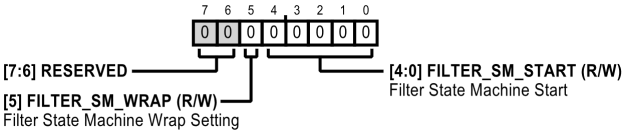

Figure 231.

Table 81. Bit Descriptions for REG020A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	FILTER_SM_WRAP	Filter State Machine Wrap Setting.	0x0	R/W
[4:0]	FILTER_SM_START	Filter State Machine Start.	0x0	R/W

Address: 0x210, Reset: 0x00, Name: REG0210

REGISTER DETAILS

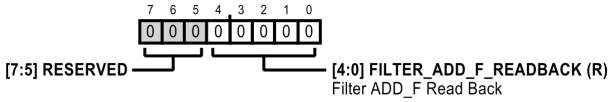

Figure 232.

Table 82. Bit Descriptions for REG0210

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_ADD_F_READBACK	Filter ADD_F Read Back.	0x0	R

Address: 0x211, Reset: 0x00, Name: REG0211

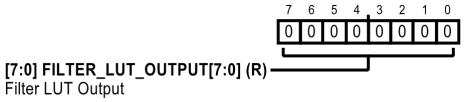

Figure 233.

Table 83. Bit Descriptions for REG0211

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[7:0]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x212, Reset: 0x00, Name: REG0212

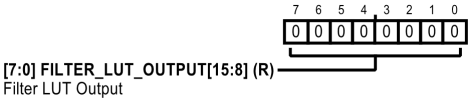

Figure 234.

Table 84. Bit Descriptions for REG0212

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[15:8]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x213, Reset: 0x00, Name: REG0213

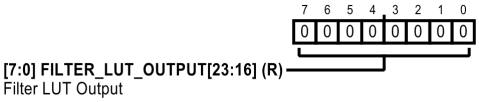

Figure 235.

Table 85. Bit Descriptions for REG0213

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[23:16]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x214, Reset: 0x00, Name: REG0214

REGISTER DETAILS

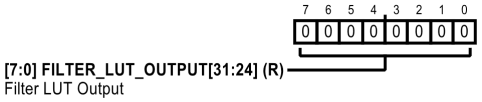

Figure 236.

Table 86. Bit Descriptions for REG0214

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[31:24]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x215, Reset: 0x00, Name: REG0215

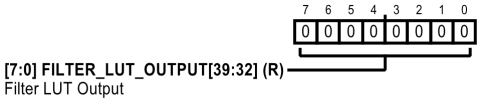

Figure 237.

Table 87. Bit Descriptions for REG0215

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[39:32]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x216, Reset: 0x00, Name: REG0216

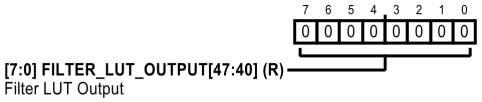

Figure 238.

Table 88. Bit Descriptions for REG0216

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[47:40]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x217, Reset: 0x00, Name: REG0217

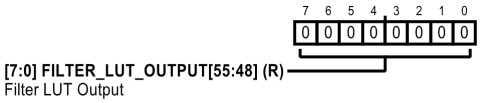

Figure 239.

Table 89. Bit Descriptions for REG0217

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[55:48]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x218, Reset: 0x00, Name: REG0218

REGISTER DETAILS

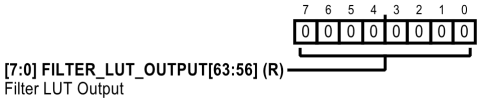

Figure 240.

Table 90. Bit Descriptions for REG0218

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[63:56]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x219, Reset: 0x00, Name: REG0219

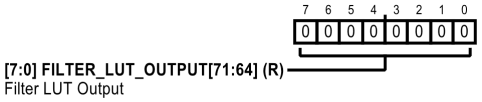

Figure 241.

Table 91. Bit Descriptions for REG0219

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[71:64]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21A, Reset: 0x00, Name: REG021A

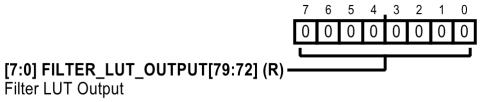

Figure 242.

Table 92. Bit Descriptions for REG021A

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[79:72]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21B, Reset: 0x00, Name: REG021B

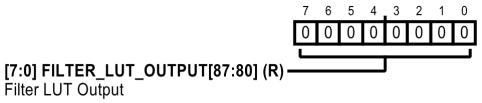

Figure 243.

Table 93. Bit Descriptions for REG021B

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[87:80]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21C, Reset: 0x00, Name: REG021C

REGISTER DETAILS

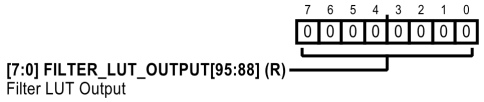

Figure 244.

Table 94. Bit Descriptions for REG021C

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[95:88]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21D, Reset: 0x00, Name: REG021D

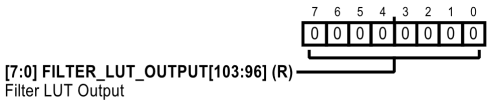

Figure 245.

Table 95. Bit Descriptions for REG021D

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[103:96]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x220, Reset: 0x00, Name: REG0220

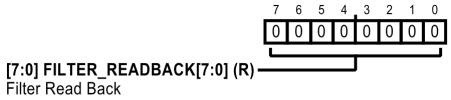

Figure 246.

Table 96. Bit Descriptions for REG0220

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[7:0]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x221, Reset: 0x00, Name: REG0221

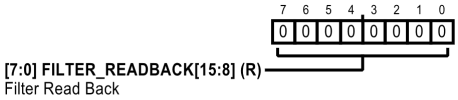

Figure 247.

Table 97. Bit Descriptions for REG0221

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[15:8]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x222, Reset: 0x00, Name: REG0222

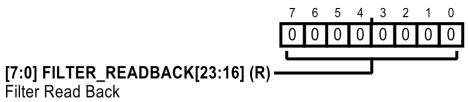

Figure 248.

REGISTER DETAILS

Table 98. Bit Descriptions for REG0222

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[23:16]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x223, Reset: 0x00, Name: REG0223

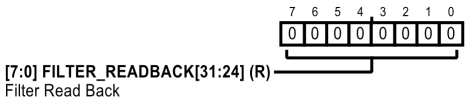

Figure 249.

Table 99. Bit Descriptions for REG0223

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[31:24]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x224, Reset: 0x00, Name: REG0224

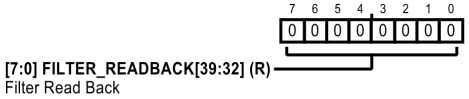

Figure 250.

Table 100. Bit Descriptions for REG0224

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[39:32]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x225, Reset: 0x00, Name: REG0225

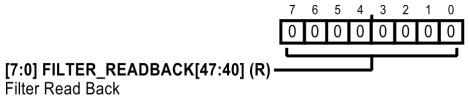

Figure 251.

Table 101. Bit Descriptions for REG0225

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[47:40]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x226, Reset: 0x00, Name: REG0226

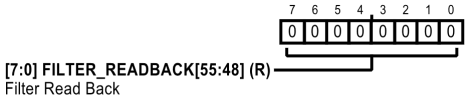

Figure 252.

Table 102. Bit Descriptions for REG0226

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[55:48]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x227, Reset: 0x00, Name: REG0227

REGISTER DETAILS

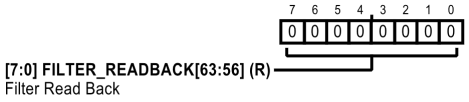

Figure 253.

Table 103. Bit Descriptions for REG0227

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[63:56]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x228, Reset: 0x00, Name: REG0228

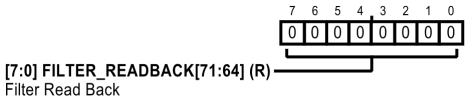

Figure 254.

Table 104. Bit Descriptions for REG0228

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[71:64]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x229, Reset: 0x00, Name: REG0229

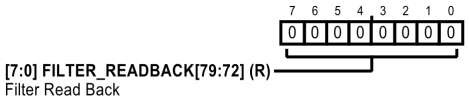

Figure 255.

Table 105. Bit Descriptions for REG0229

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[79:72]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22A, Reset: 0x00, Name: REG022A

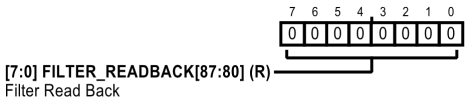

Figure 256.

Table 106. Bit Descriptions for REG022A

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[87:80]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22B, Reset: 0x00, Name: REG022B

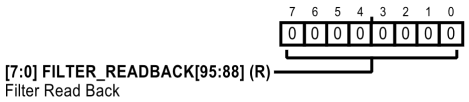

Figure 257.

REGISTER DETAILS

Table 107. Bit Descriptions for REG022B

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[95:88]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22C, Reset: 0x00, Name: REG022C

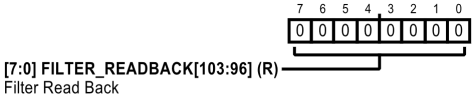

Figure 258.

Table 108. Bit Descriptions for REG022C

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[103:96]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x240, Reset: 0x00, Name: REG0240

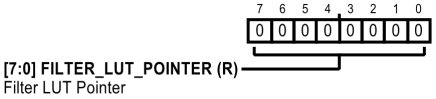

Figure 259.

Table 109. Bit Descriptions for REG0240

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_POINTER	Filter LUT Pointer. This bit field represents the index pointer for the filter LUT after the mux that is controlled by Register 0x203.	0x0	R

Address: 0x281, Reset: 0x00, Name: REG0281

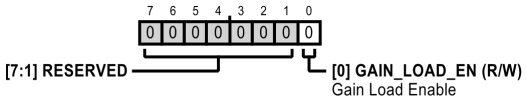

Figure 260.

Table 110. Bit Descriptions for REG0281

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LOAD_EN	Gain Load Enable. When disabled, the gain values are applied immediately. When enabled, the gain values are applied upon the rising edge of the LOAD ball. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x282, Reset: 0x00, Name: REG0282

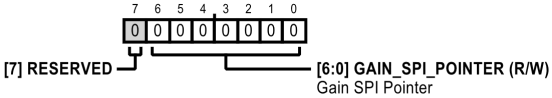

Figure 261.

REGISTER DETAILS

Table 111. Bit Descriptions for REG0282

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	GAIN_SPI_POINTER	Gain SPI Pointer.	0x0	R/W

Address: 0x283, Reset: 0x01, Name: REG0283

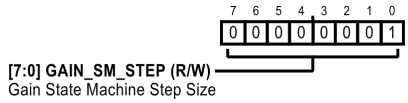

Figure 262.

Table 112. Bit Descriptions for REG0283

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_STEP	Gain State Machine Step Size. This twos complement value determines how much the gain state machine is incremented or decremented. A step size of zero is invalid.	0x1	R/W

Address: 0x284, Reset: 0x00, Name: REG0284

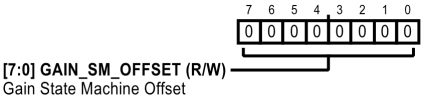

Figure 263.

Table 113. Bit Descriptions for REG0284

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_OFFSET	Gain State Machine Offset. This twos complement value determines how much the state machine output will be offset.	0x0	R/W

Address: 0x285, Reset: 0x01, Name: REG0285

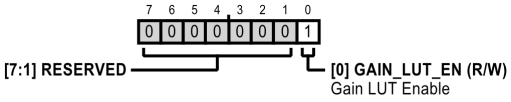

Figure 264.

Table 114. Bit Descriptions for REG0285

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LUT_EN	Gain LUT Enable. When disabled, filter settings defined using Register 0x600 to Register 0x603. When enabled, filter settings are dependent upon the LUT, that is set using Registers 0xE00 to Register 0xF0B. 0: Disable. 1: Enable.	0x1	R/W

Address: 0x286, Reset: 0x00, Name: REG0286

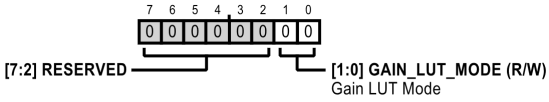

Figure 265.

REGISTER DETAILS

Table 115. Bit Descriptions for REG0286

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	GAIN_LUT_MODE	Gain LUT Mode. 00: LUT pointer selected by using the ADD_G balls. 01: LUT pointer selected by using Register 0x282 (FILTER_SPI_POINTER). 10: LUT pointer is incremented or decremented on rising edge of ADD_G5.	0x0	R/W

Address: 0x287, Reset: 0x01, Name: REG0287

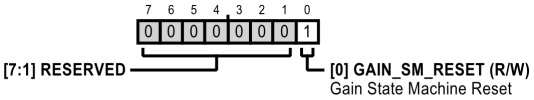

Figure 266.

Table 116. Bit Descriptions for REG0287

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_SM_RESET	Gain State Machine Reset. Active low reset. Set this bit field to 0 and then to 1 to reset the state machine to 0. When this bit field is kept at 0, the state machine remains at 0. 0: Reset Address Pointer to Zero. 1: Normal Operation.	0x1	R/W

Address: 0x288, Reset: 0x00, Name: REG0288

Figure 267.

Table 117. Bit Descriptions for REG0288

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_POINTER_PLUS_OFFSET	Gain State Machine Pointer Plus Offset.	0x0	R

Address: 0x289, Reset: 0x42, Name: REG0289

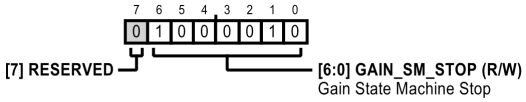

Figure 268.

Table 118. Bit Descriptions for REG0289

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	GAIN_SM_STOP	Gain State Machine Stop.	0x42	R/W

Address: 0x28A, Reset: 0x00, Name: REG028A

REGISTER DETAILS

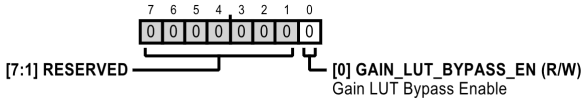

Figure 269.

Table 119. Bit Descriptions for REG028A

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LUT_BYPASS_EN	Gain LUT Bypass Enable. When enabled, gain and GPO_G values are set using Register 0x28B to Register 0x28E. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x28B, Reset: 0x00, Name: REG028B

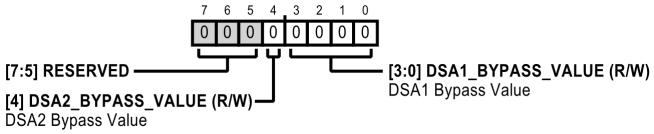

Figure 270.

Table 120. Bit Descriptions for REG028B

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	DSA2_BYPASS_VALUE	DSA2 Bypass Value. Provides gain range with single 1-bit gain step of 6dB.	0x0	R/W
[3:0]	DSA1_BYPASS_VALUE	DSA1 Bypass Value. Where 0x0 is the maximum gain and 0xF is the minimum gain.	0x0	R/W

Address: 0x28C, Reset: 0x00, Name: REG028C

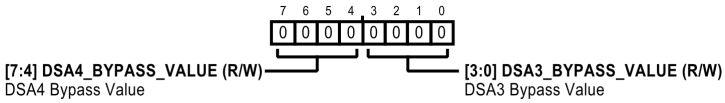

Figure 271.

Table 121. Bit Descriptions for REG028C

Bits	Bit Name	Description	Reset	Access
[7:4]	DSA4_BYPASS_VALUE	DSA4 Bypass Value. Where 0x0 is the maximum gain and 0xF is the minimum gain.	0x0	R/W
[3:0]	DSA3_BYPASS_VALUE	DSA3 Bypass Value. Where 0x0 is the maximum gain and 0xF is the minimum gain.	0x0	R/W

Address: 0x28D, Reset: 0x00, Name: REG028D

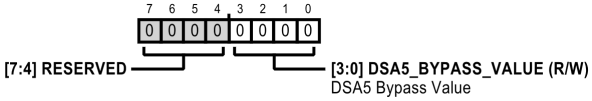

Figure 272.

Table 122. Bit Descriptions for REG028D

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 122. Bit Descriptions for REG028D (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	DSA5_BYPASS_VALUE	DSA5 Bypass Value. Where 0x0 is the maximum gain and 0xF is the minimum gain.	0x0	R/W

Address: 0x28E, Reset: 0x00, Name: REG028E

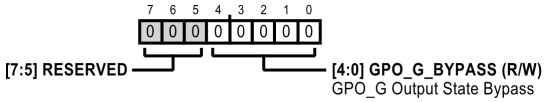

Figure 273.

Table 123. Bit Descriptions for REG028E

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G_BYPASS	GPO_G Output State Bypass.	0x0	R/W

Address: 0x28F, Reset: 0x00, Name: REG028F

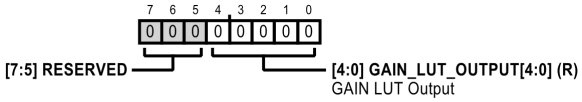

Figure 274.

Table 124. Bit Descriptions for REG028F

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_LUT_OUTPUT[4:0]	GAIN LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

Address: 0x290, Reset: 0x00, Name: REG0290

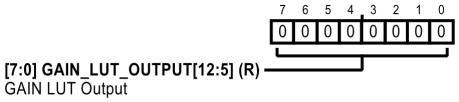

Figure 275.

Table 125. Bit Descriptions for REG0290

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_LUT_OUTPUT[12:5]	GAIN LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

Address: 0x291, Reset: 0x00, Name: REG0291

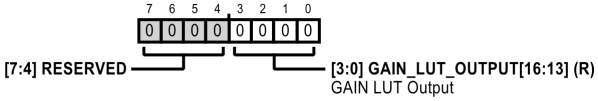

Figure 276.

REGISTER DETAILS

Table 126. Bit Descriptions for REG0291

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	GAIN_LUT_OUTPUT[16:13]	GAIN LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

Address: 0x292, Reset: 0x00, Name: REG0292

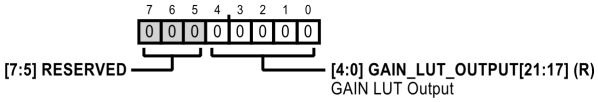

Figure 277.

Table 127. Bit Descriptions for REG0292

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_LUT_OUTPUT[21:17]	GAIN LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

Address: 0x293, Reset: 0x00, Name: REG0293

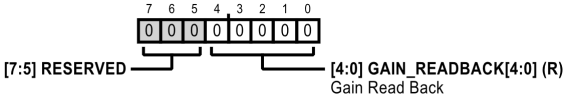

Figure 278.

Table 128. Bit Descriptions for REG0293

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_READBACK[4:0]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x294, Reset: 0x00, Name: REG0294

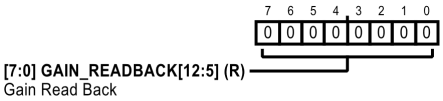

Figure 279.

Table 129. Bit Descriptions for REG0294

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_READBACK[12:5]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x295, Reset: 0x00, Name: REG0295

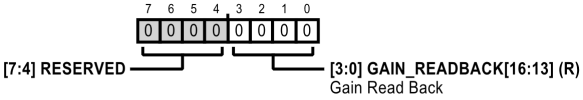

Figure 280.

REGISTER DETAILS

Table 130. Bit Descriptions for REG0295

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	GAIN_READBACK[16:13]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x296, Reset: 0x00, Name: REG0296

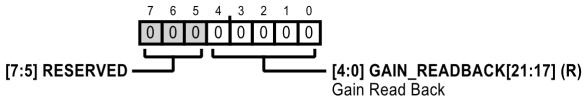

Figure 281.

Table 131. Bit Descriptions for REG0296

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_READBACK[21:17]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x298, Reset: 0x00, Name: REG0298

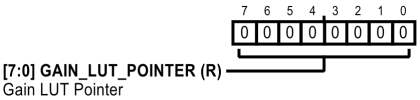

Figure 282.

Table 132. Bit Descriptions for REG0298

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_LUT_POINTER	Gain LUT Pointer. This bit field represents the index pointer for the gain LUT after the mux that is controlled by Register 0x286.	0x0	R

Address: 0x29B, Reset: 0x00, Name: REG029B

Figure 283.

Table 133. Bit Descriptions for REG029B

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_POINTER_PRE_OFFSET	Gain State Machine Pointer Pre Offset.	0x0	R

Address: 0x2A0, Reset: 0x00, Name: REG02A0

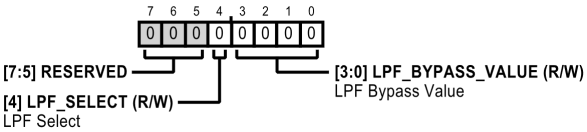

Figure 284.

REGISTER DETAILS

Table 134. Bit Descriptions for REG02A0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	LPF_SELECT	LPF Select. 0: Filter state determined from LUT or Register 0x800 to Register 0x80C. 1: Filter state determined from SPI (LPF_BYPASS_VALUE).	0x0	R/W
[3:0]	LPF_BYPASS_VALUE	LPF Bypass Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W

Address: 0x2A1, Reset: 0x00, Name: REG02A1

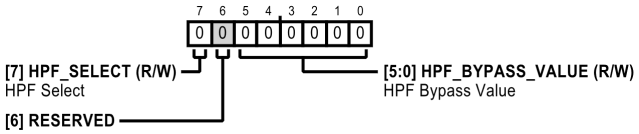

Figure 285.

Table 135. Bit Descriptions for REG02A1

Bits	Bit Name	Description	Reset	Access
7	HPF_SELECT	HPF Select. 0: Filter state determined from LUT or Register 0x800 to Register 0x80C. 1: Filter state determined from SPI (HPF_BYPASS_VALUE).	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
[5:0]	HPF_BYPASS_VALUE	HPF Bypass Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W

Address: 0x2A2, Reset: 0x00, Name: REG02A2

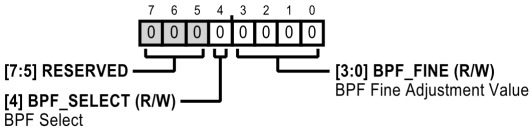

Figure 286.

Table 136. Bit Descriptions for REG02A2

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	BPF_SELECT	BPF Select. 0: BPF fine adjustment disabled. 1: BPF fine adjustment determined from SPI (BPF_FINE).	0x0	R/W
[3:0]	BPF_FINE	BPF Fine Adjustment Value. Both high and low cutoff frequencies are inversely proportional to this bit field value.	0x0	R/W

Address: 0x2A3, Reset: 0x00, Name: REG02A3

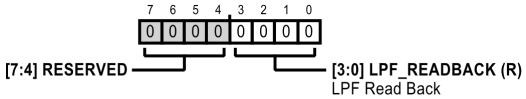

Figure 287.

Table 137. Bit Descriptions for REG02A3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 137. Bit Descriptions for REG02A3 (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	LPF_READBACK	LPF Read Back.	0x0	R

Address: 0x2A4, Reset: 0x00, Name: REG02A4

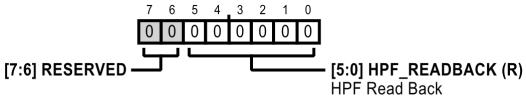

Figure 288.

Table 138. Bit Descriptions for REG02A4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	HPF_READBACK	HPF Read Back.	0x0	R

Address: 0x2A5, Reset: 0x00, Name: REG02A5

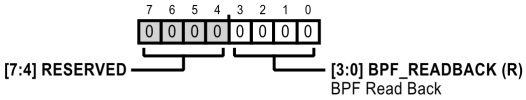

Figure 289.

Table 139. Bit Descriptions for REG02A5

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	BPF_READBACK	BPF Read Back.	0x0	R

Address: 0x2B0, Reset: 0x00, Name: REG02B0

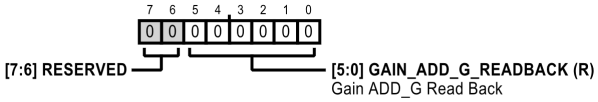

Figure 290.

Table 140. Bit Descriptions for REG02B0

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GAIN_ADD_G_READBACK	Gain ADD_G Read Back.	0x0	R

REGISTER 0X600 TO REGISTER 0X80C

Address: 0x600, Reset: 0x00, Name: REG0600

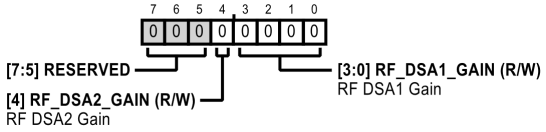

Figure 291.

REGISTER DETAILS

Table 141. Bit Descriptions for REG0600

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	RF_DSA2_GAIN	RF DSA2 Gain. Provides gain range with single 1-bit gain step of 6dB.	0x0	R/W
[3:0]	RF_DSA1_GAIN	RF DSA1 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.	0x0	R/W

Address: 0x601, Reset: 0x00, Name: REG0601

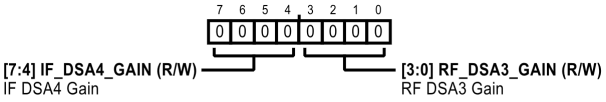

Figure 292.

Table 142. Bit Descriptions for REG0601

Bits	Bit Name	Description	Reset	Access
[7:4]	IF_DSA4_GAIN	IF DSA4 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.	0x0	R/W
[3:0]	RF_DSA3_GAIN	RF DSA3 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB.	0x0	R/W

REGISTER DETAILS

Table 142. Bit Descriptions for REG0601 (Continued)

Bits	Bit Name	Description	Reset	Access
		0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.		

Address: 0x602, Reset: 0x00, Name: REG0602

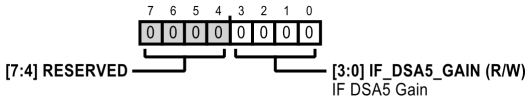

Figure 293.

Table 143. Bit Descriptions for REG0602

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	IF_DSA5_GAIN	IF DSA5 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1111: −14dB. 1110: −15dB.	0x0	R/W

Address: 0x603, Reset: 0x00, Name: REG0603

REGISTER DETAILS

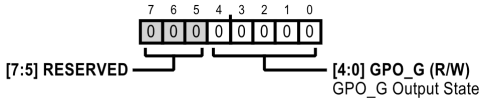

Figure 294.

Table 144. Bit Descriptions for REG0603

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G	GPO_G Output State. Use this bit field to set the logic state of the GPO_G outputs.	0x0	R/W

Address: 0x780, Reset: 0x00, Name: REG0780

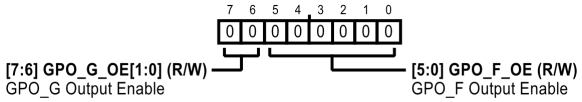

Figure 295.

Table 145. Bit Descriptions for REG0780

Bits	Bit Name	Description	Reset	Access
[7:6]	GPO_G_OE[1:0]	GPO_G Output Enable. This bit field enables the general-purpose output buffers.	0x0	R/W
[5:0]	GPO_F_OE	GPO_F Output Enable. This bit field enables the general-purpose output buffers.	0x0	R/W

Address: 0x781, Reset: 0x00, Name: REG0781

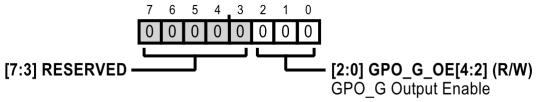

Figure 296.

Table 146. Bit Descriptions for REG0781

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	GPO_G_OE[4:2]	GPO_G Output Enable. This bit field enables the general-purpose output buffers.	0x0	R/W

Address: 0x800, Reset: 0x00, Name: REG0800

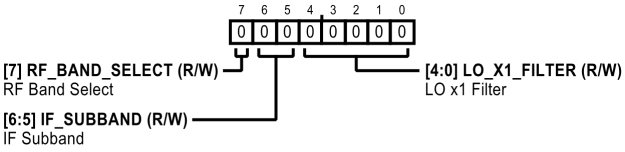

Figure 297.

Table 147. Bit Descriptions for REG0800

Bits	Bit Name	Description	Reset	Access
7	RF_BAND_SELECT	RF Band Select. 0: Low Band. 1: High Band.	0x0	R/W
[6:5]	IF_SUBBAND	IF Subband. 00: 8GHz or 10GHz.	0x0	R/W

REGISTER DETAILS

Table 147. Bit Descriptions for REG0800 (Continued)

Bits	Bit Name	Description	Reset	Access
		01: 6GHz. 11: 4GHz.		
[4:0]	LO_X1_FILTER	LO x1 Filter. 00000: LO Frequency ≥ 21GHz. 00001: 17GHz ≤ LO Frequency < 21GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 01010: 12GHz ≤ LO Frequency < 15GHz. 11111: LO Frequency < 12GHz.	0x0	R/W

Address: 0x801, Reset: 0x80, Name: REG0801

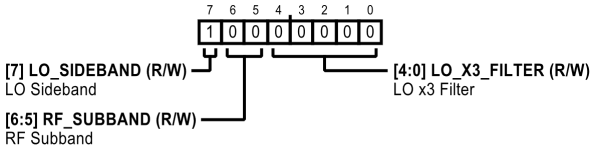

Figure 298.

Table 148. Bit Descriptions for REG0801

Bits	Bit Name	Description	Reset	Access
7	LO_SIDEBAND	LO Sideband. 0: USB. 1: LSB.	0x1	R/W
[6:5]	RF_SUBBAND	RF Subband. 00: Low Band. 11: High Band.	0x0	R/W
[4:0]	LO_X3_FILTER	LO x3 Filter. 00000: LO Frequency ≥ 24GHz. 00010: 21GHz ≤ LO Frequency < 24GHz. 00011: 19GHz ≤ LO Frequency < 21GHz. 00100: 17GHz ≤ LO Frequency < 19GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 11100: LO Frequency < 12GHz. 00111: 12GHz ≤ LO Frequency < 15GHz.	0x0	R/W

Address: 0x802, Reset: 0x00, Name: REG0802

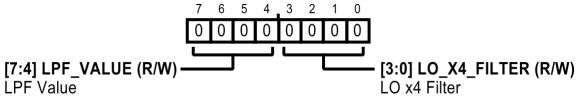

Figure 299.

Table 149. Bit Descriptions for REG0802

Bits	Bit Name	Description	Reset	Access
[7:4]	LPF_VALUE	LPF Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W
[3:0]	LO_X4_FILTER	LO x4 Filter. 0000: 10GHz ≤ LO Frequency < 14GHz. 0101: 14GHz ≤ LO Frequency < 18GHz. 0111: LO Frequency ≥ 18GHz.	0x0	R/W

REGISTER DETAILS

Table 149. Bit Descriptions for REG0802 (Continued)

Bits	Bit Name	Description	Reset	Access
		1000: LO Frequency < 10GHz.		

Address: 0x803, Reset: 0x00, Name: REG0803

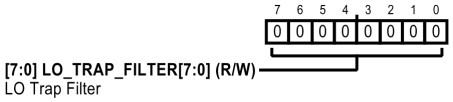

Figure 300.

Table 150. Bit Descriptions for REG0803

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_TRAP_FILTER[7:0]	LO Trap Filter. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x804, Reset: 0x00, Name: REG0804

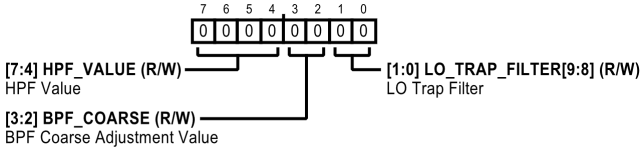

Figure 301.

Table 151. Bit Descriptions for REG0804

Bits	Bit Name	Description	Reset	Access
[7:4]	HPF_VALUE	HPF Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W
[3:2]	BPF_COARSE	BPF Coarse Adjustment Value. 00: High IF. 11: Low IF.	0x0	R/W
[1:0]	LO_TRAP_FILTER[9:8]	LO Trap Filter. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x805, Reset: 0x00, Name: REG0805

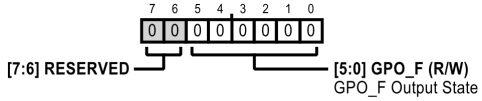

Figure 302.

REGISTER DETAILS

Table 152. Bit Descriptions for REG0805

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GPO_F	GPO_F Output State. Use this bit field to set the logic state of the GPO_F outputs.	0x0	R/W

Address: 0x806, Reset: 0x00, Name: REG0806

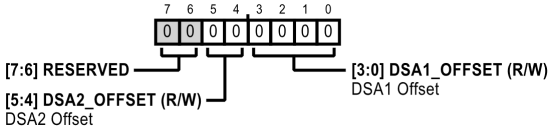

Figure 303.

Table 153. Bit Descriptions for REG0806

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	DSA2_OFFSET	DSA2 Offset.	0x0	R/W
[3:0]	DSA1_OFFSET	DSA1 Offset.	0x0	R/W

Address: 0x807, Reset: 0x00, Name: REG0807

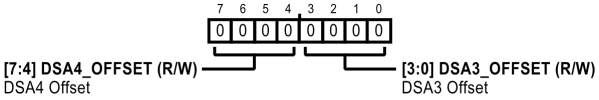

Figure 304.

Table 154. Bit Descriptions for REG0807

Bits	Bit Name	Description	Reset	Access
[7:4]	DSA4_OFFSET	DSA4 Offset.	0x0	R/W
[3:0]	DSA3_OFFSET	DSA3 Offset.	0x0	R/W

Address: 0x808, Reset: 0x00, Name: REG0808

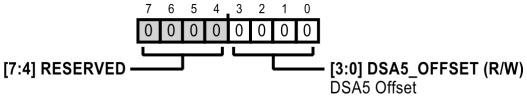

Figure 305.

Table 155. Bit Descriptions for REG0808

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DSA5_OFFSET	DSA5 Offset.	0x0	R/W

Address: 0x809, Reset: 0x00, Name: REG0809

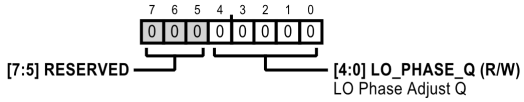

Figure 306.

REGISTER DETAILS

Table 156. Bit Descriptions for REG0809

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_PHASE_Q	LO Phase Adjust Q. This bit field adjusts the phase of the Q path within the LO block. It can be used to calibrate the image rejection.	0x0	R/W

Address: 0x80A, Reset: 0x20, Name: REG080A

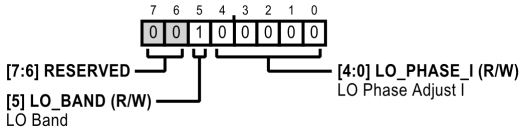

Figure 307.

Table 157. Bit Descriptions for REG080A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LO_BAND	LO Band. 0: Low Band. 1: High Band.	0x1	R/W
[4:0]	LO_PHASE_I	LO Phase Adjust I. This bit field adjusts the phase of the I path within the LO block. It can be used to calibrate the image rejection.	0x0	R/W

Address: 0x80B, Reset: 0x00, Name: REG080B

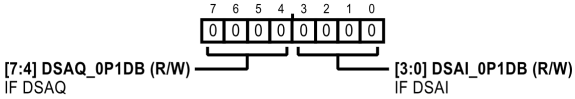

Figure 308.

Table 158. Bit Descriptions for REG080B

Bits	Bit Name	Description	Reset	Access
[7:4]	DSAQ_0P1DB	IF DSAQ. 1.5dB Range with 0.1dB Step, Used for IMR Calibration.	0x0	R/W
[3:0]	DSAI_0P1DB	IF DSAI. 1.5dB Range with 0.1dB Step, Used for IMR Calibration.	0x0	R/W

Address: 0x80C, Reset: 0x00, Name: REG080C

Figure 309.

Table 159. Bit Descriptions for REG080C

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_DOUBLER_BAND	LO Double Band. The enumeration values are general guidance. Adjust as needed to achieve system level spurious specifications. 0xC0: LO Frequency ≥ 24GHz. 0x80: 18GHz ≤ LO Frequency < 24GHz. 0x08: 14GHz ≤ LO Frequency < 18GHz. 0x04: 12GHz ≤ LO Frequency < 14GHz.	0x0	R/W

REGISTER DETAILS

Table 159. Bit Descriptions for REG080C (Continued)

Bits	Bit Name	Description	Reset	Access
		0x1D: 10GHz ≤ LO Frequency < 12GHz. 0x1F: LO Frequency < 10GHz.		

REGISTER 0X900 TO REGISTER 0XE03

Address: 0x900, Reset: 0x00, Name: REG0900

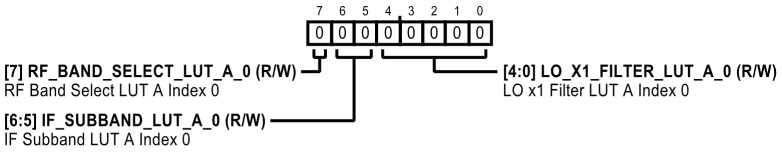

Figure 310.

Table 160. Bit Descriptions for REG0900

Bits	Bit Name	Description	Reset	Access
7	RF_BAND_SELECT_LUT_A_0	RF Band Select LUT A Index 0. 0: Low Band. 1: High Band.	0x0	R/W
[6:5]	IF_SUBBAND_LUT_A_0	IF Subband LUT A Index 0. 00: 8GHz or 10GHz. 01: 6GHz. 11: 4GHz.	0x0	R/W
[4:0]	LO_X1_FILTER_LUT_A_0	LO x1 Filter LUT A Index 0. 00000: LO Frequency ≥ 21GHz. 00001: 17GHz ≤ LO Frequency < 21GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 01010: 12GHz ≤ LO Frequency < 15GHz. 11111: LO Frequency < 12GHz.	0x0	R/W

Address: 0x901, Reset: 0x80, Name: REG0901

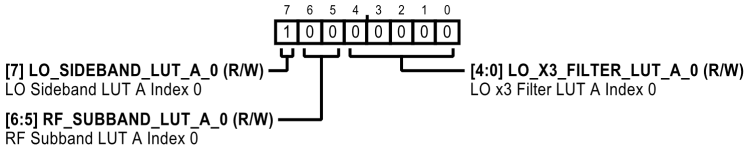

Figure 311.

Table 161. Bit Descriptions for REG0901

Bits	Bit Name	Description	Reset	Access
7	LO_SIDEBAND_LUT_A_0	LO Sideband LUT A Index 0. 0: USB. 1: LSB.	0x1	R/W
[6:5]	RF_SUBBAND_LUT_A_0	RF Subband LUT A Index 0. 00: Low Band. 11: High Band.	0x0	R/W
[4:0]	LO_X3_FILTER_LUT_A_0	LO x3 Filter LUT A Index 0. 00000: LO Frequency ≥ 24GHz.	0x0	R/W

REGISTER DETAILS

Table 161. Bit Descriptions for REG0901 (Continued)

Bits	Bit Name	Description	Reset	Access
		00010: 21GHz ≤ LO Frequency < 24GHz. 00011: 19GHz ≤ LO Frequency < 21GHz. 00100: 17GHz ≤ LO Frequency < 19GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 11100: LO Frequency < 12GHz. 00111: 12GHz ≤ LO Frequency < 15GHz.		

Address: 0x902, Reset: 0x00, Name: REG0902

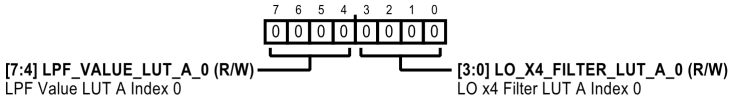

Figure 312.

Table 162. Bit Descriptions for REG0902

Bits	Bit Name	Description	Reset	Access
[7:4]	LPF_VALUE_LUT_A_0	LPF Value LUT A Index 0. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W
[3:0]	LO_X4_FILTER_LUT_A_0	LO x4 Filter LUT A Index 0. 0000: 10GHz ≤ LO Frequency < 14GHz. 0101: 14GHz ≤ LO Frequency < 18GHz. 0111: LO Frequency ≥ 18GHz. 1000: LO Frequency < 10GHz.	0x0	R/W

Address: 0x903, Reset: 0x00, Name: REG0903

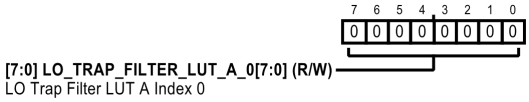

Figure 313.

Table 163. Bit Descriptions for REG0903

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_TRAP_FILTER_LUT_A_0[7:0]	LO Trap Filter LUT A Index 0. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x904, Reset: 0x00, Name: REG0904

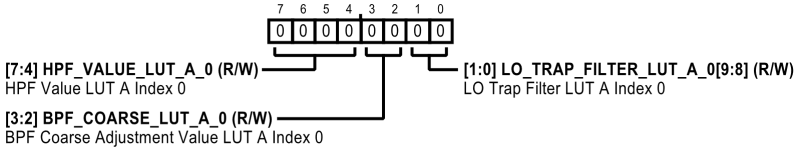

Figure 314.

REGISTER DETAILS

Table 164. Bit Descriptions for REG0904

Bits	Bit Name	Description	Reset	Access
[7:4]	HPF_VALUE_LUT_A_0	HPF Value LUT A Index 0. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W
[3:2]	BPF_COARSE_LUT_A_0	BPF Coarse Adjustment Value LUT A Index 0. 00: High IF. 11: Low IF.	0x0	R/W
[1:0]	LO_TRAP_FILTER_LUT_A_0[9:8]	LO Trap Filter LUT A Index 0. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x905, Reset: 0x00, Name: REG0905

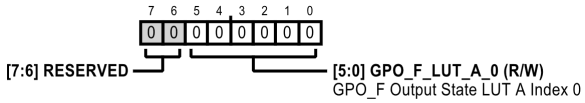

Figure 315.

Table 165. Bit Descriptions for REG0905

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GPO_F_LUT_A_0	GPO_F Output State LUT A Index 0. Use this bit field to set the logic state of the GPO_F outputs.	0x0	R/W

Address: 0x906, Reset: 0x00, Name: REG0906

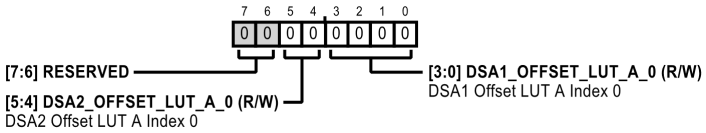

Figure 316.

Table 166. Bit Descriptions for REG0906

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	DSA2_OFFSET_LUT_A_0	DSA2 Offset LUT A Index 0.	0x0	R/W
[3:0]	DSA1_OFFSET_LUT_A_0	DSA1 Offset LUT A Index 0.	0x0	R/W

Address: 0x907, Reset: 0x00, Name: REG0907

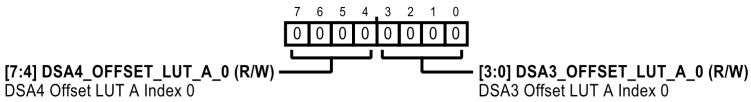

Figure 317.

Table 167. Bit Descriptions for REG0907

Bits	Bit Name	Description	Reset	Access
[7:4]	DSA4_OFFSET_LUT_A_0	DSA4 Offset LUT A Index 0.	0x0	R/W

REGISTER DETAILS

Table 167. Bit Descriptions for REG0907 (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	DSA3_OFFSET_LUT_A_0	DSA3 Offset LUT A Index 0.	0x0	R/W

Address: 0x908, Reset: 0x00, Name: REG0908

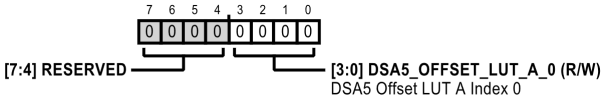

Figure 318.

Table 168. Bit Descriptions for REG0908

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DSA5_OFFSET_LUT_A_0	DSA5 Offset LUT A Index 0.	0x0	R/W

Address: 0x909, Reset: 0x00, Name: REG0909

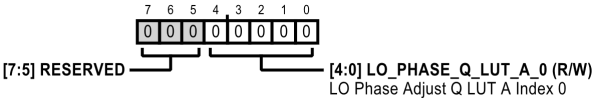

Figure 319.

Table 169. Bit Descriptions for REG0909

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_PHASE_Q_LUT_A_0	LO Phase Adjust Q LUT A Index 0. This bit field adjusts the phase of the Q path within the LO block. It can be used to calibrate the image rejection.	0x0	R/W

Address: 0x90A, Reset: 0x20, Name: REG090A

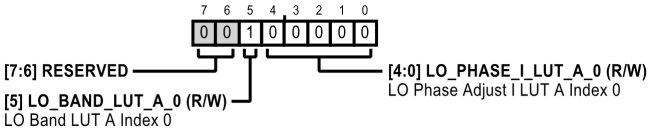

Figure 320.

Table 170. Bit Descriptions for REG090A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LO_BAND_LUT_A_0	LO Band LUT A Index 0. 0: Low Band. 1: High Band.	0x1	R/W
[4:0]	LO_PHASE_I_LUT_A_0	LO Phase Adjust I LUT A Index 0. This bit field adjusts the phase of the I path within the LO block. It can be used to calibrate the image rejection.	0x0	R/W

Address: 0x90B, Reset: 0x00, Name: REG090B

REGISTER DETAILS

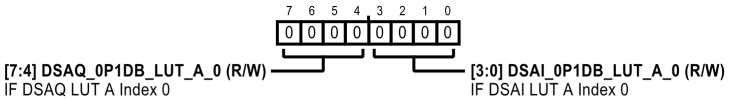

Figure 321.

Table 171. Bit Descriptions for REG090B

Bits	Bit Name	Description	Reset	Access
[7:4]	DSAQ_0P1DB_LUT_A_0	IF DSAQ LUT A Index 0. 1.5dB Range with 0.1dB Step, Used for IMR Calibration.	0x0	R/W
[3:0]	DSAI_0P1DB_LUT_A_0	IF DSAI LUT A Index 0. 1.5dB Range with 0.1dB Step, Used for IMR Calibration.	0x0	R/W

Address: 0x90C, Reset: 0x00, Name: REG090C

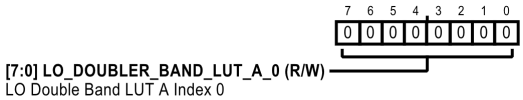

Figure 322.

Table 172. Bit Descriptions for REG090C

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_DOUBLER_BAND_LUT_A_0	LO Double Band LUT A Index 0. The enumeration values are general guidance. Adjust as needed to achieve system level spurious specifications. 0xC0: LO Frequency ≥ 24GHz. 0x80: 18GHz ≤ LO Frequency < 24GHz. 0x08: 14GHz ≤ LO Frequency < 18GHz. 0x04: 12GHz ≤ LO Frequency < 14GHz. 0x1D: 10GHz ≤ LO Frequency < 12GHz. 0x1F: LO Frequency < 10GHz.	0x0	R/W

Note: The Filter LUT A Index 1 to Gilter LUT B Index 31 bit fields functionality (Register 0x90D to Register 0xC3F) is identical to filter LUT A Index 0 bit fields functionality (Register 0x900 and Register 0x90C). See Table 27 for the register address information.

Address: 0xE00, Reset: 0x00, Name: REG0E00

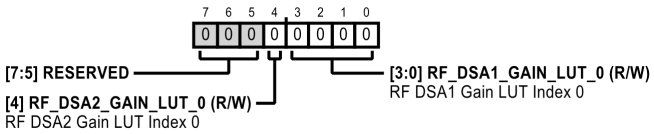

Figure 323.

Table 173. Bit Descriptions for REG0E00

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	RF_DSA2_GAIN_LUT_0	RF DSA2 Gain LUT Index 0. Provides gain range with single 1-bit gain step of 6dB.	0x0	R/W
[3:0]	RF_DSA1_GAIN_LUT_0	RF DSA1 Gain LUT Index 0. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB.	0x0	R/W

REGISTER DETAILS

Table 173. Bit Descriptions for REG0E00 (Continued)

Bits	Bit Name	Description	Reset	Access
		0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.		

Address: 0xE01, Reset: 0x00, Name: REG0E01

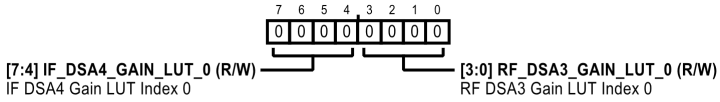

Figure 324.

Table 174. Bit Descriptions for REG0E01

Bits	Bit Name	Description	Reset	Access
[7:4]	IF_DSA4_GAIN_LUT_0	IF DSA4 Gain LUT Index 0. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.	0x0	R/W
[3:0]	RF_DSA3_GAIN_LUT_0	RF DSA3 Gain LUT Index 0. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB.	0x0	R/W

REGISTER DETAILS

Table 174. Bit Descriptions for REG0E01 (Continued)

Bits	Bit Name	Description	Reset	Access
		1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.		

Address: 0xE02, Reset: 0x00, Name: REG0E02

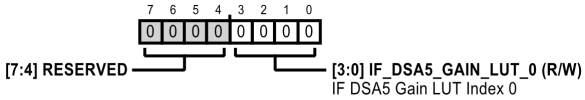

Figure 325.

Table 175. Bit Descriptions for REG0E02

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	IF_DSA5_GAIN_LUT_0	IF DSA5 Gain LUT Index 0. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1111: −14dB. 1110: −15dB.	0x0	R/W

Address: 0xE03, Reset: 0x00, Name: REG0E03

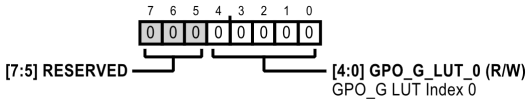

Figure 326.

Table 176. Bit Descriptions for REG0E03

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G_LUT_0	GPO_G LUT Index 0. Use this bit field to set the logic state of the GPO_G outputs.	0x0	R/W

REGISTER DETAILS

Note: The Gain LUT Index 1 to Gain LUT Index 66 bit fields functionality (Register 0xE04 to Register 0xF0B) is identical to gain LUT_0 bit fields functionality (Register 0xE00 and Register 0xE03). See Table 27 for the register address information.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
BC-120-4	CSP_BGA	120-Ball Chip Scale Package Ball Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV1455BBCZ	−40°C to +95°C	120-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	Pocket Tape	BC-120-4
ADMV1455BBCZ-R7	−40°C to +95°C	120-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	Reel, 500	BC-120-4

[1] Z = RoHS Compliant Part.