5.7 kV_{RMS} Isolated, Half-Duplex RS-485 Transceiver with Fault Protection

FEATURES

- 5.7kV_{RMS} isolated half-duplex RS-485/RS-422 transceiver
- ±60V fault protection on RS-485 A and B pins
- Meets EN 55032 Class B radiated emissions on a 2-layer PCB
- Robust protection on the RS-485 A and B bus pins
  - ≥ ±4kV IEC 61000-4-2 ESD
  - ±10kV HBM ESD
  - ≥ ±4kV IEC 61000-4-4 EFT
- Extended ±25V common-mode range
- Two speed options
  - ADM2495E - low speed 250kbps for EMI control
  - ADM2495E-1 - high speed 20Mbps data rate
- Flexible power supply inputs
  - Primary V_{DD1} supply of 1.7V to 5.5V
  - Isolated V_{DD2} supply of 3.0V to 5.5V
- PROFIBUS compliant for 5V V_{DD2}
- Wide operating temperature range: −40°C to +125°C
- High common-mode transient immunity: 250kV/µs
- Short-circuit, open-circuit, and floating input receiver fail-safe
- Supports >224 bus nodes (112kΩ receiver input impedance)
- Full hot-swap support (glitch free power-up/power-down)
- Safety and regulatory approvals
  - IEC 60747-17 (pending)
    - Reinforced V_{IORM} = 1500V_{PEAK}
  - UL 1577 (pending)
    - V_{ISO}= 5700V_{RMS} for 1 minute
  - IEC/EN/CSA 62368-1 (pending)
  - IEC/EN/CSA 61010-1 (pending)
  - IEC/CSA 60601-1 (pending)
  - GB 4943.1 (pending)
- Complies with ANSI/TIA/EIA-485-A-98 and ISO 8482:1987(E)
- 16-lead, wide body, standard SOIC_W package with 8.1 mm creepage and clearance in standard pinout

APPLICATIONS

- Solar inverters
- Electrical test and measurement
- Heating, ventilation, and air conditioning (HVAC) networks
- Industrial field buses
- Building automation

GENERAL DESCRIPTION

The ADM2495E/ADM2495E-1 are 5.7kV_{RMS}, signal isolated RS-485 transceivers with ±60V fault protection on the RS-485 A and B pins. These devices are designed for balanced transmission lines and comply with ANSI/TIA/EIA-485-A-98 and ISO 8482:1987(E). The devices can pass radiated emissions testing to the EN 55032 Class B standard with margin on a 2-layer printed circuit board (PCB) with high-frequency decoupling capacitors. The isolation barrier provides robust system level immunity to IEC 61000-4-x system level electromagnetic compatibility (EMC) standards. The devices are suitable for applications that require reinforced insulation against working voltages of 1060V_{RMS} and 1500V_{DC} for the lifetime of the device. The devices are protected against ±4kV contact IEC 61000-4-2 and ±15kV human body model (HBM) electrostatic discharge (ESD) events on the RS-485 A and B pins and ±8kV contact IEC 61000-4-2 ESD across the barrier without latch-up or damage.

The ADM2495E/ADM2495E-1 feature over voltage protection on the RS-485 A and B pins to withstand up to ±60V dc or ac peak to the transceiver side GND2. This allows for robust protection against transients and accidental connection to ±12V and ±24V power supplies. The common mode range of the device is extended to ±25V for applications with large ground offsets and long cable runs.

The ADM2495E/ADM2495E-1 are half-duplex transceivers. The ADM2495E has a reduced slew rate with 250kbps speed for operation over long cable runs with lower emissions. The ADM2495E-1 has a high 20Mbps data rate for maximum data transfer. The high differential output voltage makes these devices suitable for PROFIBUS® nodes when powered with 5V on the V_{DD2} supply. The V_{DD1} primary supply and V_{DD2} isolated supply both support a wide range of voltages (1.7V to 5.5V and 3.0V to 5.5V, respectively). The ADM2495E/ADM2495E-1 is available in the industry standard 16-lead, wide body, standard SOIC_W package with 8.1mm creepage and clearance.

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REVISION HISTORY

1/2025—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

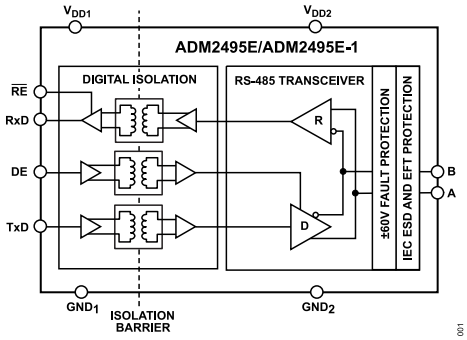

Figure 1. ADM2495E/ADM2495E-1

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to the respective ground, 1.7V ≤ V_{DD1} ≤ 5.5V, 3.0V ≤ V_{DD2} ≤ 5.5V, and T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C). All minimum and maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 3.3V, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PRIMARY SIDE SUPPLY CURRENT	I_{DD1}		5	10	mA	DE = V_{DD1}, TxD = GND_1
Quiescent	$I_{DD1 (Q)}$		0.65	1	mA	DE = GND_1, TxD = V_{DD1}
ISOLATED SIDE SUPPLY CURRENT	I_{DD2}					
ADM2495E			6	15	mA	DE = V_{DD1}
ADM2495E-1			6	10	mA	DE = V_{DD1}
Quiescent	$I_{DD2 (Q)}$		4	5	mA	DE = GND_1
ISOLATED SIDE DYNAMIC SUPPLY CURRENT	$I_{DD2 (DYN)}$					
ADM2495E			52	60	mA	V_{DD2} ≤ 3.6V, load resistance (R_L) = 54Ω, DE = V_{DD1}, $\overline{RE}$ = GND_1, data rate = 250kbps
			77	90	mA	V_{DD2} ≥ 4.5V, R_L = 54Ω, DE = V_{DD1}, $\overline{RE}$ = GND_1, data rate = 250kbps
ADM2495E-1			58	65	mA	V_{DD2} ≤ 3.6 V, R_L = 54Ω, DE = V_{DD1}, $\overline{RE}$ = GND_1, data rate = 20Mbps
			98	110	mA	V_{DD2} ≥ 4.5V, R_L = 54Ω, DE = V_{DD1}, $\overline{RE}$ = GND_1, data rate = 20Mbps
DRIVER						3.3V ≤ V_{DD2} ≤ 5.0V
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.0	2.1	V_{DD2}	V	R_L = 100Ω, see Figure 45
		1.5	1.8	V_{DD2}	V	R_L = 54Ω, see Figure 45
		2.1	3.0	V_{DD2}	V	4.5V ≤ V_{DD2} ≤ 5.0V, R_L = 54Ω, see Figure 45
Over Common-Mode Range	$\|V_{OD3}\|$	1.5	1.8	V_{DD2}	V	−7V ≤ common-mode voltage (V_{CM}) ≤ +12V, see Figure 46
		2.1	3.0	V_{DD2}	V	4.5V ≤ V_{DD2} ≤ 5.0V, −7V ≤ V_{CM} ≤ +12V, see Figure 46
$\Delta\|V_{OD2}\|$ for Complementary Output States	$\Delta\|V_{OD2}\|$			0.2	V	R_L = 54Ω or 100Ω, see Figure 45
Common-Mode Output Voltage	V_{OC}		1.5	3.0	V	R_L = 54Ω or 100Ω, see Figure 45
$\Delta\|V_{OC}\|$ for Complementary Output States	$\Delta\|V_{OC}\|$			0.2	V	R_L = 54Ω or 100Ω, see Figure 45
Short-Circuit Output Current	I_{OS}	−250		+250	mA	−60V < output voltage (V_{OUT}) < +60V
Pin Capacitance (A, B)	C_{IN}		50		pF	Input voltage (V_{IN}) = 0.4sin(10πt × 10^6)
RECEIVER						
Differential Input Threshold Voltage						−25V < V_{CM} < +25V
Positive Threshold	V_{TH+}		+125	+200	mV	
Negative Threshold	V_{TH-}	−200	−125	200	mV	
Failsafe Threshold	V_{TFS}	−200	−75	−10	mV	
Input Voltage Hysteresis	V_{HYS}		250		mV	V_{CM} = 0V
Failsafe Voltage Hysteresis	V_{HYS_FS}		50		mV	V_{CM} = 0V
Input Current (A, B)	I_I			143	µA	DE = GND_1, V_{DD2} = powered/unpowered, differential input voltage (V_{ID}) = 12V
		−100			µA	DE = GND_1, V_{DD2} = powered/unpowered, V_{ID} = −7V
Pin Capacitance (A, B)	C_{IN}		50		pF	V_{ID} = 0.4sin(10πt × 10^6)
DIGITAL LOGIC INPUTS						
Input Low Voltage	V_{IL}			0.3 × V_{DD1}	V	DE, $\overline{RE}$, and TxD
Input High Voltage	V_{IH}	0.7 × V_{DD1}			V	DE, $\overline{RE}$, and TxD
Input Current	I_{IN}	−1	+0.1	+2	µA	DE, $\overline{RE}$, TxD, V_{IN} = GND_1 or V_{DD1}
Input Capacitance[1]	C_{IN}		3.0		pF	Input capacitance

SPECIFICATIONS

Table 1. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RxD DIGITAL OUTPUT						
Output Voltage Low	V_{OL}			0.4	V	V_{DD1} = +3.6V, output current (I_{OUT}) = 2.0mA, V_{ID} ≤ −0.2V
				0.4	V	V_{DD1} = +2.7V, I_{OUT} = +1.0mA, V_{ID} ≤ −0.2V
				0.2	V	V_{DD1} = +1.95V, I_{OUT} = +500µA, V_{ID} ≤ −0.2V
Output Voltage High	V_{OH}	2.4			V	V_{DD1} = +3.0V, I_{OUT} = −2.0mA, V_{ID} ≥ +0.2V
		2.0			V	V_{DD1} = +2.3V, I_{OUT} = −1.0mA, V_{ID} ≥ +0.2V
		V_{DD1} − 0.2			V	V_{DD1} = +1.7V, I_{OUT} = −500µA, V_{ID} ≥ +0.2V
Three-State Output Leakage Current	I_{OZR}	−1	+0.01	+1	µA	$\overline{RE}$ = V_{DD1}, RxD = GND_1 or V_{DD1}
COMMON-MODE TRANSIENT IMMUNITY (CMTI)[2]	$\|CM_H\|$, $\|CM_L\|$	250			V/ns	V_{CM} ≥ ±1kV, transient magnitude measured between 20% and 80% of V_{CM}, see Figure 51 $\|CM_H\|$: TxD = V_{DD1}, $\|CM_L\|$: TxD = GND_1

[1] Input capacitance is from any input data pin to ground.

[2] The CMTI is the maximum common-mode voltage slew rate that can be sustained while maintaining specification compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to rising and falling common-mode voltage edges. Guaranteed by design and characterization, not tested in production.

TIMING SPECIFICATIONS

All minimum and maximum specifications apply over the entire recommended operation range, V_{DD1} = 1.7V to 5.5V, V_{DD2} = 3.0V to 5.5V, T_A = T_{MIN} (−40°C) to T_{MAX} (+125°C), unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 3.3V, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DRIVER - Slew Rate Limited (ADM2495E)						
Maximum Data Rate[1]		250			kbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		650	1200	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Pulse Width Distortion	t_{DPWD}		5	150	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Rise Time and Fall Time	t_{DR}, t_{DF}		750	1200	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Enable Time	t_{DZL}, t_{DZH}		400	1000	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 48
Disable Time	t_{DLZ}, t_{DHZ}		50	75	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 48
DRIVER - High Speed (ADM2495E-1)						
Maximum Data Rate[1]		20			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		40	50	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Pulse Width Distortion	t_{DPWD}		1.5	5	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Rise Time and Fall Time	t_{DR}, t_{DF}		10	20	ns	R_L = 54Ω, C_L = 100pF, see Figure 2 and Figure 47
Enable Time	t_{DZL}, t_{dZH}		35	50	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 48
Disable Time	t_{DLZ}, t_{DHZ}		50	66	ns	R_L = 110Ω, C_L = 50pF, see Figure 4 and Figure 48
RECEIVER - Slew Rate Limited (ADM2495E)						
Propagation Delay	t_{RPLH}, t_{RPHL}		400	700	ns	C_L = 15pF, see Figure 3 and Figure 49
Pulse Width Distortion	t_{RPWD}		5	30	ns	C_L = 15pF, see Figure 3 and Figure 49
Failsafe Enter Delay	t_{PFSN}		1.5	2.5	µs	C_L = 15pF, see Figure 6 and Figure 52
Failsafe Exit Delay	t_{PFSX}		0.7	1.2	µs	C_L = 15pF, see Figure 6 and Figure 52
Enable Time	t_{RZL}, t_{RZH}		10	30	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 50
Disable Time	t_{RLZ}, t_{RHZ}		20	40	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 50
RECEIVER - High Speed (ADM2495E-1)						
Propagation Delay	t_{RPLH}, t_{RPHL}		60	70	ns	C_L = 15pF, see Figure 3 and Figure 49

SPECIFICATIONS

Table 2. Timing Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width Distortion	t_{RPWD}		2.5	5	ns	C_L = 15pF, see Figure 3 and Figure 49
Failsafe Enter Delay	t_{PFSN}		110	125	ns	C_L = 15pF, see Figure 6 and Figure 52
Failsafe Exit Delay	t_{PFSX}		60	70	ns	C_L = 15pF, see Figure 6and Figure 52
Enable Time	t_{RZL}, t_{RZH}		10	15	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 50
Disable Time	t_{RLZ}, t_{RHZ}		20	25	ns	R_L = 1kΩ, C_L = 15pF, see Figure 5 and Figure 50

[1] Maximum data rate assumes a ratio of t_{DR}:t_{BIT}:t_{DF} equal to 1:1:1, where t_{BIT} is the time duration at which a bit is settled at >90% of the signal amplitude.

TIMING DIAGRAMS

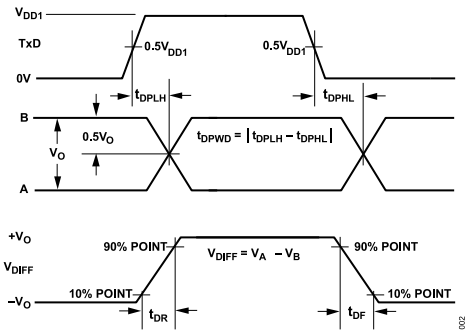

Figure 2. Driver Propagation Delay, Rise and Fall Timing

For test circuit of Figure 2, see Figure 47.

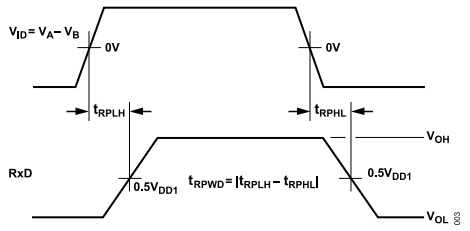

Figure 3. Receiver Propagation Delay

For test circuit of Figure 3, see Figure 49.

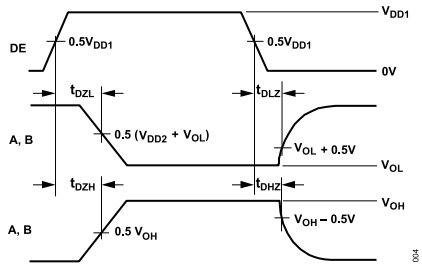

Figure 4. Driver Enable or Disable Timing

For test circuit of Figure 4, see Figure 48.

SPECIFICATIONS

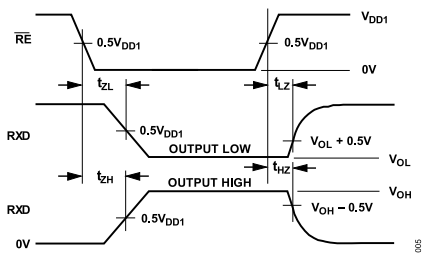

Figure 5. Receiver Enable or Disable Timing

For test circuit of Figure 5, see Figure 50.

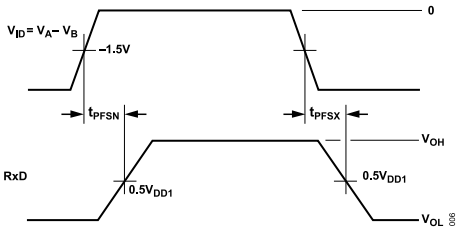

Figure 6. Failsafe Entry or Exit Delay Timing

For test circuit of Figure 6, see Figure 52.

INSULATION SPECIFICATIONS

The ADM2495E/ADM2495E-1 are suitable for safe electrical insulation only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 3. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	8.1	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	8.1	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Distance Through Insulation	DTI	42	µm	Minimum internal
Comparative tracking index	CTI	> 600	V	Per IEC 60112
Material Group		I		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤600V_{RMS}
		I to III		Rated mains voltage ≤1000V_{RMS}
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Total Power Dissipation	P_{TOT}	1.9	W	T_A=25°C , P_{TOT} = P_{SI} = P_{SO}
Derating Above Ambient (T_A)		15.6	mW/°C	T_A > 25°C, see Figure 7
Junction-to-Air Thermal Impedance	θ_{JA}	63.9	°C/W	See Table 6
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	1500	V_{PEAK}	
Maximum Isolation Working Voltage	V_{IOWM}	1060	V_{RMS}	AC voltage, end of life test, f = 60Hz
		1500	V_{PEAK}	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	8000	V_{PEAK}	V_{TEST} = 1.2 × V_{IOTM}, t =1s (100% production)
Maximum Impulse Voltage	V_{IMP}	8000	V_{PEAK}	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10400	V_{PEAK}	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5

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Table 3. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) Insulation Characteristics (Continued)

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Apparent Charge	q_{pd}	≤5	pC	Method a (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s Method b1 (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s
Resistance (Input to Output)[1]	R_{IO}	$>10^{12}$	Ω	T_A = 25°C, V_{TEST} = 500V_{DC}, t = 60s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500V_{DC}, t = 60s
Capacitance (Input to Output)[1]	C_{I-O}	2.2	pF	f_{TEST} = 1MHz
Climatic Category		40/125/21		
Pollution Degree		2		Per DIN VDE V 0110, Table 1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	5700	V_{RMS}	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 8 connected and Pin 9 to Pin 16 connected.

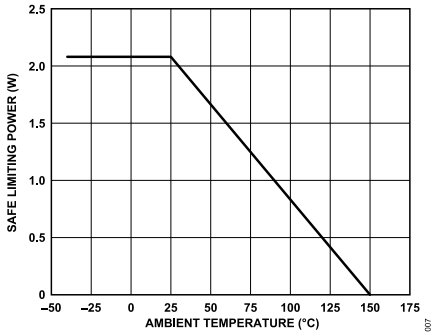

Figure 7. Thermal Derating Curve for 16-Lead Wide-body SOIC [SOIC_W] (RW-16), Dependence of Safety Limiting Values with Ambient Temperature per IEC60747-17

REGULATORY INFORMATION

The ADM2495E/ADM2495E-1 have been approved by the organizations listed in Table 4. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 4. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) Package Certifications

Regulatory Agency	Safety Standard/Rating	Certificate Number
UL	UL 1577 component recognition program Single / Basic protection, 5700V_{RMS} Isolation Voltage	(Pending)
CSA[1]	CSA No 14-18 CSA/EN/IEC 62368-1: Basic insulation at 810V_{RMS} Reinforced insulation at 405V_{RMS} CSA/EN/IEC 61010-1: Basic insulation at 600V_{RMS} from mains Reinforced insulation at 300V_{RMS} from mains CSA/IEC 60601-1: 1x MOPP 506V_{RMS} 2x MOPP 50V_{RMS}	(Pending)
VDE	IEC 60747-17: Reinforced insulation, 1500V_{PEAK}	(Pending)
CQC	GB4943.1: Reinforced insulation at 300V_{RMS} maximum working voltage, tropical climate, altitude ≤ 5000m	(Pending)

SPECIFICATIONS

Table 4. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) Package Certifications (Continued)

Regulatory Agency	Safety Standard/Rating	Certificate Number
TUV Sud	IEN/IEC 62368-1: Basic insulation at 810V_{RMS} Reinforced insulation at 405V_{RMS} EN/IEC 61010-1: Basic insulation at 600V_{RMS} from mains Reinforced insulation at 300V_{RMS} from mains	(Pending)

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADM2495E/ADM2495E-1 case material has been evaluated by CSA as Material Group I.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5. Absolute Maximum Ratings

Parameter	Rating
V_{DD1} to GND_1	−0.5V to +7.0V
V_{DD2} to GND_2	−0.5V to +6.0V
Digital Input Voltage (DE, $\overline{RE}$, TxD) to GND_1	−0.3V to V_{DD1} + 0.3V
Digital Output Voltage (RxD) to GND_1	−0.3V to V_{DD1} + 0.3V
Driver Output/Receiver Input Voltage (A,B) to GND_2	−60V to +60V
Temperature	
Ambient Operating Range (T_A)	−40°C to +125°C
Storage Range	−55°C to +150°C
Lead	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to PCB design and operating environment. Careful attention to the PCB thermal design is required.

Thermal resistance values specified in Table 6 are calculated based on the JEDEC specifications. For more details, see JEDEC JESD51-12.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
RW-16[1]	63.9	38.8	39.3	4.25	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test (DUT) or directly on the package top surface operating in the system environment is available, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the worst-case junction temperature in the system environment.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

Table 7. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) ESD Characteristics

Model	Withstand Threshold (V)	Class
HBM	≥ ±4000	3A[1]
	±10,000	3B[2]
CDM	1,250	C5[1]
IEC	≥ ±4kV (contact) to GND_2	Level 2[2]
	≥ ±8kV (contact) to GND_1	Level 4[2, 3]

[1] Pins V_{DD1}, V_{DD2}, RxD, DE, $\overline{RE}$, and TxD only.

[2] Pins A and B only.

[3] Limited by clearance across isolation barrier.

Electrical Fast Transients (EFT) Ratings

International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-4 (IEC) per IEC 61000-4-4.

Table 8. ADM2495E/ADM2495E-1, 16-Lead Wide-body SOIC [SOIC_W] (RW-16) EFT Characteristics

Model	Withstand Threshold (kV)	Repetition Frequency (kHz)	Class
IEC	≥± 4 to GND_2	5 or 100	exceeds Level 4[1]
	≥± 4 to GND_1	5 or 100	exceeds Level 4[1, 2]

[1] Pin A and Pin B only.

[2] Limited by clearance across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

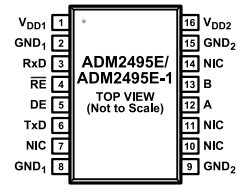

Figure 8. ADM2495E/ADM2495E-1 Pin Configuration

Table 9. ADM2495E/ADM2495E-1 Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{DD1}	1.7V to 5.5V Flexible Primary Side Power Supply. It is recommended that a 0.1µF decoupling capacitor be connected between V_{DD1} and GND_1 (Pin 1, Pin 2) to decouple the supply. An additional 10µF reservoir capacitor may be connected between V_{DD1} and GND_1 to improve noise immunity in noisy environments.
2, 8	GND_1	Ground 1, Logic Side.
3	RxD	Receiver Output Data. When the receiver is enabled ($\overline{RE}$ low) this output is high when (A − B) ≥ +200mV and low when (A − B) ≤ −200mV. This output is high when the receiver inputs are shorted, open or connected to a terminated idle bus. This output is tristated when the receiver is disabled by driving the $\overline{RE}$ pin high.
4	$\overline{RE}$	Receiver Enable Input. This pin is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places these outputs in a high impedance state.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
7, 10, 11, 14	NIC	Not Internally Connected. This pin is not internally connected and may be left open.
9, 15	GND_2	Isolated Ground 2 for the Integrated RS-485 Transceiver, Bus Side.
12	A	Noninverting Driver Output/Receiver Input.
13	B	Inverting Driver Output/Receiver Input.
16	V_{DD2}	3.0V to 5.5V Isolated Side Power Supply. Connect decoupling capacitors of 2.2pF and 0.1µF between V_{DD2} and GND_2 to decouple the supply. The 2.2pF capacitor must have a self-resonant frequency above 5GHz and be placed <2mm from V_{DD2} and GND_2. An additional 10µF reservoir capacitor may be connected between V_{DD2} and GND_2 to improve noise immunity in noisy environments.

TYPICAL PERFORMANCE CHARACTERISTICS

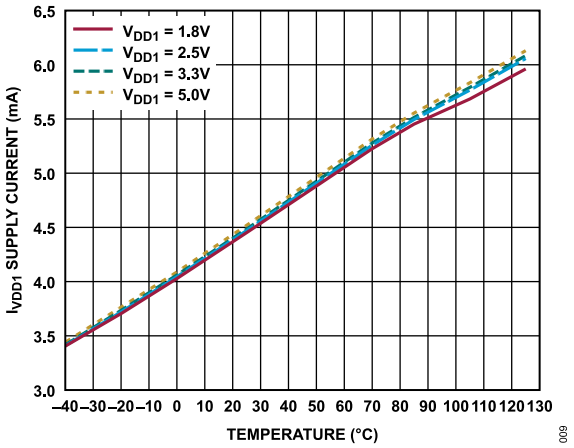

Figure 9. V_{DD1} Supply Current vs. Temperature at 250kbps (ADM2495E)

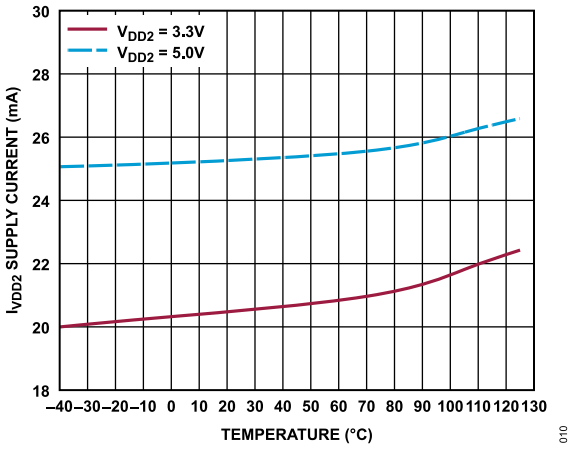

Figure 10. V_{DD2} Supply Current vs. Temperature at 250kbps (ADM2495E), Unterminated Bus

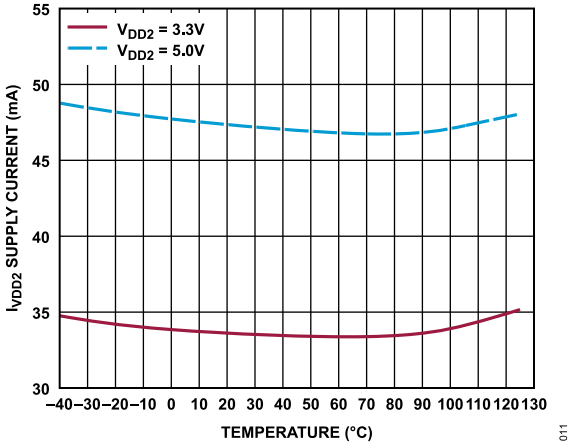

Figure 11. V_{DD2} Supply Current vs. Temperature at 250kbps (ADM2495E), 120Ω Termination

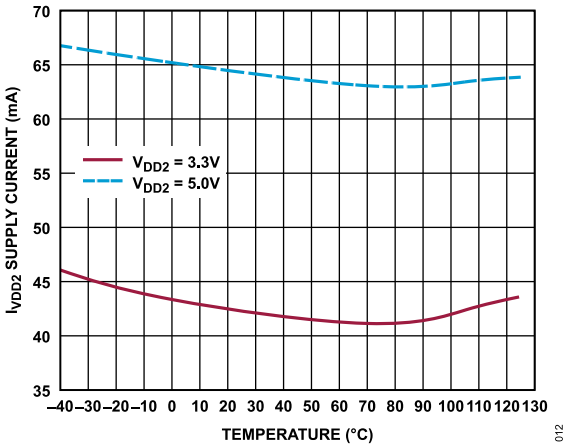

Figure 12. V_{DD2} Supply Current vs. Temperature at 250kbps (ADM2495E), 54Ω Termination

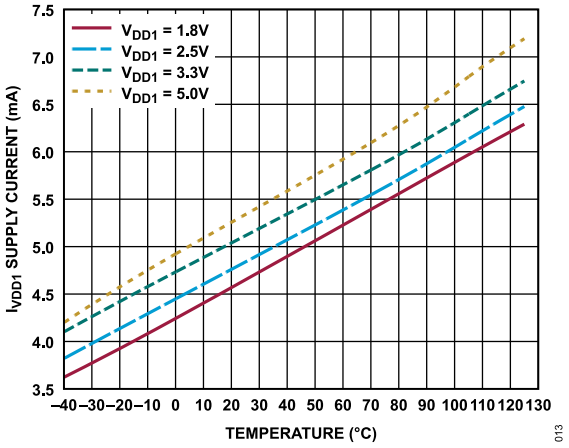

Figure 13. V_{DD1} Supply Current vs. Temperature at 20Mbps (ADM2495E-1)

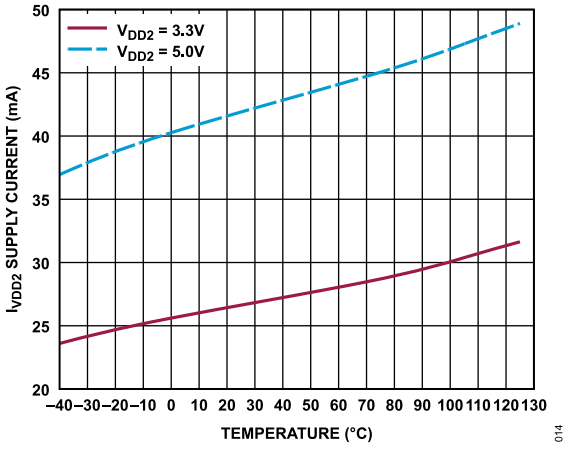

Figure 14. V_{DD2} Supply Current vs. Temperature at 20Mbps (ADM2495E-1), Unterminated Bus

TYPICAL PERFORMANCE CHARACTERISTICS

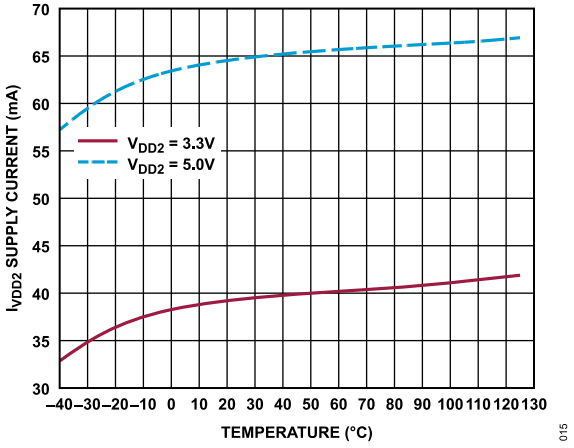

Figure 15. V_{DD2} Supply Current vs. Temperature at 20Mbps (ADM2495E-1), 120Ω Termination

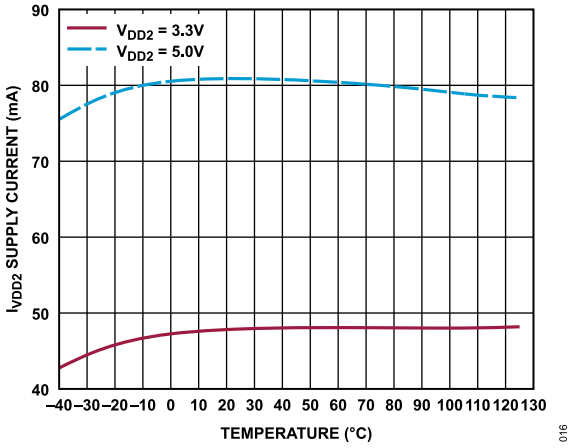

Figure 16. V_{DD2} Supply Current vs. Temperature at 20Mbps (ADM2495E-1), 54Ω Termination

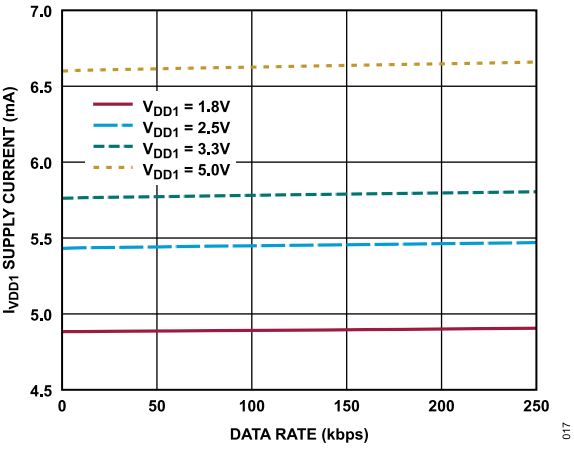

Figure 17. V_{DD1} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E)

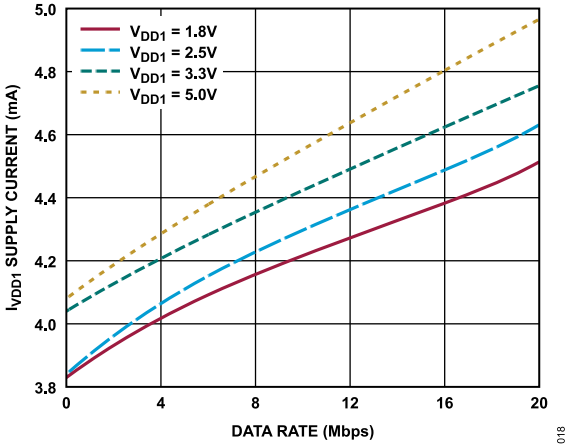

Figure 18. V_{DD1} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), Linear Scale

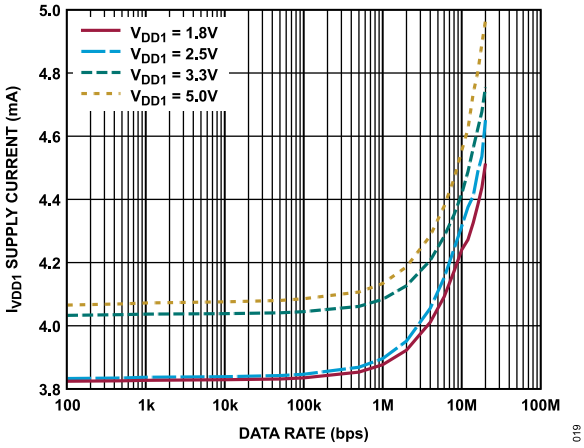

Figure 19. V_{DD1} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), Logarithmic Scale

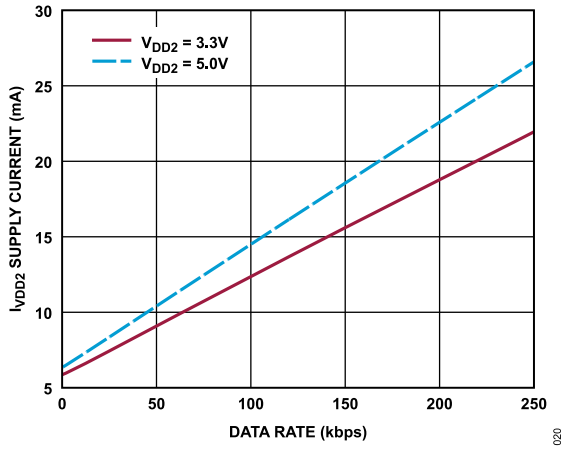

Figure 20. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E), Unterminated Bus

TYPICAL PERFORMANCE CHARACTERISTICS

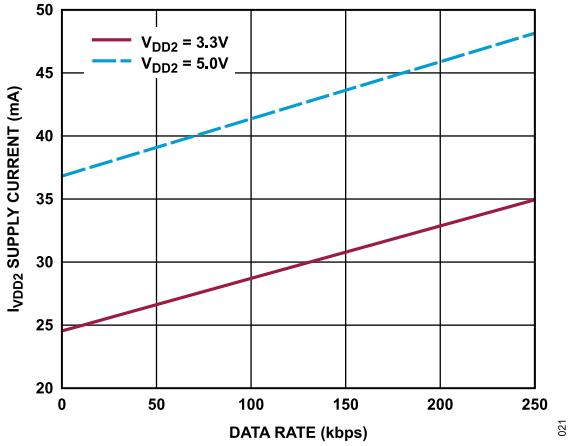

Figure 21. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E), 120Ω Termination

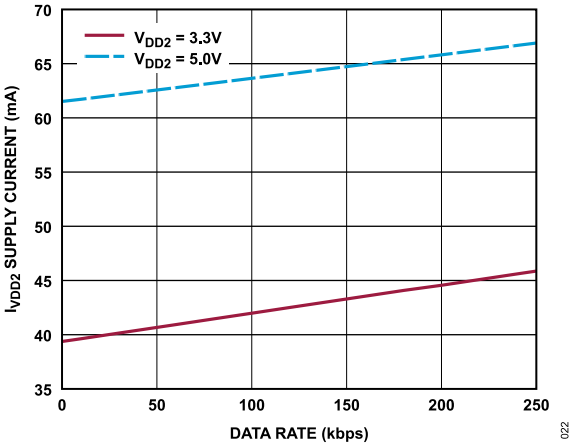

Figure 22. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E), 54Ω Termination

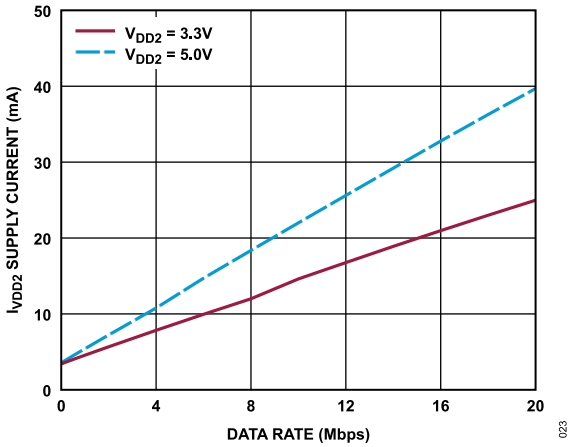

Figure 23. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), Unterminated Bus, Linear Scale

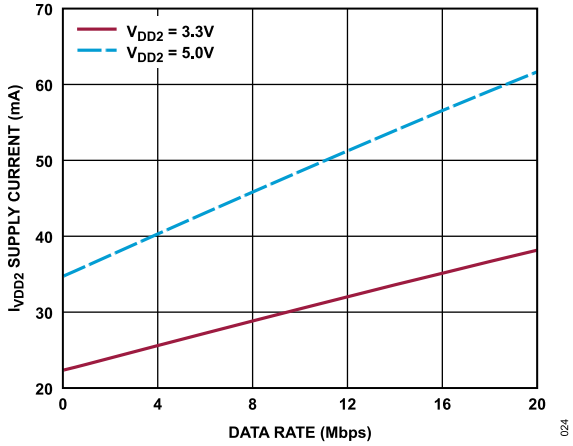

Figure 24. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), 120Ω Termination, Linear Scale

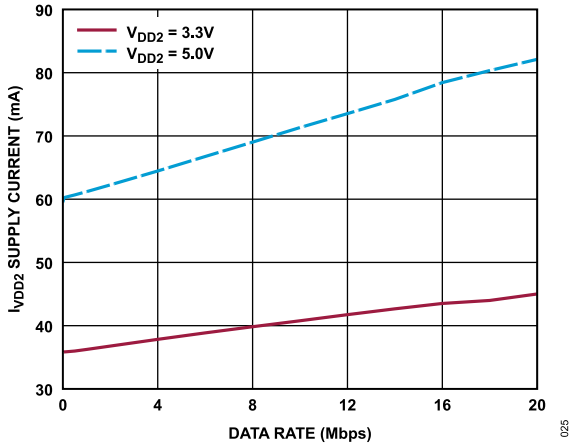

Figure 25. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), 54Ω Termination, Linear Scale

Figure 23. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), Unterminated Bus, Linear Scale

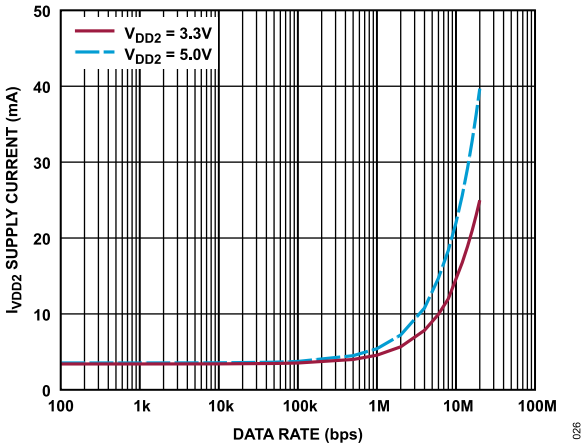

Figure 26. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), Unterminated Bus, Logarithmic Scale

TYPICAL PERFORMANCE CHARACTERISTICS

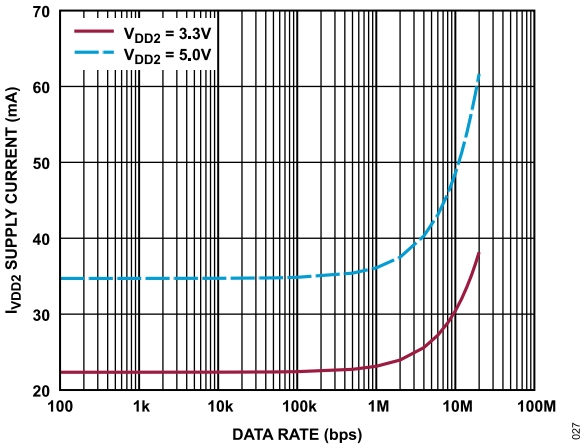

Figure 27. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), 120Ω Termination, Logarithmic Scale

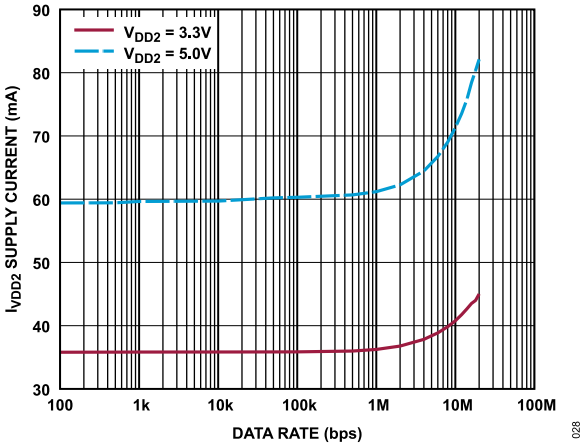

Figure 28. V_{DD2} Supply Current vs. Data Rate, T_A = 25°C (ADM2495E-1), 54Ω Termination, Logarithmic Scale

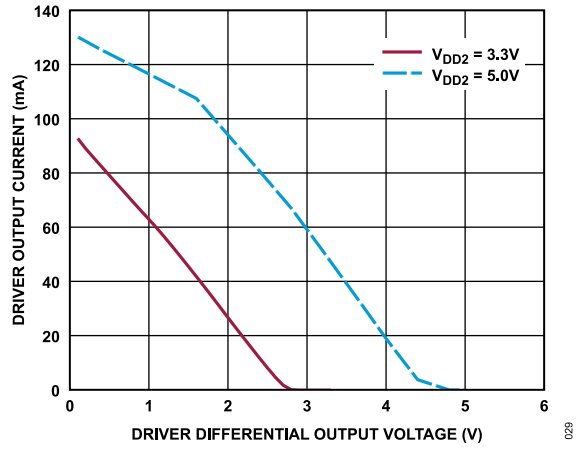

Figure 29. Driver Output Current vs. Driver Differential Output Voltage

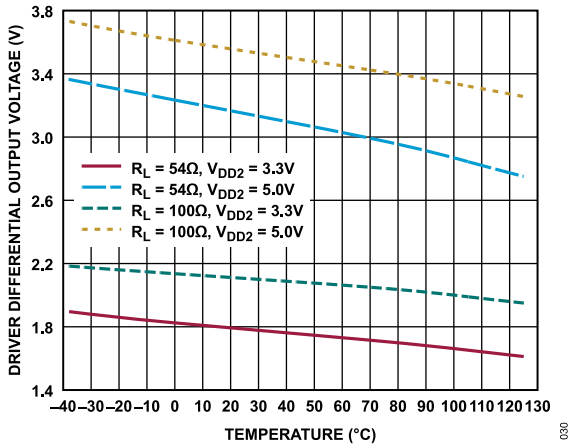

Figure 30. Driver Differential Output Voltage vs. Temperature

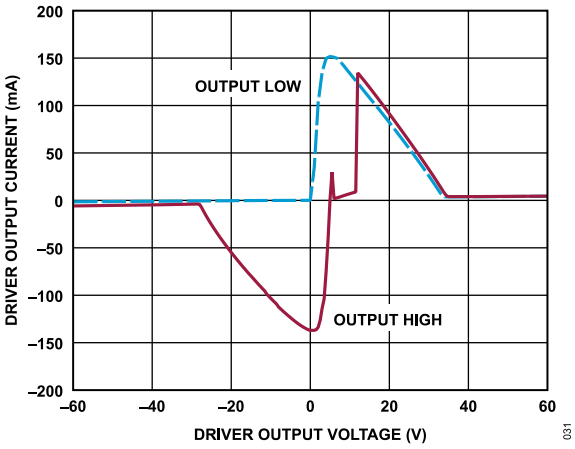

Figure 31. Driver Output Current vs. Driver Output Voltage

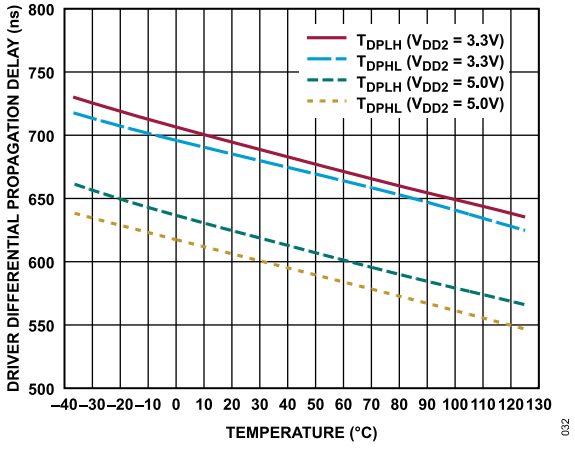

Figure 32. Driver Differential Propagation Delay vs. Temperature, 54Ω Termination (ADM2495E)

TYPICAL PERFORMANCE CHARACTERISTICS

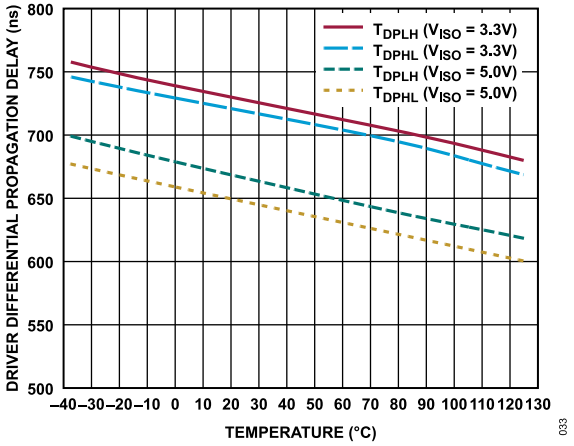

Figure 33. Driver Differential Propagation Delay vs. Temperature, 100Ω Termination (ADM2495E)

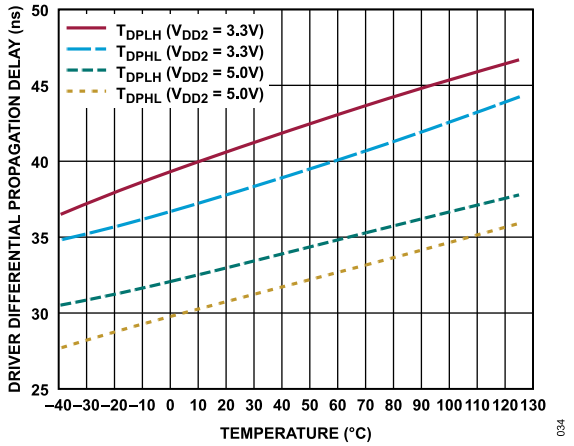

Figure 34. Driver Differential Propagation Delay vs. Temperature, 54Ω Termination (ADM2495E-1)

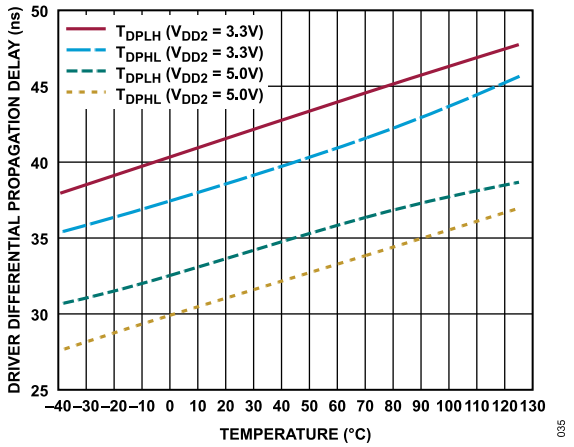

Figure 35. Driver Differential Propagation Delay vs. Temperature, 100Ω Termination (ADM2495E-1)

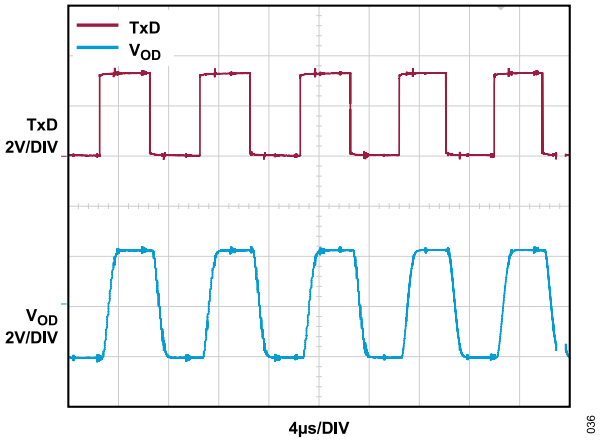

Figure 36. Driver Switching at 250kbps (ADM2495E)

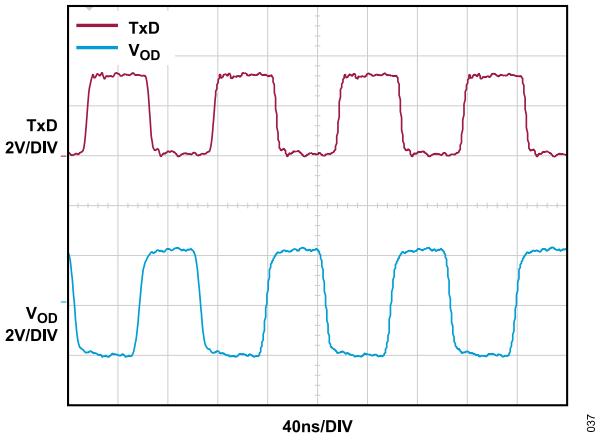

Figure 37. Driver Switching at 20Mbps (ADM2495E-1)

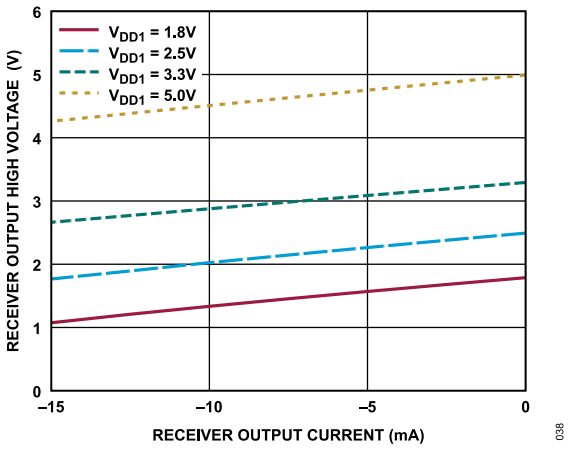

Figure 38. Receiver Output High Voltage vs. Receiver Output Current

TYPICAL PERFORMANCE CHARACTERISTICS

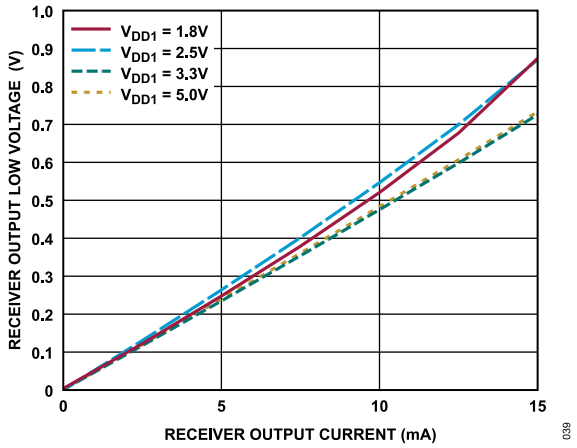

Figure 39. Receiver Output Low Voltage vs. Receiver Output Current

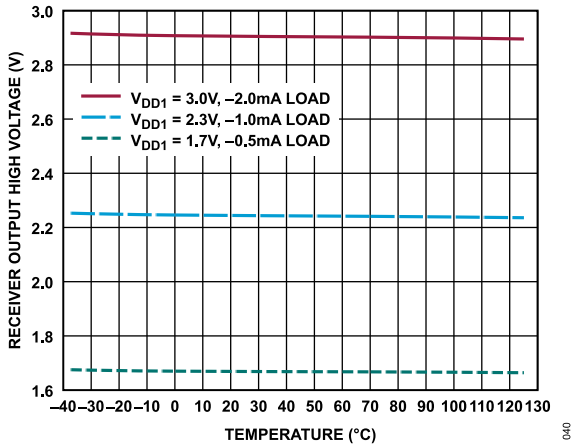

Figure 40. Receiver Output High Voltage vs. Temperature

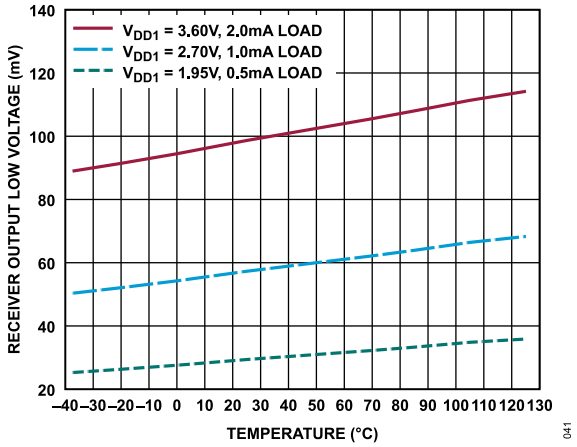

Figure 41. Receiver Output Low Voltage vs. Temperature

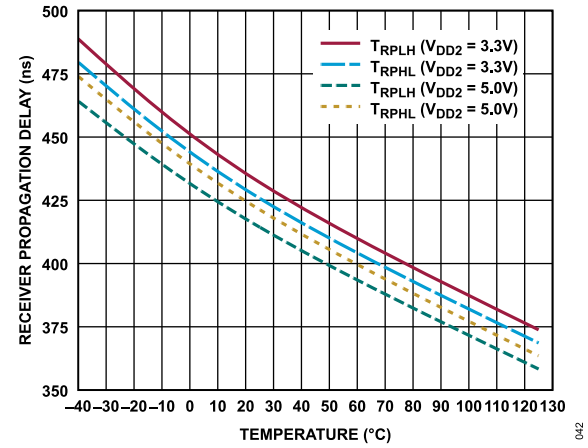

Figure 42. Receiver Propagation Delay vs. Temperature

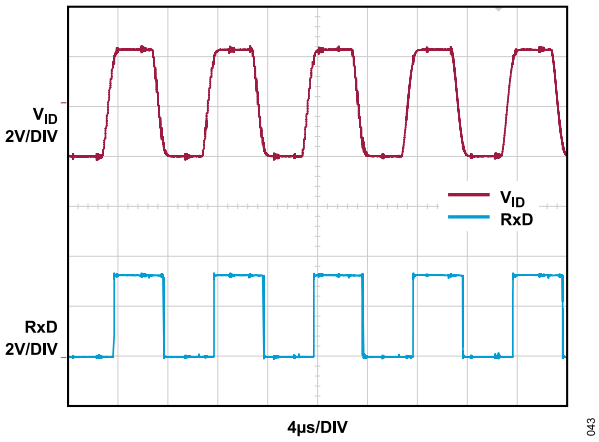

Figure 43. Receiver Switching at 250kbps (ADM2495E)

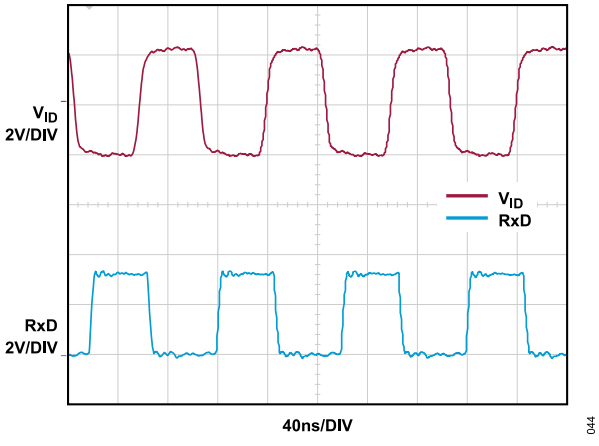

Figure 44. Receiver Switching at 20Mbps (ADM2495E-1)

TEST CIRCUITS

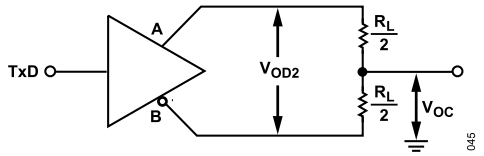

Figure 45. Driver Voltage Measurement, $|V_{OD2}|$

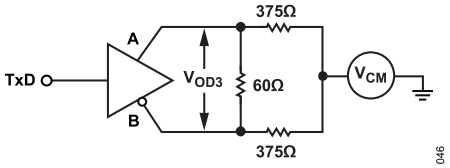

Figure 46. Driver Voltage Measurement over Common-Mode Range, $|V_{OD3}|$

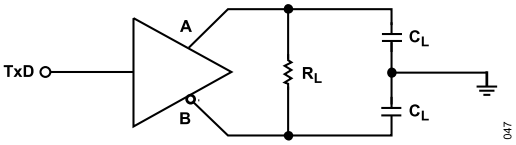

Figure 47. Driver Propagation Delay Measurement

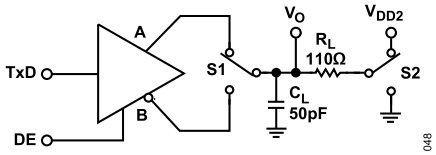

Figure 48. Driver Enable or Disable Time Measurement

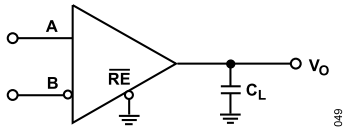

Figure 49. Receiver Propagation Delay Time Measurement

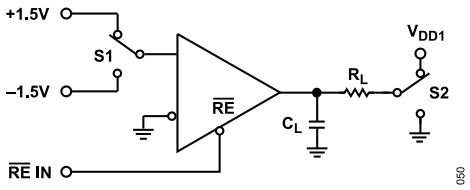

Figure 50. Receiver Enable or Disable Time Measurement

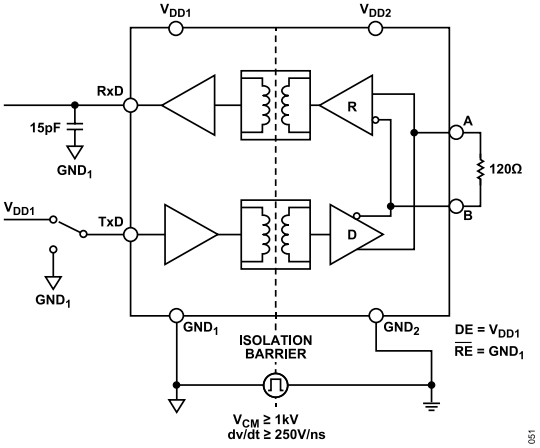

Figure 51. CMTI Test Diagram, Half-Duplex

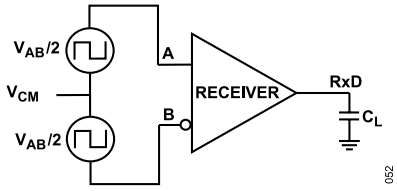

Figure 52. Failsafe Delay Measurement

THEORY OF OPERATION

ROBUST LOW POWER DIGITAL ISOLATOR

The ADM2495E/ADM2495E-1 feature a low power, digital isolator block to galvanically isolate the primary and secondary sides of the device. The use of coplanar transformer coils with an on-off keying (OOK) modulation scheme allows high data throughput across the isolation barrier while minimizing radiation emissions. This architecture provides a robust digital isolator with immunity to common-mode transients of greater than 250V/ns across the full temperature and supply range of the device. Figure 53 shows a repeated common-mode transients of 280V/ns being applied at different times relative to the TxD input transitioning from low to high while monitoring the resulting RxD output. The very small variation in the propagation delay and no errors demonstrate the robust CMTI performance of the device

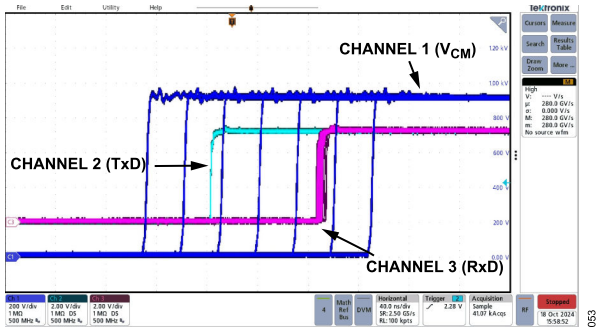

Figure 53. Switching Correctly in the Presence of >250kV/µs Common-Mode Transients

The digital isolator circuitry features a flexible V_{DD1} power supply with an input voltage range of 1.7V to 5.5V. This enables direct communications with logic devices utilizing 1.8V, 2.5V, 3.3V, or 5V supply voltages such as universal asynchronous receiver/transmitters (UARTs), application specific integrated circuits (ASICs), and microcontrollers.

ROBUST ±60V FAULT PROTECTION

The ADM2495E/ADM2495E-1 feature an improved overvoltage fault-tolerant RS-485/RS-422 transceiver, which may eliminate field failures due to overvoltage faults without using costly external protection devices. The ±60V fault tolerance on the A and B bus pins provides transceiver protection against field miswiring or cable faults to the common industrial 24V or 48V power supplies, which may be present in the cable.

The ±60V fault protection of the ADM2495E/ADM2495E-1 is achieved by using a high-voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered-off and high-impedance conditions. The driver outputs use a progressive foldback current limit design to protect against over voltage faults while still allowing high current output drive.

The high voltage rating of the ADM2495E/ADM2495E-1 makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage RS-485 transceivers, the ADM2495E/ADM2495E-1 allows the use of external protection devices with higher breakdown voltages, so as not to interfere with data transmission in the presence of large common-mode voltages.

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM2495E/ADM2495E-1 feature a proprietary transmitter architecture with a low-driver output impedance, which results in an increased driver differential output voltage. This architecture is particularly useful when operating the device over long cable runs, where the DC resistance of the transmission line dominates signal attenuation. In these applications, the increased differential voltage improves noise margin and allows transmission over longer cable lengths. In addition, when operated as a 5V transceiver (V_{DD2} > 4.5V), the ADM2495E/ADM2495E-1 meet or exceed the PROFIBUS requirement of a minimum 2.1V differential output voltage.

IEC61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. ESD has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. Air discharge testing is a more accurate representation of an actual ESD event than contact discharge but is not as repeatable. Therefore, contact discharge is the preferred test method. During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment. Figure 54 shows the 8kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1ns and pulse widths of approximately 60ns.

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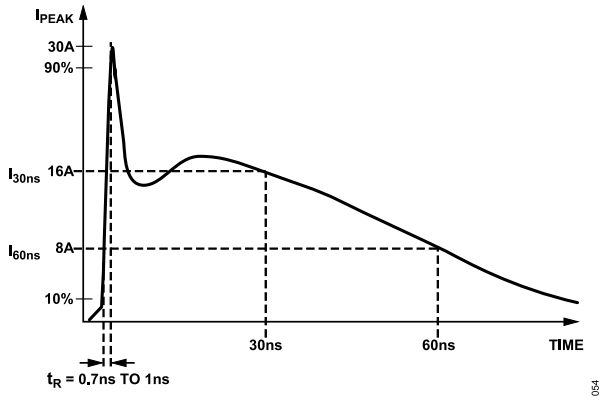

Figure 54. IEC61000-4-2 ESD Waveform (8kV)

Figure 55 shows the 8kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the HBM ESD 8kV waveform. Figure 55 shows that the two standards specify a different waveform shape and peak current (I_{PEAK}). The peak current associated with an IEC 61000-4-2 8kV pulse is 30A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1ns, compared to the 10ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, whereas in comparison, the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM2495E/ADM2495E-1 isolation barrier provides ±8kV contact protection between the bus pins and GND_1. These devices with IEC 61000-4-2 ESD ratings are better suited for operation in harsh environments when compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

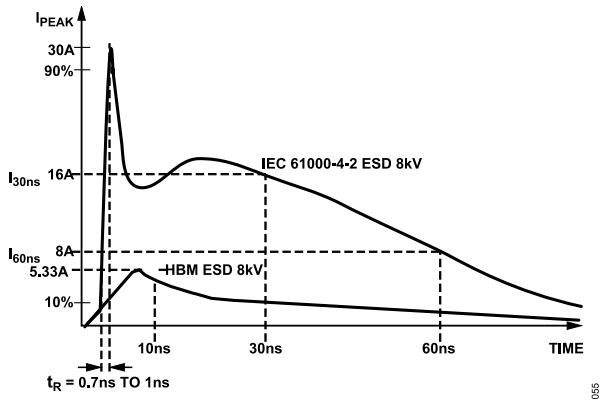

Figure 55. IEC61000-4-2 ESD 8kV Waveform Compared to HBM ESD 8kV Waveform

TRUTH TABLES

Table 11 and Table 12 use the abbreviations shown in Table 10. V_{DD1} supplies the DE, TxD, $\overline{RE}$ and RxD pins only.

Table 10. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Any state
Z	High impedance (off)
NC	Not connected

Table 11. Transmitting Truth Table

Supply Status		Inputs		Outputs	
V_{DD1}	V_{DD2}	DE	TxD	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
Off	On	X	X	Z	Z
X	Off	X	X	Z	Z

Table 12. Receiving Truth Table

Supply Status		Inputs		Outputs
V_{DD1}	V_{DD2}	A – B	$\overline{RE}$	RxD
On	On	≥−0.2 V	L	H
On	On	≤−0.2 V	L	L
On	On	−0.2 V < (A – B) < +0.2 V	L	I
On	On	Inputs open or shorted	L	H
On	X	X	H	Z
On	Off	X	L	I
Off	X	X	X	I

RECEIVER FAIL-SAFE

When the absolute value of the differential voltage between the A and B pins is greater than 200mV with the receiver enabled, the state of RO reflects the polarity of (A − B).

These parts have a fail-safe feature that guarantees the receiver output is in a logic 1 state (the idle state) when the inputs are shorted, left open, or terminated but not driven. The delay allows normal data signals to transition through the threshold region without being interpreted as a fail-safe condition. This fail-safe feature is guaranteed to work for inputs spanning the entire common-mode range of –25V to 25V.

Most competing devices achieve the fail-safe function by a simple negative offset of the input threshold voltage. This causes the receiver to interpret a zero differential voltage as a logic 1 state. The disadvantage of this approach is the input offset can introduce duty cycle asymmetry at the receiver output that becomes increasingly worse with low-input signal levels and slow-input edge rates.

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Other competing devices use internal biasing resistors to create a positive bias at the receiver inputs in the absence of an external signal. This type of fail-safe biasing is ineffective if the network lines are shorted, or if the network is terminated but not driven by an active transmitter.

The ADM2495E/ADM2495E-1 use a fully symmetric positive and negative receiver thresholds V_{TH-} and V_{TH+} (typically ±125 mV) to maintain good duty-cycle symmetry at low signal levels. The fail-safe operation is performed with a window comparator to determine when the differential input voltage falls above the V_{TFS} fail-safe threshold (typically –75 mV) but below the V_{TH+} threshold. If this condition persists for more than about 40ns for the ADM2495E-1 or 1.2µs for the ADM2495E, the fail-safe condition is asserted and the RxD pin is forced to the logic 1 state. This circuit provides full fail-safe operation and a large dynamic signal hysteresis of ~250mV between V_{TH-} and V_{TH+} with no negative impact to receiver duty-cycle symmetry, as shown in Figure 56. The input signal in Figure 56 is obtained by driving a 10Mbps RS-485 signal through 1000feet of cable, thereby attenuating it to a ±200mV signal with slow rise and fall times. Good duty-cycle symmetry is observed at RxD despite the degraded input signal.

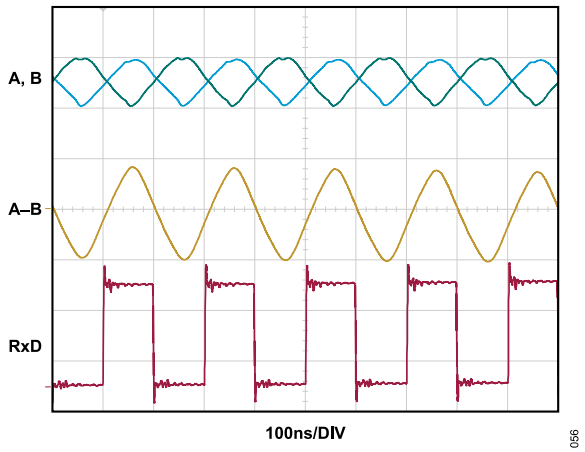

Figure 56. Duty Cycle of Balanced Receiver with ±200mV 10Mbps Input Signal

The fail-safe circuit has been enhanced with noise filtering to exit the fail-safe state. In the absence of noise filtering, a noise transient that momentarily forces the A − B differential voltage below the V_{TH-} receiver threshold causes the RxD output to go low, which may be interpreted as a false start character by the microcontroller. The ADM2495E/ADM2495E-1 receiver reduce these false signals by low pass filtering the signal to exit the fail-safe state. The noise filtering in the fail-safe circuit of the ADM2495E is much greater than in the ADM2495E-1, commensurate with its lower data rate. For example, the ADM2495E-1 exits the fail-safe state when a –1V differential pulse of about 3ns duration is applied, while the ADM2495E requires a –1V pulse of about 400ns duration to exit the fail-safe state. The minimum pulse widths to enter or exit the fail-safe state are not tested in production, but the underlying filtering is reflected in the t_{PFSN} and t_{PFSX} measurements.

These features are fully compatible with external fail-safe biasing configurations, which can be used in applications with legacy devices that lack fail-safe support, or in applications where additional noise margin is required. For more details on external fail-safe biasing, refer to the AN-960: *RS-485/RS-422 Circuit Implementation Guide*.

ENHANCED RECEIVER IMMUNITY

An additional benefit of the fully symmetric receiver thresholds is enhanced receiver noise immunity. The differential input signal must go above the positive threshold to register as a logic 1 and go below the negative threshold to register as a logic 0. This provides a hysteresis of 250mV (typical) at the receiver inputs for any valid data signal. An invalid data condition such as a DC sweep of the receiver inputs produces a different observed hysteresis due to the activation of the fail-safe circuit. Competing devices that employ a negative offset of the input threshold voltage generally have a much smaller hysteresis and subsequently have lower receiver noise immunity.

The ADM2495E provides additional noise immunity by adding low-pass filtering to the differential signal in its receiver. Commensurate with its maximum data rate of 250kbps, the ADM2495E receiver attenuates high frequency signals above approximately 660kHz. This low-pass filter removes high-frequency noise transients that might otherwise be interpreted as data. High-frequency noise filtering is not tested in production, but the underlying filtering is reflected in the t_{RPLH} and t_{RPHL} measurements.

HOT SWAP INPUTS

When a circuit board is inserted into a powered (or hot) backplane, parasitic coupling from supply and ground rails to digital inputs can occur. The ADM2495E/ADM2495E-1 contain circuitry to ensure that the RS-485 driver outputs remain in a high impedance state during power-up and then default to the correct states. For example, when V_{DD1} and V_{DD2} power up at the same time and the $\overline{RE}$ pin is pulled low with the DE and TxD pins pulled high, the A and B outputs remain in high impedance until settling at an expected default high state for the A pin and expected default low state for the B pin.

224 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12kΩ (1 unit load), and the standard driver can drive up to 32 unit loads. The ADM2495E/ADM2495E-1 transceiver have less than 1/7 unit load receiver input resistance, which allows over 224 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

DRIVER OUTPUT PROTECTION

The ADM2495E/ADM2495E-1 feature two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short-circuits over the entire

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common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs to a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature greater than 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

APPLICATIONS INFORMATION

PCB LAYOUT AND ELECTROMAGNETIC INTERFERENCE (EMI)

The ADM2495E/ADM2495E-1 use a low power, on or off keying encoding scheme with switching frequencies of approximately 3.8GHz and 4.2GHz for robust communication. These devices can be used in devices which meet EN 55032 or CISPR 32 Class B requirements with margin on a standard 2-layer PCB, without the need for complex and area intensive layout techniques.

Proper high-frequency decoupling can achieve compliance to EN 55032 Class B by placing a 2.2pF capacitor between the V_{DD2} and GND_2 pins. This capacitor must be located <2mm from the pins and must have a self-resonant frequency above 5GHz. Place the 10nF and optional 10µF capacitors next to the 2.2pF capacitor. Operation with data rates at or above 9.6kbps is recommended for increased margin to EN 55032 Class B limits.

ISOLATED PROFIBUS SOLUTION

The ADM2495E/ADM2495E-1 feature a driver that is well suited for meeting the requirements of an isolated PROFIBUS node. When operating the ADM2495E/ADM2495E-1 as a PROFIBUS transceiver, ensure that the V_{DD2} power supply is a minimum of 4.75V. The ADM2495E/ADM2495E-1 are acceptable for use in PROFIBUS applications because the output driver meets or exceeds the PROFIBUS differential output requirements. To ensure that the transmitter differential output does not exceed 7V p-p over all conditions, place 8.2Ω resistors in series with the A and B transmitter outputs.

ESD, EFT, AND SURGE

In applications where additional levels of protection against IEC 61000-4-2 ESD, IEC 61000-4-4 EFT, or IEC 61000-4-5 surge events are required, add the external protection circuits to further enhance the EMC robustness of these devices. For a recommended protection circuit, which uses a combination of 24V transient voltage suppressor (TVS) diodes and 10Ω pulse proof resistors to achieve in excess of Level 4 IEC 61000-4-2 ESD and IEC 61000-4-4 EFT protection, and Level 2 IEC 61000-4-5 surge protection while still utilizing the wide common-mode voltage range of the ADM2495E/ADM2495E-1, see Figure 57. Table 13 and Table 14 show the recommended components for protection and the protection levels.

Table 13. Recommended Components for ESD, EFT, and Surge Protection Solution

Recommended Components	Part Number
TVS	CDSOT23-T24C
10 Ω Pulse Proof Resistors	CRCW060310R0FKEAHP

Table 14. Protection Levels with Recommend Circuit

EMC Standard	Protection Level (kV)
ESD—Contact (IEC 61000-4-2)	≥±30 (exceeds Level 4)
ESD—Air (IEC 61000-4-2)	≥±30 (exceeds Level 4)
EFT (IEC 61000-4-4)	≥±4 (exceed s Level 4)
Surge (IEC 61000-4-5)	≥±1 (Level 2)

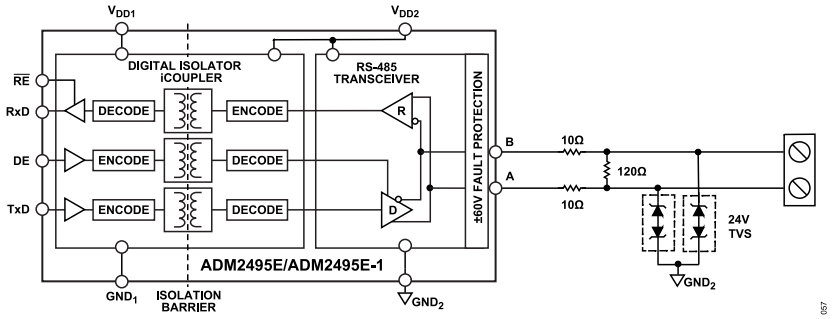

Figure 57. Isolated RS-485 Solution with ESD, EFT, and Surge Protection

TYPICAL APPLICATIONS

An example circuit using the ADM2495E/ADM2495E-1 as a half-duplex RS-485 node is shown in Figure 58. Placement of the termination resistor, R_T, is dependent on the location of the node and the network topology. For guidance on termination, refer to the AN-960: *RS-485/RS-422 Circuit Implementation Guide*. Up to 224 transceivers can be connected to the bus. To minimize reflections, terminate the line at the receiving end in its characteristic impedance and keep stub lengths off the main line as short as possible. For half-duplex operation, this means that both ends of the line must be terminated because either end can be the receiving end.

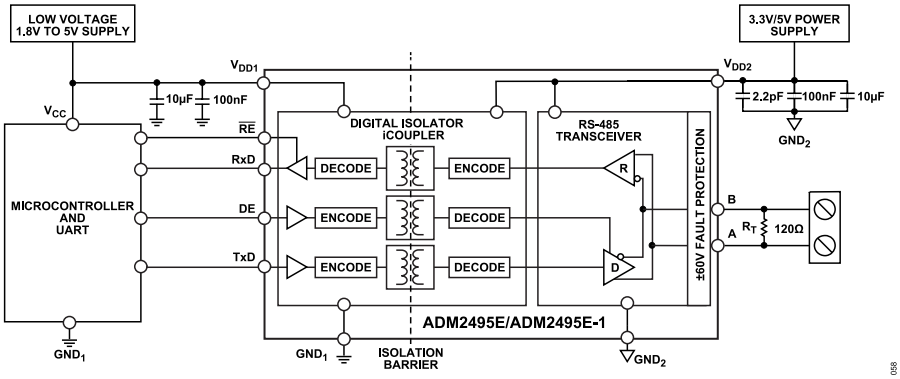

Figure 58. Example Circuit Diagram Using the ADM2495E/ADM2495E-1

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RW-16	SOIC_W	16-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADM2495EBRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	Tube, 47	RW-16
ADM2495EBRWZ-RL7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	Reel, 400	RW-16
ADM2495E-1BRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	Tube, 47	RW-16
ADM2495E-1BRWZ-RL7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	Reel, 400	RW-16

[1] Z=RoHS Compliant Part

Model[1]	Package Description
EVAL-ADM2495EEBZ	Evaluation Board

[1] Z=RoHS Compliant Part