

FEATURES

Provide programmable time delays between enable signals

Can be cascaded with power modules for multiple supply sequencing

Power supply monitoring from 0.6 V

Output stages

High voltage (up to 22 V) open-drain output (ADM1085/ADM1087)

Push-pull output (ADM1086/ADM1088)

Capacitor-adjustable time delays

High voltage (up to 22 V) enable and V_{IN} inputs

Low power consumption (15 μ A)

Specified over -40°C to $+125^{\circ}\text{C}$ temperature range

6-lead SC70 package

APPLICATIONS

Desktop/notebook computers, servers

Low power portable equipment

Routers

Base stations

Line cards

Graphics cards

GENERAL DESCRIPTION

The ADM1085/ADM1086/ADM1087/ADM1088 are simple sequencing circuits that provide a time delay between the enabling of voltage regulators and/or dc-dc converters at power-up in multiple supply systems. When the output voltage of the first power module reaches a preset threshold, a time delay is initiated before an enable signal allows subsequent regulators to power up. Any number of these devices can be cascaded with regulators to allow sequencing of multiple power supplies.

Threshold levels can be set with a pair of external resistors in a voltage divider configuration. With appropriate resistor values, the threshold can be adjusted to monitor voltages as low as 0.6 V.

The ADM1086 and ADM1088 have push-pull output stages, with active high (ENOUT) and active low ($\overline{\text{ENOUT}}$) logic outputs, respectively. The ADM1085 has an active-high (ENOUT) logic output; the ADM1087 has an active-low ($\overline{\text{ENOUT}}$) output. Both the ADM1085 and ADM1087 have open-drain output stages that can be pulled up to voltage levels as high as 22 V through an external resistor. This level-shifting property ensures compatibility with enable input logic levels of different regulators and converters.

Rev. A

[Document Feedback](#)

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

FUNCTIONAL BLOCK DIAGRAMS

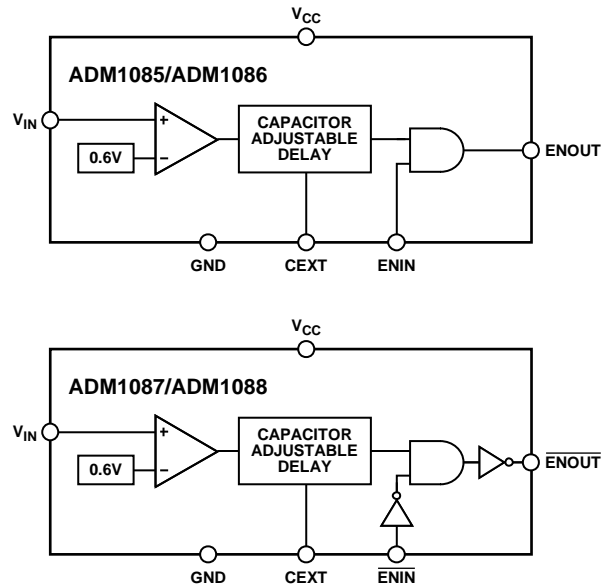


Figure 1.

04591-001

All four models have a dedicated enable input pin that allows the output signal to the regulator to be controlled externally. This is an active high input (ENIN) for the ADM1085 and ADM1086, and an active low input ($\overline{\text{ENIN}}$) for the ADM1087 and ADM1088.

The Simple Sequencers are specified over the extended -40°C to $+125^{\circ}\text{C}$ temperature range. With low current consumption of 15 μ A (typical) and 6-lead SC70 packaging, the parts are suitable for low-power portable applications.

Table 1. Selection Table

Part No.	Enable Input	Output Stage	
		$\overline{\text{ENOUT}}$	ENOUT
ADM1085	ENIN	Open-drain	Open-drain
ADM1086	ENIN		Push-pull
ADM1087	$\overline{\text{ENIN}}$	Open-drain	Push-pull
ADM1088	$\overline{\text{ENIN}}$	Push-pull	

TABLE OF CONTENTS

Features	1	Capacitor-Adjustable Delay Circuit.....	9
Applications.....	1	Open-Drain and Push-Pull Outputs	10
Functional Block Diagrams.....	1	Application Information.....	11
General Description	1	Sequencing Circuits	11
Revision History	2	Dual LOFO Sequencing	13
Specifications.....	3	Simultaneous Enabling.....	13
Absolute Maximum Ratings.....	4	Power Good Signal Delays.....	13
ESD Caution.....	4	Quad-Supply Power Good Indicator	14
Pin Configuration and Function Descriptions.....	5	Sequencing with FET Switches.....	14
Typical Performance Characteristics	6	Outline Dimensions	15
Circuit Information.....	9	Ordering Guide	15
Timing Characteristics and Truth Tables.....	9		

REVISION HISTORY

4/06—Rev. 0 to Rev. A

Added Lead-Free Models	Universal
Update Outline Dimensions	15
Changes to Ordering Guide	15

7/04—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, T_A = -40°C to $+125^{\circ}\text{C}$, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	2.25		3.6	V	
V_{IN} Operating Voltage Range	0		22	V	
Supply Current		10	15	μA	
V_{IN} Rising Threshold, V_{TH_RISING}	0.56	0.6	0.64	V	$V_{CC} = 3.3\text{ V}$
V_{IN} Falling Threshold, $V_{TH_FALLING}$	0.545	0.585	0.625	V	$V_{CC} = 3.3\text{ V}$
V_{IN} Hysteresis		15		mV	
V_{IN} to $\overline{\text{ENOUT}}/\overline{\text{ENOUT}}$ Delay					
V_{IN} Rising		35		μs	CEXT floating, $C = 20\text{ pF}$
		2		ms	CEXT = 470 pF
V_{IN} Falling		20		μs	$V_{IN} = V_{TH_FALLING}$ to $(V_{TH_FALLING} - 100\text{ mV})$
V_{IN} Leakage Current		170		μA	$V_{IN} = 22\text{ V}$
CEXT Charge Current	125	250	375	nA	
Threshold Temperature Coefficient		30		ppm/ $^{\circ}\text{C}$	
$\overline{\text{ENIN}}/\overline{\text{ENIN}}$ to $\overline{\text{ENOUT}}/\overline{\text{ENOUT}}$ Propagation Delay		0.5		μs	$V_{IN} > V_{TH_RISING}$
$\overline{\text{ENIN}}/\overline{\text{ENIN}}$ Voltage Low			$0.3 V_{CC} - 0.2$	V	
$\overline{\text{ENIN}}/\overline{\text{ENIN}}$ Voltage High	$0.3 V_{CC} + 0.2$			V	
$\overline{\text{ENIN}}/\overline{\text{ENIN}}$ Leakage Current		170		μA	$\overline{\text{ENIN}}/\overline{\text{ENIN}} = 22\text{ V}$
$\overline{\text{ENOUT}}/\overline{\text{ENOUT}}$ Voltage Low			0.4	V	$V_{IN} < V_{TH_FALLING}(\overline{\text{ENOUT}})$, $V_{IN} > V_{TH_RISING}(\overline{\text{ENOUT}})$, $I_{SINK} = 1.2\text{ mA}$
$\overline{\text{ENOUT}}/\overline{\text{ENOUT}}$ Voltage High (ADM1086/ADM1088)	$0.8 V_{CC}$			V	$V_{IN} > V_{TH_RISING}(\overline{\text{ENOUT}})$, $V_{IN} < V_{TH_FALLING}(\overline{\text{ENOUT}})$, $I_{SOURCE} = 500\text{ }\mu\text{A}$
$\overline{\text{ENOUT}}/\overline{\text{ENOUT}}$ Open-Drain Output Leakage Current (ADM1085/ADM1087)			0.4	μA	$\overline{\text{ENOUT}}/\overline{\text{ENOUT}} = 22\text{ V}$

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	–0.3 V to +6 V
V_{IN}	–0.3 V to +25 V
CEXT	–0.3 V to +6 V
ENIN, $\overline{\text{ENIN}}$	–0.3 V to +25 V
ENOUT, $\overline{\text{ENOUT}}$ (ADM1085, ADM1087)	–0.3 V to +25 V
ENOUT, $\overline{\text{ENOUT}}$ (ADM1086, ADM1088)	–0.3 V to +6 V
Operating Temperature Range	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
θ_{JA} Thermal Impedance, SC70	146°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

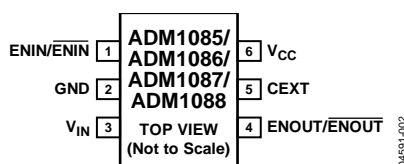


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ENIN, $\overline{\text{ENIN}}$	Enable Input. Controls the status of the enable output. Active high for ADM1085/ADM1086. Active low for ADM1087/ADM1088.
2	GND	Ground.
3	V_{IN}	Input for the Monitored Voltage Signal. Can be biased via a voltage divider resistor network to customize the effective input threshold. Can precisely monitor an analog power supply output signal and detect when it has powered up. The voltage applied at this pin is compared with a 0.6 V on-chip reference. With this reference, digital signals with various logic level thresholds can also be detected.
4	ENOUT, $\overline{\text{ENOUT}}$	Enable Output. Asserted when the voltage at V_{IN} is above $V_{\text{TH_RISING}}$ and the time delay has elapsed, provided that the enable input is asserted. Active high for the ADM1085/ADM1086. Active low for the ADM1087/ADM1088.
5	CEXT	External Capacitor Pin. The capacitance on this pin determines the time delay on the enable output. The delay is seen only when the voltage at V_{IN} rises past $V_{\text{TH_RISING}}$, and not when it falls below $V_{\text{TH_FALLING}}$.
6	V_{CC}	Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

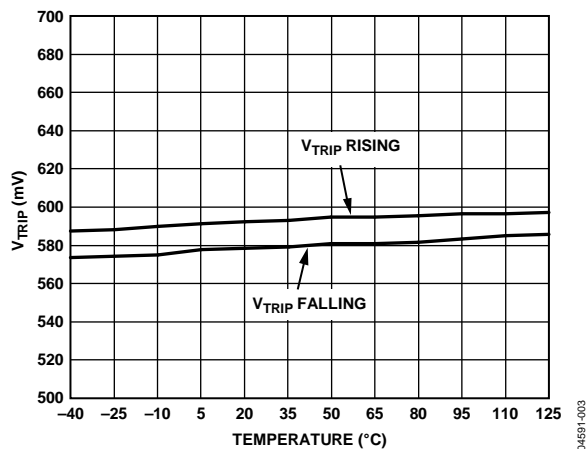


Figure 3. V_{IN} Threshold vs. Temperature

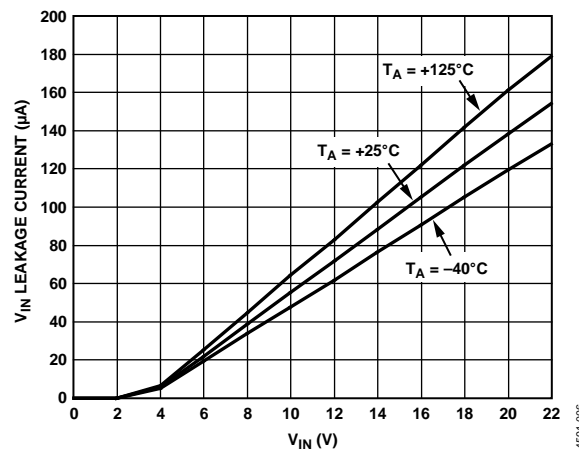


Figure 6. V_{IN} Leakage Current vs. V_{IN} Voltage

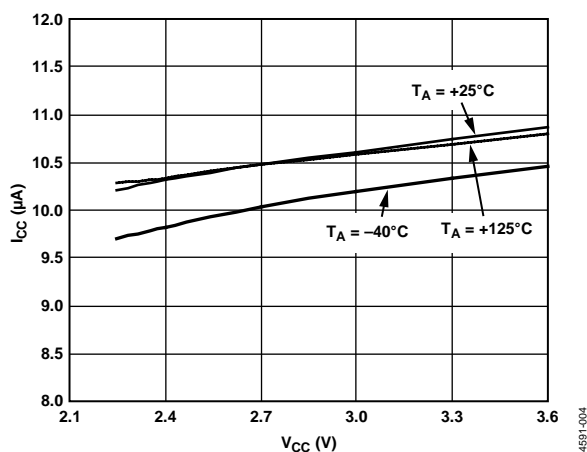


Figure 4. Supply Current vs. Supply Voltage

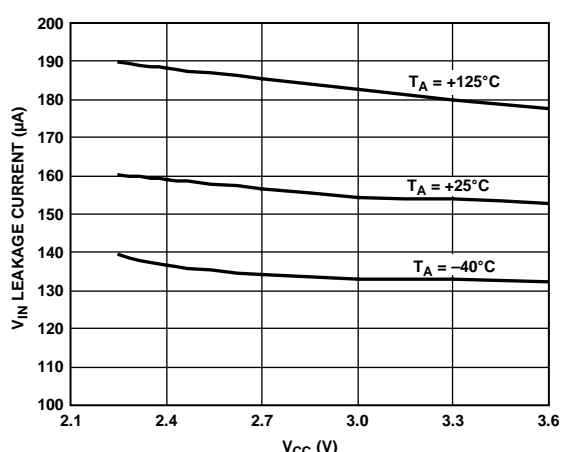


Figure 7. V_{IN} Leakage Current vs. V_{CC} Voltage

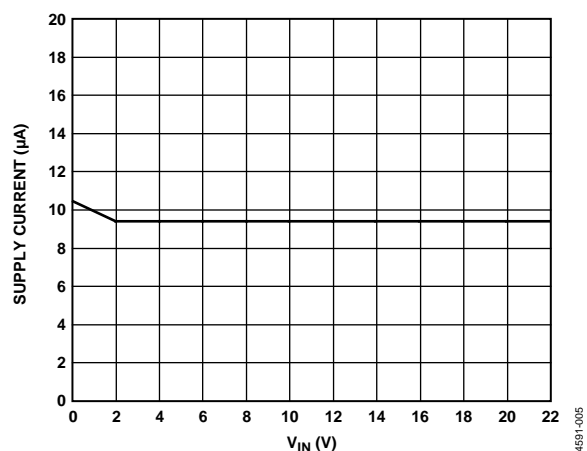


Figure 5. Supply Current vs. V_{IN} Voltage

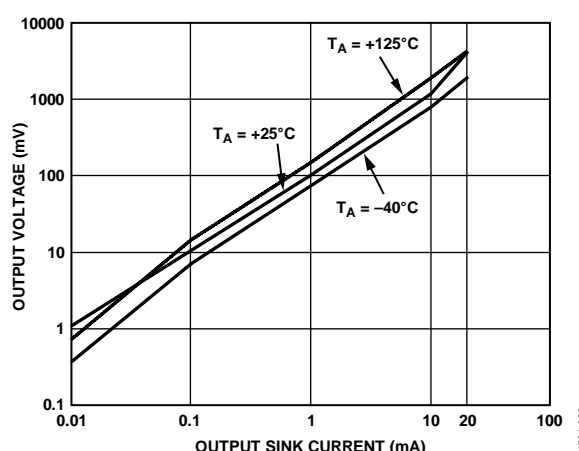


Figure 8. Output Voltage vs. Output Sink Current

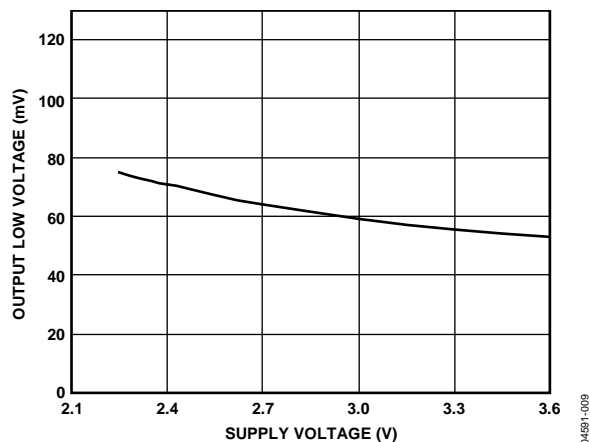


Figure 9. Output Low Voltage vs. Supply Voltage

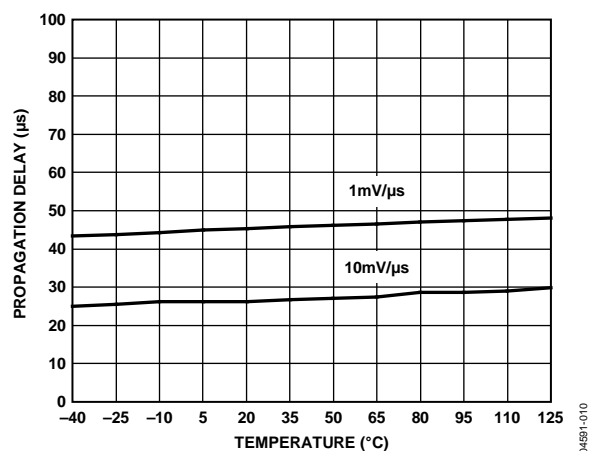
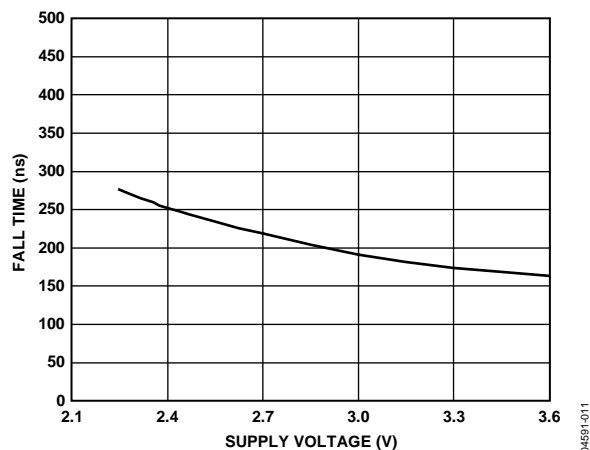
Figure 10. V_{CC} Falling Propagation Delay vs. Temperature

Figure 11. Output Fall Time vs. Supply Voltage

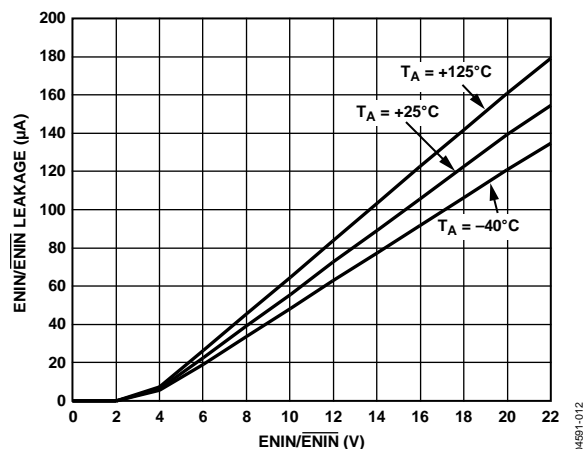
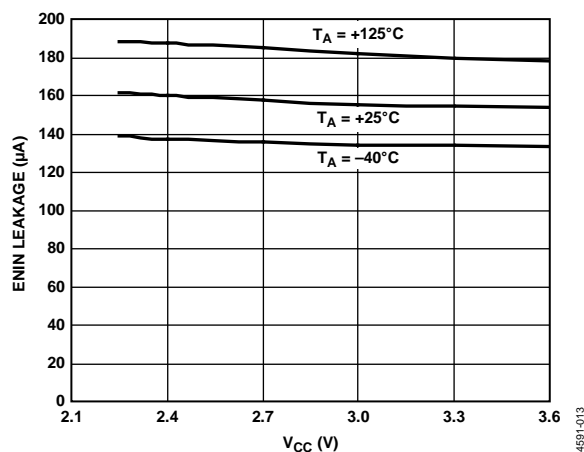
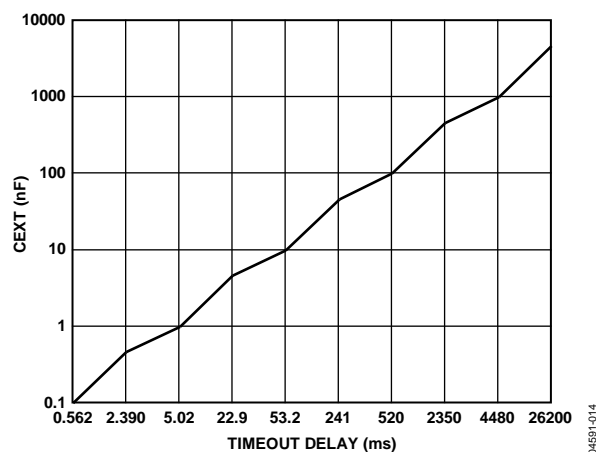
Figure 12. $\overline{\text{ENIN}}/\overline{\text{ENIN}}$ Leakage Current vs. $\overline{\text{ENIN}}/\overline{\text{ENIN}}$ VoltageFigure 13. $\overline{\text{ENIN}}/\overline{\text{ENIN}}$ Leakage Current vs. V_{CC} Voltage

Figure 14. CEXT Capacitance vs. Timeout Delay

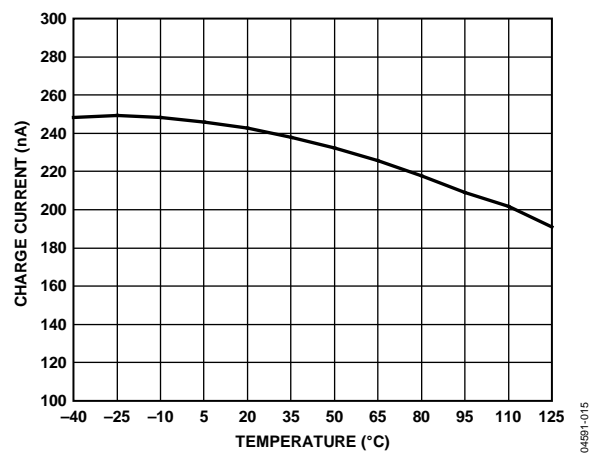


Figure 15. CEXT Charge Current vs. Temperature

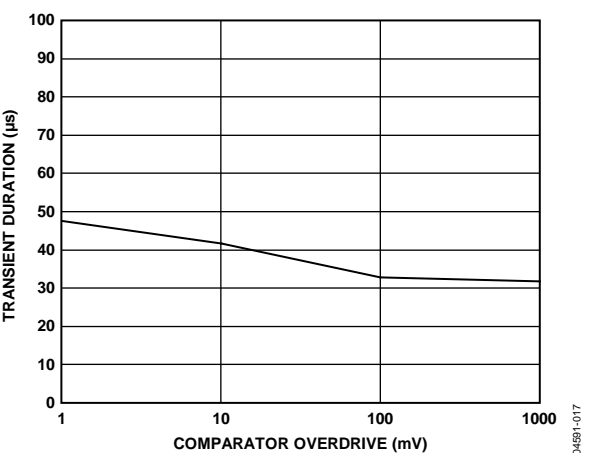


Figure 17. Maximum V_{IN} Transient Duration vs. Comparator Overdrive

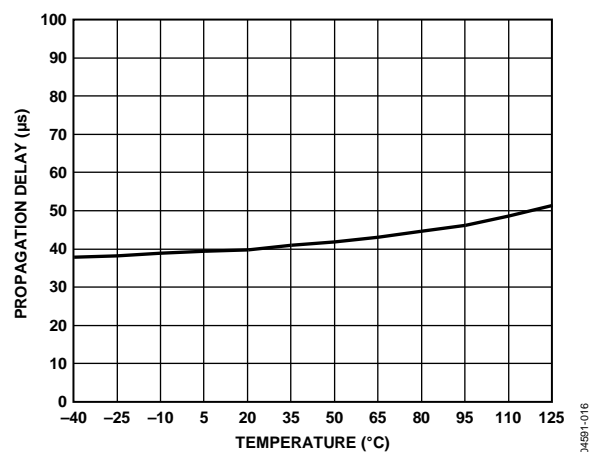


Figure 16. V_{IN} to $\overline{ENOUT}/\overline{ENOUT}$ Propagation Delay (CEXT Floating) vs. Temperature

CIRCUIT INFORMATION

TIMING CHARACTERISTICS AND TRUTH TABLES

The enable outputs of the ADM1085/ADM1086/ADM1087/ADM1088 are related to the V_{IN} and enable inputs by a simple AND function. The enable output is asserted only if the enable input is asserted and the voltage at V_{IN} is above V_{TH_RISING} , with the time delay elapsed. Table 5 and Table 6 show the enable output logic states for different V_{IN} /enable input combinations when the capacitor delay has elapsed. The timing diagrams in Figure 18 and Figure 19 give a graphical representation of how the ADM1085/ADM1086/ADM1087/ADM1088 enable outputs respond to V_{IN} and enable input signals.

Table 5. ADM1085/ADM1086 Truth Table

V_{IN}	ENIN	ENOUT
$<V_{TH_FALLING}$	0	0
$<V_{TH_FALLING}$	1	0
$>V_{TH_RISING}$	0	0
$>V_{TH_RISING}$	1	1

Table 6. ADM1087/ADM1088 Truth Table

V_{IN}	ENIN	ENOUT
$<V_{TH_FALLING}$	1	1
$<V_{TH_FALLING}$	0	1
$>V_{TH_RISING}$	1	1
$>V_{TH_RISING}$	0	0

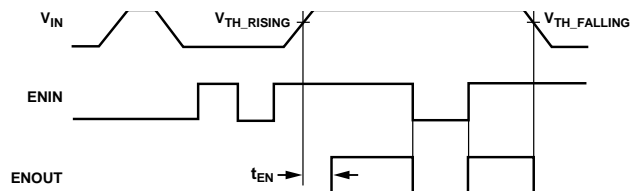


Figure 18. ADM1085/ADM1086 Timing Diagram

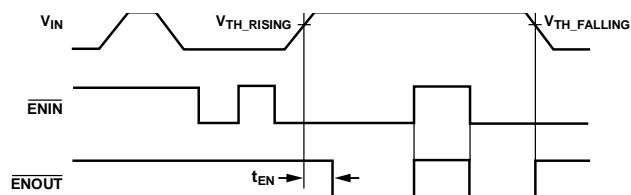


Figure 19. ADM1087/ADM1088 Timing Diagram

When V_{IN} reaches the upper threshold voltage (V_{TH_RISING}), an internal circuit generates a delay (t_{EN}) before the enable output is asserted. If V_{IN} drops below the lower threshold voltage ($V_{TH_FALLING}$), the enable output is deasserted immediately.

Similarly, if the enable input is disabled while V_{IN} is above the threshold, the enable output deasserts immediately. Unlike V_{IN} , a low-to-high transition on ENIN (or high-to-low on \overline{ENIN}) does not yield a time delay on ENOUT (\overline{ENOUT}).

CAPACITOR-ADJUSTABLE DELAY CIRCUIT

Figure 20 shows the internal circuitry used to generate the time delay on the enable output. A 250 nA current source charges a small internal parasitic capacitance (C_{INT}). When the capacitor voltage reaches 1.2 V, the enable output is asserted. The time taken for the capacitor to reach 1.2 V, in addition to the propagation delay of the comparator, constitutes the enable timeout, which is typically 35 μ s.

To minimize the delay between V_{IN} falling below $V_{TH_FALLING}$ and the enable output deasserting, an NMOS transistor is connected in parallel with C_{INT} . The output of the voltage detector is connected to the gate of this transistor so that, when V_{IN} falls below $V_{TH_FALLING}$, the transistor switches on and C_{INT} discharges quickly.

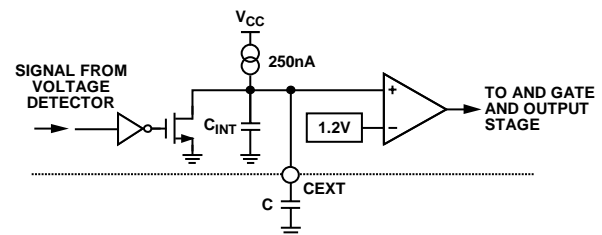


Figure 20. Capacitor-Adjustable Delay Circuit

Connecting an external capacitor to the CEXT pin delays the rise time—and therefore the enable timeout—further. The relationship between the value of the external capacitor and the resulting timeout is characterized by the following equation:

$$t_{EN} = (C \times 4.8 \times 10^6) + 35 \mu s$$

OPEN-DRAIN AND PUSH-PULL OUTPUTS

The ADM1085 and ADM1087 have open-drain output stages that require an external pull-up resistor to provide a logic high voltage level. The geometry of the NMOS transistor enables the output to be pulled up to voltage levels as high as 22 V.

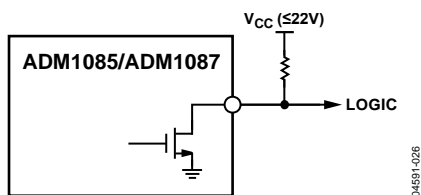


Figure 21. Open-Drain Output Stage

The ADM1086 and ADM1088 have push-pull (CMOS) output stages that require no external components to drive other logic circuits. An internal PMOS pull-up transistor provides the logic high voltage level.

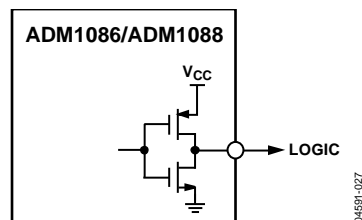


Figure 22. Push-Pull Output Stage

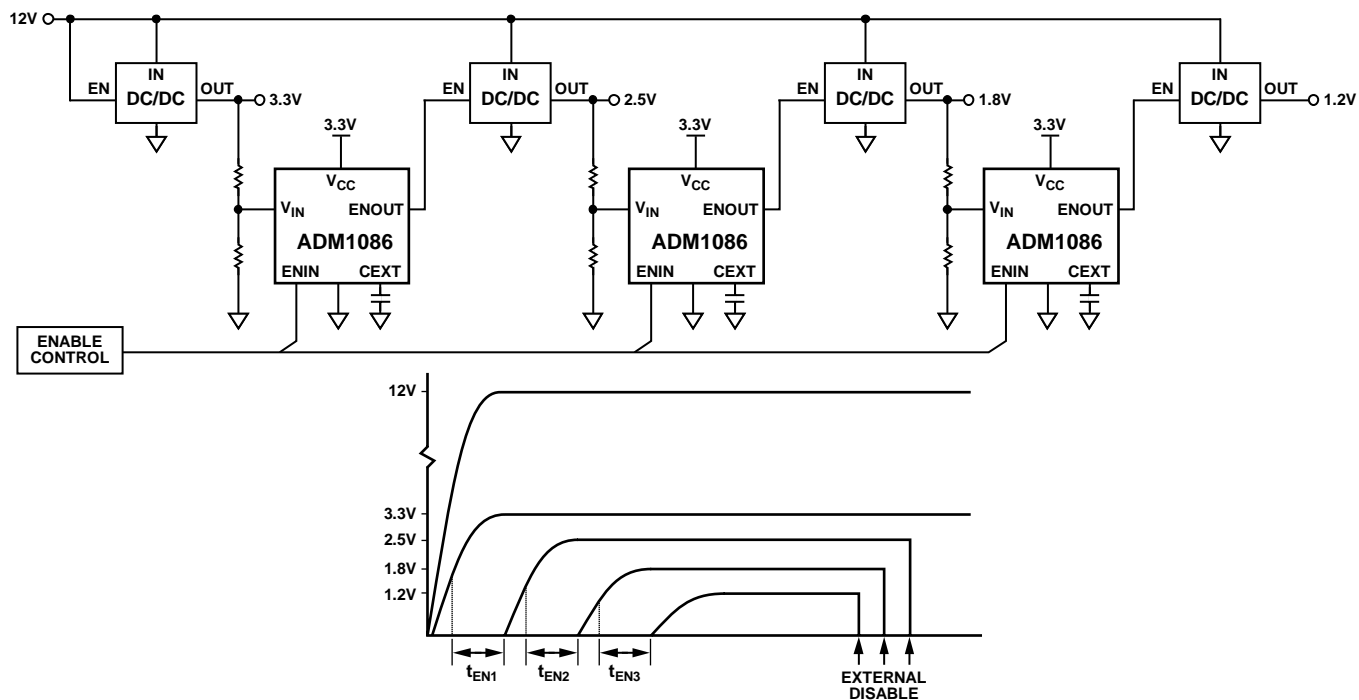


Figure 24. Typical ADM1086 Application Circuit

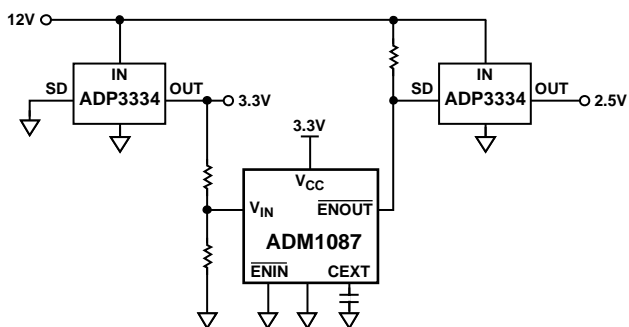


Figure 25. Typical ADM1087 Application Circuit Using ADP3334 Voltage Regulators

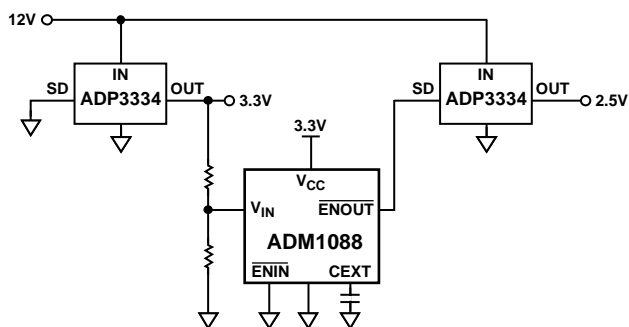


Figure 26. Typical ADM1088 Application Circuit Using ADP3334 Voltage Regulators

QUAD-SUPPLY POWER GOOD INDICATOR

The enable output of the Simple Sequencers is equivalent to an AND function of V_{IN} and ENIN. ENOUT is high only when the voltage at V_{IN} is above the threshold and the enable input (ENIN) is high as well. Although ENIN is a digital input, it can tolerate voltages as high as 22 V and can detect if a supply is present. Therefore, a simple sequencer can monitor two supplies and assert what can be interpreted as a power good signal when both supplies are present. The outputs of two ADM1085s can be wire-AND'ed together to make a quad-supply power good indicator.

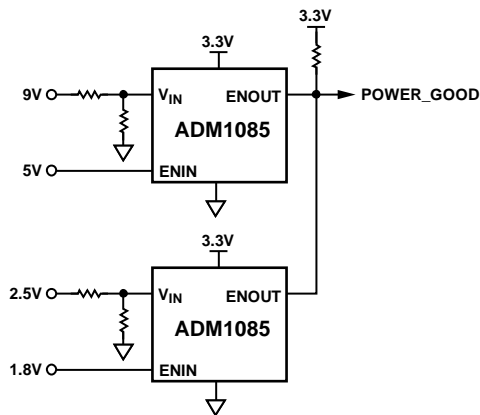


Figure 30. Quad-Supply Power Good Indicator

04591-035

SEQUENCING WITH FET SWITCHES

The open-drain outputs of the ADM1085 and ADM1087 can drive external FET transistors that can switch on power supply rails. All that is needed is a pull-up resistor to a voltage source that is high enough to turn on the FET.

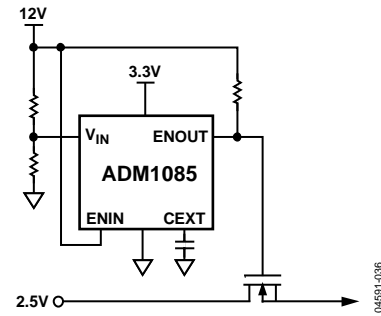


Figure 31. Sequencing with a FET Switch

04591-036

OUTLINE DIMENSIONS

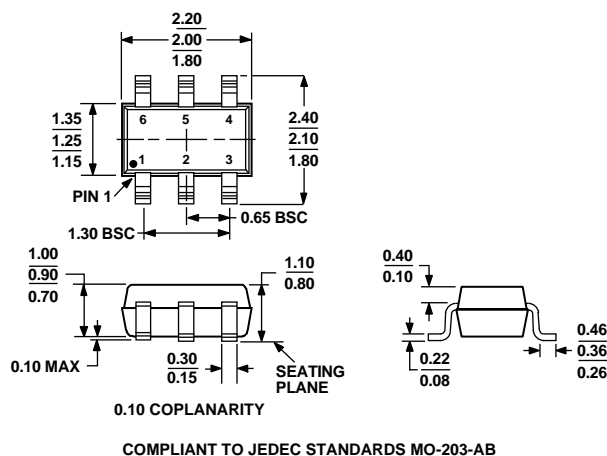


Figure 32. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Ordering Quantity	Package Description	Package Option	Branding
ADM1085AKS-REEL7	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M0V
ADM1085AKSZ-REEL7 ¹	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M7R
ADM1086AKS-REEL7	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M0W
ADM1086AKSZ-REEL7 ¹	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M8M
ADM1087AKS-REEL7	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M0X
ADM1087AKSZ-REEL7 ¹	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M7S
ADM1088AKS-REEL7	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M0Y
ADM1088AKSZ-REEL7 ¹	-40°C to +125°C	3k	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	M8N
EVAL-ADM1087EB			Evaluation Board for the ADM1087 device. This board can also be used to evaluate the other devices in the family. Sample can be ordered separately.		

¹ Z = Pb-free part.

NOTES