

## 3.8 $\Omega$ On-Resistance, SPDT Switch

### FEATURES

- ▶ 3.8  $\Omega$  on resistance
- ▶ Specified at
  - ▶  $V_{DD} = +5\text{ V} \pm 10\%$
  - ▶  $V_{SS} = -4.5\text{ V to } -8.8\text{ V}$
- ▶ No  $V_L$  supply required
- ▶ 3 V logic-compatible inputs
- ▶ Up to 310 mA continuous current
- ▶ Rail-to-rail operation
- ▶ 8-lead, 2 mm  $\times$  3 mm LFCSP

### APPLICATIONS

- ▶ LDMOS power amplifier gate drive
- ▶ GAN power amplifier gate drive
- ▶ Communication systems
- ▶ Automatic test equipment
- ▶ Data acquisition systems
- ▶ Sample-and-hold systems

### GENERAL DESCRIPTION

The ADG1519 is a single-pole, double throw (SPDT) switch. An EN input on the lead frame chip scale package (LFCSP) is used to enable or disable the device. When disabled, the switch terminals (SA, SB, and D) are high impedance.

The ADG1519 is fully specified at  $V_{DD} = +5\text{ V} \pm 10\%$  and  $V_{SS} = -4.5\text{ V to } -8.8\text{ V}$  for applications that require asymmetrical supplies. The ADG1519 on-resistance profile is flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals. The construction ensures ultra low power dissipation, making the device ideally suited for portable and battery-powered instruments.

The switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. The ADG1519 exhibits break-before-make switching action for use in multiplexer applications.

### FUNCTIONAL BLOCK DIAGRAM

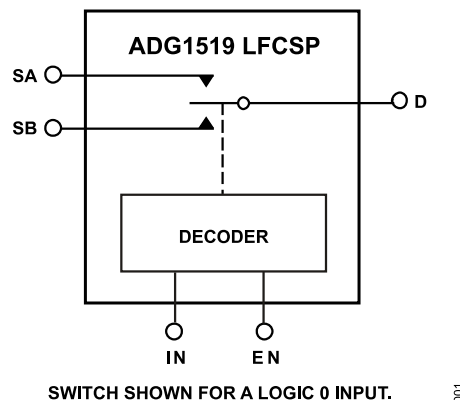


Figure 1.

### PRODUCT HIGHLIGHTS

1. 5.2  $\Omega$  maximum on resistance at 25°C.
2. -98 dB THD.
3. 3 V logic-compatible digital inputs:  $V_{INH} = 2.0\text{ V}$  minimum and  $V_{INL} = 0.8\text{ V}$  maximum.
4. No logic power supply voltage ( $V_L$ ) required.
5. 8-lead, 2 mm  $\times$  3 mm LFCSP (see the [Outline Dimensions](#) section).

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**REVISION HISTORY****11/2023—Rev. A to Rev. B**

Change to Product Highlights Section.....	1
Changes to Figure 9 and Figure 14.....	8
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**10/2023—Rev. 0 to Rev. A**

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**1/2022—Revision 0: Initial Version**

## SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -4.5\text{ V}$  to  $-8.8\text{ V}$ , and  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
ANALOG SWITCH					$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -7.2\text{ V}$
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	3.8			$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ , and see Figure 18 <sup>1</sup>
	5.2	6.2	7	$\Omega$ max	
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.1			$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ <sup>1</sup>
	0.3	0.35	0.4	$\Omega$ max	
On-Resistance Flatness, $R_{FLAT} (ON)$	1.15			$\Omega$ typ	$V_S = V_{SS}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ <sup>1</sup>
	1.6	1.85	2	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage, $I_S$ (Off)	$\pm 0.1$			nA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -8.8\text{ V}$ $V_S$ and $V_D = V_{DD} - 1\text{ V}$ to $V_{SS} + 1\text{ V}$ , see Figure 19 <sup>1, 2</sup>
	$\pm 10$	$\pm 12$	$\pm 100$	nA max	
Drain Off Leakage, $I_D$ (Off)	$\pm 0.1$			nA typ	$V_S$ and $V_D = V_{DD} - 1\text{ V}$ to $V_{SS} + 1\text{ V}$ , see Figure 19 <sup>1, 2</sup>
	$\pm 10$	$\pm 13$	$\pm 140$	nA max	
Channel On Leakage, $I_D$ , $I_S$ (On)	$\pm 0.1$			nA typ	$V_S = V_D = V_{DD} - 1\text{ V}$ to $V_{SS} + 1\text{ V}$ , see Figure 20 <sup>1, 2</sup>
	$\pm 10$	$\pm 13$	$\pm 110$	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current, $I_{INL}$ or $I_{INH}$	0.001			$\mu\text{A}$ typ	$V_{IN} = V_{GND}$ or $V_{DD}$ <sup>3</sup>
			$\pm 0.1$	$\mu\text{A}$ max	
Digital Input Capacitance, $C_{IN}$	4			pF typ	
<b>DYNAMIC CHARACTERISTICS</b>					
Transition Time, $t_{TRANSITION}$	240			ns typ	$V_{DD} = +5\text{ V}$ , $V_{SS} = -8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ <sup>4</sup>
	305	365	400	ns max	$V_S = 3\text{ V}$ , see Figure 21 <sup>1</sup>
$t_{ON} (EN)$	215			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ <sup>4</sup>
	275	325	360	ns max	$V_S = 3\text{ V}$ , see Figure 23 <sup>1</sup>
$t_{OFF} (EN)$	265			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ <sup>4</sup>
	335	380	415	ns max	$V_S = 3\text{ V}$ , see Figure 23 <sup>1</sup>
Break-Before-Make Time Delay, $t_D$	65			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ <sup>4</sup>
			38	ns min	$V_{SA} = V_{SB} = 3\text{ V}$ , see Figure 22 <sup>5</sup>
Charge Injection	12			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 24 <sup>1, 4, 6</sup>
Off Isolation	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 1 MHz, see Figure 25 <sup>4</sup>
Channel-to-Channel Crosstalk	-60			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , frequency = 1 MHz, see Figure 26 <sup>4</sup>
Total Harmonic Distortion Plus Noise, THD + N	0.0019			% typ	$R_L = 10\text{ k}\Omega$ , 5 V p-p, frequency = 20 Hz to 20 kHz, see Figure 28 <sup>4</sup>
	-94			dB typ	
Total Harmonic Distortion, THD	-98			dB typ	$R_L = 10\text{ k}\Omega$ , 5 V p-p, frequency = 1 kHz <sup>4</sup>
	-96			dB typ	$R_L = 10\text{ k}\Omega$ , 5 V p-p, frequency = 20 kHz <sup>4</sup>
	-85			dB typ	$R_L = 10\text{ k}\Omega$ , 5 V p-p, frequency = 100 kHz <sup>4</sup>

## SPECIFICATIONS

Table 1. (Continued)

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth	95			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , see Figure 27 <sup>4</sup>
Insertion Loss	0.3			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , frequency = 1 MHz, see Figure 27 <sup>4</sup>
Source Capacitance, $C_S$ (Off)	27			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz <sup>1</sup>
Drain Capacitance, $C_D$ (Off)	58			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz <sup>1</sup>
$C_D$ , $C_S$ (On)	129			pF typ	$V_S = 0\ \text{V}$ , frequency = 1 MHz <sup>1</sup>
POWER REQUIREMENTS					$V_{DD} = +5.5\ \text{V}$ , $V_{SS} = -8.8\ \text{V}$
Positive Supply Current, $I_{DD}$	0.001		1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$
Negative Supply Current, $I_{SS}$	0.001		1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital inputs = 0 V or $V_{DD}$

<sup>1</sup>  $V_S$  is the analog voltage for Terminal SA or Terminal SB and  $I_S$  is the analog current for Terminal Sx.

<sup>2</sup>  $V_D$  is the analog voltage on Terminal D.

<sup>3</sup>  $V_{IN}$  is the IN voltage, and  $V_{GND}$  is the GND voltage.

<sup>4</sup>  $R_L$  is the load resistance and  $C_L$  is the load capacitance.

<sup>5</sup>  $V_{SA}$  is the Source A voltage, and  $V_{SB}$  is the Source B voltage.

<sup>6</sup>  $R_S$  is the source resistance.

## CONTINUOUS CURRENT PER CHANNEL, SX OR D

Table 2.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL					
Dual Supply					$V_{DD} = +4.5\ \text{V}$ , $V_{SS} = -7.2\ \text{V}$
8-Lead LFCSP ( $\theta_{JA} = 64.9^\circ\text{C/W}$ )	310	180	95	mA maximum	

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	18 V
$V_{DD}$ to GND	-0.3 V to +16.5 V
$V_{SS}$ to GND	+0.3 V to -16.5 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or D (Pulsed at 1 ms, 10% Duty-Cycle Maximum)	600 mA
Continuous Current per Channel, Sx or D	Data in Table 2 + 15% mA
Temperature	
Operating Range	-40°C to +125°C
Storage Range	-65°C to +150°C
Junction	150°C
Reflow Soldering Peak, Pb Free	JEDEC-J-STD-020
Peak Temperature	260°C

<sup>1</sup> Over voltages at IN, Sx, or D are clamped by internal diodes. Limit the current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and  $\theta_{JC}$  is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type <sup>1</sup>	$\theta_{JA}$	$\theta_{JC}$	Unit
CP-8-31	64.90	14.31	°C/W

<sup>1</sup> Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

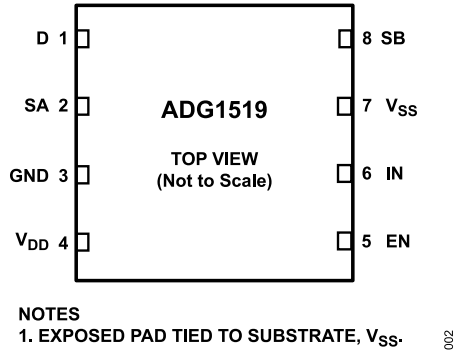


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. The D pin can be an input or output.
2	SA	Source Terminal. The SA pin can be an input or output.
3	GND	Ground (0 V) Reference.
4	$V_{DD}$	Most Positive Power Supply Potential. Decouple the $V_{DD}$ pin using a 0.1 $\mu$ F capacitor to GND.
5	EN	Active High Digital Input. When the EN pin is low, the device is disabled, and the SA, SB, and D terminals are high impedance. When the EN pin is high, the IN logic input determines which switch is turned on.
6	IN	Logic Control Input.
7	$V_{SS}$	Most Negative Power Supply Potential. Decouple the $V_{SS}$ pin using a 0.1 $\mu$ F capacitor to GND.
8	SB	Source Terminal. The SB pin can be an input or output.
0	EPAD	Exposed Pad. Exposed pad tied to substrate, $V_{SS}$ .

Table 6. Truth Table

EN	IN	D
0	X <sup>1</sup>	High impedance
1	0	SA
1	1	SB

<sup>1</sup> X means don't care.

## TYPICAL PERFORMANCE CHARACTERISTICS

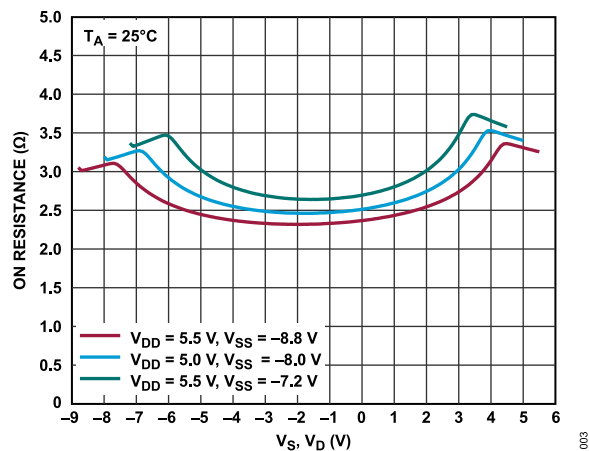
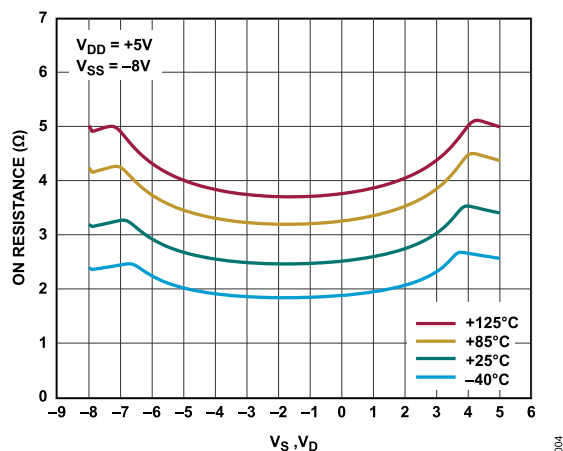
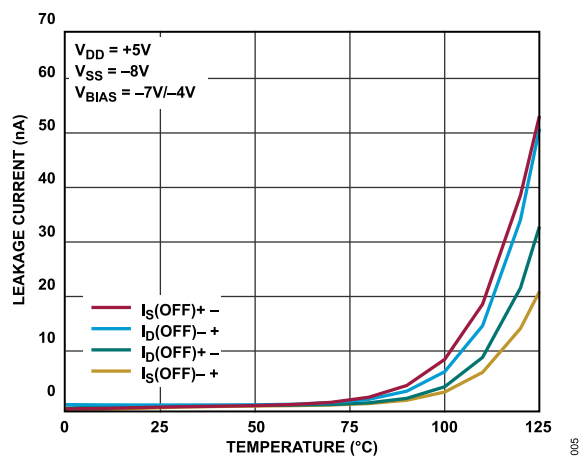
Figure 3. On Resistance as a Function of  $V_S$  and  $V_D$ Figure 4. On Resistance as a Function of  $V_S$  and  $V_D$  for Different Temperatures

Figure 5. Off Leakage as a Function of Temperature

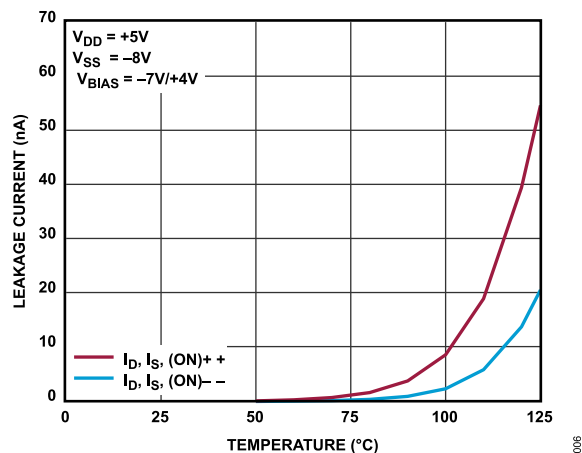
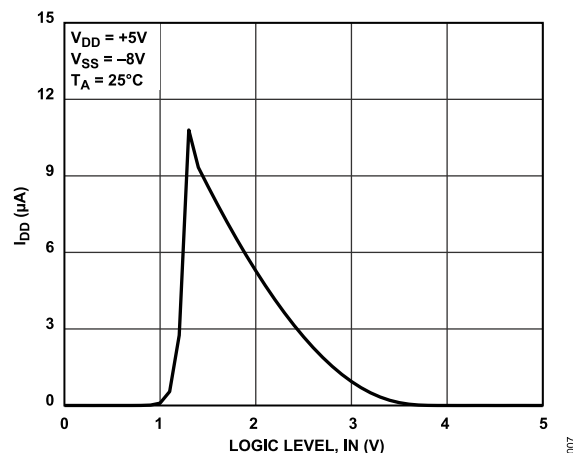
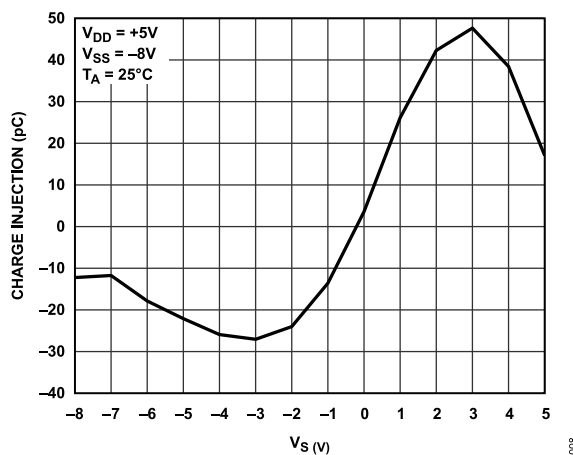


Figure 6. On Leakage as a Function of Temperature

Figure 7.  $I_{DD}$  vs. Logic Level,  $I_N$ Figure 8. Charge Injection vs.  $V_S$

## TYPICAL PERFORMANCE CHARACTERISTICS

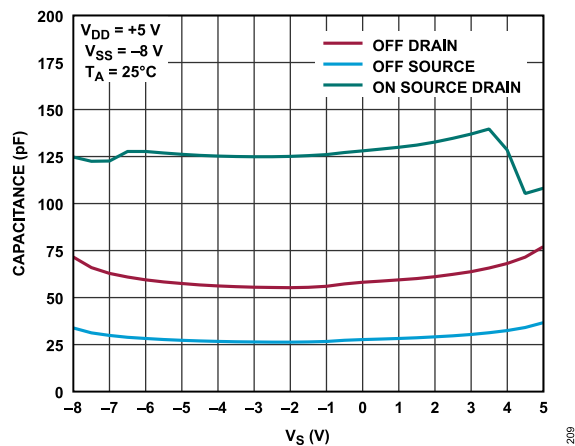
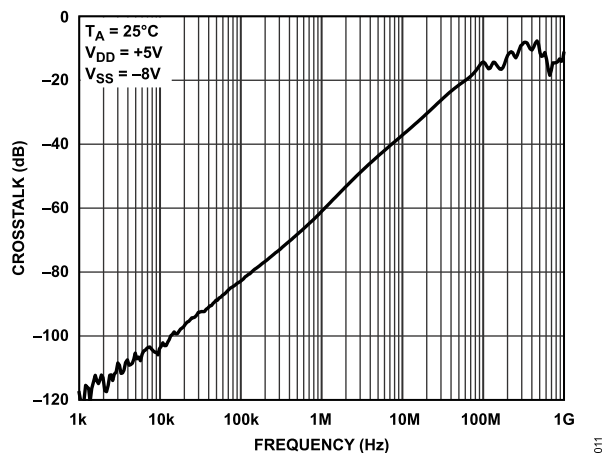
Figure 9. Capacitance vs.  $V_S$ 

Figure 12. Crosstalk vs. Frequency

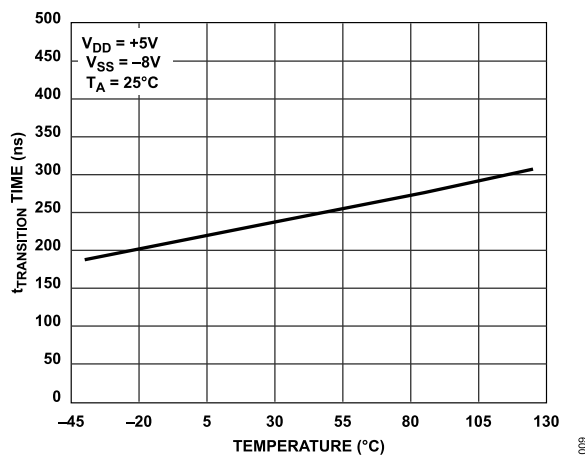
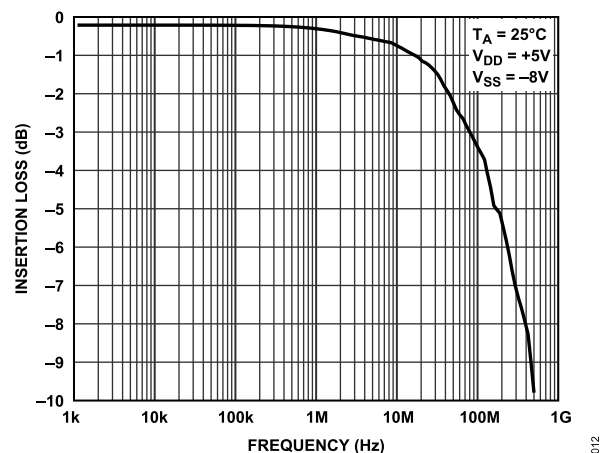
Figure 10.  $t_{\text{TRANSITION}}$  Time vs. Temperature

Figure 13. Insertion Loss vs. Frequency

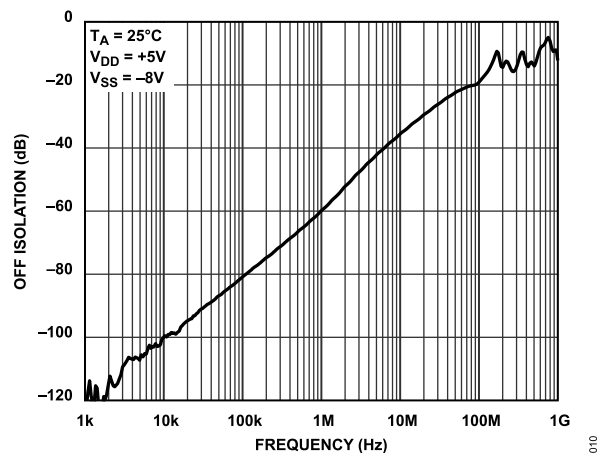


Figure 11. Off Isolation vs. Frequency

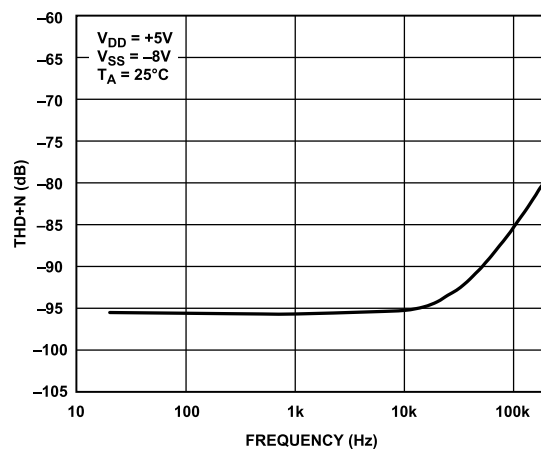


Figure 14. THD + N vs. Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

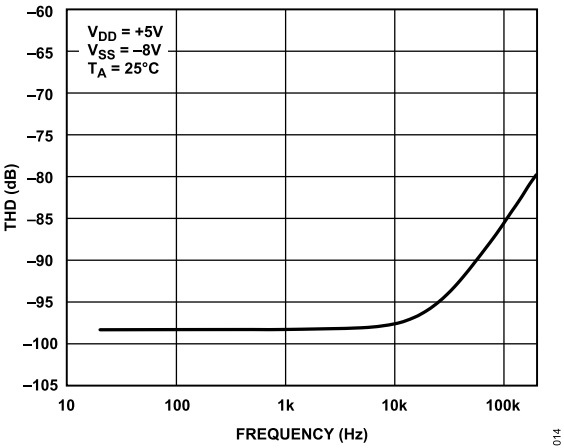


Figure 15. THD vs. Frequency

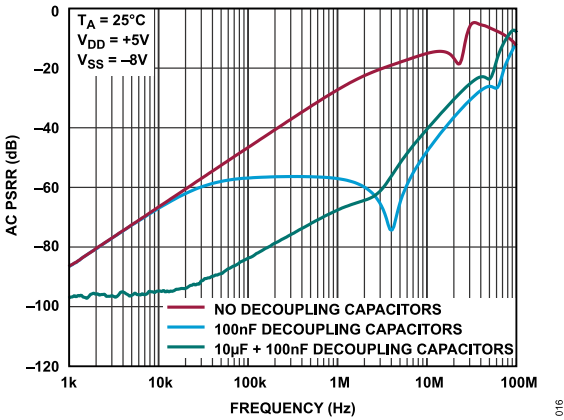


Figure 17. AC Power Supply Rejection Ratio (PSRR) vs. Frequency

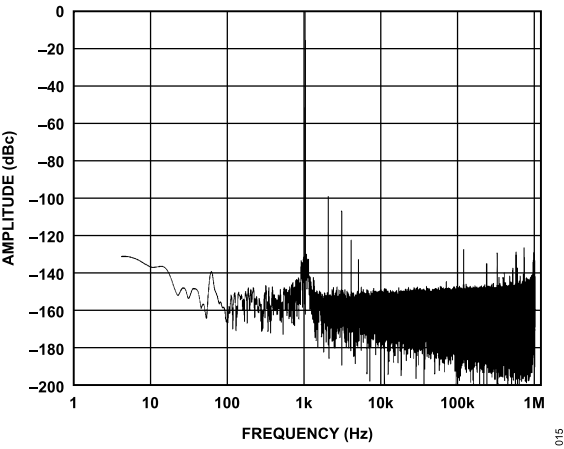


Figure 16. THD Fast Fourier Transform (FFT)

## TEST CIRCUITS

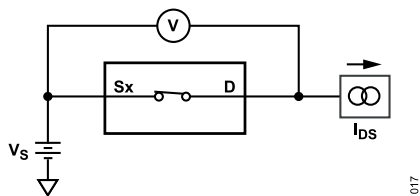
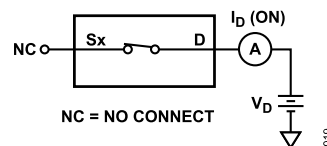
Figure 18. On Resistance ( $I_{DS}$  is the Drain to Source Current.)

Figure 20. On Leakage

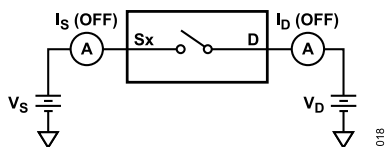


Figure 19. Off Leakage

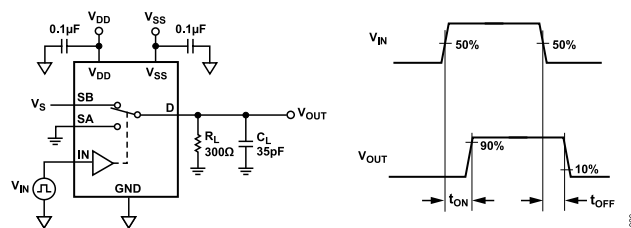
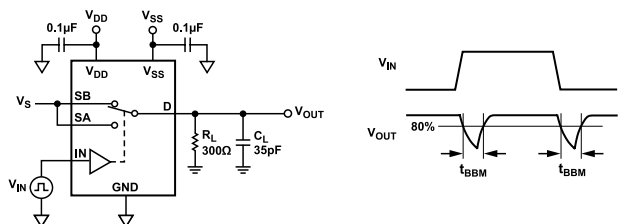
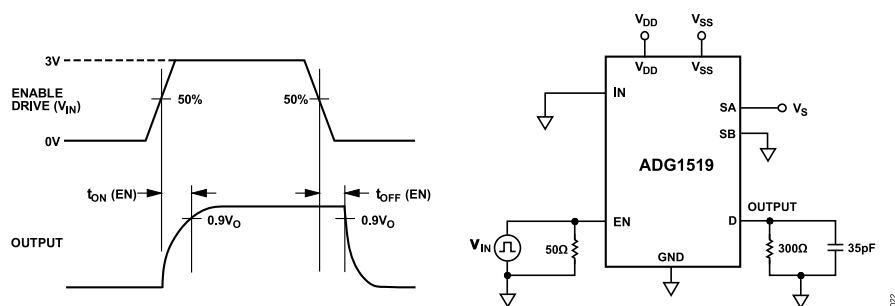
Figure 21. Switching Times,  $t_{ON}$  and  $t_{OFF}$  ( $V_{OUT}$  is the Output Voltage.)

Figure 22. Break-Before-Make Time Delay

Figure 23. Enable Delay,  $t_{ON} (EN)$ ,  $t_{OFF} (EN)$

TEST CIRCUITS

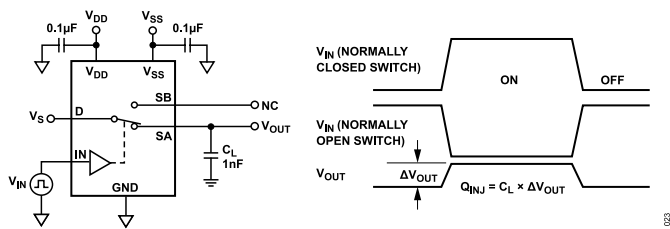


Figure 24. Charge Injection

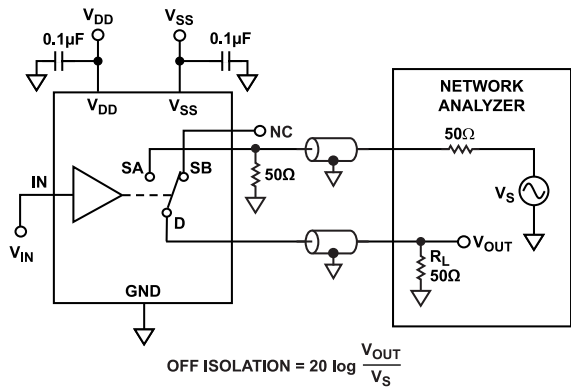


Figure 25. Off Isolation

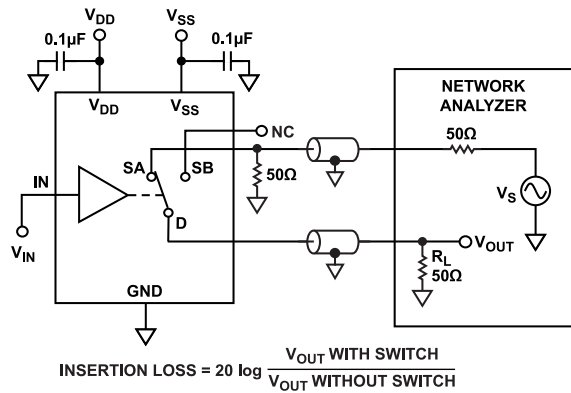


Figure 27. Bandwidth

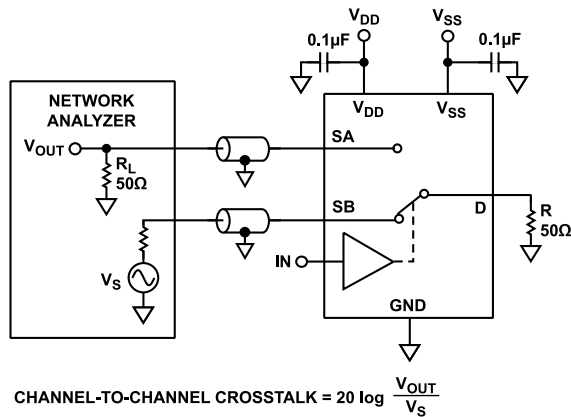


Figure 26. Channel-to-Channel Crosstalk

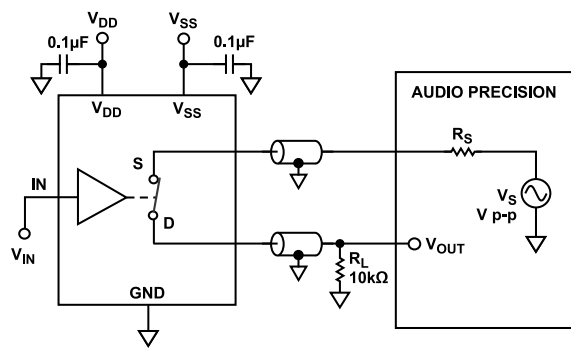


Figure 28. THD and THD + N

**TERMINOLOGY** **$I_{DD}$** 

The positive supply current.

 **$I_{SS}$** 

The negative supply current.

 **$V_D$  and  $V_S$** 

The analog voltage on Terminal D and Terminal S.

 **$R_{ON}$** 

The ohmic resistance between Terminal D and Terminal S.

 **$R_{FLAT\ ON}$** 

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

 **$I_S\ Off$** 

The source leakage current with the switch off.

 **$I_D\ Off$** 

The drain leakage current with the switch off.

 **$I_D$  and  $I_S\ On$** 

The channel leakage current for Terminal D and Terminal S with the switch on.

 **$V_{INL}$** 

The maximum input voltage for Logic 0.

 **$V_{INH}$** 

The minimum input voltage for Logic 1.

 **$I_{INL}$  and  $I_{INH}$** 

The input high and low current of the digital input.

 **$C_S\ Off$** 

The off switch source capacitance, measured with reference to ground.

 **$C_D\ Off$** 

The off switch drain capacitance, measured with reference to ground.

 **$C_D$  and  $C_S\ On$** 

The on switch capacitance for Terminal D and Terminal S, measured with reference to ground.

 **$C_{IN}$** 

The digital input capacitance.

 **$t_{ON\ EN}$** 

Delay time between the 50% and 90% points of the digital input and switch on condition. See [Figure 23](#).

 **$t_{OFF\ EN}$** 

Delay time between the 50% and 90% points of the digital input and switch off condition. See [Figure 23](#).

 **$t_{TRANSITION}$** 

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

 **$T_D$** 

Off time measured between the 80% point of both switches when switching from one address state to another. See [Figure 22](#).

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching. See [Figure 24](#).

**Off Isolation**

A measure of unwanted signal coupling through an off switch. See [Figure 25](#).

**Crosstalk**

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. See [Figure 26](#).

**Bandwidth**

The frequency at which the output is attenuated by 3 dB. See [Figure 27](#).

**Insertion Loss**

The loss due to the on resistance of the switch. See [Figure 27](#).

**THD + N**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental. See [Figure 28](#).

**THD**

THD is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. See [Figure 28](#).

**TERMINOLOGY****AC PSRR**

AC PSRR measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of the signal on the output to the amplitude of the modulation is the AC PSRR. See [Figure 17](#).

APPLICATIONS INFORMATION

POWER AMPLIFIER GATE DRIVE

Figure 29 shows a typical application where the ADG1519 is used to set the gate bias voltage for an RF power amplifier for communications applications. The asymmetrical dual supply and rail-to-rail operation of the ADG1519 allows for negative voltages of up to  $-8\text{ V}$  for biasing gallium nitride (GaN) power amplifiers while the positive  $+5\text{ V}$  rail is ideal for laterally diffused metal-oxide semiconductor (LDMOS) power amplifiers.

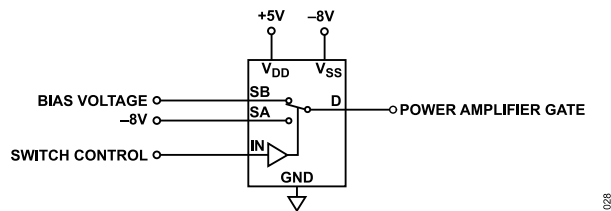


Figure 29. GaN Power Amplifier Gate Drive

POWER SUPPLY RAILS

To guarantee correct operation of the ADG1519,  $0.1\text{ }\mu\text{F}$  decoupling capacitors are required on the  $V_{DD}$  and  $V_{SS}$  pins.

The ADG1519 can operate with asymmetrical bipolar supplies between of  $V_{DD} = +5\text{ V} \pm 10\%$  and  $V_{SS} = -4.5\text{ V}$  to  $-8.8\text{ V}$ . The supplies on  $V_{DD}$  and  $V_{SS}$  do not have to be asymmetrical. However, the  $V_{DD}$  to  $V_{SS}$  range must not exceed  $18\text{ V}$  as stated in the [Absolute Maximum Ratings](#) section.

POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of an asymmetrical bipolar power solution is shown in Figure 30. The ADP5070 (dual switching regulator) generates a positive and negative supply rail for the ADG1519. Also shown in Figure 30 are two optional low dropout regulators (LDOs), the ADP7118 and ADP7182 positive and negative LDOs, respectively, that can be used to reduce the output ripple of the ADP5070 in ultralow noise sensitive applications.

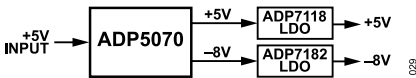


Figure 30. Bipolar Power Solution

Table 7. Recommended Power Management Devices

Product	Description
ADP5070	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
ADP7118	20 V, 200 mA, low noise, complementary metal oxide semiconductor (CMOS) LDO linear regulator
ADP7182	$-28\text{ V}$ , $-200\text{ mA}$ , low noise, LDO linear regulator

OUTLINE DIMENSIONS

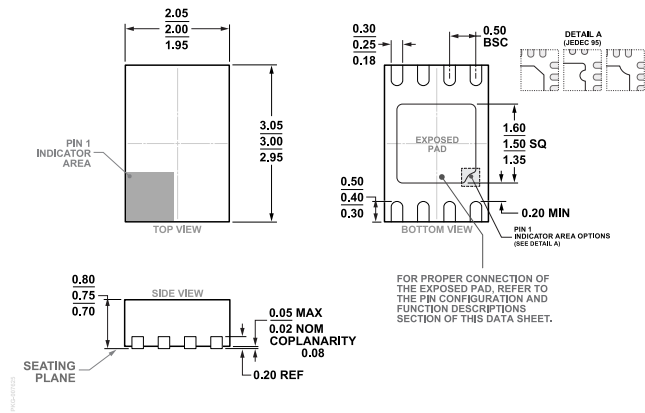


Figure 31. 8-Lead Lead Frame Chip Scale Package [LFCSP]  
2 mm x 3 mm Body and 0.75 mm Package Height  
(CP-8-31)  
Dimensions shown in millimeters

Updated: August 09, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADG1519BCPZ-RL7	-40°C to +125°C	8-lead LFCSP, 2 mm x 3 mm x 0.75	Reel, 3000	CP-8-31	S59

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Model <sup>1</sup>	Description
EVAL-ADG1519EBZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.