Ultralow Noise Drivers for Low Voltage ADCs

Enhanced Product

ADA4930-1-EP

FEATURES

- Low input voltage noise: 1.2 nV/√Hz
- Low common-mode output: 0.9 V on single supply
- Extremely low harmonic distortion
  - HD2/HD3: −104/−101 dBc at 10 MHz
  - HD2/HD3: −79/−82 dBc at 70 MHz
  - HD2/HD3: −73/−75 dBc at 100 MHz
- High speed
  - −3 dB bandwidth: 1.35 GHz, G = 1
  - Slew rate: 3400 V/µs
  - 0.1 dB gain flatness: 380 MHz
  - Fast overdrive recovery: 1.5 ns
- Offset voltage: 0.5 mV typical
- Externally adjustable gain
- Differential-to-differential or single-ended-to-differential operation
- Adjustable output common-mode voltage
- Single-supply operation: 3.3 V or 5 V

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended temperature range: −55°C to +105°C
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- ADC drivers
- Single-ended-to-differential converters
- IF and baseband gain blocks
- Differential buffers
- Line drivers

GENERAL DESCRIPTION

The ADA4930-1-EP is a very low noise, low distortion, high speed differential amplifier. It is an ideal choice for driving 1.8 V high performance ADCs with resolutions up to 14 bits from dc to 70 MHz. The adjustable output common-mode voltage setting allows the ADA4930-1-EP to match the input of the ADC for maximum dynamic range. The internal common-mode feedback loop provides exceptional output balance, suppression of even-order harmonic distortion products, and dc level translation.

FUNCTIONAL BLOCK DIAGRAMS

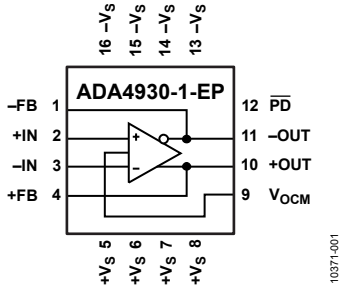

Figure 1.

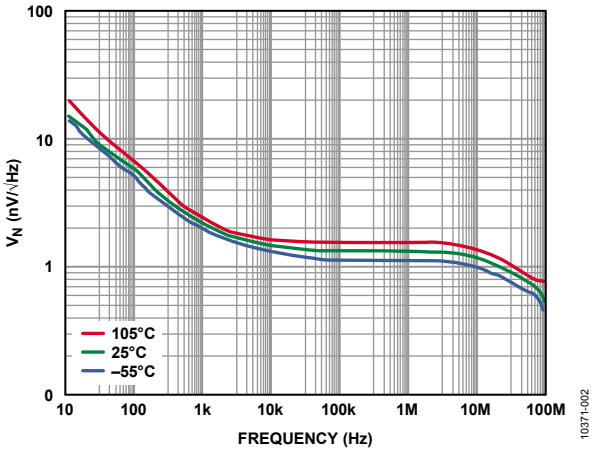

Figure 2. Voltage Noise Spectral Density

With the ADA4930-1-EP, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier.

The ADA4930-1-EP is fabricated using Analog Devices, Inc., proprietary silicon-germanium (SiGe), complementary bipolar process, enabling it to achieve very low levels of distortion with an input voltage noise of only 1.2 nV/√Hz.

The low dc offset and excellent dynamic performance of the ADA4930-1-EP make it well suited for a wide variety of data acquisition and signal processing applications.

The ADA4930-1-EP is available in a 3 mm × 3 mm 16-lead LFCSP. The pinout has been optimized to facilitate printed circuit board (PCB) layout and minimize distortion. The ADA4930-1-EP is specified to operate over the −55°C to +105°C temperature range for 3.3 V or 5 V supply voltages.

Additional application and technical information can be found in the ADA4930-1/ADA4930-2 data sheet.

Rev. B
Document Feedback

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REVISION HISTORY

11/2017—Rev. A to Rev. B

Changed CP-16-21 to CP-16-35 ..... Throughout
Updated Outline Dimensions 9
Changes to Ordering Guide 9

6/2013—Rev. 0 to Rev. A

Changes to Ordering Guide 9

10/2012—Revision 0: Initial Version

SPECIFICATIONS

3.3 V OPERATION

V_S = 3.3 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, R_F = 301 Ω, R_G = 301 Ω, $R_{L, dm}$ = 1 kΩ, single-ended input, differential output, T_A = 25°C, T_{MIN} to T_{MAX} = −55°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p		1430		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p		887		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm}$ = 0.1 V p-p		380		MHz
Slew Rate	$V_{O, dm}$ = 2 V step, 25% to 75%		2877		V/µs
Settling Time to 0.1%	$V_{O, dm}$ = 2 V step, R_L = 200 Ω		6.3		ns
Overdrive Recovery Time	G = 3, $V_{IN, dm}$ = 0.7 V p-p pulse		1.5		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{O, dm}$ = 2 V p-p, f_C = 10 MHz, T_{MIN} to T_{MAX}		−98/−97		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 30 MHz, T_{MIN} to T_{MAX}		−91/−88		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 70 MHz, T_{MIN} to T_{MAX}		−79/−79		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 100 MHz, T_{MIN} to T_{MAX}		−73/−73		dBc
Third-Order IMD	$V_{O, dm}$ = 1 V p-p/tone, f_C = 70.05 MHz ± 0.05 MHz		91		dBc
	$V_{O, dm}$ = 1 V p-p/tone, f_C = 140.05 MHz ± 0.05 MHz		86		dBc
Input Voltage Noise	f = 100 kHz		1.15		nV/√Hz
	T_{MIN} to T_{MAX}		1.2		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	$V_{IP} = V_{IN} = V_{OCM}$ = 0 V, R_L = open circuit, T_{MIN} to T_{MAX}	−3.1	−0.5	+3.1	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2.75		µV/°C
Input Bias Current		−36	−24	−16	µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−0.05		µA/°C
Input Offset Current		−1.8	+0.1	+1.8	µA
Open-Loop Gain	$R_F = R_G$ = 10 kΩ, ΔV_O = 0.5 V, R_L = open circuit		64		dB
	T_{MIN} to T_{MAX}		61		dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		0.3		1.2	V
Input Resistance	Differential		150		kΩ
	Common mode		3		MΩ
Input Capacitance	Common mode		1		pF
CMRR	ΔV_{ICM} = 0.5 V dc; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−82	−77	dB
	T_{MIN} to T_{MAX}		−76		dB
OUTPUT CHARACTERISTICS					
Output Voltage	Each single-ended output; $R_F = R_G$ = 10 kΩ	0.11		1.74	V
	Each single-ended output; $R_F = R_G$ = 10 kΩ, T_{MIN} to T_{MAX}			1.54	V
Linear Output Current	Each single-ended output; f = 1 MHz, THD ≤ 60 dBc		30		mA
Output Balance Error	f = 1 MHz		55		dB

3.3 V V_{OCM} TO $V_{O, CM}$ PERFORMANCE

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		745		MHz
Slew Rate	$V_{O, cm}$ = 2 V p-p, 25% to 75%		828		V/µs
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		0.8		1.1	V
Input Resistance		7.0	8.3	10.3	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−25	+15.4	+31	mV
Input Voltage Noise	f = 100 kHz		23.5		nV/√Hz
Gain		0.99	1	1.02	V/V
	T_{MIN} to T_{MAX}		1.01		V/V
CMRR	ΔV_{OCM} = 0.5 V dc; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−83	−77	dB
	T_{MIN} to T_{MAX}		−76		dB

3.3 V GENERAL PERFORMANCE

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3.3		V
Quiescent Current per Amplifier	Enabled	32	35	40	mA
	Enabled, T_{MIN} to T_{MAX} variation		81		µA/°C
	Disabled	0.44	1.8	2.35	mA
	T_{MIN} to T_{MAX}		2.4		mA
+PSRR	ΔV_{ICM} = 0.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−74	−70	dB
	T_{MIN} to T_{MAX}		−68		dB
−PSRR	ΔV_{ICM} = 0.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−87	−76	dB
	T_{MIN} to T_{MAX}		−77		dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Disabled		<0.8		V
	Enabled		>1.3		V
Turn-Off Time			1		µs
Turn-On Time			12		ns
$\overline{PD}$ Pin Bias Current					
Enabled	$\overline{PD}$ = 3.3 V		0.09		µA
Disabled	$\overline{PD}$ = 0 V		97		µA
OPERATING TEMPERATURE RANGE		−55		+105	°C

5 V OPERATION

V_S = 5 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, R_F = 301 Ω, R_G = 301 Ω, $R_{L, dm}$ = 1 kΩ, single-ended input, differential output, T_A= 25°C, T_{MIN} to T_{MAX} = −55°C to +105°C, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p		1350		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p		937		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm}$ = 0.1 V p-p		369		MHz
Slew Rate	$V_{O, dm}$ = 2 V step, 25% to 75%		3400		V/µs
Settling Time to 0.1%	$V_{O, dm}$ = 2 V step, R_L = 200 Ω		6		ns
Overdrive Recovery Time	G = 3, $V_{IN, dm}$ = 0.7 V p-p pulse		1.5		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{O, dm}$ = 2 V p-p, f_C = 10 MHz, T_{MIN} to T_{MAX}		−104/−101		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 30 MHz, T_{MIN} to T_{MAX}		−91/−93		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 70 MHz, T_{MIN} to T_{MAX}		−79/−82		dBc
	$V_{O, dm}$ = 2 V p-p, f_C = 100 MHz, T_{MIN} to T_{MAX}		−73/−75		dBc
Third-Order IMD	$V_{O, dm}$ = 1 V p-p/tone, f_C = 70.05 MHz ± 0.05 MHz		94		dBc
	$V_{O, dm}$ = 1 V p-p/tone, f_C = 140.05 MHz ± 0.05 MHz		90		dBc
Input Voltage Noise	f = 100 kHz		1.2		nV/√Hz
	T_{MIN} to T_{MAX}		1.3		nV/√Hz
Input Current Noise	f = 100 kHz		2.8		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V, R_L = open circuit, T_{MIN} to T_{MAX}	−3.1	−0.15	+3.1	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.8		µV/°C
Input Bias Current		−34	−23	−15	µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−0.05		µA/°C
Input Offset Current		−0.82	+0.1	+0.82	µA
Open-Loop Gain	R_F = R_G = 10 kΩ, ΔV_O = 1 V, R_L = open circuit		64		dB
	T_{MIN} to T_{MAX}		61		dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		0.3		2.8	V
Input Resistance	Differential		150		kΩ
	Common mode		3		MΩ
Input Capacitance	Common mode		1		pF
CMRR	ΔV_{ICM} = 1 V dc; R_F = R_G = 10 kΩ, R_L = open circuit		−82	−77	dB
	T_{MIN} to T_{MAX}		−76		dB
OUTPUT CHARACTERISTICS					
Output Voltage	Each single-ended output; R_F = R_G = 10 kΩ, T_{MIN} to T_{MAX}	0.18		3.38	V
Linear Output Current	Each single-ended output; f = 1 MHz, TDH ≤ 60 dBc		30		mA
Output Balance Error	f = 1 MHz		55		dB

5 V V_{OCM} TO $V_{O, CM}$ PERFORMANCE

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		740		MHz
Slew Rate	$V_{O, cm}$ = 2 V p-p, 25% to 75%		1224		V/µs
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		0.5		2.3	V
Input Resistance		7.0	8.3	10.2	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−25	+0.35	+15	mV
Input Voltage Noise	f = 100 kHz		23.5		nV/√Hz
Gain		0.99	1	1.02	V/V
	T_{MIN} to T_{MAX}		1		V/V
CMRR	ΔV_{OCM} = 1.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−80	−77	dB
	T_{MIN} to T_{MAX}		−76		dB

5 V GENERAL PERFORMANCE

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			5		V
Quiescent Current per Amplifier	Enabled	31.1	34	38.4	mA
	Enabled, T_{MIN} to T_{MAX} variation		74.5		µA/°C
	Disabled	0.45	1.8	2.6	mA
	T_{MIN} to T_{MAX}		2.7		mA
+PSRR	ΔV_{ICM} = 1 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−74	−71	dB
	T_{MIN} to T_{MAX}		−70		dB
−PSRR	ΔV_{ICM} = 1 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−91	−75	dB
	T_{MIN} to T_{MAX}		−78		dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Disabled		<2.5		V
	Enabled		>3		V
Turn-Off Time			1		µs
Turn-On Time			12		ns
$\overline{PD}$ Pin Bias Current					
Enabled	$\overline{PD}$ = 5 V		0.09		µA
Disabled	$\overline{PD}$ = 0 V		97		µA
OPERATING TEMPERATURE RANGE		−55		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−55°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD51-7.The θ_{JA} for the 16-Lead LFCSP(exposed pad) package is 81.6 °C/W.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4930-1-EP package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4930-1-EP. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends on the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation vs. the ambient temperature for the ADA4930-1-EP single 16-lead LFCSP (81.6°C/W) on a JEDEC standard 4-layer board.

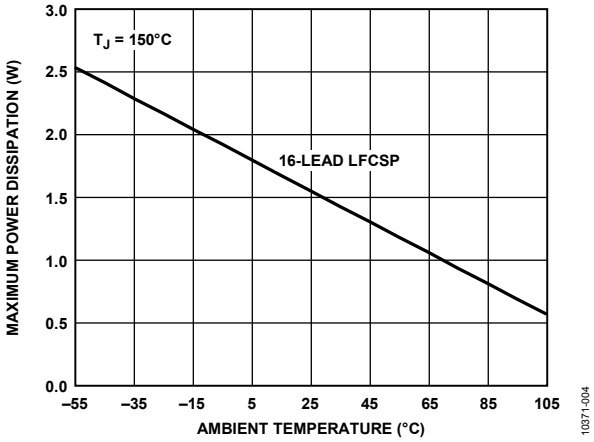

Figure 3. Maximum Power Dissipation vs. Ambient Temperature, 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

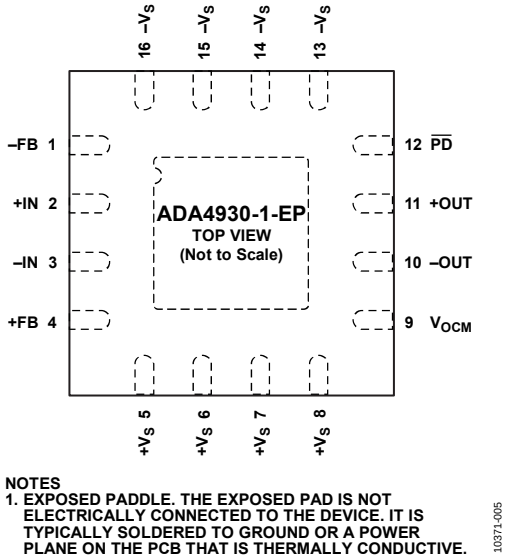

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection.
2	+IN	Positive Input Summing Node.
3	−IN	Negative Input Summing Node.
4	+FB	Positive Output for Feedback Component Connection.
5 to 8	$+V_S$	Positive Supply Voltage.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output for Load Connection.
11	−OUT	Negative Output for Load Connection.
12	$\overline{PD}$	Power-Down Pin.
13 to 16	$-V_S$	Negative Supply Voltage.
	EPAD	Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive.

OUTLINE DIMENSIONS

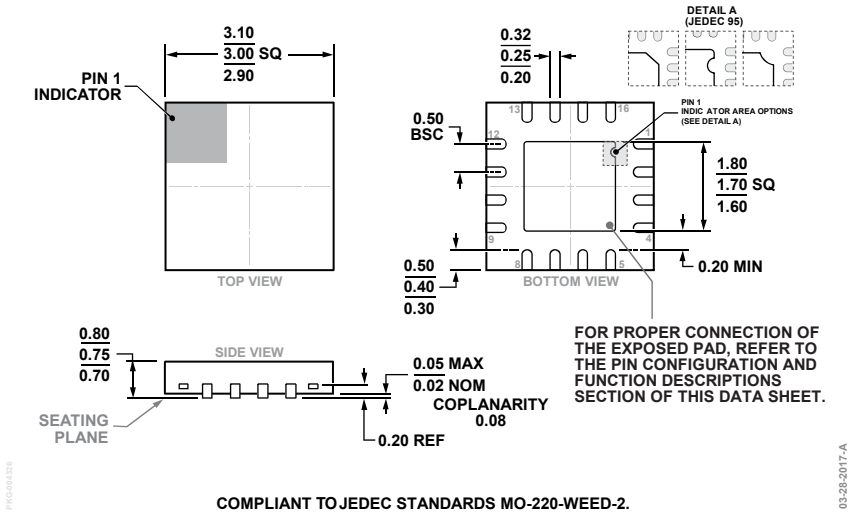

Figure 5. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-35)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4930-1SCPZ-EPR2	−55°C to +105°C	16-Lead LFCSP	CP-16-35	250	H2X
ADA4930-1SCPZ-EPR7	−55°C to +105°C	16-Lead LFCSP	CP-16-35	1,500	H2X
ADA4930-1SCPZ-EPRL	−55°C to +105°C	16-Lead LFCSP	CP-16-35	5,000	H2X

[1] Z = RoHS Compliant Part.

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