Data Sheet

ADA4077-1/ADA4077-2/ADA4077-4

4 MHz, 7 nV/√Hz, Low Offset and Drift, High Precision Amplifiers

FEATURES

- Offset voltage:
  - 25 μV maximum at 25°C (B grade, 8-lead SOIC, single/ dual)
  - 50 μV maximum at 25°C (A grade, 8-lead SOIC, single/ dual)
  - 50 μV maximum at 25°C (A grade, 14-lead SOIC, quad)
- Offset voltage drift:
  - 0.25 μV/°C maximum (B grade, 8-lead SOIC, single/dual)
  - 0.55 μV/°C maximum (A grade, 8-lead SOIC, single/dual)
  - 0.75 μV/°C maximum (A grade, 14-lead SOIC, quad)
- MSL1 rated
- Low input bias current: 1 nA maximum at T_A = 25°C
- Low voltage noise density: 6.9 nV/√Hz typical at f = 1000 Hz
- CMRR, PSRR, and A_V > 120 dB minimum
- Low supply current: 400 μA per amplifier typical
- Wide gain bandwidth product: 3.9 MHz at ±5 V
- Dual-supply operation:
  - Specified at ±5 V to ±15 V
  - Operates at ±2.5 V to ±15 V
- Unity gain stable
- No phase reversal
- Long-term offset voltage drift (10,000 hours): 0.5 μV typical
- Temperature hysteresis: 1 μV typical

APPLICATIONS

- Process control front-end amplifiers
- Optical network control circuits
- Instrumentation
- Precision sensors and controls
- Precision filters

PIN CONNECTION DIAGRAMS

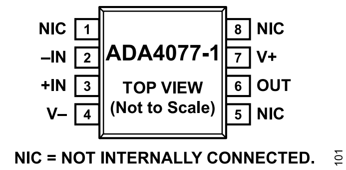

Figure 1. ADA4077-1, 8-Lead SOIC and 8-Lead MSOP

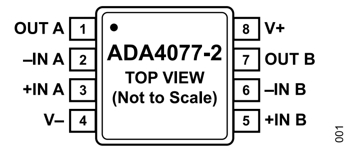

Figure 2. ADA4077-2, 8-Lead MSOP and 8-Lead SOIC

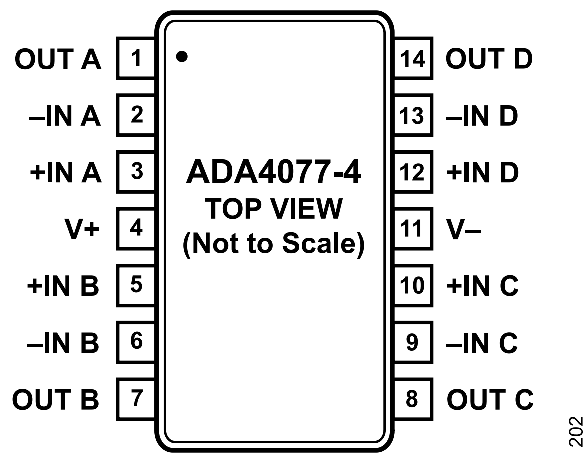

Figure 3. ADA4077-4, 14-Lead TSSOP and 14-Lead SOIC

GENERAL DESCRIPTION

The single ADA4077-1, dual ADA4077-2, and quad ADA4077-4 amplifiers feature extremely low offset voltage and drift, and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, resistance temperature detectors (RTDs), strain gages), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The ADA4077-1/ADA4077-2/ADA4077-4 are useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

Unlike other amplifiers, the ADA4077-1/ADA4077-2/ADA4077-4 have an MSL1 rating that is compliant with the most stringent of assembly processes, and they are specified over the extended industrial temperature range from −40°C to +125°C for the most demanding operating environments.

Table 1. Evolution of Precision Devices by Generation

Op Amp	First	Second	Third	Fourth	Fifth	Sixth
Single	OP07	OP77	OP177	OP1177	AD8677	ADA4077-1
Dual				OP2177		ADA4077-2
Quad				OP4177		ADA4077-4

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REVISION HISTORY

8/2022—Rev. E to Rev. F

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Changes to Typical Performance Characteristics Section ... 10

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SY} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
ADA4077-1/ADA4077-2						
B Grade, SOIC				10	25	µV
		−40°C < T_A < +125°C			65	µV
A Grade, SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
A Grade, MSOP				50	90	µV
		−40°C < T_A < +125°C			220	µV
ADA4077-4						
A Grade, SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
A Grade, TSSOP				15	120	µV
		−40°C < T_A < +125°C			220	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C				
ADA4077-1/ADA4077-2						
B Grade, SOIC				0.1	0.25	µV/°C
A Grade, SOIC				0.25	0.55	µV/°C
A Grade, MSOP				0.5	1.2	µV/°C
ADA4077-4						
A Grade, SOIC				0.4	0.75	µV/°C
A Grade, TSSOP				0.5	1.2	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA
		−40°C < T_A < +125°C	−1		+1	nA
Input Voltage Range			−3.8		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −3.8 V to +3 V	122	140		dB
		V_{CM} = −3.8 V to +3 V, −40°C < T_A < +85°C	120			dB
		V_{CM} = −3.8 V to +2.8 V, 85°C < T_A < 125°C	120			dB
Large Signal Voltage Gain	Av	R_L = 2 kΩ, V_O = −3.0 V to +3.0 V	121	130		dB
		−40°C < T_A < +125°C	120			dB
Input Capacitance	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	3.5			V
		−40°C < T_A < +125°C	3.2			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−3.5	V
		−40°C < T_A < +125°C			−3.2	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.6 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−40°C < T_A < +125°C	120			dB

SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	450	µA
		−40°C < T_A < +125°C			650	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/µs
Settling Time to 0.1%	t_S	V_{IN} = 1 V step, R_L = 2 kΩ, A_V = −1		3		µs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.9		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.9		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		55		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		µV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ELECTRICAL CHARACTERISTICS, ±15 V

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
ADA4077-1/ADA4077-2						
B Grade, SOIC				10	35	µV
		−40°C < T_A < +125°C			65	µV
A Grade, SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
A Grade, MSOP				50	90	µV
		−40°C < T_A < +125°C			220	µV
ADA4077-4						
A Grade, SOIC				15	50	µV
		−40°C < T_A < +125°C			105	µV
A Grade, TSSOP				15	120	µV
		−40°C < T_A < +125°C			220	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					
ADA4077-1/ADA4077-2						
B Grade, SOIC		−40°C < T_A < +125°C		0.1	0.25	µV/°C
A Grade, SOIC		−40°C < T_A < +125°C		0.25	0.55	µV/°C
A Grade, MSOP		−40°C < T_A < +125°C		0.5	1.2	µV/°C
ADA4077-4						
A Grade, SOIC		−40°C < T_A < +125°C		0.4	0.75	µV/°C
A Grade, TSSOP		−40°C < T_A < +125°C		0.5	1.2	µV/°C
Input Bias Current	I_B		−1	−0.4	+1	nA
		−40°C < T_A < +125°C	−1.5		+1.5	nA
Input Offset Current	I_{OS}		−0.5	+0.1	+0.5	nA

SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		−40°C < T_A < +125°C	−1		+1	nA
Input Voltage Range			−13.8		+13	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.8 V to +13 V	132	150		dB
		−40°C < T_A < +125°C	130			dB
Large Signal Voltage Gain	Av					
ADA4077-1/ADA4077-2 (SOIC, MSOP)		R_L = 2 kΩ, V_O = −13.0 V to +13.0 V	125	130		dB
		−40°C < T_A < +125°C	120			dB
ADA4077-4 (SOIC, TSSOP)		R_L = 2 kΩ, V_O = −13.0 V to +13.0 V	122	130		dB
		−40°C < T_A < +125°C	120			dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA	13.5			V
		−40°C < T_A < +125°C	13.2			V
Output Voltage Low	V_{OL}	I_L = 1 mA			−13.5	V
		−40°C < T_A < +125°C			−13.2	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short-Circuit Current	I_{SC}	T_A = 25°C		22		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ±18 V	123	128		dB
		−40°C < T_A < +125°C	120			dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		400	500	μA
		−40°C < T_A < +125°C			650	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1.2		V/μs
Settling Time to 0.01%	t_s	V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		16		μs
Settling Time to 0.1%	t_s	V_{IN} = 10 V p-p, R_L = 2 kΩ, A_V = −1		10		μs
Gain Bandwidth Product	GBP	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +100		3.6		MHz
Unity-Gain Crossover	UGC	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		3.9		MHz
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = +1, V_{IN} = 10 mV p-p, R_L = 2 kΩ		5.5		MHz
Phase Margin	ΦM	V_{IN} = 10 mV p-p, R_L = 2 kΩ, A_V = +1		58		Degrees
Total Harmonic Distortion Plus Noise	THD + N	V_{IN} = 1 V rms, A_V = +1, R_L = 2 kΩ, f = 1 kHz		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		μV p-p
Voltage Noise Density	e_n	f = 1 Hz		13		nV/√Hz
		f = 100 Hz		7		nV/√Hz
		f = 1000 Hz		6.9		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	f = 1 kHz, R_L = 10 kΩ		−125		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Input Current[1]	±10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Maximum Reflow Temperature (MSL1 Rating)[2]	260°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)[3]	6 kV
Field Induced Charge Device Model (FICDM)[4]	1.25 kV

1 The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

2 IPC/JEDEC J-STD-020 applicable standard

3 ESDA/JEDEC JS-001-2011 applicable standard.

4 JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W
14-Lead TSSOP	240	43	°C/W
14-Lead SOIC	115	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

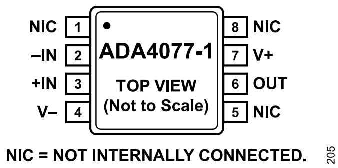

Figure 4. ADA4077-1 Pin Configuration, 8-Lead MSOP (RM-8)

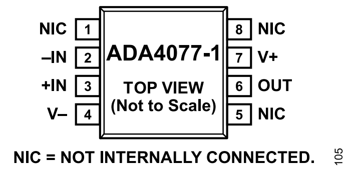

Figure 5. ADA4077-1 Pin Configuration, 8-Lead SOIC (R-8)

Table 6. ADA4077-1 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not internally connected.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	V−	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

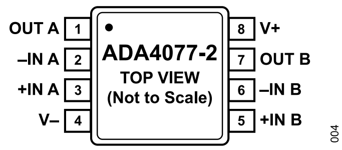

Figure 6. ADA4077-2 Pin Configuration, 8-Lead MSOP

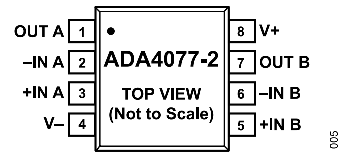

Figure 7. ADA4077-2 Pin Configuration, 8-Lead SOIC

Table 7. ADA4077-2 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

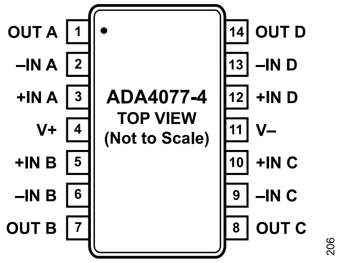

Figure 8. ADA4077-4 Pin Configuration, 14-Lead TSSOP

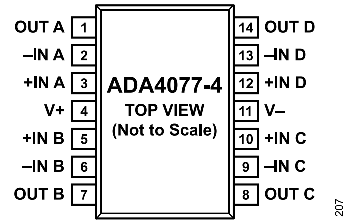

Figure 9. ADA4077-4 Pin Configuration, 14-Lead SOIC

Table 8. ADA4077-4 Pin Function Descriptions, 14-Lead TSSOP and 14-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Negative Input Channel A.
3	+IN A	Positive Input Channel A.
4	V+	Positive Supply Voltage.
5	+IN B	Positive Input Channel B.
6	−IN B	Negative Input Channel B.
7	OUT B	Output Channel B.
8	OUT C	Output Channel C.
9	−IN C	Negative Input Channel C.
10	+IN C	Positive Input Channel C.
11	V−	Negative Supply Voltage.
12	+IN D	Positive Input Channel D.
13	−IN D	Negative Input Channel D.
14	OUT D	Output Channel D.

TYPICAL PERFORMANCE CHARACTERISTICS

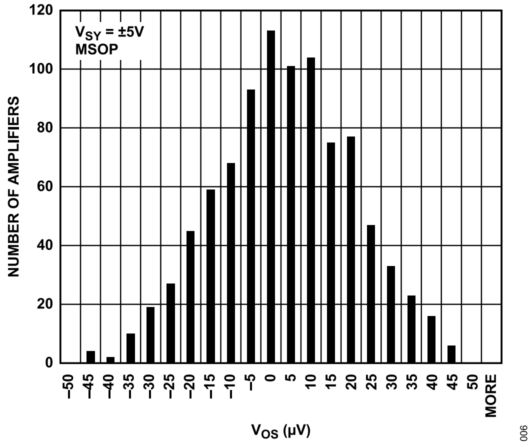

Figure 10. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

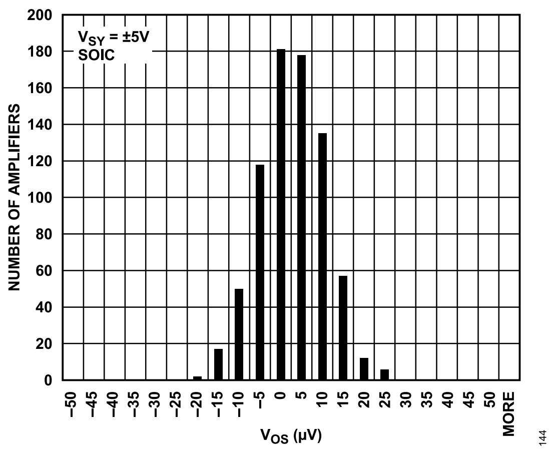

Figure 11. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

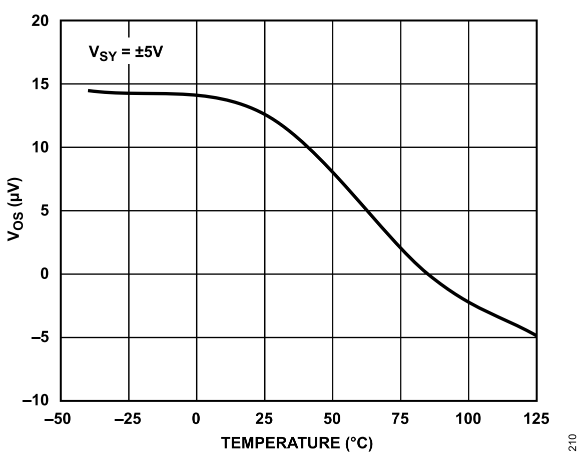

Figure 12. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±5 V

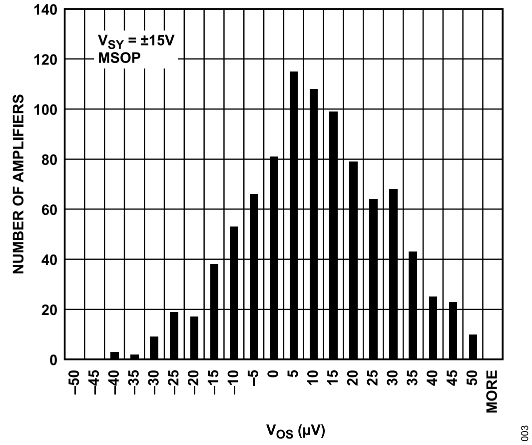

Figure 13. ADA4077-2 Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

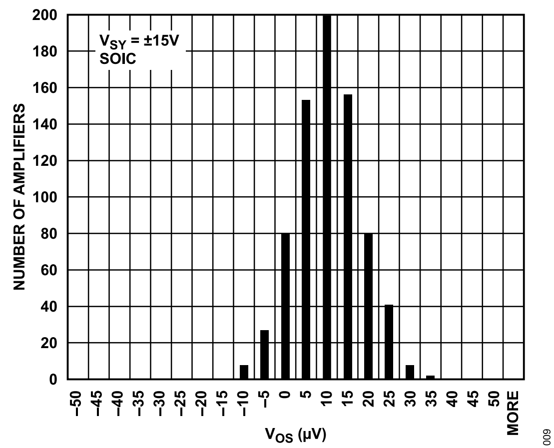

Figure 14. Offset Voltage (V_{OS}) Distribution, V_{SY} = ±15 V

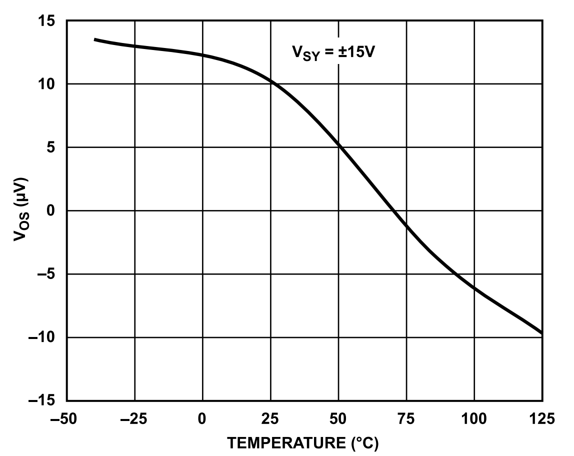

Figure 15. Offset Voltage (V_{OS}) vs. Temperature, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

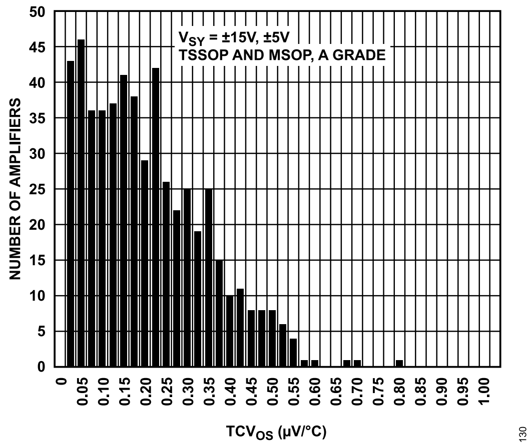

Figure 16. TCV_{OS} Distribution (TSSOP and MSOP, A Grade)

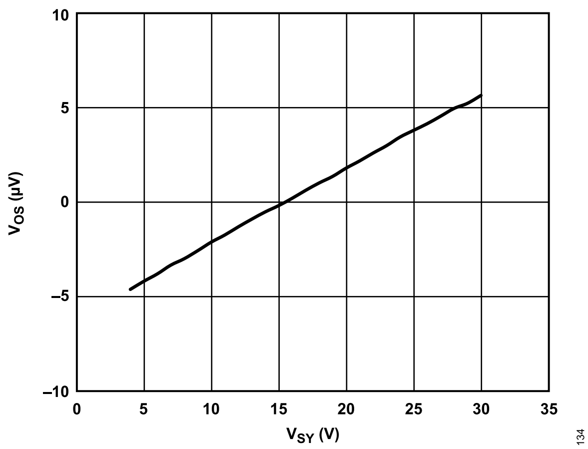

Figure 17. Offset Voltage (V_{OS}) vs. Power Supply Voltage (V_{SY})

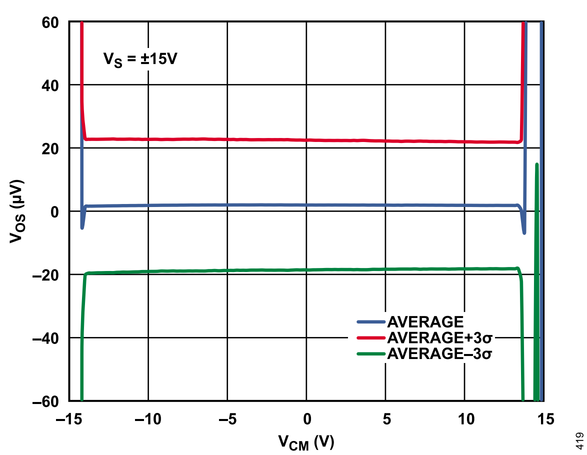

Figure 18. Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = ±15 V

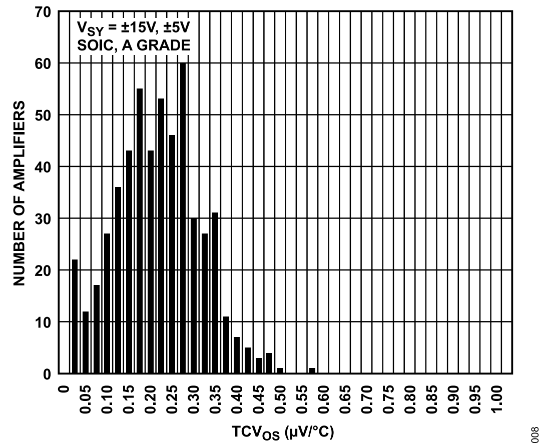

Figure 19. TCV_{OS} Distribution (SOIC, A Grade)

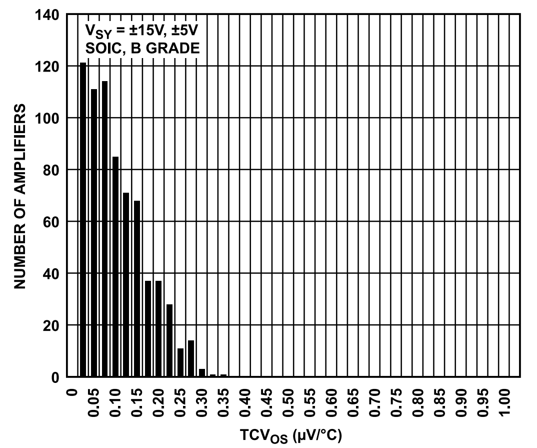

Figure 20. TCV_{OS} Distribution (SOIC, B Grade)

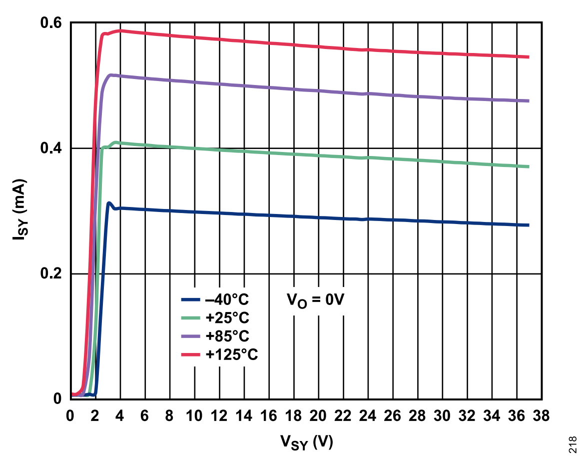

Figure 21. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

TYPICAL PERFORMANCE CHARACTERISTICS

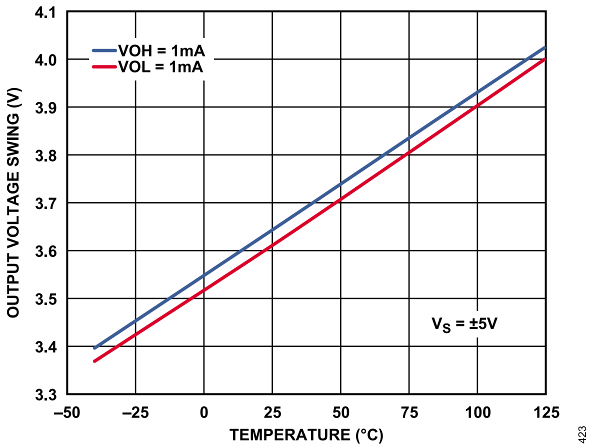

Figure 22. Output Voltage Swing vs. Temperature, V_{SY} = ±5 V

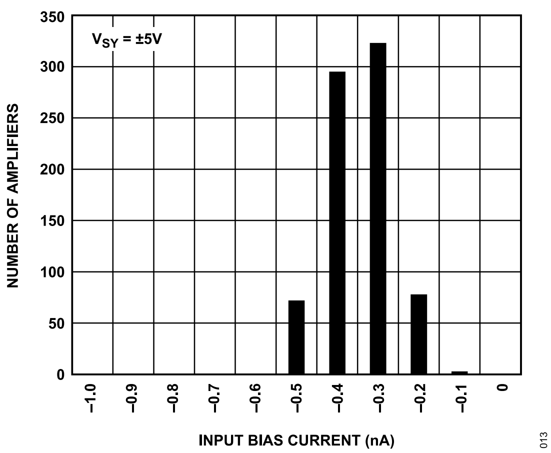

Figure 23. Input Bias Current Distribution, V_{SY} = ±5 V

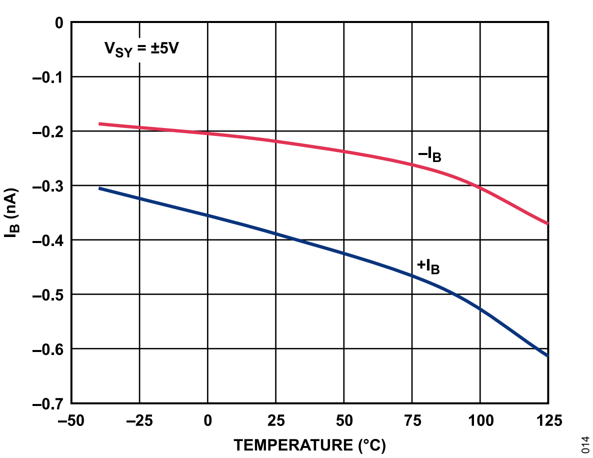

Figure 24. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±5 V

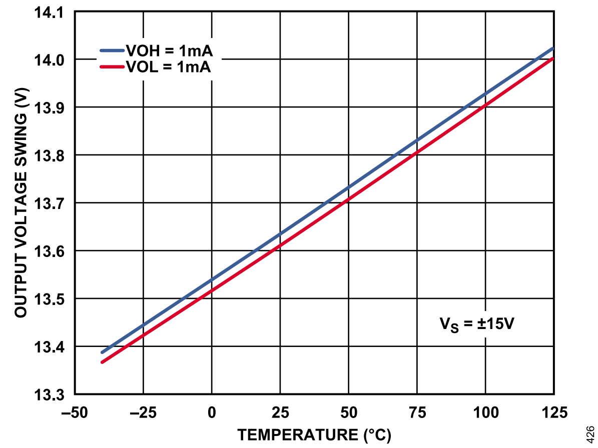

Figure 25. Output Voltage Swing vs. Temperature, V_{SY} = ±15 V

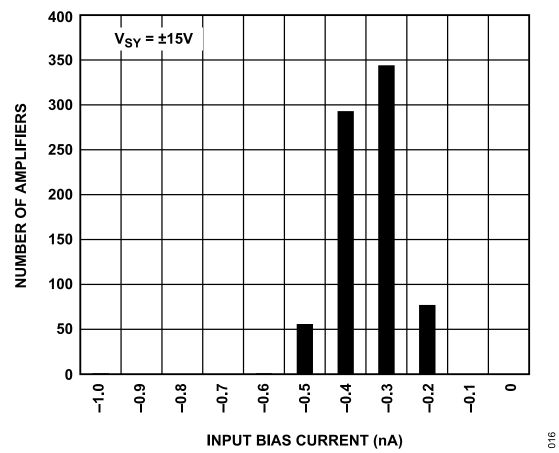

Figure 26. Input Bias Current Distribution, V_{SY} = ±15 V

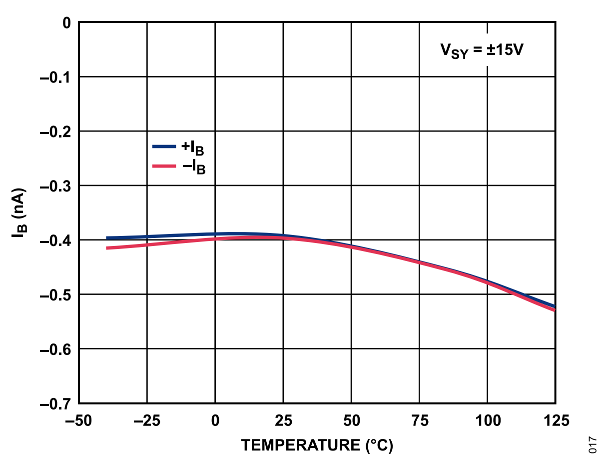

Figure 27. Input Bias Current (I_B) vs. Temperature, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

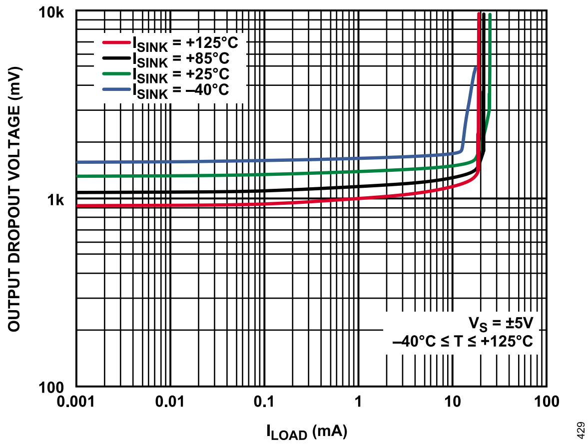

Figure 28. Output Dropout Voltage vs. I_{LOAD}, Sink Current, V_{SY} = ±5 V

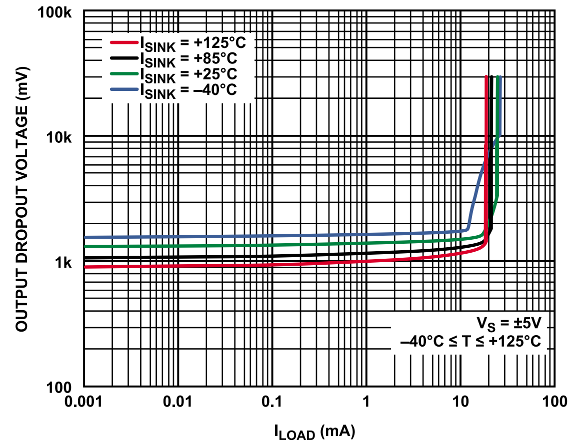

Figure 31. Output Dropout Voltage vs. I_{LOAD}, Sink Current, V_{SY} = ±15 V

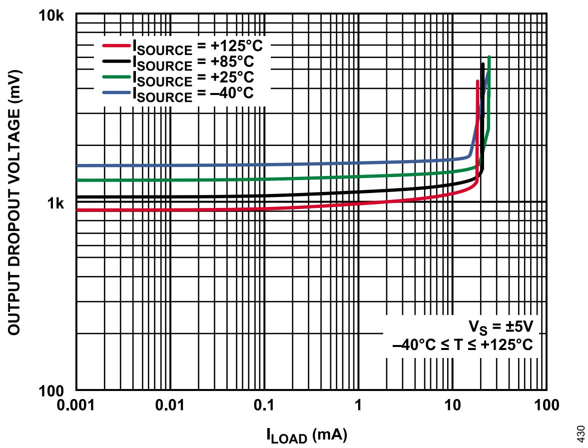

Figure 29. Output Dropout Voltage vs. I_{LOAD}, Source Current, V_{SY} = ±5 V

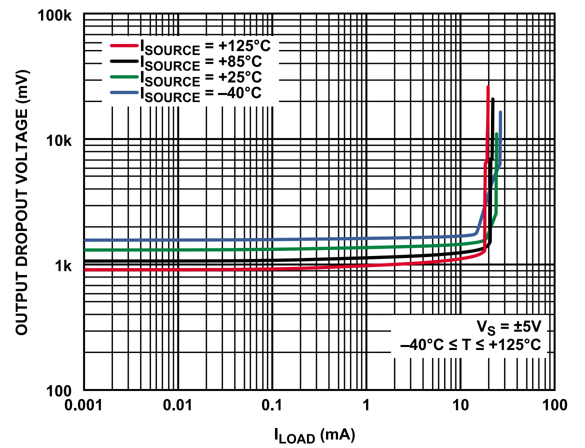

Figure 32. Output Dropout Voltage vs. I_{LOAD}, Source Current, V_{SY} = ±15 V

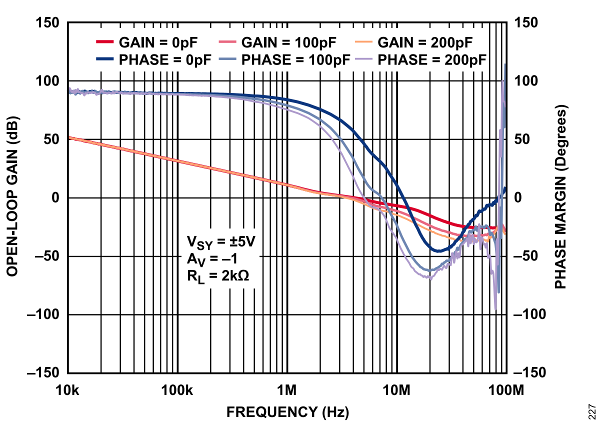

Figure 30. Open-Loop Gain and Phase Margin vs. Frequency, V_{SY} = ±5 V

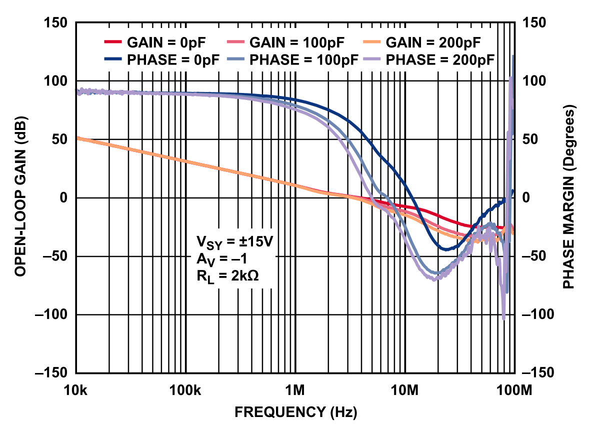

Figure 33. Open-Loop Gain and Phase Margin vs. Frequency, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

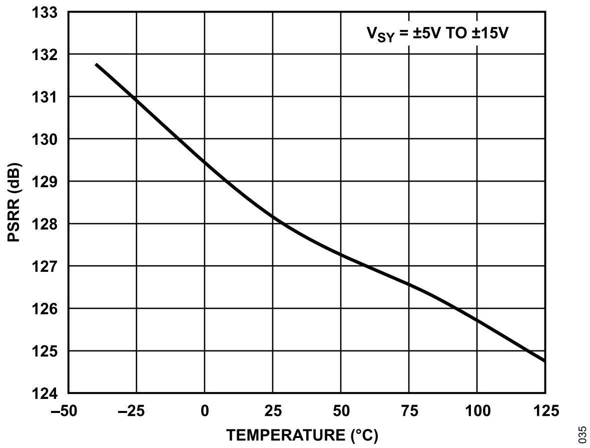

Figure 34. PSRR vs. Temperature, V_{SY} = ±5 V to ±15 V

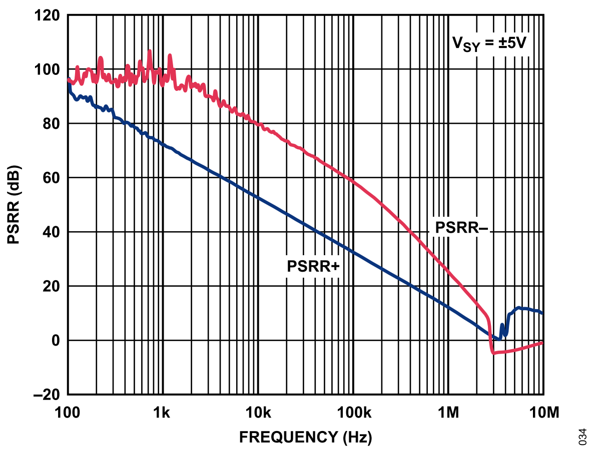

Figure 35. PSRR vs. Frequency, V_{SY} = ±5 V

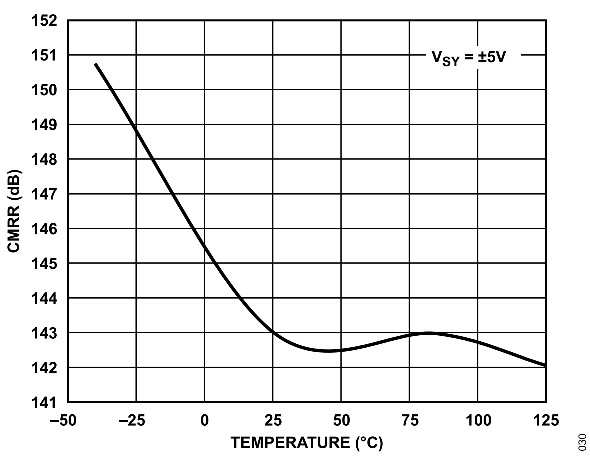

Figure 36. CMRR vs. Temperature, V_{SY} = ±5 V

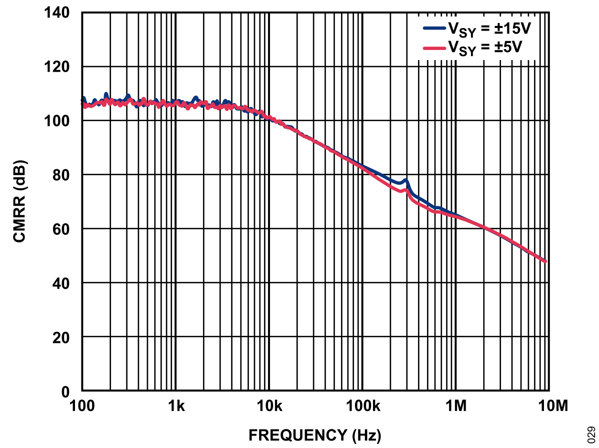

Figure 37. CMRR vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

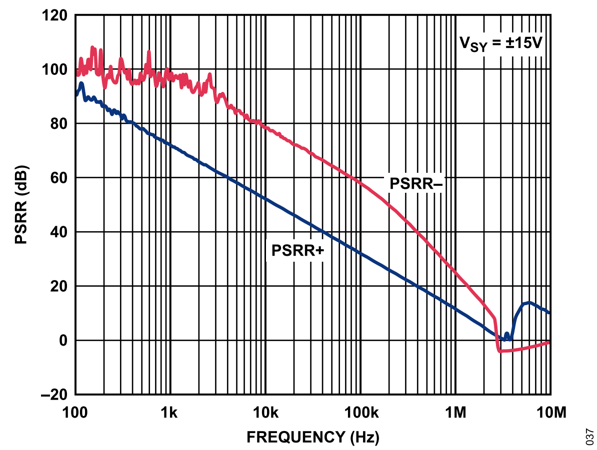

Figure 38. PSRR vs. Frequency, V_{SY} = ±15 V

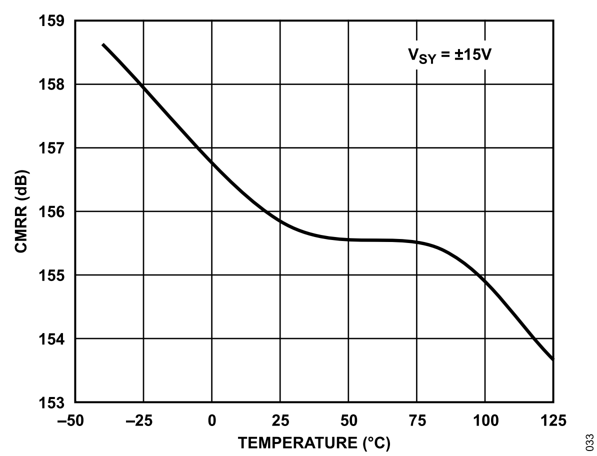

Figure 39. CMRR vs. Temperature, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

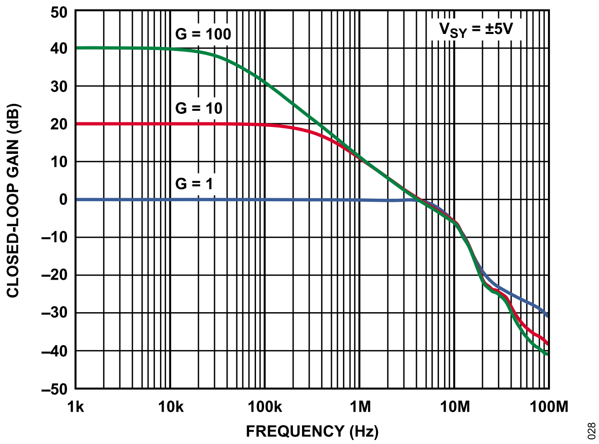

Figure 40. Closed-Loop Gain vs. Frequency, V_{SY} = ±5 V

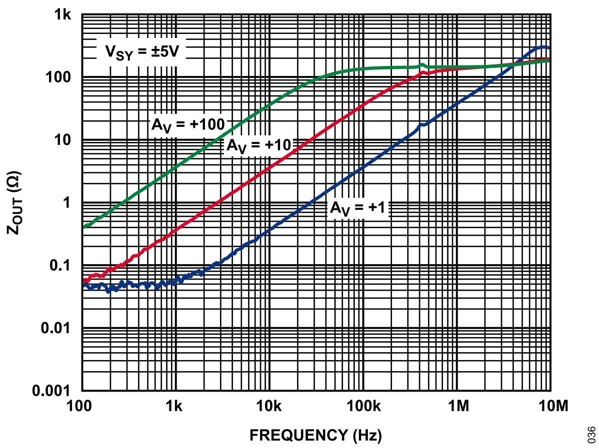

Figure 41. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±5 V

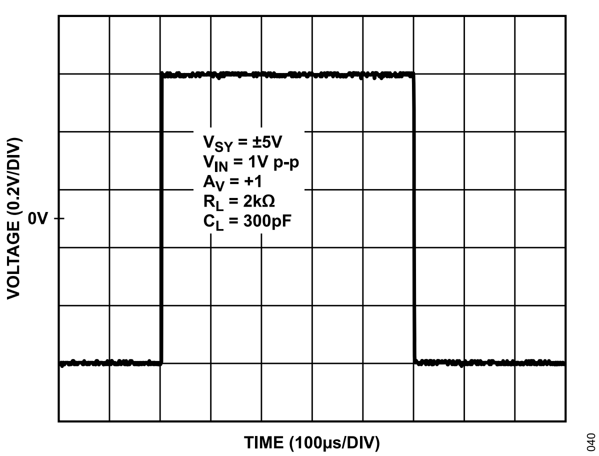

Figure 42. Large Signal Transient Response, V_{SY} = ±5 V

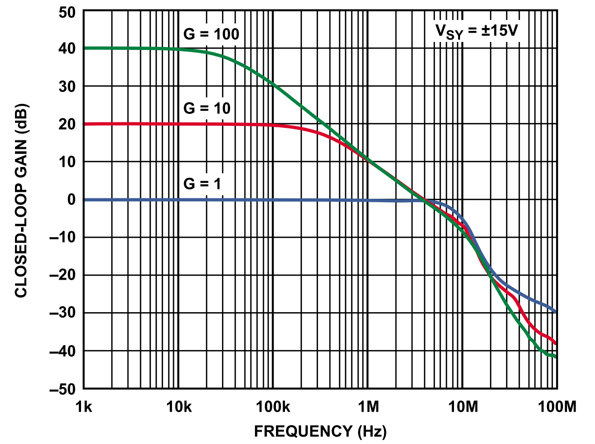

Figure 43. Closed-Loop Gain vs. Frequency, V_{SY} = ±15 V

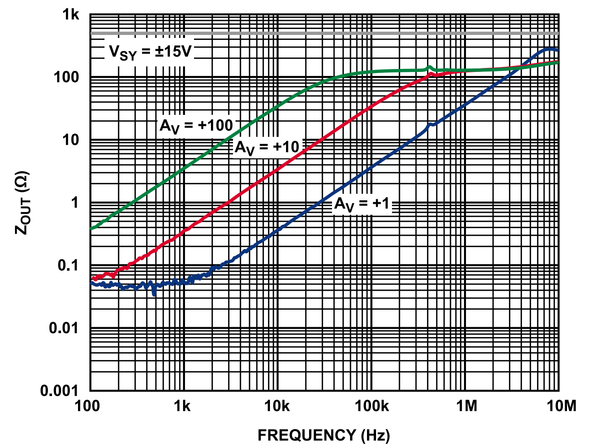

Figure 44. Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = ±15 V

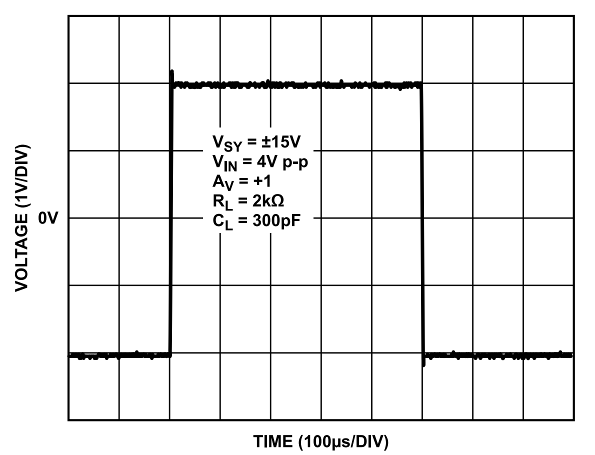

Figure 45. Large Signal Transient Response, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

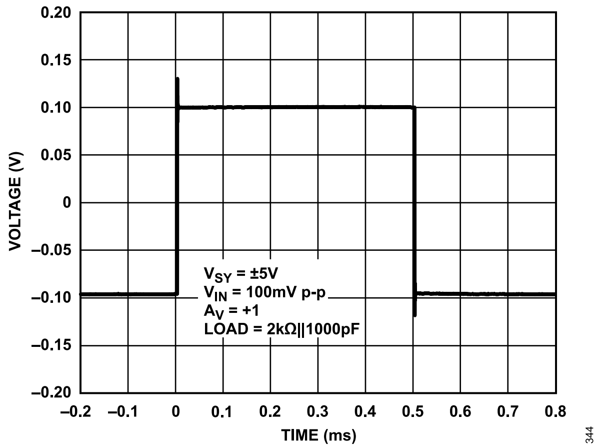

Figure 46. Small Signal Transient Response, V_{SY} = ±5 V

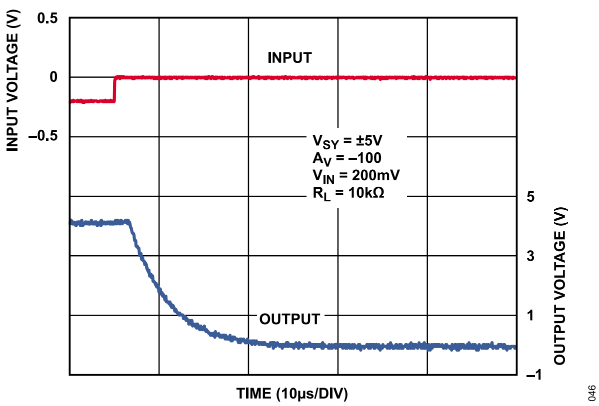

Figure 47. Positive Overload Recovery, V_{SY} = ±5 V

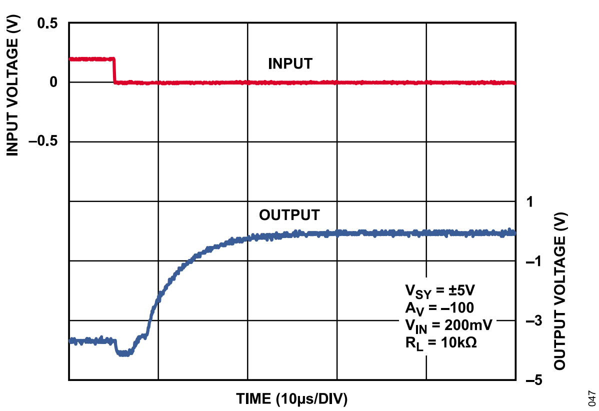

Figure 48. Negative Overload Recovery, V_{SY} = ±5 V

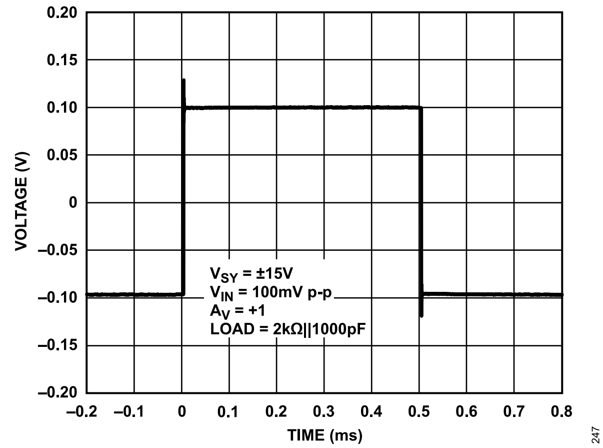

Figure 49. Small Signal Transient Response, V_{SY} = ±15 V

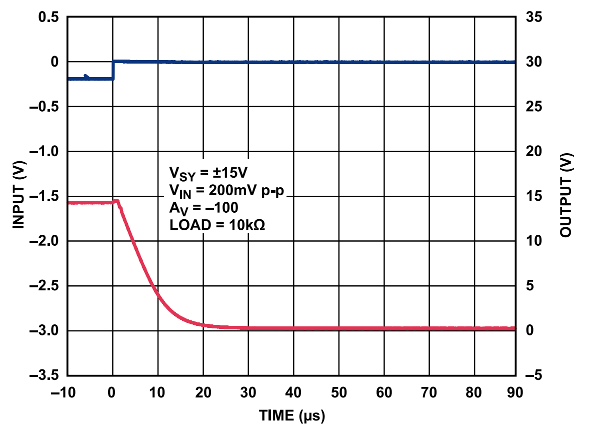

Figure 50. Positive Overload Recovery, V_{SY} = ±15 V

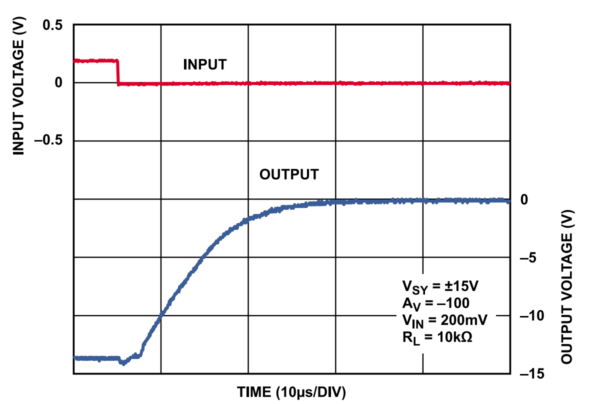

Figure 51. Negative Overload Recovery, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

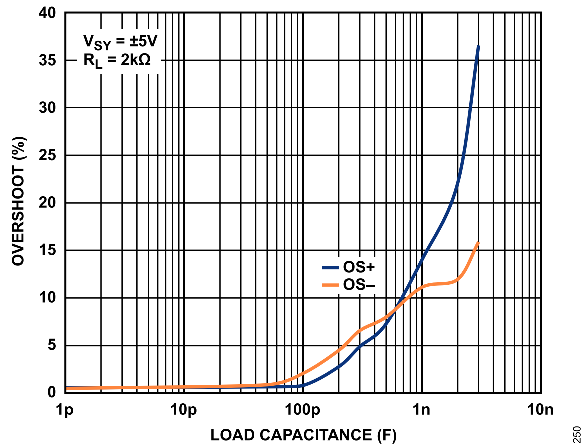

Figure 52. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±5 V

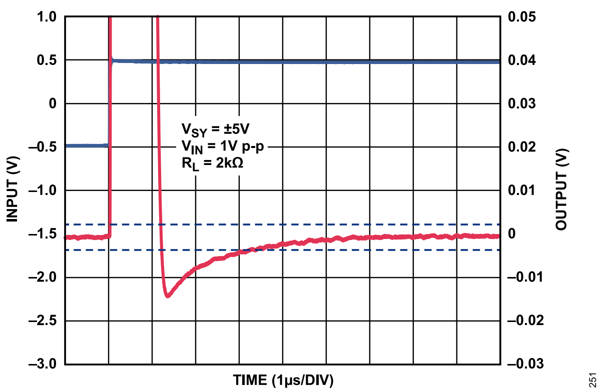

Figure 53. Positive 0.1% Settling Time, V_{SY} = ±5 V

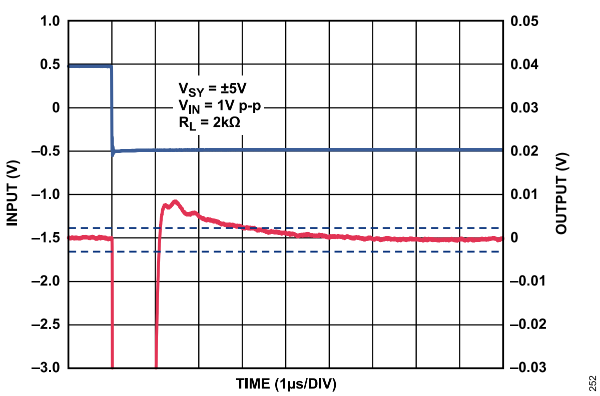

Figure 54. Negative 0.1% Settling Time, V_{SY} = ±5 V

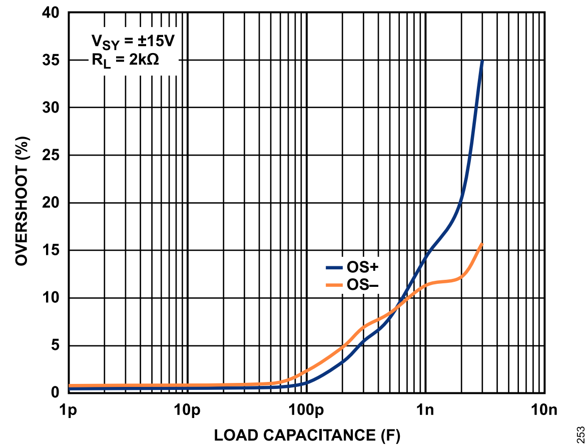

Figure 55. Small Signal Overshoot vs. Load Capacitance, V_{SY} = ±15 V

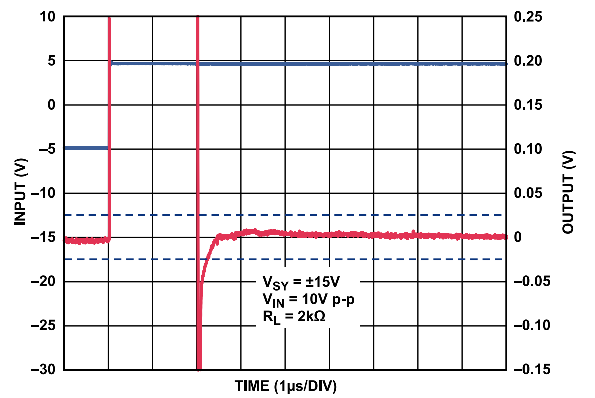

Figure 56. Positive 0.1% Settling Time, V_{SY} = ±15 V

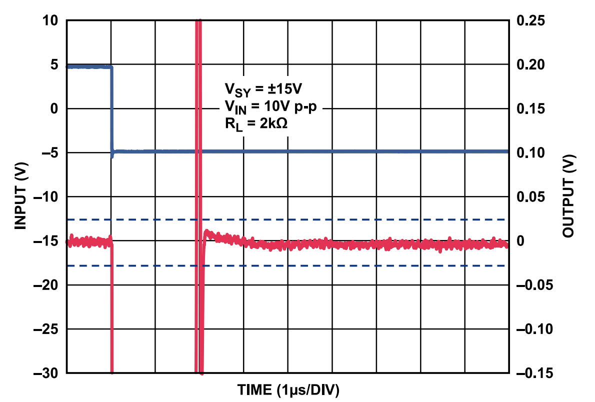

Figure 57. Negative 0.1% Settling Time, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

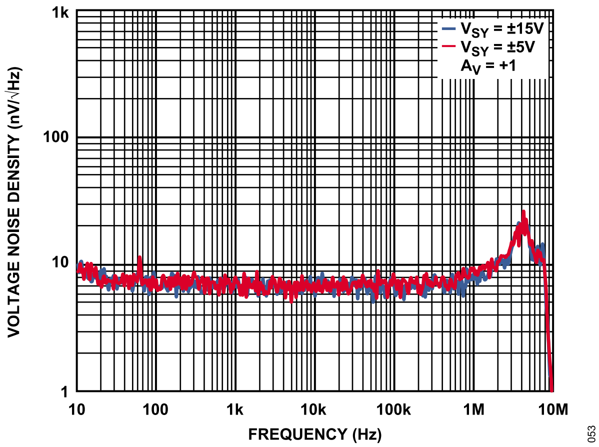

Figure 58. Voltage Noise Density vs. Frequency, V_{SY} = ±5 V and V_{SY} = ±15 V

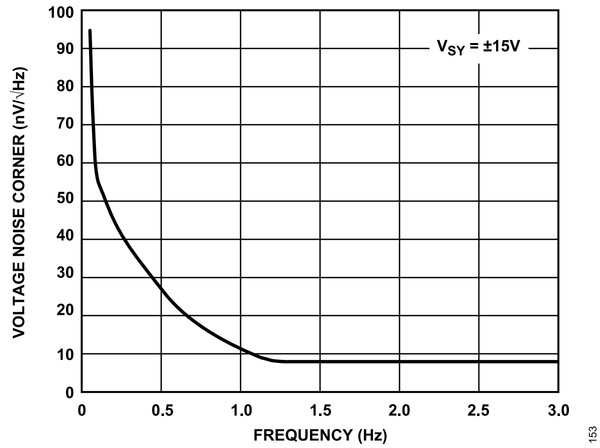

Figure 61. Voltage Noise Corner vs. Frequency, V_{SY} = ±15 V and V_{SY} = ±5 V

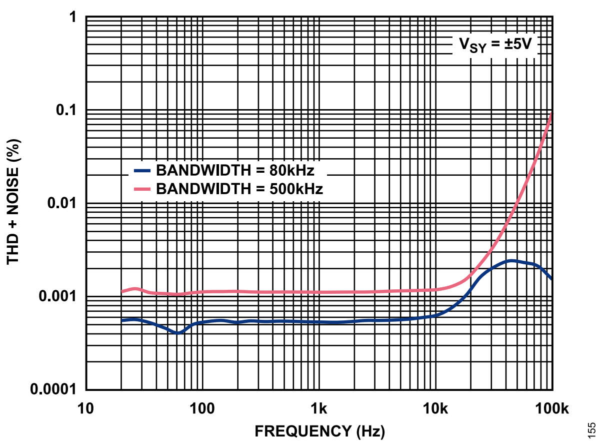

Figure 59. THD + Noise vs. Frequency, V_{SY} = ±5 V

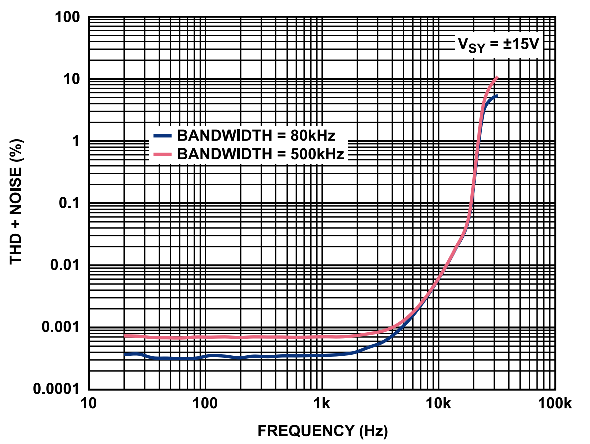

Figure 62. THD + Noise vs. Frequency, V_{SY} = ±15 V

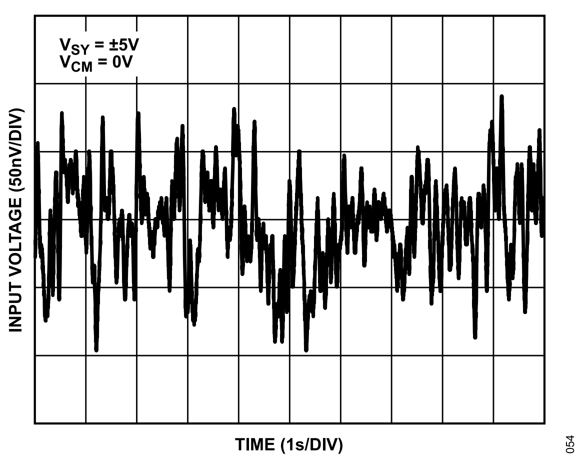

Figure 60. 0.1 Hz to 10 Hz Noise, V_{SY} = ±5 V

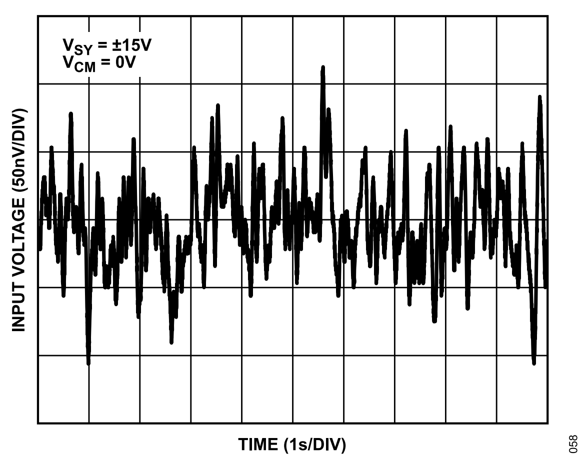

Figure 63. 0.1 Hz to 10 Hz Noise, V_{SY} = ±15 V

TYPICAL PERFORMANCE CHARACTERISTICS

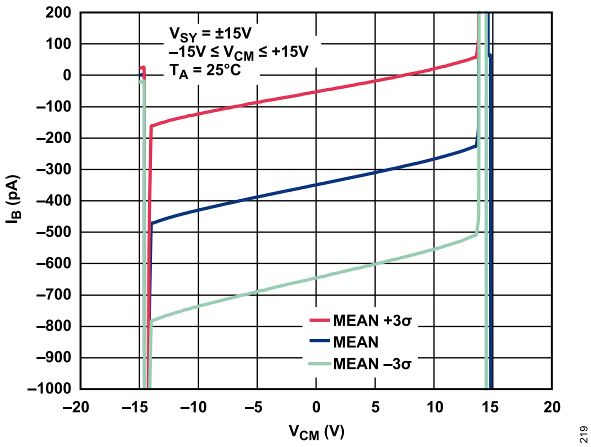

Figure 64. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM})

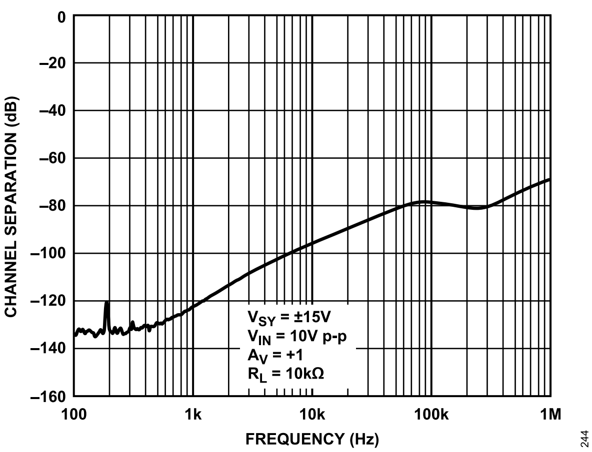

Figure 65. Channel Separation, V_{SY} = ±15 V (See Figure 69)

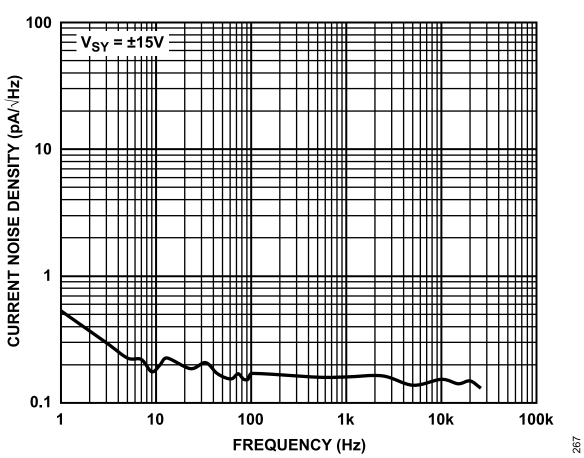

Figure 66. Current Noise Density, V_{SY} = ±15 V

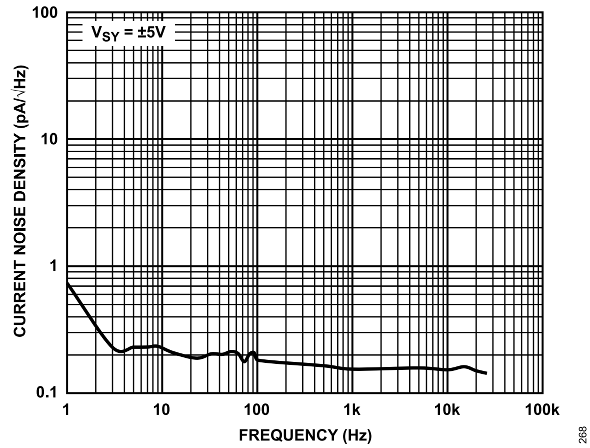

Figure 67. Current Noise Density, V_{SY} = ±5 V

TEST CIRCUIT

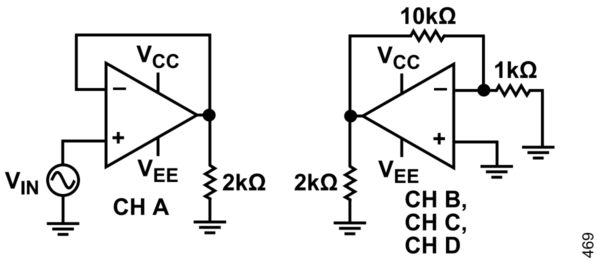

Figure 68. Test Circuit for Channel Separation vs. Frequency

THEORY OF OPERATION

The ADA4077-1/ADA4077-2/ADA4077-4 are the sixth generation of the Analog Devices, Inc., industry-standard OP07 amplifier family. The ADA4077-1/ADA4077-2/ADA4077-4 are high precision, low noise operational amplifiers with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced high voltage amplifiers with superior performance to the OP07/OP77/OP177/OP1177 in tiny, 8-lead SOIC and 8-lead MSOP packages (ADA4077-1 and ADA4077-2) and 14-lead TSSOP and 14-lead SOIC packages (ADA4077-4). Despite their small size, the ADA4077-1/ADA4077-2/ADA4077-4 offer numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The ADA4077-1/ADA4077-2/ADA4077-4 have an operating temperature range of −40°C to +125°C with an MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This MSL1 rating is increasingly important as printed circuit board (PCB) and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the ADA4077-1/ADA4077-2/ADA4077-4, the power consumption is reduced by a factor of four compared to the OP177, and the bandwidth and slew rate are both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also reduce warmup drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this phase reversal can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ADA4077-1/ADA4077-2/ADA4077-4 are immune to phase reversal problems even at input voltages beyond the power supply settings.

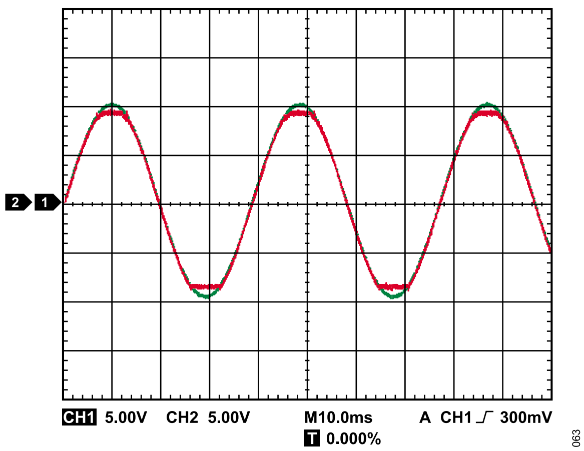

Figure 69. No Phase Reversal

LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is an RTD thermometer amplifier, as shown in Figure 70. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs can have a thermal resistance as high as 0.5°C/mW to 0.8°C/mW. To minimize errors due to resistor drift, keep the current low through each leg of the bridge. In this circuit, the amplifier supply current flows through the bridge. However, at a maximum supply current of 500 µA for the ADA4077-2, the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Therefore, errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge is made at the minimum value of the temperature to be measured by adjusting R_P until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint, and apply a 500°C temperature to the sensor, or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance, and adjust the linearity potentiometer for a 2.5 V output. The circuit achieves higher than ±0.5°C accuracy after adjustment.

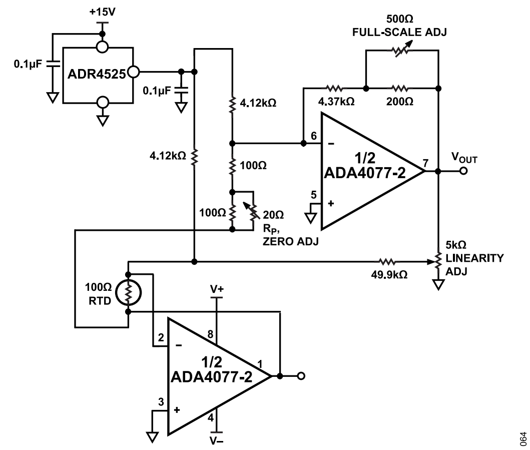

Figure 70. Low Power Linearized RTD Circuit

PROPER BOARD LAYOUT

The ADA4077-1/ADA4077-2/ADA4077-4 are high precision devices. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture free board surface. Coating the surface creates a barrier to moisture accumulation, and reduces parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes the power supply disturbances caused by the output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that the signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Ensure, where possible, that input signal paths contain matching numbers and types of components, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other, and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces electromagnetic interference (EMI) noise and maintains a constant temperature across the circuit board.

LONG-TERM DRIFT

The stability of a precision signal path over its lifetime or between calibration procedures is dependent on the long-term stability of the

APPLICATIONS INFORMATION

analog components in the path, such as op amps, references, and data converters. To help system designers predict the long-term drift of circuits that use the ADA4077-1/ADA4077-2/ADA4077-4, Analog Devices measured the offset voltage of multiple units for 10,000 hours (more than 13 months) using a high precision measurement system, including an ultrastable oil bath. To replicate real-world system performance, the devices under test (DUTs) were soldered onto an FR4 PCB using a standard reflow profile (as defined in the JEDEC J-STD-020D standard), as opposed to testing them in sockets. This manner of testing is important because expansion and contraction of the PCB can apply stress to the integrated circuit (IC) package and contribute to shifts in the offset voltage.

The ADA4077-1/ADA4077-2/ADA4077-4 have extremely low long-term drift (LTD). Figure 71 shows the LTD of the ADA4077-1 (SOIC package). The red, blue, and green traces show sample units. Note that the mean drift over 10,000 hours is less than 0.5 µV, or less than 2% of their maximum specified offset voltage of 25 µV at room temperature.

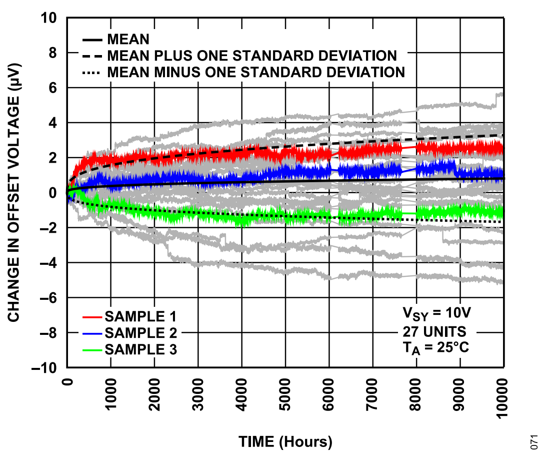

Figure 71. Measured Long-Term Drift of the ADA4077-1/ADA4077-2/ ADA4077-4 Offset Voltage over 10,000 Hours

TEMPERATURE HYSTERESIS

In addition to stability over time as described in the Long-Term Drift section, it is useful to know the temperature hysteresis, that is, the stability vs. cycling of temperature. Hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and subsequent return to room temperature. Figure 72 shows the change in input offset voltage as the temperature cycles three times from room temperature to 125°C to −40°C and back to room temperature. The dotted line is an initial preconditioning cycle to eliminate the original temperature-induced offset shift from exposure to production solder reflow temperatures. In the three full cycles, the offset hysteresis is typically only 1 µV, or 1.5% of its 65 µV maximum offset voltage over the full operating temperature range. The histogram in Figure 73 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to 125°C and back to room temperature.

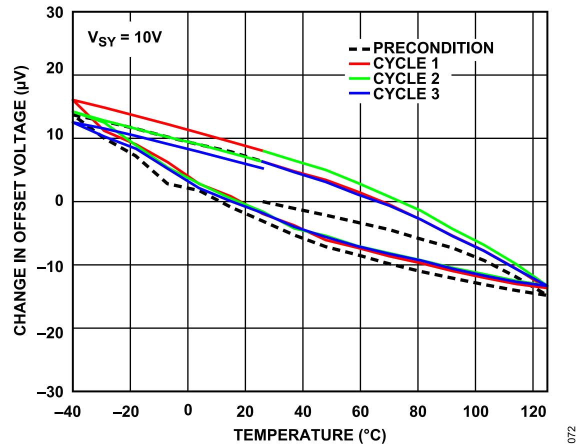

Figure 72. Change in Offset Voltage over Three Full Temperature Cycles

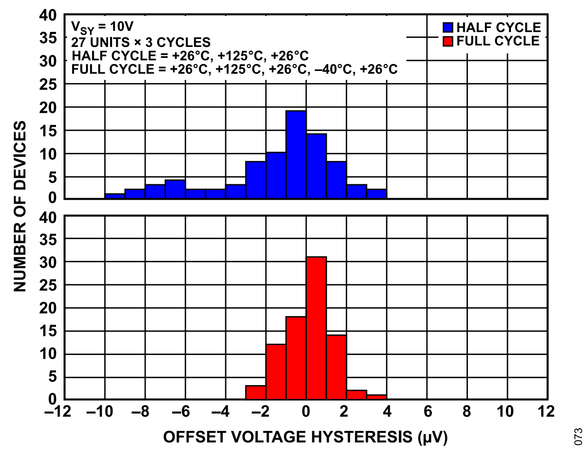

Figure 73. Histogram Showing the Temperature Hysteresis of the Offset Voltage over Three Full Cycles and over Three Half Cycles

OUTLINE DIMENSIONS

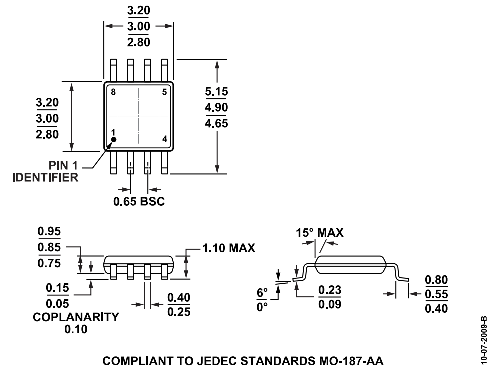

Figure 74. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

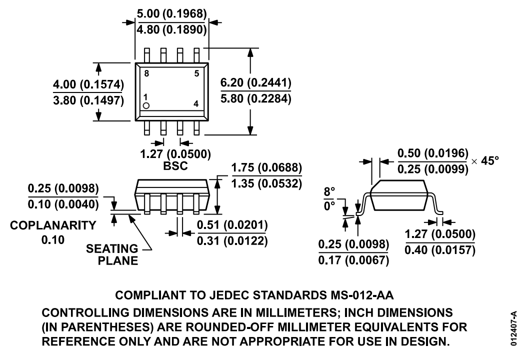

Figure 75. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

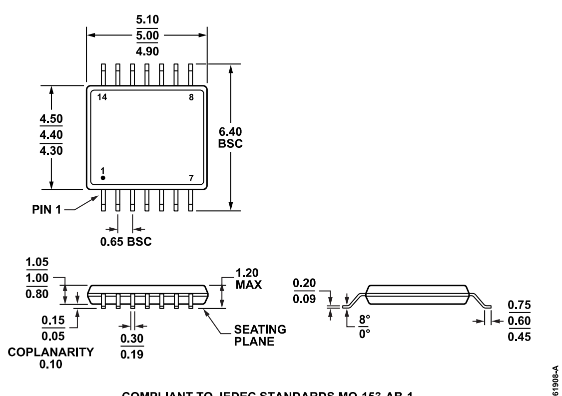

Figure 76. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

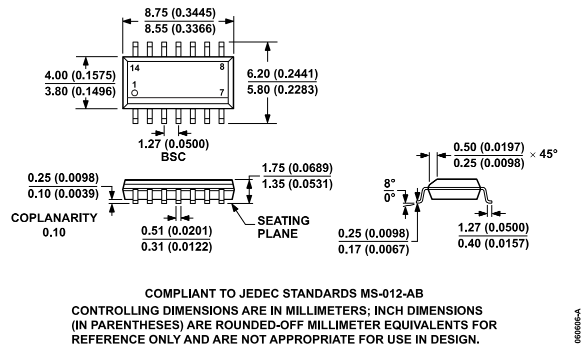

Figure 77. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

Updated: July 18, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
ADA4077-1ARMZ	-40°C to +125°C	8-Lead MSOP		RM-8	A35
ADA4077-1ARMZ-R7	-40°C to +125°C	8-Lead MSOP	Reel, 1000	RM-8	A35
ADA4077-1ARMZ-RL	-40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A35
ADA4077-1ARZ	-40°C to +125°C	8-Lead SOIC		R-8	
ADA4077-1ARZ-R7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8	
ADA4077-1ARZ-RL	-40°C to +125°C	8-Lead SOIC	Reel, 2500	R-8	
ADA4077-1BRZ	-40°C to +125°C	8-Lead SOIC		R-8	
ADA4077-1BRZ-R7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8	
ADA4077-1BRZ-RL	-40°C to +125°C	8-Lead SOIC	Reel, 2500	R-8	
ADA4077-2ARMZ	-40°C to +125°C	8-Lead MSOP		RM-8	A2X
ADA4077-2ARMZ-R7	-40°C to +125°C	8-Lead MSOP	Reel, 1000	RM-8	A2X
ADA4077-2ARMZ-RL	-40°C to +125°C	8-Lead MSOP	Reel, 3000	RM-8	A2X
ADA4077-2ARZ	-40°C to +125°C	8-Lead SOIC		R-8	
ADA4077-2ARZ-R7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8	
ADA4077-2ARZ-RL	-40°C to +125°C	8-Lead SOIC	Reel, 2500	R-8	
ADA4077-2BRZ	-40°C to +125°C	8-Lead SOIC		R-8	
ADA4077-2BRZ-R7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8	
ADA4077-2BRZ-RL	-40°C to +125°C	8-Lead SOIC	Reel, 2500	R-8	
ADA4077-4ARUZ	-40°C to +125°C	14-Lead TSSOP		RU-14	
ADA4077-4ARUZ-R7	-40°C to +125°C	14-Lead TSSOP	Reel, 1000	RU-14	
ADA4077-4ARUZ-RL	-40°C to +125°C	14-Lead TSSOP	Reel, 2500	RU-14	
ADA4077-4ARZ	-40°C to +125°C	14-Lead SOIC		R-14	
ADA4077-4ARZ-R7	-40°C to +125°C	14-Lead SOIC	Reel, 1000	R-14	
ADA4077-4ARZ-RL	-40°C to +125°C	14-Lead SOIC	Reel, 2500	R-14	

[1] Z = RoHS Compliant Part.