



JFET Input Instrumentation Amplifier with Rail-to-Rail Output in MSOP Package

Enhanced Product

AD8220-EP

FEATURES

Low input currents

25 pA maximum input bias current

2 pA maximum input offset current

High CMRR

92 dB CMRR (minimum) to 60 Hz, $G = 10$

72 dB CMRR (minimum) at 5 kHz, $G = 1$

Excellent ac specifications and low power

1.5 MHz bandwidth ($G = 1$)

14 nV/ $\sqrt{\text{Hz}}$ input noise (1 kHz)

Slew rate: 2 V/ μs

1 mA maximum quiescent supply current

Versatile

MSOP package

Rail-to-rail output

Input voltage range to below negative supply rail

7 kV ESD HBM protection

4.5 V to 36 V single supply

± 2.25 V to ± 18 V dual supply

Gain set with single resistor ($G = 1$ to 1000)

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)

Extended industrial temperature range: -55°C to $+125^{\circ}\text{C}$

Controlled manufacturing baseline

1 assembly/test site

1 fabrication site

Product change notification

Qualification data available on request

APPLICATIONS

Medical instrumentation

Precision data acquisition

Transducer interfaces

GENERAL DESCRIPTION

The **AD8220-EP** is the first single-supply, JFET input instrumentation amplifier available in an MSOP package. Designed to meet the needs of high performance, portable instrumentation, the **AD8220-EP** has a minimum common-mode rejection ratio (CMRR) of 77 dB at dc and a minimum CMRR of 72 dB at 5 kHz for $G = 1$. Maximum input bias current at 25°C is 25 pA and remains below 100 nA over the entire extended industrial temperature range. Despite the JFET inputs, the **AD8220-EP** typically has a noise corner of only 10 Hz.

With the proliferation of mixed-signal processing, the number of power supplies required in each system has grown. The **AD8220-EP** is designed to alleviate this problem. The **AD8220-EP**

PIN CONFIGURATION

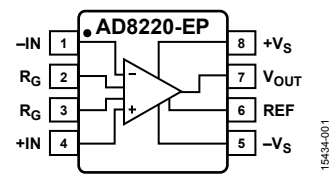


Figure 1.

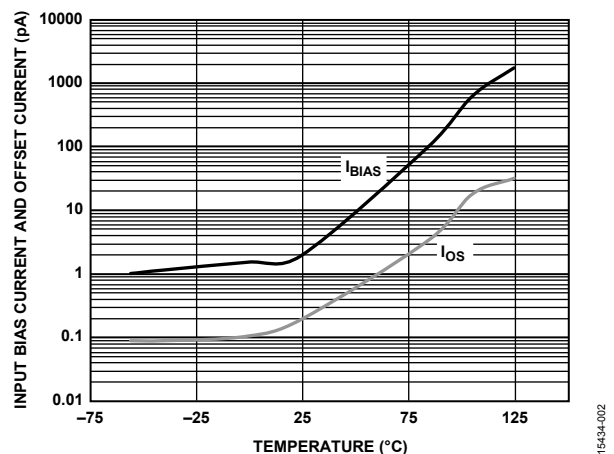


Figure 2. Input Bias Current and Offset Current vs. Temperature

can operate on a ± 18 V dual supply, as well as on a single 5 V supply. Its rail-to-rail output stage maximizes dynamic range on the low voltage supplies common in portable applications. Its ability to run on a single 5 V supply eliminates the need to use higher voltage, dual supplies. The **AD8220-EP** draws a maximum of 750 μA of quiescent current at 25°C , making it ideal for battery powered devices.

Gain is set from 1 to 1000 with a single resistor. Increasing the gain increases the common-mode rejection. Measurements that need higher CMRR when reading small signals benefit when the **AD8220-EP** is set for large gains.

A reference pin allows the user to offset the output voltage. This feature is useful when interfacing with analog-to-digital converters.

The **AD8220-EP** is available in an MSOP that takes roughly half the board area of an SOIC. Performance is specified over the extended industrial temperature range of -55°C to $+125^{\circ}\text{C}$.

Additional application and technical information can be found in the **AD8220** data sheet.

Rev. A

Document Feedback

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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

Changes to Table 1	4
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4/2017—Revision 0: Initial Version

SPECIFICATIONS

$+V_S = 15\text{ V}$, $-V_S = -15\text{ V}$, $V_{REF} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, $T_{OPR} = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 1$, $R_L = 2\text{ k}\Omega$,¹ unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	T_{OPR}				
CMRR from DC to 60 Hz with 1 k Ω Source Imbalance	$V_{CM} = \pm 10\text{ V}$				
$G = 1$		77			dB
$G = 10$		92			dB
$G = 100$		92			dB
$G = 1000$		92			dB
CMRR at 5 kHz	$V_{CM} = \pm 10\text{ V}$				
$G = 1$		72			dB
$G = 10$		80			dB
$G = 100$		80			dB
$G = 1000$		80			dB
NOISE	Referred to input (RTI) noise = $\sqrt{(e_{ni})^2 + (e_{no}/G)^2}$, T_A				
Voltage Noise, 1 kHz					
Input Voltage Noise, e_{ni}	$V_{IN+}, V_{IN-} = 0\text{ V}$		14		nV/ $\sqrt{\text{Hz}}$
Output Voltage Noise, e_{no}	$V_{IN+}, V_{IN-} = 0\text{ V}$		90		nV/ $\sqrt{\text{Hz}}$
RTI, 0.1 Hz to 10 Hz					
$G = 1$			5		$\mu\text{V p-p}$
$G = 1000$			0.8		$\mu\text{V p-p}$
Current Noise	$f = 1\text{ kHz}$		1		fA/ $\sqrt{\text{Hz}}$
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$				
Input Offset, V_{OSI}	T_A	-250		+250	μV
Average Temperature Coefficient (TC)	T_{OPR}	-10		+10	$\mu\text{V}/^\circ\text{C}$
Output Offset, V_{OSO}	T_A	-750		+750	μV
Average TC	T_{OPR}	-10		+10	$\mu\text{V}/^\circ\text{C}$
Offset RTI vs. Supply (PSR)	$V_S = \pm 5\text{ V}$ to $\pm 15\text{ V}$, T_{OPR}				
$G = 1$		80			dB
$G = 10$		92			dB
$G = 100$		92			dB
$G = 1000$		92			dB
INPUT CURRENT					
Input Bias Current	T_A			25	pA
Over Temperature	T_{OPR}			100	nA
Input Offset Current	T_A			2	pA
Over Temperature	T_{OPR}			10	nA
DYNAMIC RESPONSE					
Small Signal Bandwidth, -3 dB	T_A				
$G = 1$			1500		kHz
$G = 10$			800		kHz
$G = 100$			120		kHz
$G = 1000$			14		kHz
Settling Time 0.01%	10 V step, T_A				
$G = 1$			5		μs
$G = 10$			4.3		μs
$G = 100$			8.1		μs
$G = 1000$			58		μs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Settling Time 0.001%	10 V step, T_A				
$G = 1$			6		μs
$G = 10$			4.6		μs
$G = 100$			9.6		μs
$G = 1000$			74		μs
Slew Rate					
$G = 1$ to 100	T_A	2			V/ μs
GAIN	$G = 1 + (49.4 \text{ k}\Omega/R_G)$, T_{OPR}				
Gain Range		1		1000	V/V
Gain Error	$V_{\text{OUT}} = \pm 10 \text{ V}$				
$G = 1$		−0.1		+0.1	%
$G = 10$		−0.8		+0.8	%
$G = 100$		−0.8		+0.8	%
$G = 1000$		−0.8		+0.8	%
Gain Nonlinearity	$V_{\text{OUT}} = -10 \text{ V to } +10 \text{ V}$, T_A				
$G = 1$	$R_L = 10 \text{ k}\Omega$		10	15	ppm
$G = 10$	$R_L = 10 \text{ k}\Omega$		5	10	ppm
$G = 100$	$R_L = 10 \text{ k}\Omega$		30	60	ppm
$G = 1000$	$R_L = 10 \text{ k}\Omega$		400	500	ppm
$G = 1$	$R_L = 2 \text{ k}\Omega$		10	15	ppm
$G = 10$	$R_L = 2 \text{ k}\Omega$		10	15	ppm
$G = 100$	$R_L = 2 \text{ k}\Omega$		50	75	ppm
Gain vs. Temperature					
$G = 1$			3	10	ppm/ $^{\circ}\text{C}$
$G > 10$				−50	ppm/ $^{\circ}\text{C}$
INPUT					
Impedance (Pin to Ground) ²	T_A		$10^4 5$		$\text{G}\Omega \text{pF}$
Input Operating Voltage Range ³	$V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$ for dual supplies, T_A	− $V_S - 0.1$		+ $V_S - 2$	V
Over Temperature	T_{OPR}	− $V_S - 0.1$		+ $V_S - 2.2$	V
OUTPUT					
Output Swing	$R_L = 10 \text{ k}\Omega$, T_A	−14.7		+14.7	V
Over Temperature	T_{OPR}	−14.3		+14.3	V
Short-Circuit Current	T_A		15		mA
REFERENCE INPUT	T_A				
R_{IN}			40		k Ω
I_{IN}	$V_{\text{IN}+}, V_{\text{IN}-} = 0 \text{ V}$			70	μA
Voltage Range				+ V_S	V
Gain to Output	T_A			1 ± 0.0001	V/V
POWER SUPPLY					
Operating Range ⁴		± 2.25		± 18	V
Quiescent Current	T_A			750	μA
Over Temperature	T_{OPR}			1000	μA
TEMPERATURE RANGE					
For Specified Performance	T_{OPR}	−55		+125	$^{\circ}\text{C}$

¹ When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 k Ω .

² Differential and common-mode input impedance (Z_{DIFF} and Z_{CM}) can be calculated from the pin impedance (Z_{PIN}): $Z_{\text{DIFF}} = 2(Z_{\text{PIN}})$; $Z_{\text{CM}} = Z_{\text{PIN}}/2$.

³ The AD8220-EP can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.

⁴ At the minimum supply voltage of $\pm 2.25 \text{ V}$, ensure that the input common-mode voltage is within the input voltage range specification.

$+V_S = 5\text{ V}$, $-V_S = 0\text{ V}$, $V_{REF} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, $T_{OPR} = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $G = 1$, $R_L = 2\text{ k}\Omega^1$, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	T_{OPR}				
CMRR from DC to 60 Hz with 1 k Ω Source Imbalance	$V_{CM} = 0\text{ V}$ to 2.5 V				
$G = 1$		77			dB
$G = 10$		92			dB
$G = 100$		92			dB
$G = 1000$		92			dB
CMRR at 5 kHz	$V_{CM} = 0\text{ V}$ to 2.5 V				
$G = 1$		72			dB
$G = 10$		80			dB
$G = 100$		80			dB
$G = 1000$		80			dB
NOISE	$RTI\text{ noise} = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, T_A				
Voltage Noise, 1 kHz	$V_S = \pm 2.5\text{ V}$				
Input Voltage Noise, e_{ni}	$V_{IN+}, V_{IN-} = 0\text{ V}$, $V_{REF} = 0\text{ V}$		14		nV/ $\sqrt{\text{Hz}}$
Output Voltage Noise, e_{no}	$V_{IN+}, V_{IN-} = 0\text{ V}$, $V_{REF} = 0\text{ V}$		90		nV/ $\sqrt{\text{Hz}}$
RTI, 0.1 Hz to 10 Hz					
$G = 1$			5		$\mu\text{V p-p}$
$G = 1000$			0.8		$\mu\text{V p-p}$
Current Noise	$f = 1\text{ kHz}$		1		fA/ $\sqrt{\text{Hz}}$
VOLTAGE OFFSET	$V_{OS} = V_{OSI} + V_{OSO}/G$				
Input Offset, V_{OSI}	T_A	-300		+300	μV
Average TC	T_{OPR}	-10		+10	$\mu\text{V}/^\circ\text{C}$
Output Offset, V_{OSO}	T_A	-800		+800	μV
Average TC	T_{OPR}	-10		+10	$\mu\text{V}/^\circ\text{C}$
Offset RTI vs. Supply (PSR)	T_{OPR}				
$G = 1$		80			dB
$G = 10$		92			dB
$G = 100$		92			dB
$G = 1000$		92			dB
INPUT CURRENT					
Input Bias Current	T_A			25	pA
Over Temperature	T_{OPR}			100	nA
Input Offset Current	T_A			2	pA
Over Temperature	T_{OPR}			10	nA
DYNAMIC RESPONSE	T_A				
Small Signal Bandwidth, -3 dB					
$G = 1$			1500		kHz
$G = 10$			800		kHz
$G = 100$			120		kHz
$G = 1000$			14		kHz
Settling Time 0.01%	T_A				
$G = 1$	3 V step		2.5		μs
$G = 10$	4 V step		2.5		μs
$G = 100$	4 V step		7.5		μs
$G = 1000$	4 V step		30		μs
Settling Time 0.001%	T_A				
$G = 1$	3 V step		3.5		μs
$G = 10$	4 V step		3.5		μs
$G = 100$	4 V step		8.5		μs
$G = 1000$	4 V step		37		μs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Slew Rate G = 1 to 100	T _A	2			V/μs
GAIN	G = 1 + (49.4 kΩ/R _G), T _{OPR}				
Gain Range		1		1000	V/V
Gain Error	V _{OUT} = 0.3 V to 2.9 V for G = 1, V _{OUT} = 0.3 V to 3.8 V for G > 1				
G = 1		−0.1		+0.1	%
G = 10		−0.8		+0.8	%
G = 100		−0.8		+0.8	%
G = 1000		−0.8		+0.8	%
Nonlinearity	V _{OUT} = 0.3 V to 2.9 V for G = 1, V _{OUT} = 0.3 V to 3.8 V for G > 1, T _A				
G = 1	R _L = 10 kΩ			50	ppm
G = 10	R _L = 10 kΩ			50	ppm
G = 100	R _L = 10 kΩ			75	ppm
G = 1000	R _L = 10 kΩ			750	ppm
G = 1	R _L = 2 kΩ			50	ppm
G = 10	R _L = 2 kΩ			50	ppm
G = 100	R _L = 2 kΩ			75	ppm
Gain vs. Temperature					
G = 1			3	10	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Impedance (Pin to Ground) ²	T _A		10 ⁴ 6		GΩ pF
Input Voltage Range ³	T _A				V
Over Temperature	T _{OPR}	−0.1		+V _S − 2.2	V
OUTPUT					
Output Swing	R _L = 10 kΩ	0.15		4.85	V
Over Temperature	T _{OPR}	0.3		4.70	V
Short-Circuit Current			15		mA
REFERENCE INPUT					
R _{IN}	T _A		40		kΩ
I _{IN}	V _{IN+} , V _{IN−} = 0 V			70	μA
Voltage Range		−V _S		+V _S	V
Gain to Output	T _A		1 ± 0.0001		V/V
POWER SUPPLY					
Operating Range		4.5		36	V
Quiescent Current	T _A			750	μA
Over Temperature	T _{OPR}			1000	μA
TEMPERATURE RANGE					
T _{OPR} , For Specified Performance	T _{OPR}	−55		+125	°C

¹ When the output sinks more than 4 mA, use a 47 pF capacitor in parallel with the load to prevent ringing. Otherwise, use a larger load, such as 10 kΩ.

² Differential and common-mode impedance can be calculated from the pin impedance: Z_{DIFF} = 2(Z_{PIN}); Z_{CM} = Z_{PIN}/2.

³ The AD8220-EP can operate up to a diode drop below the negative supply but the bias current increases sharply. The input voltage range reflects the maximum allowable voltage where the input bias current is within the specification.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Power Dissipation	See Figure 3
Output Short-Circuit Current	Indefinite ¹
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Operating Temperature Range	-55°C to $+125^\circ\text{C}$
Reflow Temperature	260°C
Junction Temperature	140°C
θ_{JA} (4-Layer JEDEC Standard Board) ²	189°C/W
ESD	
Human Body Model	7 kV
Charge Device Model	1.25 kV
Machine Model	0.4 kV

¹ Assumes the load is referenced to midsupply.² θ_{JA} value is an approximation.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the MSOP on a 4-layer JEDEC standard board.

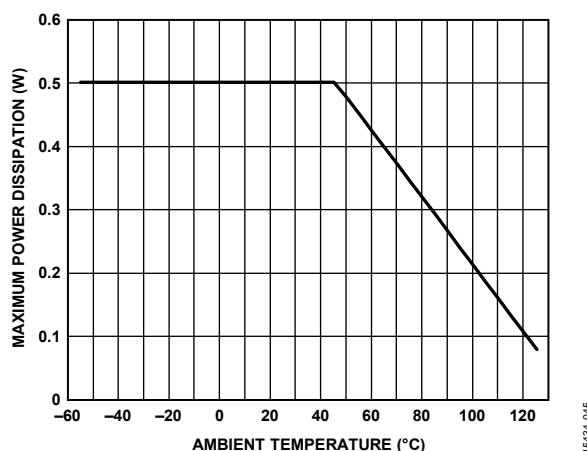


Figure 3. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

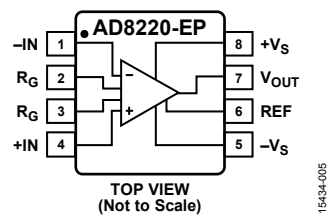


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input Terminal (True Differential Input).
2, 3	R _G	Gain Setting Terminals. Place a resistor across the R _G pins.
4	+IN	Positive Input Terminal (True Differential Input).
5	–V _S	Negative Power Supply Terminal.
6	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level shift the output.
7	V _{OUT}	Output Terminal.
8	+V _S	Positive Power Supply Terminal.

TYPICAL PERFORMANCE CHARACTERISTICS

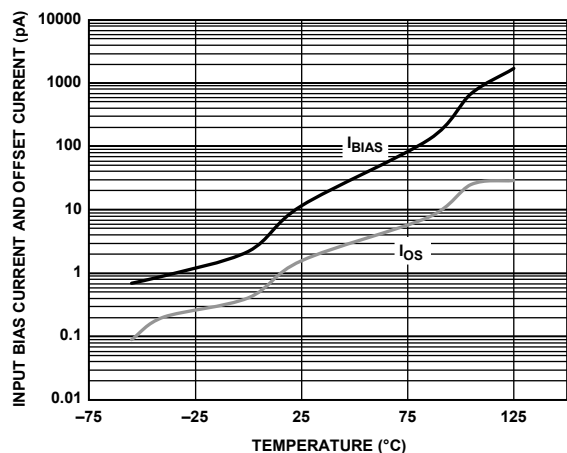


Figure 5. Input Bias Current and Offset Current vs. Temperature, $V_S = \pm 15 V$, $V_{REF} = 0 V$

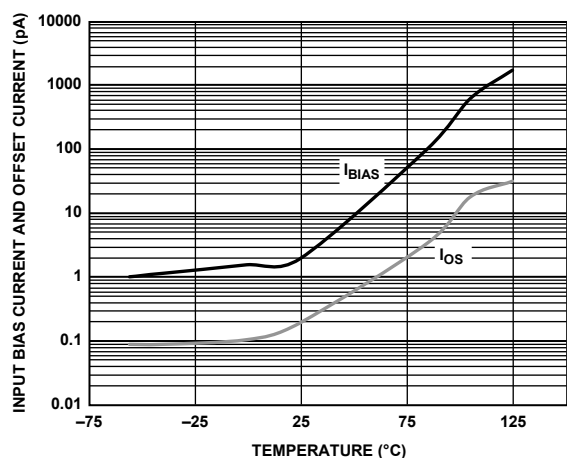


Figure 6. Input Bias Current and Offset Current vs. Temperature, $V_S = 5 V$, $V_{REF} = 2.5 V$

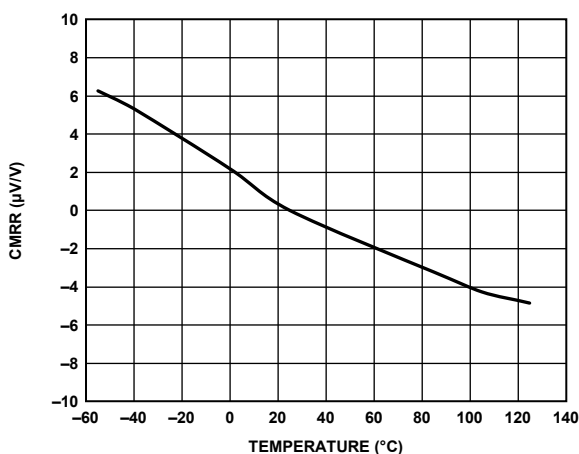


Figure 7. CMRR vs. Temperature, $G = 1$

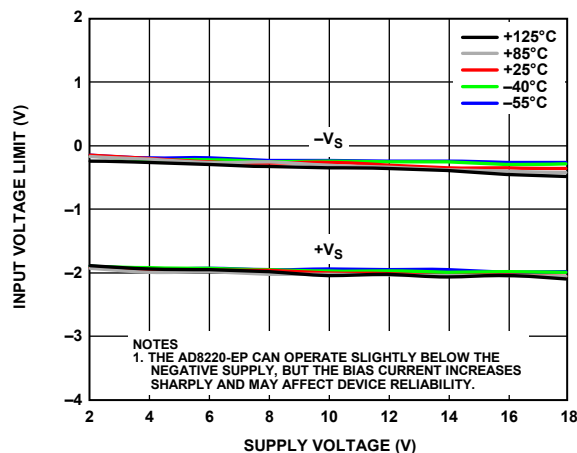


Figure 8. Input Voltage Limit vs. Supply Voltage, $G = 1$, $V_{REF} = 0 V$

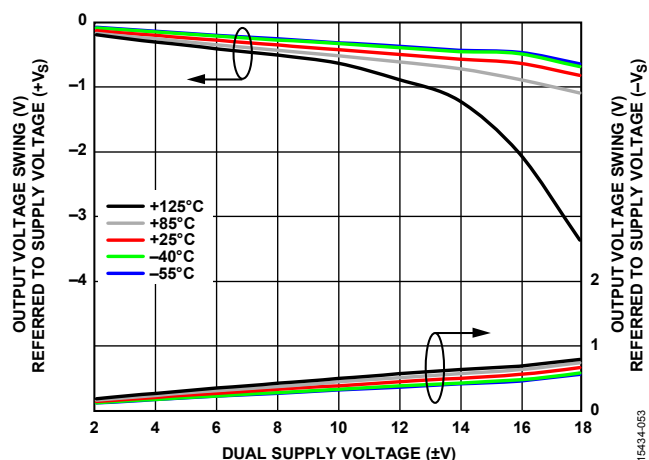


Figure 9. Output Voltage Swing Referred to Supply Voltage vs. Dual Supply Voltage, $R_{LOAD} = 2 k\Omega$, $G = 10$, $V_{REF} = 0 V$

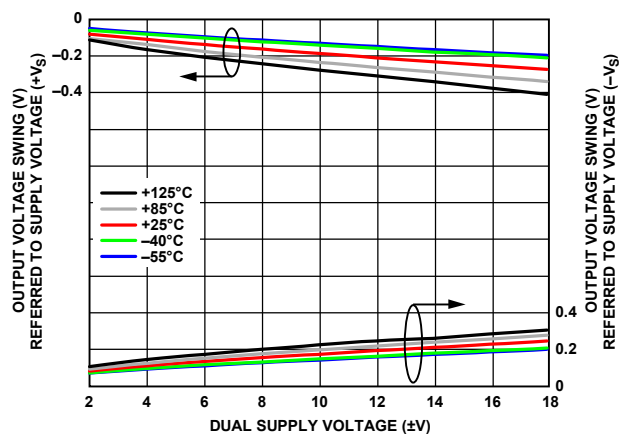


Figure 10. Output Voltage Swing Referred to Supply Voltage vs. Dual Supply Voltage, $R_{LOAD} = 10 k\Omega$, $G = 10$, $V_{REF} = 0 V$

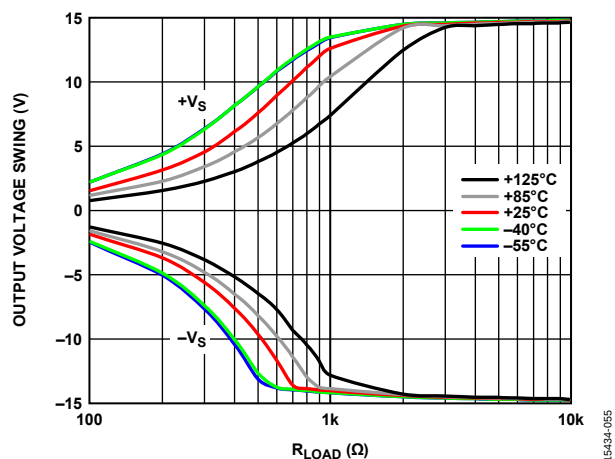


Figure 11. Output Voltage Swing vs. Load Resistance (R_{LOAD}), $V_S = \pm 15\text{ V}$, $V_{REF} = 0\text{ V}$

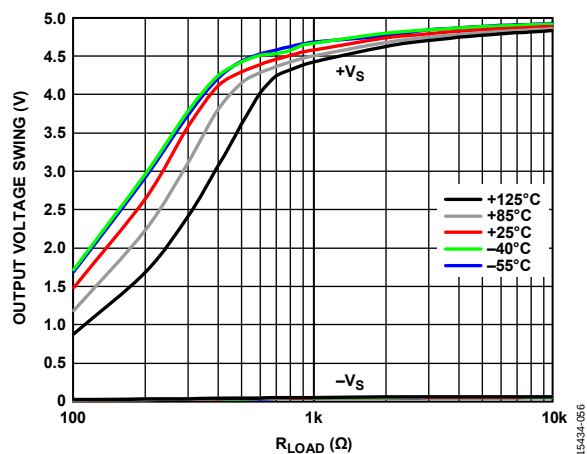


Figure 12. Output Voltage Swing vs. Load Resistance (R_{LOAD}), $V_S = 5\text{ V}$, $V_{REF} = 2.5\text{ V}$

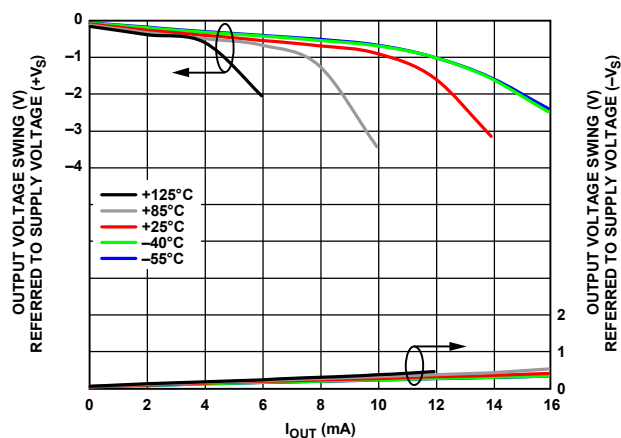


Figure 13. Output Voltage Swing Referred to Supply Voltage vs. Output Current (I_{OUT}), $V_S = \pm 15\text{ V}$, $V_{REF} = 0\text{ V}$

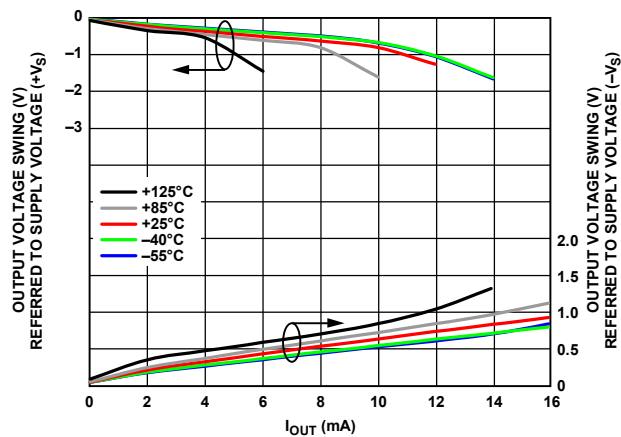


Figure 14. Output Voltage Swing Referred to Supply Voltage vs. Output Current (I_{OUT}), $V_S = 5\text{ V}$, $V_{REF} = 2.5\text{ V}$

