Data Sheet

AD74416H

Quad-Channel, Software Configurable Input and Output with HART Modem

FEATURES

- Quad-channel software configurable input and output
- Adaptive power switching reduces power dissipation by 40%
- Multiple configurable modes to a single pin
  - Voltage input/output
  - Current input/output
  - Digital input/output
  - 2- or 3-wire RTD measurement
  - Thermocouple measurement
- Overvoltage tolerant on screw terminal facing pins, powered or unpowered
- Auxiliary sense pins
- 10ppm/°C reference temperature coefficient
- 24-bit, Σ-Δ ADC with optional 50Hz and 60Hz rejection
- 16-bit monotonic DAC per channel
- Unipolar and bipolar capability
- Integrated HART® modem per channel
- On-chip diagnostics
  - Open-circuit and short-circuit detection
  - Auxiliary channel measurements
  - Power supply measurements
- Internal temperature sensor, ±5°C accuracy
- SPI-compatible
- Addressable up to four devices
- Watchdog timer
- Wide power-supply range
- Temperature range: −40°C to +105°C
- Available in a 64-lead LFCSP

APPLICATIONS

- Industrial control systems
- Process control
- Factory automation

COMPANION PRODUCTS

- Voltage reference: ADR4525
- Flyback converter: MAX17691A, MAX17691B

GENERAL DESCRIPTION

The AD74416H is a quad-channel, software configurable, input and output device for industrial control applications. The AD74416H provides a wide range of use cases integrated on a single chip. These use cases include analog input/output, digital input/output, resistance temperature detector (RTD), and thermocouple measurement capability.

The AD74416H also has an integrated highway addressable remote transducer (HART) modem per channel. The input and output communications and the HART communications for all four channels are both supported using a single serial-peripheral interface (SPI).

The AD74416H provides two address pins to support up to four devices with a single SPI bus. The digital input/outputs can be accessed by the SPI or the general-purpose input/output (GPIO) pins to support higher speed data rates.

The AD74416H features a 16-bit digital-to-analog converter (DAC) per channel and a single 24-bit, Σ-Δ analog-to-digital converter (ADC). The AD74416H contains a high accuracy 2.5V on-chip reference that can be used as the DAC and ADC reference.

The AD74416H supports adaptive power switching, which allows the output stage to dynamically transition between two independent power sources. This transitioning ability saves up to 40% overall power consumption, thereby reducing dissipated heat in the module.

FUNCTIONAL BLOCK DIAGRAM

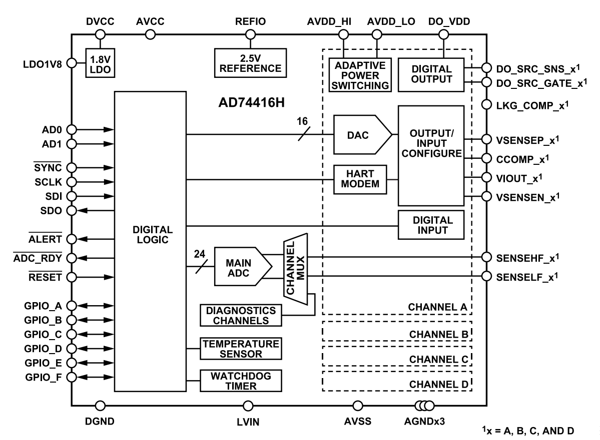

Figure 1. Functional Block Diagram

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REVISION HISTORY

3/2025—Revision 0: Initial Version

SPECIFICATIONS

VOLTAGE OUTPUT

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. The sense resistor (R_{SENSE}) = 12Ω (ideal), the load resistor (R_{LOAD}) = 100kΩ, and the load capacitor (C_{LOAD}) = 4.7nF per the recommended configuration. Note that the headroom specification for AVDD_HI, AVDD_LO, and AVSS must be considered when setting supply voltages.

Table 1. Voltage Output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE OUTPUT					
Resolution	16			Bits	
Output Range	0		12	V	
	−12		+12	V	
ACCURACY					
Total Unadjusted Error (TUE)	−0.2		+0.2	% FSR	
TUE at 25°C	−0.1		+0.1	% FSR	
Integral Nonlinearity (INL)	−12.0		+12.0	LSB	
Differential Nonlinearity (DNL)	−1.0		+1.0	LSB	Guaranteed monotonic
Offset Error	−5.5		+5.5	mV	Error with code 0x0000 loaded to the DAC, 0V to 12V range only
Offset Error at 25°C	−3.0		+3.0	mV	0V to 12V range only
Bipolar Zero Error	−17		+17	mV	Error with midscale code loaded to the DAC in a ±12V range
Bipolar Zero Error at 25°C	−16		+16	mV	±12V range only
Gain Error	−0.2		+0.2	% FSR	
Gain Error 25°C	−0.12		+0.12	% FSR	
Common Mode Rejection (CMR) at VSENSEN pin		1.7		mV/V	Relevant only to 4-wire sensing feedback mode Error in sensing voltage due to change in VSENSEN (±7V)
OUTPUT CHARACTERISTICS					
Resistive Load	1	100		kΩ	
Headroom	1.85			V	Voltage difference required between AVDD_HI (or AVDD_LO)[1] and the input/output positive (I/OP_x[2]) screw terminal to provide 12V across a 1kΩ load
Footroom	1.85			V	Voltage difference required between the I/OP_x[2] screw terminal and AVSS to provide −12V across a 1kΩ load
Short-Circuit Current		16		mA	Sourcing and sinking, I_LIMIT bit = 0 (default)
		8		mA	Sourcing and sinking, I_LIMIT bit = 1
Short-Circuit Alert Activation Time[3]		4		ms	Time in short-circuit before alert is generated ALARM_DEG_PERIOD bit = 0
		20		ms	ALARM_DEG_PERIOD bit = 1
Maximum External Capacitive Load[3]			10	nF	Value of the maximum external load capacitance connected to I/OP screw terminal, specification is taking into account recommended loading capacitor 4.7nF Compensation capacitor (C_{COMP}) is not connected
			2	µF	Maximum external capacitance when C_{COMP} = 220pF is connected
DC Output Impedance[3]		0.1		Ω	
DC Power-Supply Rejection Ratio (PSRR)		5		µV/V	PSRR measured with a change in AVDD_HI (or AVDD_LO)[1]
DYNAMIC PERFORMANCE[3]					
Output Voltage (V_{OUT}) Settling Time		40		µs	11V step (0.5V to 11.5V or 11.5V to 0.5V) to ±0.05% FSR, C_{LOAD} = 4.7nF, and no C_{COMP} is connected
		60		µs	22V step (−11V to +11V or +11V to −11V) to ±0.05% FSR, C_{LOAD} = 4.7nF, and no C_{COMP} is connected
Output Voltage Settling Time with CCOMP Connected		300		µs	11V step (0.5V to 11.5V or 11.5V to 0.5V) to ±0.05% FSR, C_{LOAD} = 4.7nF, and 220pF C_{COMP} is connected

SPECIFICATIONS

Table 1. Voltage Output (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
		300		μs	22V step (−11V to +11V or +11V to −11V) to ±0.05% FSR, C_{LOAD} = 4.7nF, and 220pF C_{COMP} is connected
Noise (External Reference)					Measured at the I/OP screw terminal, 2.5V output
Output Noise		0.5		LSB p-p	0.1Hz to 10Hz bandwidth, 10kΩ load, ±12V range
Output Noise Spectral Density					
0V to 12V Range		540		nV/√Hz	Measured at 1kHz, midscale output
−12V to +12V Range		750		nV/√Hz	Measured at 1kHz, midscale output
AC PSRR		65		dB	200mV at 1kHz sine wave superimposed on the AVDD_HI (or AVDD_LO)[1]
		55		dB	200mV at 1kHz sine wave superimposed on the AVSS supply

1 Currently active voltage rail connected by adaptive power switching block. For more details, see the Adaptive Power Switching section.

2 x = A, B, C, and D.

3 Guaranteed by design and characterization.

SPECIFICATIONS

CURRENT OUTPUT (I_{OUT}) AND I_{OUT} WITH HART

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C. Bit field AVDD_SELECT of OUTPUT_CONFIGn register is set to 0 (LOCK_HI), unless otherwise noted. R_{SENSE} = 12Ω (ideal), R_{LOAD} = 500Ω, and C_{LOAD} = 4.7nF per the recommended configuration. Note that the headroom specification for AVDD_HI, AVDD_LO must be considered when setting supply voltages.

Table 2. Current Output (I_{OUT}) and I_{OUT} with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
I_{OUT}					
Resolution	16			Bits	
Output Range	0		25	mA	
ACCURACY					
TUE	−0.2		+0.2	% FSR	The error of the internal sensing resistor is included (external R_{SENSE} is not used for output current regulation)
TUE at 25°C	−0.1		+0.1	% FSR	The error of the internal sensing resistor is included (external R_{SENSE} is not used for output current regulation)
TUE Long-Term Stability		80		ppm FSR	Drift after 1000 hours, T_A = 90°C
INL	−14		+14	LSB	From zero-scale to full-scale
DNL	−1		+1	LSB	Guaranteed monotonic
Offset Error	−10		+10	μA	
Offset Error at 25°C	−7		+7	μA	
Gain Error	−0.2		+0.2	% FSR	
Gain Error at 25°C	−0.1		+0.1	% FSR	
OUTPUT CHARACTERISTICS					
Headroom	3.8			V	Voltage difference required between AVDD_HI (or AVDD_LO)[1] and the I/OP screw terminal to source 25mA
Open-Circuit Voltage		AVDD_x[1, 2]		V	
Open-Circuit Alert Activation Time[3]		4		ms	Time in short-circuit before alert is generated ALARM_DEG_PERIOD bit = 0
		20		ms	ALARM_DEG_PERIOD bit = 1
Output Impedance		20		MΩ	
DC PSRR		25		nA/V	PSRR measured with a change in AVDD_HI (or AVDD_LO)[1]
DYNAMIC PERFORMANCE[3]					
Output Current Settling Time		10		μs	3.2mA to 23mA step up or down, time to settle within a window of ±100μA of final current
Output Current Settling Time (with HART Slew Enabled)		60		ms	With HART slew enabled, 3.2mA to 23mA, step up or step down, and time to settle within a window of ±100μA of final current
Noise					Measured at the I/OP screw terminal with 250Ω load, 12.5mA output
Output Noise		0.38		LSB p-p	0.1Hz to 10Hz bandwidth, 250Ω load
Output Noise Spectral Density		2		nA/√Hz	Measured at 1kHz, 12.5mA output
AC PSRR		75		dB	Measured at the I/OP screw terminal with 250Ω load 200mV at 1kHz sine wave superimposed on the AVDD_HI (or AVDD_LO)[1] supply

[1] Currently active voltage rail connected by adaptive power switching block. For more details, see the Adaptive Power Switching section.

[2] x = A, B, C, and D.

[3] Guaranteed by design and characterization.

SPECIFICATIONS

VOLTAGE INPUT

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal), and C_{LOAD} = 4.7nF per the recommended configuration. Note that the required input range for AVDD_HI and AVSS must be considered when setting the supply voltages.

Table 3. Voltage Input

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE INPUT					
Input Resolution	24			Bits	
Input Range (SENSELF)	0		12	V	
	−12		+12	V	
ACCURACY					
TUE	−0.1		+0.1	% FSR	
TUE at 25°C	−0.01		+0.01	% FSR	
INL	−60		+60	ppm FSR	
Offset Error	−60		+60	ppm FSR	
Offset Error at 25°C	−45		+45	ppm FSR	
Gain Error	−750		+750	ppm FSR	
Gain Error at 25°C	−330		+330	ppm FSR	
OTHER INPUT SPECIFICATIONS					
Footroom	AVSS + 2			V	
Headroom			AVDD_HI − 0.2	V	
DC PSRR		10		μV/V	PSRR measured with a change in AVDD_HI, AVDD_LO, AVSS, AVCC, and DVCC
Normal Mode Rejection[1]		80		dB	50Hz ± 1Hz and 60Hz ± 1Hz
Input Bias Current	−30		+30	nA	As seen from the I/OP screw terminal, ADC is either idle or converting, does not include transient voltage suppressor (TVS) leakage
Input Bias Current at 25°C		±6		nA	

[1] Guaranteed by design and characterization.

SPECIFICATIONS

CURRENT INPUT EXTERNALLY POWERED AND CURRENT INPUT EXTERNALLY POWERED WITH HART

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (Ideal), and C_{LOAD} = 4.7nF per the recommended configuration. Note that in HART mode, the compliance specification for AVDD_HI, AVDD_LO must be considered when setting supply voltages.

Table 4. Current Input Externally Powered and Current Input Externally Powered with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUT					
Input Resolution	24			Bits	
Input Range	0		25	mA	Sensed across the external 12Ω resistor
Screw Terminal Voltage	0			V	
Short-Circuit Current Limit	25	29	35	mA	Nonprogrammable
ACCURACY					FSR refers to the maximum code of the ADC at the range from −0.3125V to 0V, for more details, see Table 25
TUE[1]	−0.1		+0.1	% FSR	
TUE at 25°C[1]	−0.025		+0.025	% FSR	
INL	−60	±30	+60	ppm FSR	Linearity is specified from 0.1mA to 25mA range
Offset Error	−155		+155	ppm FSR	
Offset Error at 25°C	−100		+100	ppm FSR	
Gain Error[1, 2]	−250		+250	ppm FSR	
Gain Error at 25°C[1, 2]	−100		+100	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[2]		In order of noise			
Input Impedance (without HART Termination)		80		Ω	Current input, externally powered selected, including 12Ω R_{SENSE}
Input Impedance (with HART Termination)	270		390	Ω	Current input, externally powered with HART selected, including 12Ω R_{SENSE}
Compliance (without HART Termination)		2.0	2.6	V	Current input, externally powered selected, and minimum voltage required at the I/OP screw terminal to sink 25mA
Compliance (with HART Termination)		6.4	7.5	V	Current input, externally powered with HART selected, and minimum voltage required at the I/OP screw terminal to sink 20mA

1 R_{SENSE} accuracy directly impacts the TUE and gain error.

2 Guaranteed by design and characterization.

SPECIFICATIONS

CURRENT INPUT LOOP POWERED AND CURRENT INPUT LOOP POWERED WITH HART

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal), and C_{LOAD} = 4.7nF per the recommended configuration. Note that in HART mode, the headroom specification for AVDD_HI, AVDD_LO must be considered when setting supply voltages.

Table 5. Current Input Loop Powered and Current Input Loop Powered with HART

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUTS					
Input Resolution	24			Bits	
Input Range	0		25	mA	Sensed across external 12Ω resistor
Screw Terminal Voltage			AVDD_x[1, 2]	V	
NonHART Current Limit	0		25	mA	Range of the programmable current limit, 16-bit resolution, use DAC_CODE[n] register
HART Mode Current Limit	25	30	35	mA	Current input, loop powered with HART enabled, nonprogrammable
ACCURACY					FSR refers to the maximum code of the ADC at the range from 0V to 0.3125V, for more details, see Table 25
TUE[3]	−0.1		+0.1	% FSR	
TUE at 25°C[3]	−0.025		+0.025	% FSR	
INL	−60	±30	+60	ppm FSR	Linearity is specified from 0.1mA to 25mA range for mode without HART, for mode with HART linearity is specified from 3mA to 23mA range
Offset Error	−155		+155	ppm FSR	
Offset Error at 25°C	−100		+100	ppm FSR	
Gain Error[3, 4]	−250		+250	ppm FSR	
Gain Error at 25°C[3, 4]	−100		+100	ppm FSR	
OTHER INPUT SPECIFICATIONS					
DC PSRR[4]		In order of noise			
Input Impedance (without HART Termination)		120		Ω	With current input, loop powered selected, includes 12Ω R_{SENSE}
Input Impedance (with HART Termination)	270		460	Ω	With current input, loop powered with HART selected, includes 12Ω R_{SENSE}
Headroom (without HART Termination)	5.0	4.0		V	Required difference between AVDD_HI (or AVDD_LO)[2] and the I/OP screw terminal voltage to source 25mA, current input, loop powered selected
Headroom (with HART Termination)	8.0	6.6		V	Required difference between AVDD_HI (or AVDD_LO)[2] and the I/OP screw terminal voltage to source 20mA, current input, loop powered with HART selected

1 x = A, B, C, and D.

2 Selected voltage rail, configured by AVDD_SELECT bit field in OUTPUT_CONFIGn register.

3 R_{SENSE} accuracy directly impacts the TUE and gain error.

4 Guaranteed by design and characterization.

SPECIFICATIONS

2-WIRE RTD MEASUREMENT

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal), SENSEHF_x filter resistor = 2kΩ (ideal), and C_{LOAD} = 4.7nF per the recommended configuration.

Table 6. Resistance 2-Wire Measurement

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0.001		4	kΩ	2-wire RTD measurements supported
Excitation Current		500		µA	
Open-Circuit Detect Voltage					Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit
SENSEHF_x[1]		3.85		V	
ACCURACY[2]					Does not include external components and external sources of error
Measurement Range					
100Ω to 4kΩ					Suitable for Pt1000, and 500µA excitation current, and 0V to 12V ADC range Total error [Ω] = RTD [Ω] × (Gain error [%]/100) + Offset error [Ω]
Gain Error	−0.085		+0.085	%	
Gain Error at 25°C	−0.034		+0.034	%	
Offset Error	−1.14		+1.14	Ω	
Offset Error at 25°C	−0.301		+0.301	Ω	

1 x = A, B, C, and D.

2 Guaranteed by design and characterization.

SPECIFICATIONS

3-WIRE RTD MEASUREMENT

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal), SENSEHF_x filter resistor = 2kΩ (ideal), and C_{LOAD} = 4.7nF per the recommended configuration.

Table 7. 3-Wire RTD Measurement

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE MEASUREMENT					
Input Range	0.001		4	kΩ	
Programmable Excitation Current		500		µA	
		1		mA	The voltage generated across the (reference resistor (R_{REF}) + the RTD resistor (R_{RTD})) must be less than the AVCC voltage (V_{AVCC})
Current Matching					
Excitation Current Matching	−0.45		+0.45	%	For 500µA
	−0.3		+0.3	%	For 1mA
Current Matching Drift[1]		5		ppm/°C	
Open-Circuit Detect Voltage					Excitation current and resistor combinations generating a voltage greater than this are treated as open-circuit
VSENSEN_x[2]		2.4		V	
SENSEHF_x[2]		3.7		V	
ACCURACY[1]					Does not include external components and external sources of error
Measurement Range					
1Ω to 40Ω					Suitable for Pt10, Cu10, or similar, 1mA excitation current and ±104.16mV ADC range Total error [Ω] = RTD [Ω] × (Gain error [%]/100) + Offset error [Ω]
Gain Error	−0.066		+0.066	%	
Gain Error at 25°C	−0.030		+0.030	%	
Offset Error	−0.033		+0.033	Ω	
Offset Error at 25°C	−0.021		+0.021	Ω	
10Ω to 400Ω					Suitable for Pt100 or similar, 1mA excitation current, and 0.625V ADC range Total error [Ω] = RTD [Ω] × (Gain error [%]/100) + Offset error [Ω]
Gain Error	−0.035		+0.035	%	
Gain Error at 25°C	−0.015		+0.015	%	
Offset Error	−0.053		+0.053	Ω	
Offset Error at 25°C	−0.034		+0.034	Ω	
100Ω to 4kΩ					Suitable for Pt1000, and 500µA excitation current, and 0V to 12V ADC range Total error [Ω] = RTD [Ω] × (Gain error [%]/100) + Offset error [Ω]
Gain Error	−0.083		+0.083	%	
Gain Error at 25°C	−0.034		+0.034	%	
Offset Error	−1.044		+1.044	Ω	
Offset Error at 25°C	−0.317		+0.317	Ω	

1 Guaranteed by design and characterization.

2 x = A, B, C, and D.

SPECIFICATIONS

DIGITAL INPUT LOGIC

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal) and C_{LOAD} = 4.7nF per the recommended configuration.

Table 8. Digital Input Logic

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Unbuffered Input Data Rate			200	kHz	The VIOUT_x[1] pin is driven by a low impedance source, 0V to 12V signal, duty cycle: 60:40
Buffered Input Data Rate		20		kHz	The VSENSEP_x[1] pin is driven by a low impedance source, 0V to 12V signal, duty cycle: 60:40
Input Voltage Range[2]	−45		+45	V	
Input Resistance		1.2		MΩ	High speed mode
Open-Circuit Detect Current	0.05		0.35	mA	Window for open-circuit detection for compliance with IEC 61131-2 Type 3D
Short-Circuit Detect Current	6			mA	For IEC 61131-2 Type 3D
CURRENT SINK					
Range 0					
Series Resistor Value		2.8		kΩ	
Current Sink Range	0		3.7	mA	Typical programmable current sink to AGND
Current Sink Resolution		120		µA	
Current Sink Accuracy		±2		% FSR	
Current Sink at Decimal Code 20	2.1	2.4		mA	Recommended for IEC 61131-2 Type I and Type III for the I/OP screw terminal > 6V, DIN_SINK = Decimal Code 20
Current Sink at Decimal 15		1.8		mA	Recommended for IEC 61131-2 Type 3D, DIN_SINK bits = Decimal Code 15
Range 1					
Series Resistor Value		1		kΩ	
Current Sink Range	0		7.4	mA	Typical programmable current sink to AGND
Current Sink Resolution		240		µA	
Current Sink Accuracy		±2		% FSR	
Current Sink at Decimal Code 29	6.1	7.0		mA	Recommended for IEC 61131-2 Type II for the I/OP screw terminal > 7V, DIN_SINK bits = Decimal Code 29
VOLTAGE THRESHOLDS MODES					
Threshold Range	AVSS + 2.0		AVDD_HI – 1.5	V	Programmable trip level
AVDD_HI Threshold Mode					
Threshold Resolution		AVDD_HI/50		V	
Hysteresis		AVDD_HI/50		V	
Fixed Threshold Mode					
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Voltage at Decimal Code 55	8.0	8.5	8.8	V	Rising trip point, recommended for IEC 61131-2 Type I, Type II, and Type III, COMP_THRESH bits = Decimal Code 55
Threshold Accuracy		2		% FSR	

[1] x = A, B, C, and D.

[2] Guaranteed by design and characterization.

SPECIFICATIONS

DIGITAL INPUT LOOP POWERED

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal) and C_{LOAD} = 4.7nF per the recommended configuration. Note that the headroom specification for AVDD_HI, AVDD_LO must be considered when setting supply voltages.

Table 9. Digital Input Loop Powered

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input Data Rate[1]			5	kHz	Unfiltered input, typically dominated by wetting current, load capacitance, and threshold voltage
Dry Contact Wetting Current Range	0		25	mA	Loop powered, programmable current, use DAC_CODE[n] register
Headroom	3.8			V	Required voltage difference between AVDD_HI (or AVDD_LO)[2] and the I/OP screw terminal to source 25mA
THRESHOLD MODES					
Threshold Range	AVSS + 2.0		AVDD_HI – 1.5	V	Programmable trip level
AVDD_HI Threshold Mode					
Threshold Resolution		AVDD_HI/50		V	
Hysteresis		AVDD_HI/50		V	
Fixed Threshold Mode					
Threshold Resolution		0.5		V	
Hysteresis		0.5		V	
Threshold Accuracy		2		% FSR	

1 Guaranteed by design and characterization.

2 Currently active voltage rail connected by adaptive power switching block. For more details, see the Adaptive Power Switching section.

SPECIFICATIONS

DIGITAL OUTPUT

DO_VDD = +10V to +35V, AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. C_{LOAD} = 4.7nF per the recommended configuration.

Table 10. Digital Output

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DO_VDD SUPPLY RANGE	10	24	35	V	
Short-Circuit					
Short-Circuit Voltage, $V_{SC}1$	160		240	mV	With a 0.15Ω set resistor (R_{SET}), the current clamps at 1.3A
Short-Circuit Voltage, $V_{SC}2$	80		120	mV	With a 0.15Ω R_{SET}, the current clamps at 667mA
Short-Circuit Clamp Time[1]		2		µs	FET input capacitance (C_{ISS}) < 500pF, and the time for the short-circuit clamp to engage during a 0Ω short-circuit
Time Out 1, T1[1]	0.1		100	ms	Typical programmable times
Time Out 2, T2[1]	0.1			ms	Typical programmable times
On and Off Times[1]					
On Time, t_{ON}		15		µs	FET C_{ISS} < 500pF, and the time from $\overline{SYNC}$ rising edge to settle to 90%
Off Time, t_{OFF}		4		µs	FET C_{ISS} < 500pF, and the time from the $\overline{SYNC}$ rising edge to FET disable
Gate Drive Voltage	−12	−10	−8	V	The DO_SRC_GATE_x[2] voltage with respect to DO_VDD

[1] Guaranteed by design and characterization.

[2] x = A, B, C, and D.

SPECIFICATIONS

ADC SPECIFICATIONS

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal) and C_{LOAD} = 4.7nF per the recommended configuration. Note that the required input range for AVDD_HI and AVSS must be considered when setting the supply voltages.

Table 11. ADC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC SPECIFICATIONS					
Resolution	24			Bits	
No Missing Codes[1, 2]	24			Bits	
Conversion Rates[1]					Sample rates vary depending on the number of ADC measurements selected and the use of single or continuous conversion modes
		10		SPS	50Hz and 60Hz rejection enabled, rejection of HART fundamental frequencies implemented
		20		SPS	50Hz and 60Hz rejection enabled
		20		SPS	50Hz and 60Hz rejection enabled, rejection of HART fundamental frequencies implemented
		200		SPS	50Hz and 60Hz rejection disabled, moderate rejection of HART fundamental frequencies implemented
		200		SPS	50Hz and 60Hz rejection disabled, rejection of HART fundamental frequencies implemented
		1.2		kSPS	50Hz and 60Hz rejection disabled
		1.2		kSPS	50Hz and 60Hz rejection disabled, rejection of HART fundamental frequencies implemented
		4.8		kSPS	50Hz and 60Hz rejection disabled
		9.6		kSPS	50Hz and 60Hz rejection disabled
		19.2		kSPS	50Hz and 60Hz rejection disabled, available for diagnostics measurements only
Absolute Input Voltage	AVSS + 2		AVDD_HI − 0.2		At ADC pin (SENSEHF_x[3] or SENSELF_x[3])
Noise[1]					See Table 28
Common-Mode Rejection Ratio (CMRR)		95		dB	
ADC INPUT RANGES					
0V to +12V, ±12V					Typically used to measure the voltage across the I/OP to I/ON screw terminals (I/OP is the input and output positive, and I/ON is the input and output negative), and also used for VSENSEP_x[3] and VSENSEN_x[3]
Range	0		12	V	
	−12		+12	V	
TUE	−0.1		+0.1	% FSR	
INL	−60		+60	ppm FSR	
Offset Error	−60		+60	ppm FSR	
Gain Error	−750		+750	ppm FSR	
±2.5V					Typically used to measure the current through the R_{SENSE} resistor
Range	−2.5		+2.5	V	Typically used to measure bidirectional current across the 12Ω R_{SENSE} in voltage output mode
TUE	−0.1		+0.1	% FSR	
INL	−60		+60	ppm FSR	
Offset Error	−60		+60	ppm FSR	
Gain Error	−250		+250	ppm FSR	

SPECIFICATIONS

Table 11. ADC Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
0V to +0.625V, 0V to +0.3125V, −0.3125V to 0V, ±0.3125V					Typically used to measure 3-wire RTDs
Range	0		0.625	V	
	0		+0.3125	V	
	−0.3125		0	V	
	−0.3125		+0.3125	V	
TUE	−0.1		+0.1	% FSR	
INL	−60		+60	ppm FSR	
Offset Error[1]	−155		+155	ppm FSR	
Gain Error[1]	−250		+250	ppm FSR	
±104.16mV					Typically used to measure thermocouple voltages in voltage input mode
Range	−104.16		+104.16	mV	
TUE	−0.1		+0.1	% FSR	
INL	−60		+60	ppm FSR	
Offset Error[1]	−382	+45.8	+382	ppm FSR	Offset at high temperatures is dominated by leakage through external R_{SENSE}
Gain Error[1]	−500		+500	ppm FSR	
DIAGNOSTICS SPECIFICATIONS					
External Diagnostics					
LVIN Pin 2.5V Range					
Range	0		2.5	V	
TUE	−0.05		+0.05	% FSR	
INL	−60		+60	ppm FSR	
Offset Error	−60		+60	ppm FSR	
Offset Error		±300		ppm FSR	Conversion rate 19.2kSPS
Gain Error	−200		+200	ppm FSR	
Noise[1]					For typical values, see Table 29
Sense Pins Diagnostics					VSENSEP_x[3], and VSENSEN_x[3]
Accuracy		±0.25		% FSR	
DO Current Sense Accuracy					
External DO		±2		mV	
Internal Diagnostics					
Accuracy		±2		%	Percentage of measured value
TEMPERATURE SENSOR[1]					
Accuracy		±5		°C	
Resolution		0.11		°C	

1 Guaranteed by design and characterization, not production tested.

2 Does not include 9.6kSPS rate.

3 x = A, B, C, and D.

SPECIFICATIONS

HART MODEM COMMUNICATIONS

AVDD_HI = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal), R_{LOAD} = 500Ω, and C_{LOAD} = 4.7nF per the recommended configuration.

Table 12. HART Modem Communications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Power-Up Time[1]		50		µs	Transition time from HART power down to normal operation mode HART modem is powered up by the MODEM_PWRUP bit in the HART_CONFIG register
HART Receive signal ranges					
Data Carrier Detect Assert	85	100	110	mV p-p	Range within which assert occurs
High Impedance Devices[1]	120		1500	mV p-p	
Low Impedance Devices[1]	120		800	mV p-p	
HART Transmit signal ranges					
Output Voltage Range					
Current Output mode	400		600	mV p-p	Measured at the I/OP screw terminal with a current range of 3.2mA to 23mA, and a 500Ω load in current output mode
Current Input mode	400		600	mV p-p	Measured at the I/OP screw terminal with a current range of 3.2mA to 23mA, and a 1kΩ load in current input (loop powered or externally powered) mode
Mark Frequency		1200		Hz	
Space Frequency		2200		Hz	
Frequency Error	−1.0		+1.0	%	

[1] Guaranteed by design and characterization, not production tested.

SPECIFICATIONS

GENERAL SPECIFICATIONS

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted. R_{SENSE} = 12Ω (ideal) and C_{LOAD} = 4.7nF per the recommended configuration.

Table 13. General Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SPECIFICATIONS					
Reference Input					
Reference Input Voltage		2.5		V	Accuracy of the external reference has an impact on the accuracy of the AD74416H
DC Input Current		45		µA	
Reference Output					
Output Voltage	2.495	2.5	2.505	V	T_A = 25°C
Reference Temperature Coefficient[1]			10	ppm/°C	Box method have been used
Output Voltage Drift vs. Time[1]		500		ppm FSR	Drift after 1000hours, T_A = 90°C
Output Noise[1]		18		µV p-p	0.1Hz to 10Hz bandwidth
Output Noise Spectral Density[1]		95		nV/√Hz	Frequency = 10kHz
Capacitive Load[1]		22	50	nF	On REFIO pin
FET LEAKAGE COMPENSATION[1]					
Input Voltage Range					Voltage range on the I/OP terminal when leakage compensation is enabled
Sourcing External FET	AVSS + 2		AVDD_x[2, 3] − 1		
Voltage Across External Blocking Diode		30		mV	FET leakage compensation enabled, for currents up to 40µA leakage current in screw terminal, for more details on typical performance, see Figure 33
SENSE PINS					SENSEHF_x[3], SENSELF_x[3], VSENSEP_x[3], VSENSEN_x[3]
Input Bias Current	−25		+25	nA	
Input Bias Current at 25°C		±2		nA	
Input Bias Matching			10	nA	Worst-case difference between any of the SENSEHF_x[3], SENSELF_x[3], VSENSEP_x[3], VSENSEN_x[3] pins
High Voltage ADC Buffer - Power Saving					Difference of current drawn between low power mode (standby) and active mode of the buffer
AVDD_HI Current		190		µA	Each buffer draws current from AVDD_HI and AVSS pin
AVSS Current		190		µA	Each buffer draws current from AVDD_HI and AVSS pin
AVCC Current		190		µA	SENSE_AGND_OPT buffer draws current from AVCC and AVSS pin
High Voltage ADC Buffer Power-Up Time[1]		100		µs	
BURNOUT CURRENTS					Programmable source or sink currents
VIOUT_x[3] Current		0.1, 1, 10		µA	
VSENSEN_x[3] pin Current		0.1, 1, 10		µA	
TEMPERATURE ALERT AND RESET[1]					
Temperature Alert		115		°C	Junction temperature, high temperature event flags the alert status and the $\overline{\text{ALERT}}$ pin (if unmasked)
Temperature Alert Accuracy		5		°C	
Temperature Reset		145		°C	Junction temperature, resets the device if over temperature event when the EN_THERM_RST bit = 1

SPECIFICATIONS

Table 13. General Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Temperature Reset Accuracy		5		°C	
LOGIC INPUTS					SCLK, SDI, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, GPIO_x[3] (as inputs), AD0, AD1
Input Voltage					
High (V_{IH})	0.7 × DVCC			V	
Low (V_{IL})			0.2 × DVCC	V	
Input Current	−1		+1	μA	Per pin, SCLK, SDI, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, GPIO_x[3] (as inputs)
Input Capacitance[1]		3		pF	Per pin
Pull-Down Resistance		100		kΩ	Applicable only to AD0, AD1 and GPIO_x[3] (as inputs)
LOGIC OUTPUTS					
SDO Pin					
Output Low Voltage (V_{OL})			0.4	V	Sink current (I_{SINK}) = 200μA
Output High Voltage (V_{OH})	DVCC − 0.4			V	Source current (I_{SOURCE}) = 200μA
High-Impedance Leakage Current	−1		+1	μA	SDO pin only
High-Impedance Output Capacitance[1]		3		pF	SDO pin only
GPIO_x[3] Pin					As outputs
V_{OL}			0.4	V	GPIO_A, B, C, and D, I_{SINK} = 3mA GPIO_E and F, I_{SINK} = 250μA
V_{OH}	DVCC − 0.4			V	GPIO_A, B, C, and D, I_{SOURCE} = 3mA GPIO_E and F, I_{SOURCE} = 250μA
High-Impedance Leakage Current	−1		+1	μA	
OPEN-DRAIN LOGIC OUTPUTS					$\overline{\text{ADC\_RDY}}$ and $\overline{\text{ALERT}}$
V_{OL}			0.4	V	Capable of sinking 2.5mA
High Impedance Leakage Current	−1		+1	μA	
POWER SUPPLY MONITORS					Falling thresholds
AVDD_HI Threshold		5.4		V	
AVDD_LO Threshold		5.4		V	
AVSS Threshold		−1.6		V	
AVCC Threshold		4.1		V	
DVCC Threshold		2.3		V	
DO_VDD Threshold		9.2		V	
POWER REQUIREMENTS					
Supply Voltages[1]					
AVDD_HI	6	24	28.8	V	Headroom requirements must be met for specific application
AVDD_LO	6	14.5	28.8	V	For power efficiency, see the Adaptive Power Switching section
AVSS	−18	−15	−2.5	V	Footroom requirements must be met for specific application
DVCC	2.7	3.3	5.5	V	
AVCC	4.5	5.0	5.5	V	
DO_VDD	10	24	35	V	
Supply Quiescent Currents[1]					Typical (Typ) measurements are obtained using typ supply voltage setting and T_A = 25°C
High Impedance					4x Channels configured to high impedance, ADC is disabled
AVDD_HI Current	5.5	7.5	9.0	mA	
AVDD_LO Current	0	0.3	0.5	mA	AVDD_LO power supply is at least 200mV lower than AVDD_HI

SPECIFICATIONS

Table 13. General Specifications (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AVSS Current	5.5	7.8	9.5	mA	
DVCC Current	2.0	2.8	3.3	mA	
AVCC Current	2.0	3.4	4.5	mA	
DO_VDD Current	100	170	220	µA	
Channel Functions					4x Channels configured to any analog or digital, input or output mode, ADC is enabled, no load current, unless specified otherwise
AVDD_HI Current	8.0	10.0	11.5	mA	Except for voltage output and RTD measurements
	8.5	11.0	12.5	mA	4x Channels configured to voltage output, ADC is disabled
	13.0	16.5	18.5	mA	4x Channels configured to resistance measurement, ADC is enabled (RTD_CURRENT is set to 1mA)
AVDD_LO Current	0	0.7	3.0	mA	AVDD_LO power supply is at least 200mV lower than AVDD_HI
AVSS Current	5.5	8.0	10.0	mA	Except for Voltage output
	9.0	11.0	13.0	mA	4x Channels configured to voltage output, ADC is disabled
DVCC Current	2.0	2.8	3.3	mA	
AVCC Current	5.5	7.2	8.5	mA	
DO_VDD Current	300	400	480	µA	4x Channels configured to high impedance with DO enabled, ADC is disabled, no load
CONFIGURATION TIMING[1]					
Device Power-Up Time		1		ms	After all supplies are powered up
Device Reset Time		1		ms	Time taken for device reset and calibration memory upload to complete hardware or software reset events after the device is powered up (for the pulse-width specifications, see Table 14)
Channel Function Initialization Time		300		µs	Time in use case before changing to another use case, wait time after the CH_FUNC_SETUP register is programmed before new DAC codes can be loaded
IOUT_HART Channel Function Initialization Time		4.2		ms	VIOUT_DRV_EN_DLY = 0, during channel initialization time, output does not settle
		300		µs	VIOUT_DRV_EN_DLY = 1

1 Guaranteed by design and characterization.

2 AVDD_HI (or AVDD_LO): Currently active voltage rail connected by adaptive power switching block. For detailed description, see the Adaptive Power Switching section.

3 x = A, B, C, and D.

SPECIFICATIONS

SPI TIMING CHARACTERISTICS

SPI Timing Specifications

AVDD_HI = +6V to +28.8V, AVDD_LO = +6V to +28.8V, AVSS = −2.5V to −18V, AGND = DGND = 0V, REFIO = +2.5V (ideal), DVCC = +2.7V to +5.5V, AVCC = +4.5V to +5.5V, and all specifications are at T_A = −40°C to +105°C, unless otherwise noted.

Table 14. SPI Timing Specifications

Parameter[1, 2]	Description	SDO C_{LOAD} = 30pF	SDO C_{LOAD} = 50pF	Unit
t_1	SCLK pin cycle time	50	62.5	ns min
t_2	SCLK high time	17	23	ns min
t_3	SCLK low time	17	23	ns min
t_4	SYNC falling edge to SCLK falling edge setup time	t1/2	t1/2	ns min
t_5	Last SCLK falling edge to SYNC rising edge	t1/2	t1/2	ns min
t_6	SYNC high time	420	420	ns min
t_7	Data setup time	5	5	ns min
t_8	Data hold time	5	5	ns min
t_9	RESET pulse width	50	50	µs min
t_{10}	SCLK rising edge to SDO valid	23	28	ns max
t_{11}	SYNC falling edge to SDO valid (for readback MSB only)	22	25	ns max
t_{12}	SYNC rising edge to SDO tristate	14	16	ns max
t_{13}	SYNC rising edge to DAC output response time	2	2	µs typ
t_{14}[3]	ADC_RDY pulse	25	25	µs typ

[1] All input signals are specified with t_R = t_F = 5ns (10% to 90% of the voltage on the DVCC pin (V_{DVCC})) and timed from a voltage level of V_{DVDD}/2.

[2] Guaranteed by design and characterization, not production tested.

[3] See Figure 51.

SPI Timing Diagram

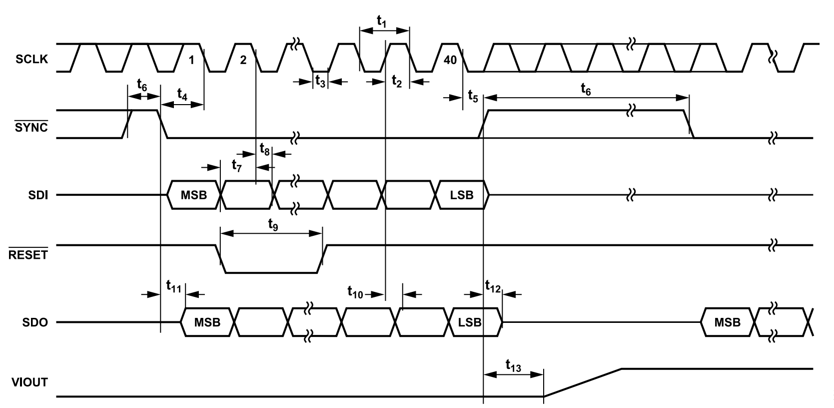


Figure 2. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 15. Absolute Maximum Ratings

Parameter	Rating
AVDD_HI and AVDD_LO to AGND	−0.3V to +36V
AVSS to AGND	−20V to +0.3V
AVDD_HI and AVDD_LO to AVSS	56V
DVCC to AGND	−0.3V to +6V
AVCC to AGND	−0.3V to +6V
DO_VDD to AGND	−0.3V to +40V
REFIO and LVIN to AGND	−0.3V to AVCC + 0.3V
SENSEHF_x[1], SENSELF_x[1], VSENSEP_x[1] and VSENSEP_x[1] to AGND	−50V to +50V
VIOUT_x[1] to AGND	−50V to +50V
CCOMP_x[1] to AGND	AVSS − 0.3V to +50V
DO_SRC_SNS_x[1] to DO_VDD	−6V to +0.3V
DO_SRC_GATE_x[1] to DO_VDD	−15V to +0.3V
LKG_COMP_x[1] to AGND	−50V to DO_VDD + 0.3V
Digital Inputs to DGND ($\overline{\text{RESET}}$, $\overline{\text{SYNC}}$, SCLK, and SDI)	−0.3V to DVCC + 0.3V
Logic Digital Outputs to DGND (GPIO_n[2], SDO, $\overline{\text{ALERT}}$, $\overline{\text{ADC\_RDY}}$)	−0.3V to DVCC + 0.3V
DGND to AGND	−0.3V to +0.3V
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C
T_J Maximum[3]	125°C
Reflow Profile	JEDEC Industry Standard J-STD-020
Power Dissipation	(T_J maximum − T_A)/θ_{JA}

[1] x = A, B, C, and D.

[2] n = A, B, C, D, E, and F.

[3] It is important to manage the power dissipation of the AD74416H to ensure that the maximum T_J is not violated. It is also recommended to enable the thermal shutdown function to avoid damage to the AD74416H.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance.

Table 16. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-64-15	23.8	0.8	°C/W

[1] Based on simulated data using a JEDEC 2S2P thermal test board with a 7 × 7 array of thermal vias in a JEDEC natural convection environment. For more details, refer to the JEDEC specification JESD-51.

[2] Read at the exposed paddle surface with the cold plate in direct contact with the package top surface.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in and ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

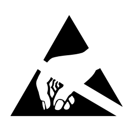
Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD74416H

Table 17. AD74416H, 64-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±1750	1C
FICDM	±500	C2a

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

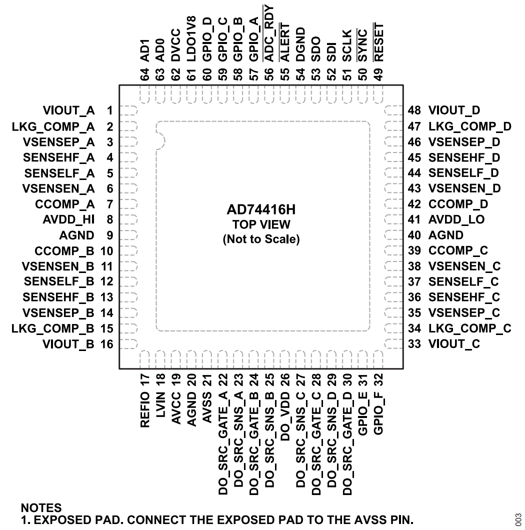


Figure 3. Pin Configuration

Table 18. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	VIOUT_A	Voltage or Current Force Pin on Channel A. VIOUT_A provides a voltage or a current to the I/OP screw terminal.
2	LKG_COMP_A	Leakage Compensation on Channel A. The LKG_COMP_A pin provides leakage compensation for high precision measurements. Leakage of the PMOS transistor used in digital output mode is compensated using this pin. If the digital output function with an external FET is not used, leave the LKG_COMP_A pin unconnected.
3	VSENSEP_A	Positive Voltage Sensing Pin on Channel A.
4	SENSEHF_A	Filtered High-Side Sense Pin on Channel A. The SENSEHF_A pin can be switched to an ADC input and is routed to the AD74416H side of R_{SENSE} through the off-chip filter.
5	SENSELF_A	Filtered Low-Side Sense Pin on Channel A. The SENSELF_A pin can be switched to an ADC input and is routed to the I/OP screw terminal side of R_{SENSE} through the off-chip filter.
6	VSENSEN_A	Negative Voltage Sensing Pin on Channel A. The VSENSEN_A pin can be used as auxiliary high voltage sensing pin.
7	CCOMP_A	Compensation Capacitor Pin on Channel A. The CCOMP_A pin allows the AD74416H to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_A pin and the I/O screw terminal.
8	AVDD_HI[1]	Positive Analog Supply High. If the adaptive power switching feature is not used, connect the AVDD_HI pin and the AVDD_LO pin together.
9	AGND	Analog Ground.
10	CCOMP_B	Compensation Capacitor Pin on Channel B. CCOMP_B allows the AD74416H to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP pin and the I/O screw terminal.
11	VSENSEN_B	Negative Voltage Sensing Pin on Channel B. Use as auxiliary high voltage sensing pin.
12	SENSELF_B	Filtered Low-Side Sense Pin on Channel B. The SENSELF_B pin can be switched to an ADC input and is routed to the I/OP screw terminal side of R_{SENSE} through the off-chip filter.
13	SENSEHF_B	Filtered High-Side Sense Pin on Channel B. The SENSEHF_B pin can be switched to an ADC input and is routed to the AD74416H side of R_{SENSE} through the off-chip filter.
14	VSENSEP_B	Positive Voltage Sensing Pin on Channel B.
15	LKG_COMP_B	Leakage Compensation on Channel B. The LKG_COMP_B pin provides leakage compensation for high precision measurements. Leakage of the PMOS transistor used in digital output mode is compensated using this pin. If the digital output function with an external FET is not used, leave the LKG_COMP_B pin unconnected.
16	VIOUT_B	Voltage or Current Force Pin on Channel B. The VIOUT_B pin provides a voltage or a current to the I/OP screw terminal.
17	REFIO[1]	Internal 2.5V Reference Input and Output.
18	LVIN	Low Voltage Input Pin. The voltage on the LVIN pin can be measured by selecting the LVIN option in the diagnostics block. The measurement voltage range is 0V to 2.5V. For best performance, use an anti-aliasing filter on the LVIN pin.
19	AVCC[1]	5V Analog Supply.
20	AGND	Analog Ground.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 18. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Description
21	AVSS[1]	Negative Analog Supply.
22	DO_SRC_GATE_A	Sourcing Digital Output Gate Drive on Channel A. If the digital output function with an external FET is not used, leave the DO_SRC_GATE_A pin unconnected.
23	DO_SRC_SNS_A	Sourcing Digital Output Sense Pin on Channel A. If the digital output function with an external FET is not used, connect the DO_SRC_SNS_A pin to the DO_VDD pin.
24	DO_SRC_GATE_B	Sourcing Digital Output Gate Drive on Channel B. If the digital output function with an external FET is not used, leave the DO_SRC_GATE_B pin unconnected.
25	DO_SRC_SNS_B	Sourcing Digital Output Sense Pin on Channel B. If the digital output function with an external FET is not used, connect the DO_SRC_SNS_B pin to the DO_VDD pin.
26	DO_VDD[1]	Positive Supply for Digital Output Circuit. If the digital output functions with external FETs are not used, connect the DO_VDD pin to the AVDD_HI pin.
27	DO_SRC_SNS_C	Sourcing Digital Output Sense Pin on Channel C. If the digital output function with an external FET is not used, connect the DO_SRC_S NS_C pin to the DO_VDD pin.
28	DO_SRC_GATE_C	Sourcing Digital Output Gate Drive on Channel C. If the digital output function with an external FET is not used, leave the DO_SRC_GATE_C pin unconnected.
29	DO_SRC_SNS_D	Sourcing Digital Output Sense Pin on Channel D. If the digital output function with an external FET is not used, connect the DO_SRC_SNS_D pin to the DO_VDD pin.
30	DO_SRC_GATE_D	Sourcing Digital Output Gate Drive on Channel D. If the digital output function with an external FET is not used, leave the DO_SRC_GATE_D pin unconnected.
31	GPIO_E	General-Purpose Input and Output Pin E.
32	GPIO_F	General-Purpose Input and Output Pin F.
33	VIOUT_C	Voltage or Current Force Pin on Channel C. The VIOUT_C pin provides a voltage or a current to the I/OP screw terminal.
34	LKG_COMP_C	Leakage Compensation on Channel C. The LKG_COMP_C pin provides leakage compensation for high precision measurements. Leakage of the PMOS transistor used in digital output mode is compensated using this pin. If the digital output function with an external FET is not used, leave the LKG_COMP_C pin unconnected.
35	VSENSEP_C	Positive Voltage Sensing Pin on Channel C.
36	SENSEHF_C	Filtered High-Side Sense Pin on Channel C. The SENSEHF_C pin can be switched to an ADC input and is routed to the AD74416H side of R_{SENSE} through the off-chip filter.
37	SENSELF_C	Filtered Low-Side Sense Pin on Channel C. The SENSELF_C pin can be switched to an ADC input and is routed to the I/OP screw terminal side of R_{SENSE} through the off-chip filter.
38	VSENSEN_C	Negative Voltage Sensing Pin on Channel C. The VSENSEN_C pin can be used as auxiliary high voltage sensing pin.
39	CCOMP_C	Compensation Capacitor Pin on Channel C. The CCOMP_C pin allows the AD74416H to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_C pin and the I/O screw terminal.
40	AGND	Analog Ground.
41	AVDD_LO[1]	Positive Analog Supply Low. If adaptive power switching feature is not used, connect the AVDD_HI pin and the AVDD_LO pin together.
42	CCOMP_D	Compensation Capacitor Pin on Channel D. The CCOMP_D pin allows the AD74416H to drive high capacitive loads in the voltage output use case. Connect the capacitor between the CCOMP_D pin and the I/O screw terminal.
43	VSENSEN_D	Negative Voltage Sensing Pin on Channel D. The VSENSEN_D pin can be used as auxiliary high voltage sensing pin.
44	SENSELF_D	Filtered Low-Side Sense Pin on Channel D. The SENSELF_D pin can be switched to an ADC input and is routed to the I/OP screw terminal side of R_{SENSE} through the off-chip filter.
45	SENSEHF_D	Filtered High-Side Sense Pin on Channel D. The SENSEHF_D pin can be switched to an ADC input and is routed to the AD74416H side of R_{SENSE} through the off-chip filter.
46	VSENSEP_D	Positive Voltage Sensing Pin on Channel D.
47	LKG_COMP_D	Leakage Compensation on Channel D. The LKG_COMP_D pin provides leakage compensation for high precision measurements. Leakage of the PMOS transistor used in digital output mode is compensated using this pin. If the digital output function with an external FET is not used, leave the LKG_COMP_D pin unconnected.
48	VIOUT_D	Voltage or Current Force Pin on Channel B. The VIOUT_D pin provides a voltage or a current to the I/OP screw terminal.
49	$\overline{RESET}$	Hardware Reset Pin. Active low input. The $\overline{RESET}$ pin resets the AD74416H to the power-on state.
50	$\overline{SYNC}$	Serial Interface Frame Synchronization Pin. Active low input.
51	SCLK	Serial Interface Clock.
52	SDI	Serial Interface Data In.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 18. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Description
53	SDO	Serial Interface Data Out.
54	DGND	Digital Ground.
55	$\overline{\text{ALERT}}$	Active Low, Open-Drain Output. The $\overline{\text{ALERT}}$ pin asserts low when an alert condition occurs. Read the ALERT_STATUS register when this pin is asserted. Connect this pin to the DVCC pin via a pull-up resistor.
56	$\overline{\text{ADC\_RDY}}$	Active Low, Open-Drain Output. The $\overline{\text{ADC\_RDY}}$ pin asserts when ADC conversion result(s) are ready to be read. Connect the $\overline{\text{ADC\_RDY}}$ pin to a pull-up resistor to the DVCC pin.
57	GPIO_A	General-Purpose Input and Output Pin A.
58	GPIO_B	General-Purpose Input and Output Pin B.
59	GPIO_C	General-Purpose Input and Output Pin C.
60	GPIO_D	General-Purpose Input and Output Pin D.
61	LDO1V8[1]	1.8V Low Dropout Output (LDO). Do not use the LDO1V8 pin externally.
62	DVCC[1]	Digital Supply. Decouple the DVCC pin with the recommended capacitor listed in Table 38.
63	AD0	Device Address Pin 0. The AD0 pin and the AD1 pin set the address for the SPI. AD0 and AD1 are internally connected to DGND by weak pull-down resistors.
64	AD1	Device Address Pin 1. The AD0 pin and the AD1 pin set the address for the SPI. AD0 and AD1 are internally connected to DGND by weak pull-down resistors.
	Exposed Pad	Exposed Pad. Connect the exposed pad to the AVSS pin.

[1] Connect the recommended decoupling capacitors, as shown in Table 38.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE OUTPUT

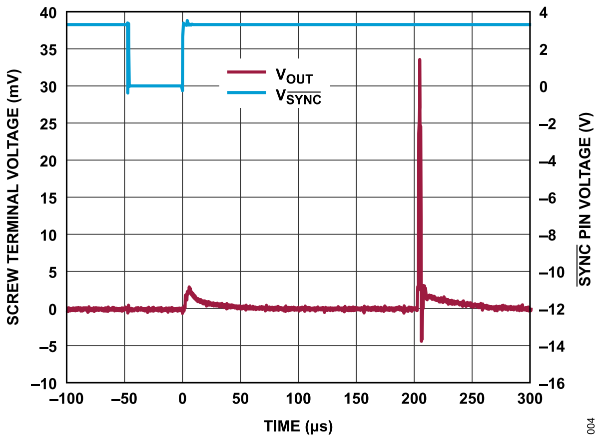


Figure 4. Screw Terminal Voltage (V_{OUT}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Voltage Output Enabled

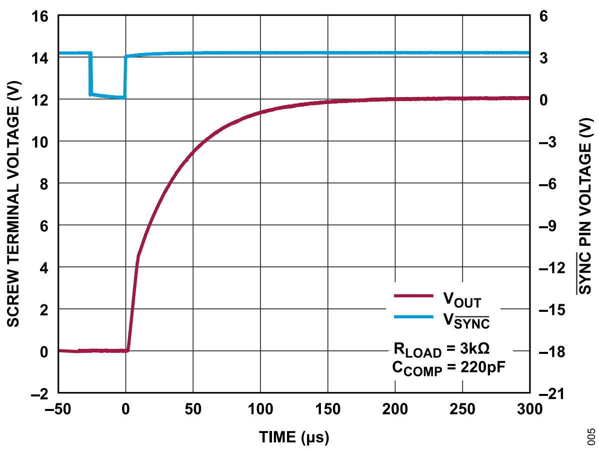


Figure 5. Full-Scale Positive Step with C_{COMP} Connected

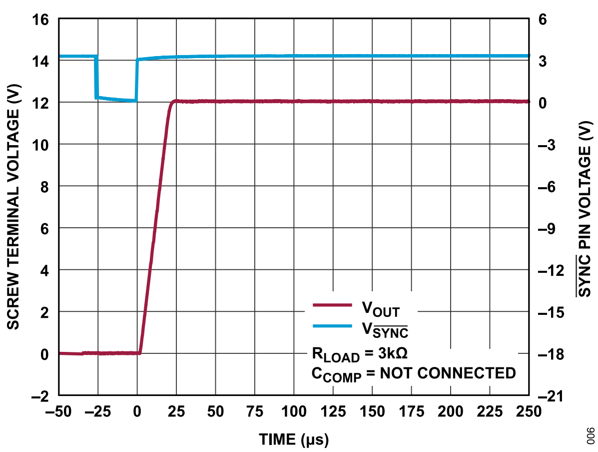


Figure 6. Full-Scale Positive Step without C_{COMP}

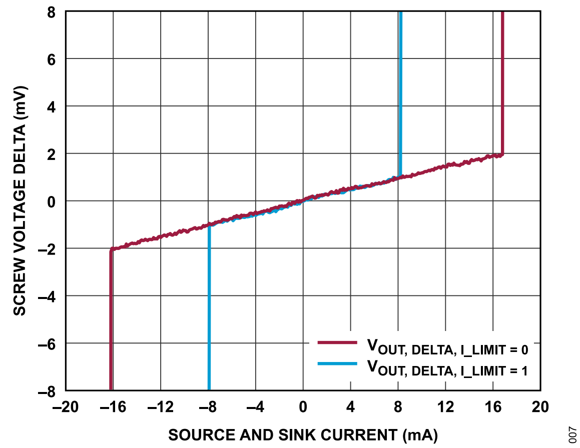


Figure 7. Output Voltage Change ($V_{OUT, DELTA}$) vs. Source and Sink Current

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT OUTPUT (I_{OUT})

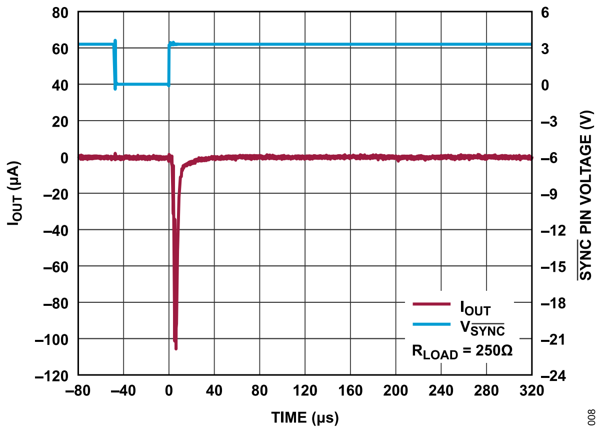


Figure 8. I_{OUT} and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time on Current Output Enable

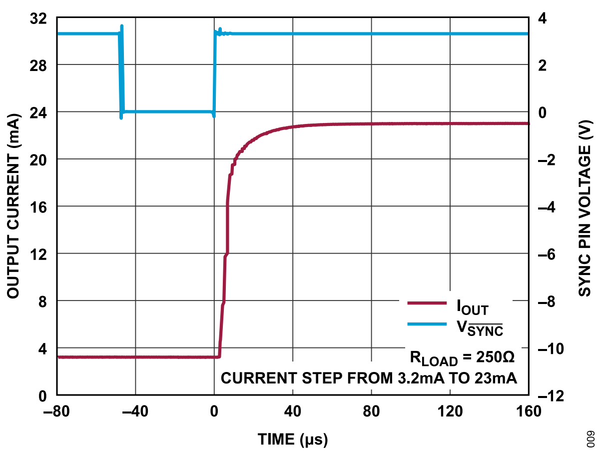


Figure 9. Output Current (I_{OUT}) and $\overline{SYNC}$ Pin Voltage ($V_{\overline{SYNC}}$) vs. Time

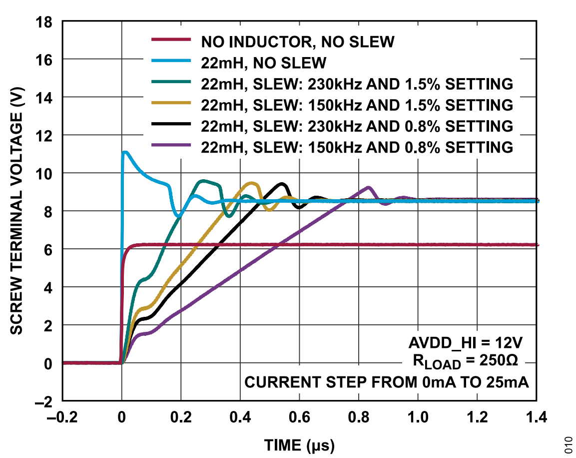


Figure 10. I_{OUT} Settling Time with Inductive Load and with and Without Slew Rate Enabled

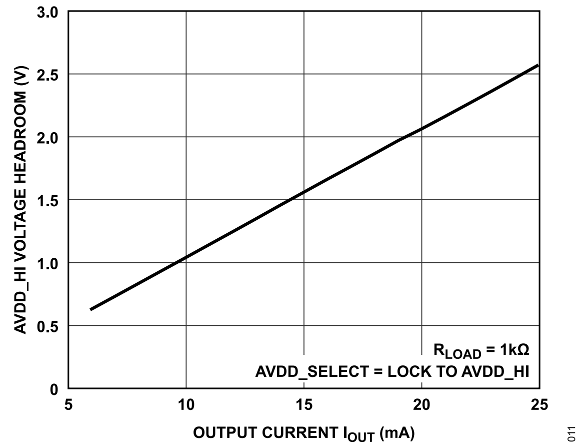


Figure 11. AVDD_HI Voltage Headroom vs. I_{OUT}

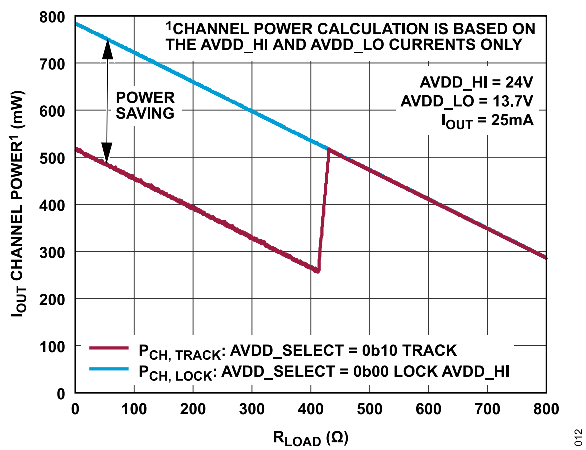


Figure 12. Advantage of Adaptive Power Switching in AD74416H Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS

RTD MEASUREMENT

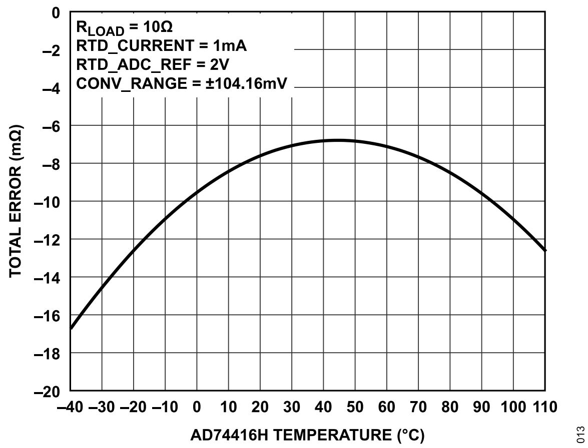


Figure 13. Total Error of the 3-Wire PT10 at Nominal Resistance

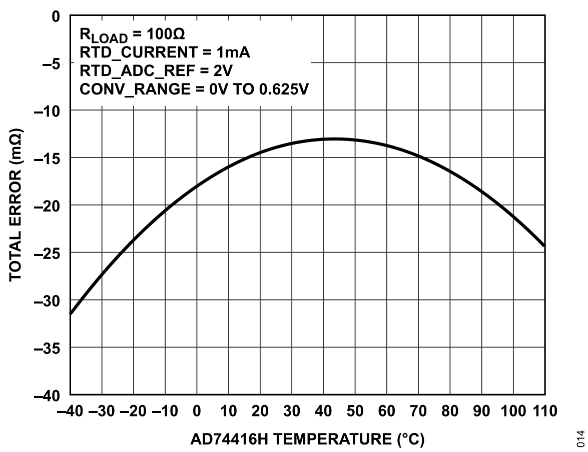


Figure 14. Total Error of the 3-Wire PT100 at Nominal Resistance

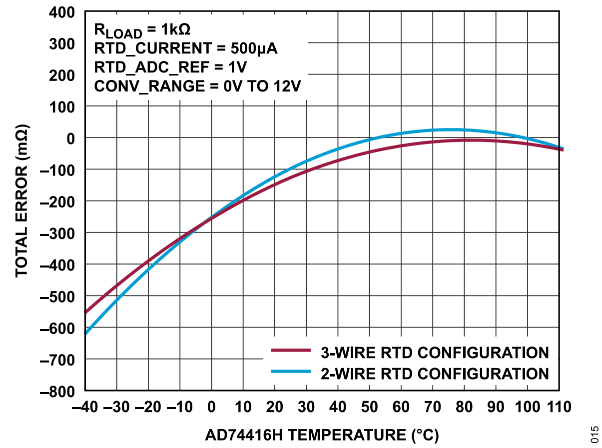


Figure 15. Total Error of the 2-Wire and 3-Wire PT1000 at Nominal Resistance

TYPICAL PERFORMANCE CHARACTERISTICS

ADC

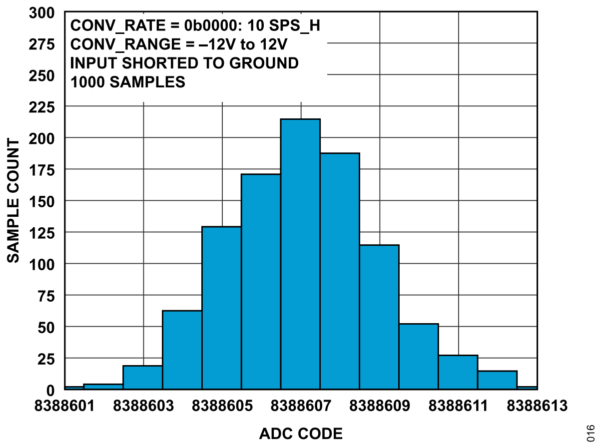


Figure 16. ADC Noise Histogram with Output Data Rate (ODR) = 10SPS

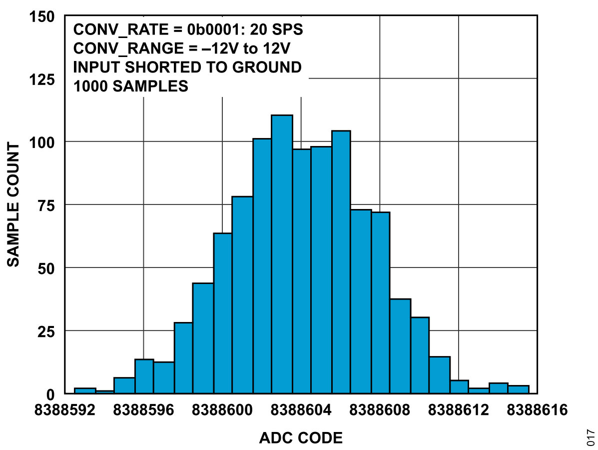


Figure 17. ADC Noise Histogram with ODR = 20SPS

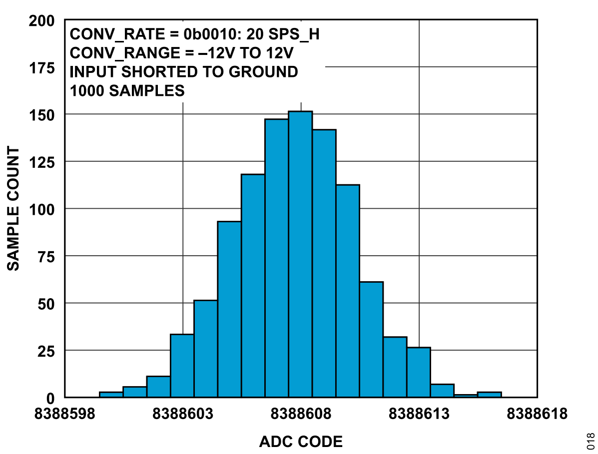


Figure 18. ADC Noise Histogram with ODR = 20SPS_H

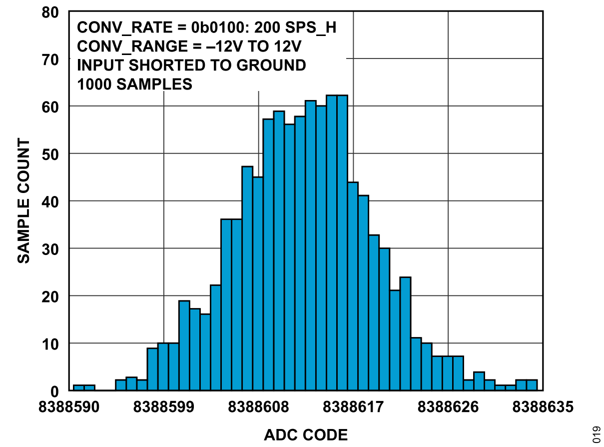


Figure 19. ADC Noise Histogram with ODR = 200SPS_H

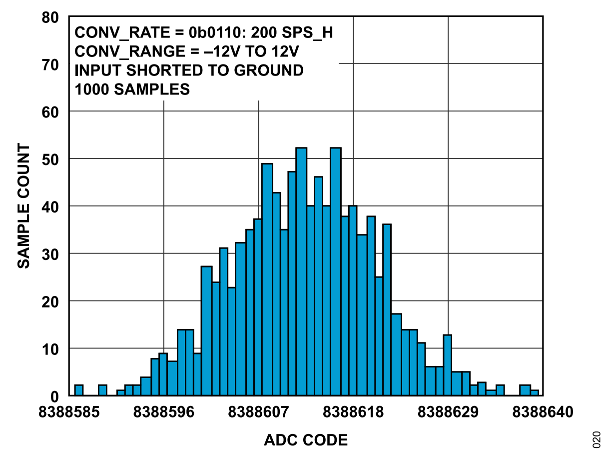


Figure 20. ADC Noise Histogram with ODR = 200SPS_H1

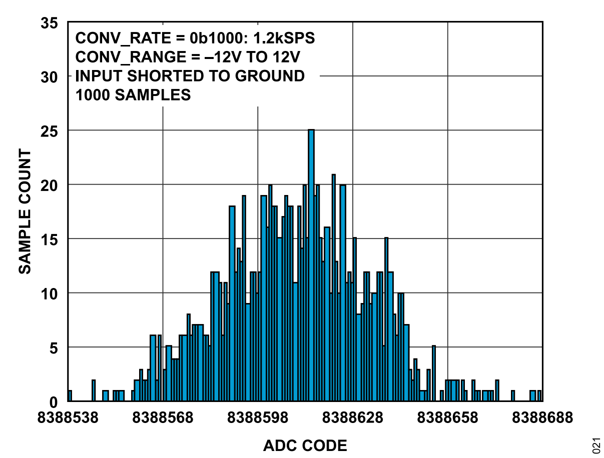


Figure 21. ADC Noise Histogram with ODR = 1.2kSPS

TYPICAL PERFORMANCE CHARACTERISTICS

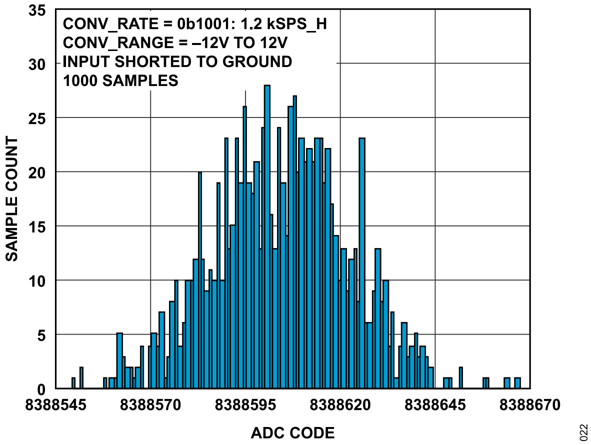


Figure 22. ADC Noise Histogram with ODR = 1.2kSPS_H

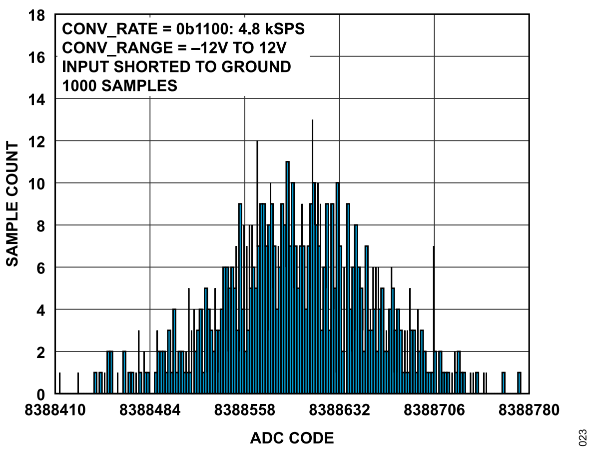


Figure 23. ADC Noise Histogram with ODR = 4.8kSPS

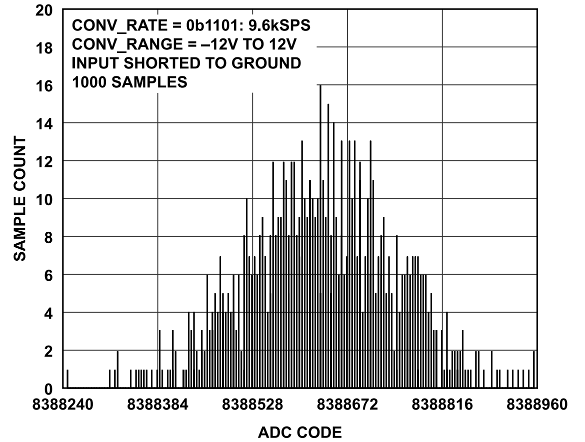


Figure 24. ADC Noise Histogram with ODR = 9.6kSPS

TYPICAL PERFORMANCE CHARACTERISTICS

REFERENCE

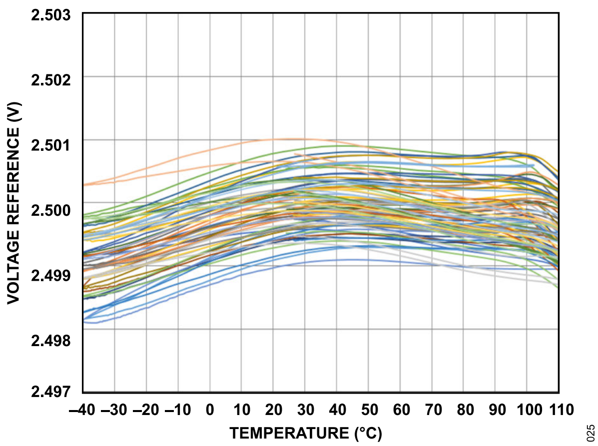


Figure 25. Voltage Reference vs. Temperature

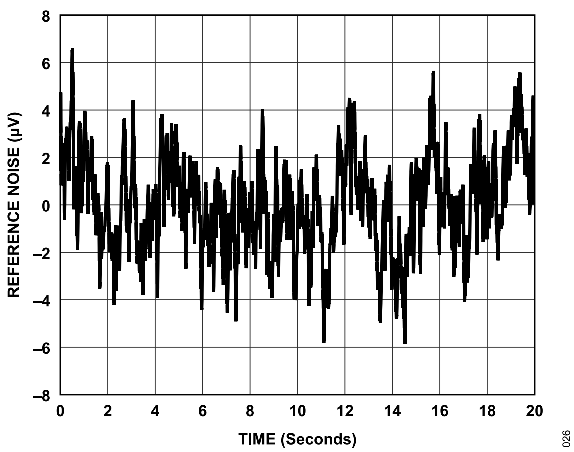


Figure 26. Peak-to-Peak Noise (0.1Hz to 10Hz Bandwidth)

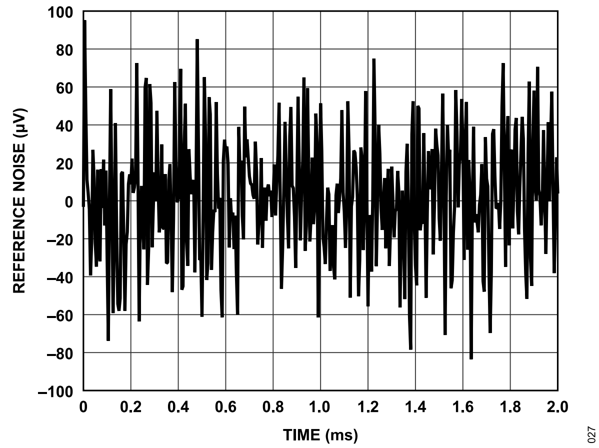


Figure 27. Peak-to-Peak Noise (100kHz Bandwidth)

TYPICAL PERFORMANCE CHARACTERISTICS

HART

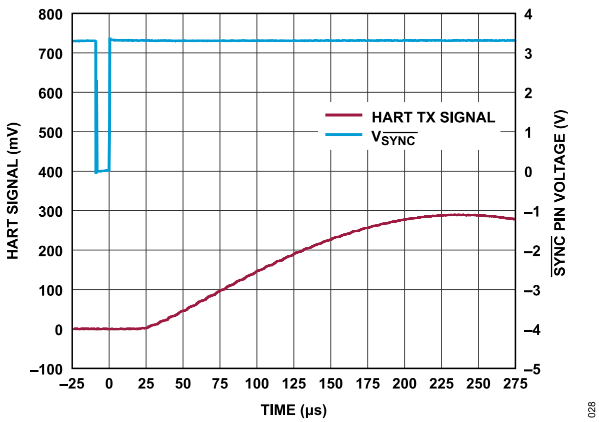


Figure 28. Carrier Start Time

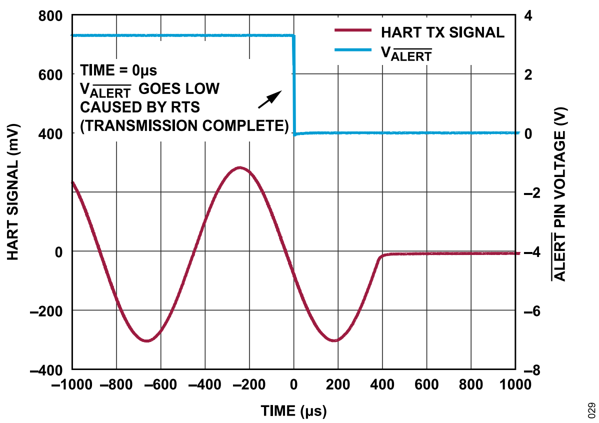


Figure 29. Carrier Stop Time

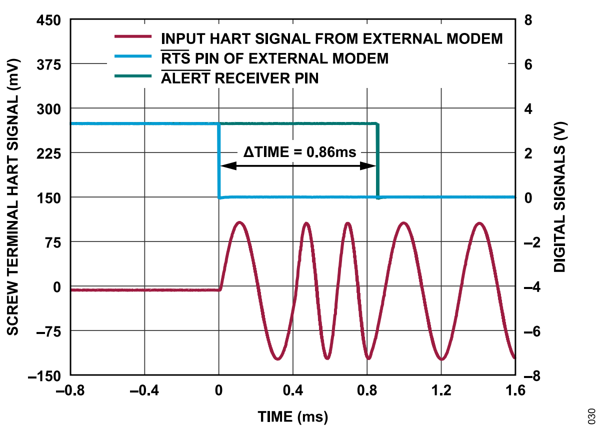


Figure 30. Carrier Detect On Time (Assertion of $\overline{ALERT}$ Pin)

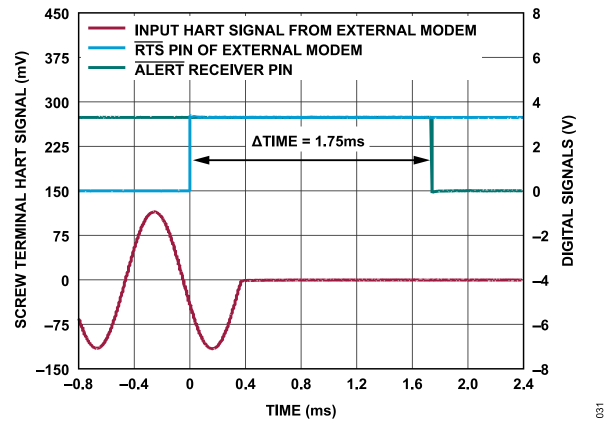


Figure 31. Carrier Detect Off Time (Till $\overline{ALERT}$ Pin Assert)

TYPICAL PERFORMANCE CHARACTERISTICS

OTHERS

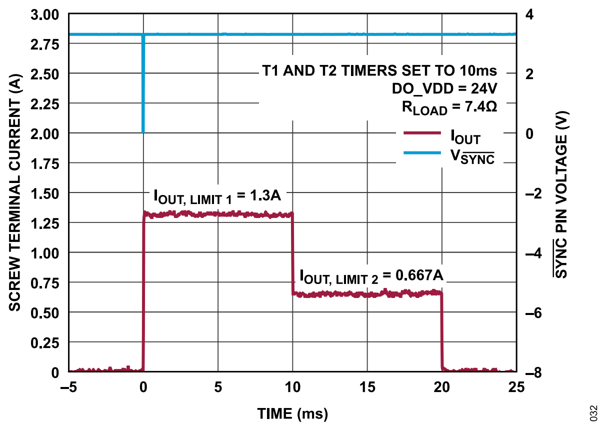


Figure 32. Digital Output Programmable Short-Circuit Activation

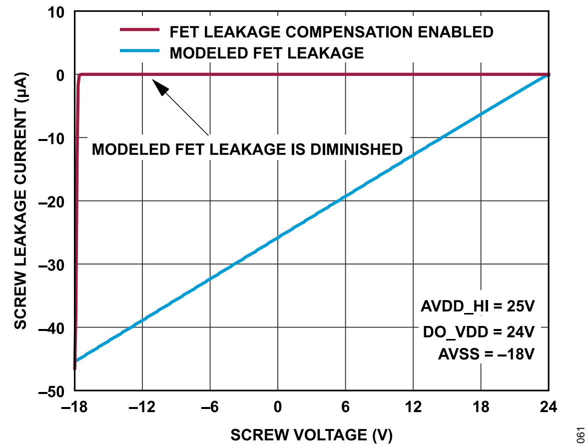


Figure 33. Function of Current Leakage Compensation

TERMINOLOGY

ADC Offset Error

For unipolar input ranges, ADC offset error is the deviation from the zero-scale code (0x000000) when inputs are shorted, 0V. The error is expressed in ppm FSR.

For bipolar input ranges, ADC offset error is the deviation from the midscale code (0x800000) when inputs are shorted, 0V. The error is expressed in ppm FSR.

ADC Gain Error

Gain error applies to both unipolar and bipolar ranges. Gain error is a measure of the span error of the ADC.

For input ranges, gain error is defined as the full-scale error minus the zero-scale error. The error is expressed in ppm FSR.

DAC Offset Error

Offset error is the deviation of the analog output from the ideal zero-scale output when the DAC output register is loaded with 0x0. The offset error is expressed in mV or µA in case of I_{OUT} mode.

DAC Bipolar Zero Error

Bipolar zero error is the deviation of the analog output from the ideal midscale output of 0V when the DAC output register is loaded with 0x8000. This error applies only to bipolar output ranges.

DAC Gain Error

Gain error is a measure of the span error of the DAC. This error is the deviation in slope of the DAC transfer characteristic from the ideal expressed in % FSR.

Total Unadjusted Error (TUE)

TUE is the total deviation of the output from the ideal. TUE includes INL, offset, and gain error.

THEORY OF OPERATION

The AD74416H is a quad-channel, software configurable input and output device that is designed to meet the requirements of process control and factory automation applications. The device provides a fully integrated single chip solution for input and output operation. The AD74416H features a single 24-bit, Σ-Δ ADC, four 16-bit DACs, and the device is packaged in a 9 mm × 9 mm, 64-lead LFCSP. The AD74416H also includes four integrated HART modems, one per channel.

The channel is configured by writing to the configuration registers. Users can refine the default configurations of each operation mode by the AD74416H register map. For a detailed functional block diagram of the AD74416H, see Figure 34.

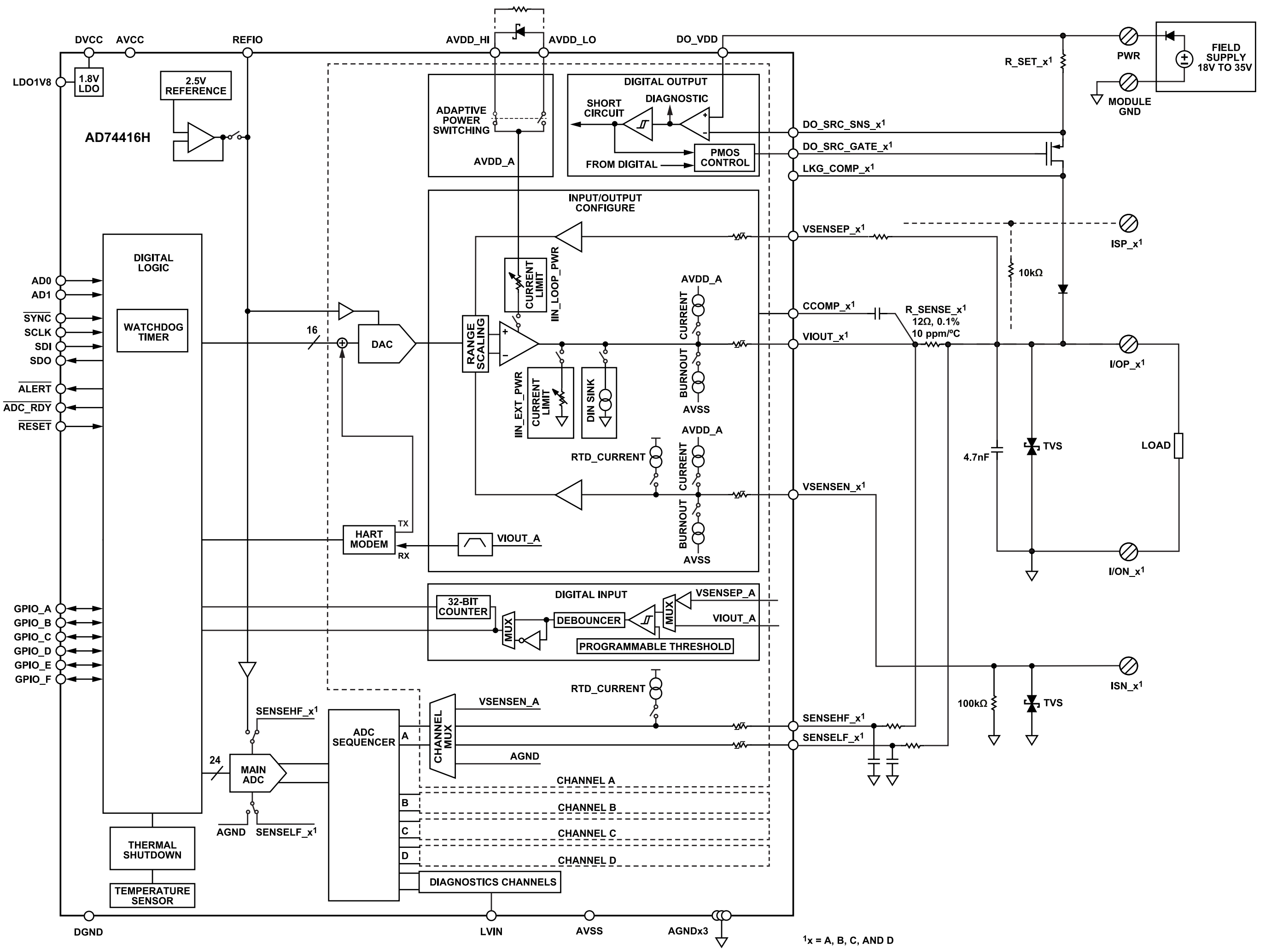


Figure 34. Detailed Functional Block Diagram

THEORY OF OPERATION

OPERATIONAL OUTLINE

Table 19 shows the operational use of the screw terminals of the AD74416H in different function configuration. For detailed description of each function, see the sections mentioned under Theory of Operation.

Table 19. Operational Outline of the AD74416H

	Main I/O Screw Terminals		Sensing Terminals		Auxiliary Measurement	
AD74416H Function	I/OP_x[1] Input/Output Positive	I/ON_x[1] Input/Output Negative	ISP_x[1] Input Sense Positive	ISN_x[1] Input Sense Negative	LVIN Pin[2] Low Voltage ADC INPUT[3]	Func. Access
High Impedance	High Impedance	High Impedance	N/A[4]	Auxiliary ADC input	Available[5]	N/A[4]
Voltage Output 2-Wire Feedback[6]	Output and Feedback Sensing	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Voltage Output 3-Wire Feedback[6]	Output	Return Path	Feedback Sensing	Auxiliary ADC Input	Available[5]	SPI
Voltage Output 4-Wire Feedback[6]	Output	Return Path	Feedback Sensing	Feedback Sensing	Available[5]	SPI
Current Output	Output	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Voltage Input	Input	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Current Input, Externally Powered	Input	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Current Input, Loop Powered	Input	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Resistance Measurement 3-Wire RTD	Terminal 1	Terminal 2	N/A[4]	Terminal 3	Available[5]	SPI
Resistance Measurement 2-Wire RTD	Terminal 1	Terminal 2	N/A[4]	Auxiliary ADC Input	Available[5]	SPI
Digital Input Logic	Input	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI and GPIO
Digital Input, Loop Powered	Input	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI and GPIO
Digital Output	Output	Return Path	N/A[4]	Auxiliary ADC Input	Available[5]	SPI and GPIO

1 x = A, B, C, and D, which corresponds to channel A, B, C, and D.

2 Use channel diagnostic to enable LVIN pin.

3 For detailed description, see the Diagnostics section.

4 N/A means not applicable.

5 Diagnostic measurements are available to use.

6 For detailed description, see the 4-, 3-, and 2-Wire Feedback Sensing Modes section.

THEORY OF OPERATION

ROBUST ARCHITECTURE

The AD74416H system is robust in noisy environments and can withstand overvoltage scenarios such as miswire and surge events.

On-chip line protectors ensure that the I/OP screw terminal does not provide power to the IC when brought to a higher potential than the AVDD_HI pin or AVDD_LO supplies.

The recommended external components shown in Figure 34 and Table 38, which include the transient voltage suppressor (TVS), are selected to withstand surges on the input and output terminals.

With the recommended components, the I/OP and I/ON screw terminals tolerate overvoltages up to DC ± 36V (limited by the external TVS), when part is configured to any channel function.

A cyclic redundancy check (CRC) function is built into the SPI to ensure error free communications in noisy environments.

POWER SUPPLIES AND REFERENCE

A maximum of six external voltage supply rails are required to power up the AD74416H as follows:

- +AVDD_HI and +AVDD_LO are the two positive analog supply to offer adaptive power switching functionality.
- −AVSS is the negative analog supply.
- +AVCC is the low-voltage analog supply.
- +DVCC is the digital supply, which determines the voltage levels of the digital interface.
- +DO_VDD is the supply for digital output, typically implemented as field supply.

For the voltage range of the external power supplies and the associated conditions, see Table 13. It is possible to connect the DVCC and AVCC together to limit number of power supplies in the system.

AVDD_HI must always be more positive than AVDD_LO. If this cannot be guaranteed, especially during power-up transients, a Schottky diode is placed between the AVDD_HI pin and the AVDD_LO pin, as shown in Figure 35. The recommended Schottky diode is shown in Table 38.

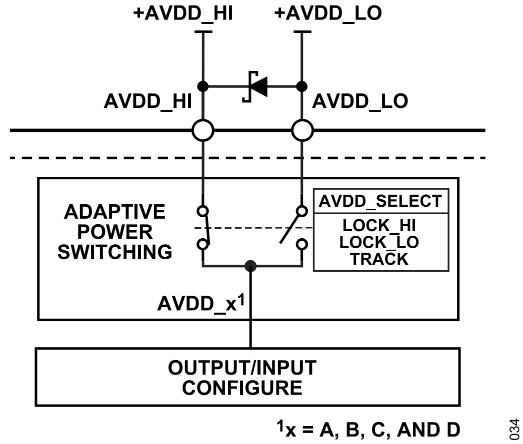


Figure 35. Dual AVDD Supply Configuration

Use a single AVDD supply configuration when adaptive power switching functionality is not required. Corresponding voltage supply rail to AVDD_HI pin is provided and resistor placed between AVDD_HI and AVDD_LO pins, as shown in the Figure 36. Resistor value is specified in Table 38. The LOCK_HI option for the AVDD_SELECT pin is automatically forced once the AVDD_HI pin and the AVDD_LO pin are connected together by the resistor. For more details concerning adaptive power switching and relevant configurations, see the Adaptive Power Switching section.

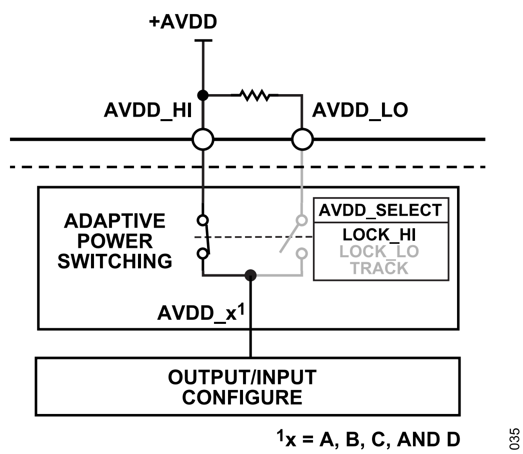


Figure 36. Single AVDD Supply Configuration

Powering on the AD74416H

When powering up the AD74416H, apply ground connections first. After power-up, wait for the device power-up time (see Table 13) before any transaction to the device can take place.

Upon initial power-up or a device reset of the AD74416H, the output channel is disabled and placed in a high-impedance state by default.

THEORY OF OPERATION

Adaptive Power Switching

The AD74416H features adaptive power switching. When enabled, the AD74416H adaptive power switching allows power savings and reduced heat dissipation.

Adaptive power switching is using two separated voltage supply rails, AVDD_HI and AVDD_LO. AVDD_HI stands for AVDD supply voltage high, and AVDD_LO stands for AVDD supply voltage low. Determine a precise ratio of the AVDD_HI and AVDD_LO based upon specific application to obtain required results and power saving. For the examples of recommended AVDD supply configurations, see Table 20.

When the AD74416H is configured in current output mode, the voltage headroom determines which supply rail is providing power to the load. The automatic transition takes place of the relevant supply rail (AVDD_HI or AVDD_LO) to the connected load. An example of the single current output channel power saving is shown in Figure 12.

Table 20. Recommended Main AVDD Supply Configuration

AVDD_HI	AVDD_LO	Maximal Load (Ω)[1]
25.1V ± 5%	14.3V ± 5%	800
24.0V ± 5%	13.7V ± 5%	760
22.5V ± 5%	13.0V ± 5%	700
21.2V ± 5%	12.3V ± 5%	650
19.8V ± 5%	11.6V ± 5%	600
18.5V ± 5%	10.9V ± 5%	550
17.2V ± 5%	10.3V ± 5%	500

[1] Assumed output current for maximal load condition is 25mA.

Adaptive power switching is automatically enabled once current output mode or current output with HART is selected using CH_FUNC_SETUP[n] register. If the adaptive power switching function is not required, lock power supply to use either the AVDD_HI supply rail or the AVDD_LO supply rail.

An adaptive power switching supply lock is available in the AVDD_SELECT bit field of the OUTPUT_CONFIG[n] register and allows manual switching to the required supply rail.

Reference

The AD74416H can operate with either an external or an internal reference. The reference input requires 2.5V for the AD74416H to function correctly. The reference voltage is internally buffered before being applied to the DAC and the ADC.

To enable internal reference, set the REF_EN bit in the PWR_OPTIM_CONFIG register.

DEVICE FUNCTIONS

The following sections describe the various programmable device functions of the AD74416H with block diagrams and guidelines on how to interpret the ADC results if converting with the default settings. These functions are programmed within the CH_FUNC_SETUP[n] register.

Each device function is configured with default measurement settings. However, users can adjust these settings as required within the register map.

High Impedance

High impedance is the default function upon power-up or after a device reset.

If a channel is held in high impedance for an extended time, such as when the analog input and output functions are not in use, it is recommended to enable a sinking burnout current of 1μA by programming the following bits in the I_BURNOUT_CONFIG register:

- BRN_VIOUT_POL to 0
- BRN_VIOUT_CURR to 10 binary

Interpreting ADC Data

In high-impedance mode, the ADC, by default, measures the voltage across the screw terminals (I/OP to I/ON) in a 0V to 12V range. Use the following equation to calculate the ADC measurement result:

$$V_{ADC} = (ADC\_CODE/16,777,216) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.
Voltage Range is the measurement range of the ADC and is 12V.

THEORY OF OPERATION

Voltage Output

The voltage output amplifier can generate unipolar or bipolar voltages in the 0V to +12V and ±12V ranges, respectively. Each range has 16 bits of resolution.

Voltage output is available in three feedback sensing modes described in the 4-, 3-, and 2-Wire Feedback Sensing Modes section.

In voltage output mode, the output range is set to 0V to 12V by default. To select bipolar mode, use the following sequence:

- Write 0x8000 to the DAC_CODE register to ensure 0V output.
- Set the VOUT_RANGE bit in the OUTPUT_CONFIG[n] register to 1 for bipolar outputs.
- Select the voltage output use case in the CH_FUNC bits, CH_FUNC_SETUP register.

Figure 37 shows the current path flowing from the VIOUT pin to the load, and the voltage feedback load sensing system adjusts V_{OUT} (output) voltage. Optionally, read the current flow to the load by using ADC measurement.

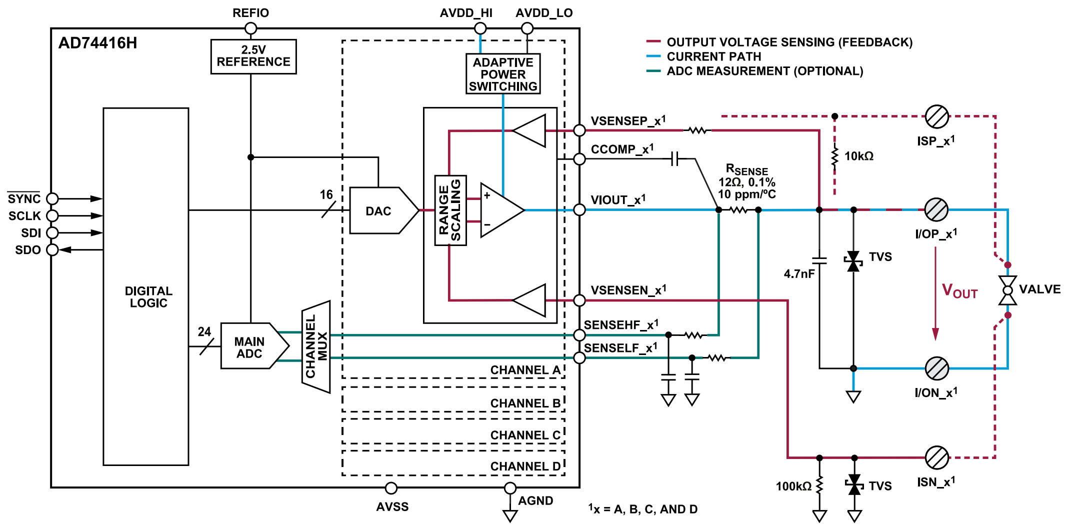


Figure 37. Voltage Output Mode Configuration

Short-Circuit Detection

There are two available short-circuit limits that a user can select by setting the I_LIMIT bit in the OUTPUT_CONFIG[n] registers. For the specified short-circuit current values, see Table 1. If the selected short-circuit limit is reached on a channel, a voltage output short-circuit error is flagged for that channel, and the ALERT pin asserts.

Interpreting ADC Data

In voltage output mode, the ADC, by default, measures the current through the R_{SENSE} in a −25mA to +25mA range. Use the ADC measurement result to calculate the current through the R_{SENSE} with the following equation:

$$I_{RSENSE} = \frac{\left(V_{MIN} + \left(\left(\frac{ADC\_CODE}{16,777,216}\right) \times Voltage\ Range\right)\right)}{R_{SENSE}}$$

where:

I_{RSENSE} is the measured current in amps. A negative current indicates that the current is sourced from the AD74416H. A positive current indicates that the AD74416H is sinking the current.

V_{MIN} is the minimum voltage of the selected ADC range, which is −0.3125V by default.

ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.

Voltage Range is the full span of the ADC range, which is 0.625V.

R_{SENSE} is the R_{SENSE} resistor, which is 12Ω.

4-, 3-, and 2-Wire Feedback Sensing Modes

The AD74416H offers voltage output mode in several feedback sensing modes: 4-wire, 3-wire, and 2-wire.

A 4-wire voltage output configuration uses the VSENSEP_x and the VSENSEN_x pins to sense the load voltage. The ISP_x and ISN_x terminals are connected to the load in the field. This results in a more accurate measurement as the output voltage is sensed differentially. To configure the channel as a 4-wire voltage output, set the VOUT_4W_EN bit in OUTPUT_CONFIG[n] register. Channel function is then set in the CH_FUNC_SETUP[n] register to voltage output by setting the CH_FUNC bit field to 1.

In 4-wire feedback sensing mode, a 100kΩ resistor must be connected between the VSENSEN_x pin and AGND to prevent a faulty state resulting from the ISN_x terminal disconnection from the load.

In 4- or 3-wire feedback sensing modes, a 10kΩ feedback resistor must be connected between the I/OP_x and ISP_x terminals. The feedback resistor closes the feedback loop and maintains stability in the event of the ISP_x terminal disconnection from the load.

THEORY OF OPERATION

The 3-wire configuration uses an ISP_x terminal connected to a VSENSEP_x pin to sense voltage on the load. To configure the channel as a 3-wire voltage output, clear the VOUT_4W_EN bit in the OUTPUT_CONFIG[n] register. Then the channel function is set in the CH_FUNC_SETUP[n] register to voltage output by setting the CH_FUNC bit field to 1.

Use the spare VSENSEN_x pin as an auxiliary input for the ADC.

A 2-wire configuration is possible to achieve by connecting the I/OP_x screw terminal directly to the VSENSEP_x pin by a serial protecting resistor. The voltage output channel in a 2-wire feedback sensing mode is configured in the same way as a 3-wire. The 2-wire configuration does not require a 10kΩ feedback resistor, and this resistor should not be connected to the system.

The VSENSEP_x serial resistor must be connected at all times. This resistor limits the input current to the VSENSEP_x pin during high voltage events. The recommended value of the VSENSEP_x serial resistor is shown in Table 38.

THEORY OF OPERATION

Current Output

In current output mode, the DAC provides a current output on the VIOUT_x pin that is regulated by an internal sensing resistor.

Figure 38 shows the output current path of the current output mode. Optionally, read the load voltage by using ADC measurement.

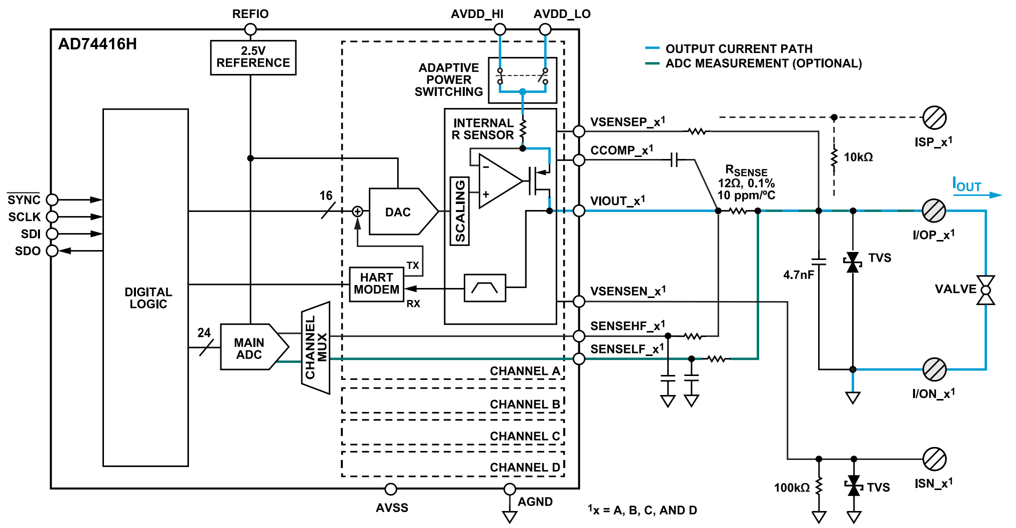


Figure 38. Current Output Mode Configuration

Open-Circuit Detection

In current output mode, if the headroom voltage falls below the compliance voltage (see Table 2), due to an open-loop circuit on the channel, a current output open-circuit error is flagged for that channel, and the ALERT pin asserts. If V_{AVDD_HI} (or V_{AVDD_LO}) is insufficient to drive the programmed current output, the open-circuit error is flagged.

Interpreting ADC Data

In current output mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/OP to I/ON) in a 0V to 12V range. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = (ADC\_CODE/16{,}777{,}216) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.
Voltage Range is the measurement range of the ADC and is 12V.

Current Output Mode with HART Compatibility

Current output mode with HART is compatible with HART transmit functionality when the HART compliant slew option by the SLEW_EN bit in the OUTPUT_CONFIG[n] register is enabled.

THEORY OF OPERATION

Voltage Input

In voltage input mode, the voltage across the screw terminals (I/OP_x to I/ON_x) is measured by the ADC by the SENSELF_x pin and the AGND pin. Figure 39 shows the burnout current and ADC measurement paths of the voltage input mode.

In voltage input mode, a user can measure the voltage up to ±12V. However, there is also an option to measure the I/OP_x screw terminal voltage using the diagnostics function. The diagnostics function allows the voltage to be measured across the full supply rails. For more details on the diagnostics measurements, see the Diagnostics section.

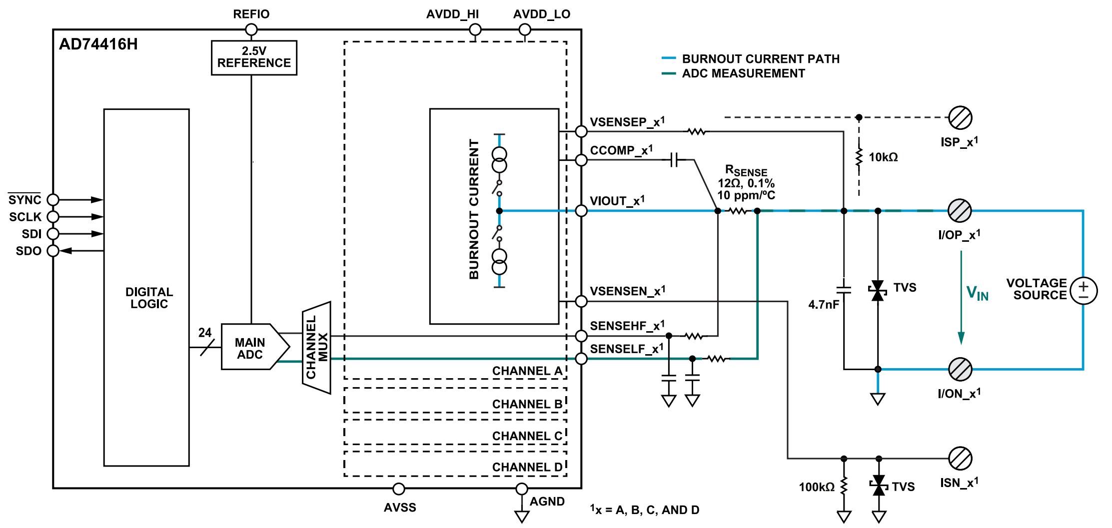


Figure 39. Voltage Input Mode Configuration

Open-Circuit Detection

Use the programmable burnout currents to detect an open-circuit in voltage input mode (see the Burnout Currents section). Configure the VIOUT_x pin with the required burnout current by writing to the I_BURNOUT_CONFIG[n] register.

If the I/OP_x screw terminal is floating, the SENSELF_x pin is pulled to the supply rail, and the ADC result generates a conversion error. Therefore, it is recommended to choose a burnout current value that is high enough to cover for the leakage currents in the circuit.

Interpreting the ADC Data

In voltage input mode, the ADC, by default, is configured to measure the voltage across the screw terminals (I/OP_x to I/ON_x) in a 0V to 12V range. Select a different range by using the CONV_RANGE bits in the ADC_CONFIG[n] register. Use the ADC measurement result to calculate the voltage across these screw terminals by using the following equation:

$$V_{ADC} = V_0 + (ADC\_CODE/16{,}777{,}216) \times Voltage\ Range$$

where:
V_0 is input voltage reading corresponding to ADC_CODE = 0 of the selected ADC range and is 0V by default (see Table 24).
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.
Voltage Range is the measurement range of the ADC and is 12V.

Thermocouple Measurement

Voltage input mode can measure the voltage of a thermocouple when the thermocouple is connected across the screw terminals (I/OP_x to I/ON_x). To accurately measure the thermocouple voltage, select the ±104mV input range by the ADC_CONFIG[n] register in voltage input mode.

THEORY OF OPERATION

Current Input, Externally Powered

In current input, externally powered mode, the AD74416H provides a current-limited path to ground by the VIOUT_x pin for an external current source. The 24-bit, Σ-Δ ADC is configured to measure the current through the R_{SENSE}. The current is measured by digitizing the voltage across the R_{SENSE} by the SENSEHF_x and the SENSELF_x pins. Figure 40 shows the input current and ADC measurement paths of the current input, externally powered mode.

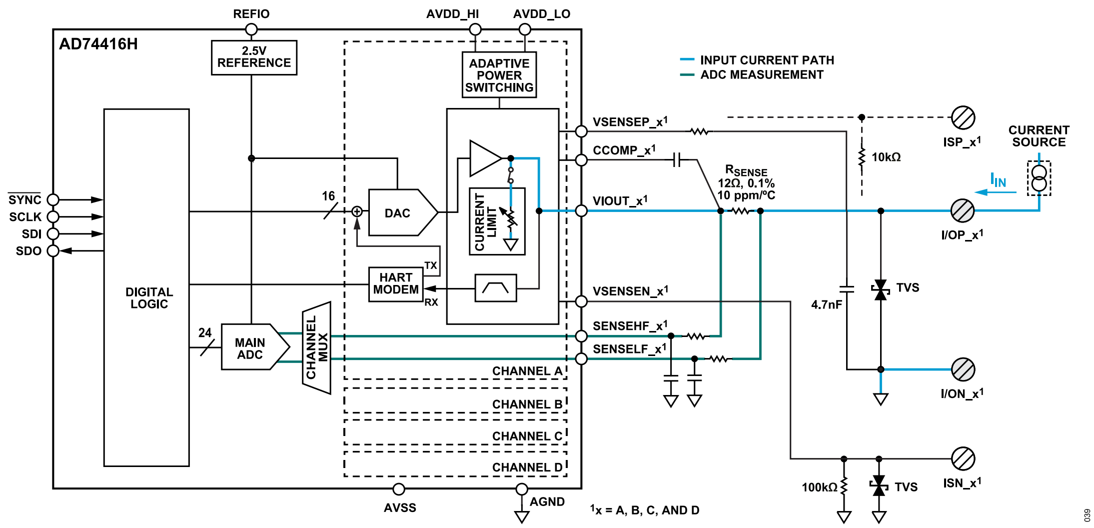


Figure 40. Current Input, Externally Powered Mode Configuration

Short-Circuit Protection and Detection

A short-circuit limit protects the external circuitry and limits the power dissipated on the AD74416H device. The value of the short-circuit limit is shown in Table 4.

In current input, externally powered mode, the digital input comparator is enabled by default to detect a short-circuit condition. The digital input comparator is enabled with a threshold voltage of AVDD_HI/2. In normal operation, the voltage on I/OP_x is typically within 5V of ground. If the current source attempts to sink a higher current than the short-circuit limit into the AD74416H, the voltage on the SENSEP_x pin instantly ramps. When the voltage on the I/OP_x screw terminal is more than the programmed threshold voltage, the comparator trips, sets the ANALOG_IO_SC bit in the CHANNEL_ALERT_STATUS[n] register.

Interpreting ADC Data

In current input mode, the ADC, by default, measures the current flowing from the I/OP_x screw terminal into the AD74416H through the R_{SENSE} in a 25mA range. Use the ADC measurement result to calculate the current through the R_{SENSE} with the following equation:

$$I_{R_{SENSE}} = \frac{\left(\left(\frac{ADC\_CODE}{16,777,216}\right) \times Voltage\ Range\right)}{R_{SENSE}}$$

where:

$I_{R_{SENSE}}$ is the measured current in amps.

ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.

Voltage Range is the full span of the ADC range and is 0.3125V.

R_{SENSE} is the sense resistor, which is set to 12Ω.

Current Input, Externally Powered with HART Mode

This mode is a HART-compatible version of the current input, externally powered mode. The input impedance is set to a minimum of 230Ω to be compliant with the HART receive impedance.

THEORY OF OPERATION

Current Input, Loop Powered

In current input loop, powered mode, the AD74416H provides a current-limited voltage to the I/OP_x screw terminal. Program the DAC_CODE[n] register to set the required current limit within the loop. DAC code setting is recommended to be performed before changing channel function to current input, loop powered. Switching to the channel function before setting the DAC code to the required value may cause irrelevant detection of short-circuit.

The input current is measured by digitizing the voltage across the R_{SENSE} by the SENSEHF_x and the SENSELF_x pins. Figure 41 shows the loop current and ADC measurement paths of the current input, loop powered mode.

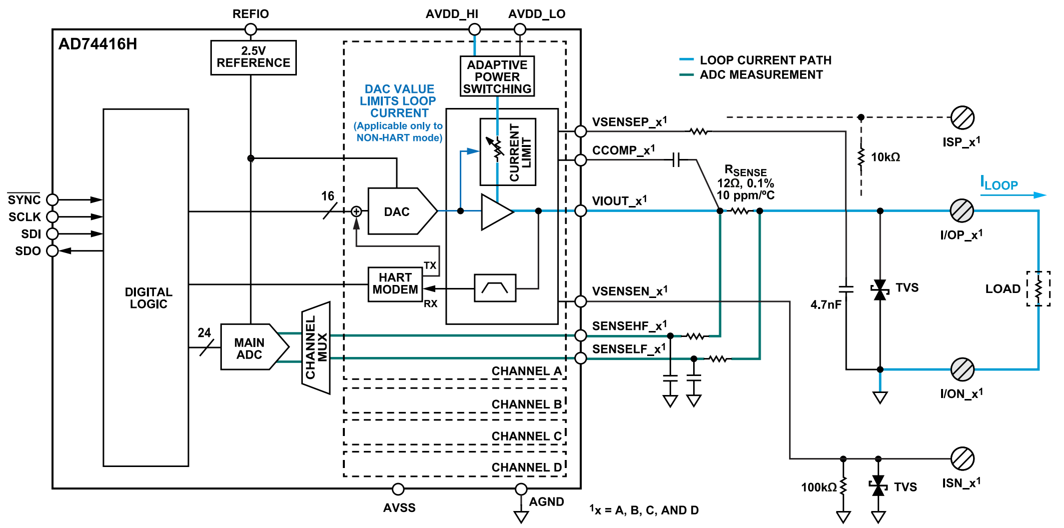


Figure 41. Current Input, Loop Powered Mode Configuration

Short-Circuit Protection and Detection

The current from the AD74416H is limited by short-circuit limit protection circuitry, with the value of the short-circuit limit, as shown in Table 5. The comparator is enabled by default to detect a short-circuit.

The digital input comparator is enabled with a threshold voltage of AVDD_HI/2 and with the output inverted. During normal operation, the voltage on I/OP_x is typically within 5V of the V_{AVDD_HI}. If the load is short-circuited to ground, the voltage on the I/OP_x is pulled to ground. When the voltage on the I/OP_x screw terminal falls to less than the programmed threshold level, the comparator trips, sets the ANALOG_IO_SC bit in the CHANNEL_ALERT_STATUS[n] register.

Interpreting ADC Data

In current input loop, powered mode, the ADC, by default, measures the current flowing from the AD74416H into the I/OP_x screw terminal through the R_{SENSE} in a 25mA range. Use the ADC measurement result to calculate the current with the following equation:

$$I_{RSENSE} = \frac{\left(\left(\frac{ADC\_CODE}{16,777,216}\right) \times Voltage\ Range\right)}{R_{SENSE}}$$

where:
I_{RSENSE} is the measured current in amps.
ADC_CODE is the value of the CONV_RES bit field from ADC_RESULT_UPR[n] and ADC_RESULT[n] registers.
Voltage Range is the full ADC span of the ADC range and is 0.3125V.
R_{SENSE} is the sense resistor, which has a value of 12Ω.

Current Input, Loop Powered with HART Compatibility Mode

The current input, loop powered mode is a HART-compatible version of the current input, loop powered mode. The HART compatibility mode can provide resistive termination in current input, loop powered mode. Input impedance is set to a minimum of 230Ω to be compliant with the HART receive impedance.

Loop current limit in HART compatible mode is a fixed value, for more details, see Table 5.

THEORY OF OPERATION

2-Wire RTD Measurements

Two-wire RTD measurements are supported with the AD74416H.

Figure 42 shows a simplified configuration of the 2-wire RTD method. Excitation current I1 creates a voltage drop at precise 2kΩ + 12Ω resistors, which creates reference voltage for the ADC. Excitation current I1 also creates voltage drop over the RTD connected to IOP_x and ION_x terminals. Voltage on the IOP_x terminal is measured by SENSELF_x pin in reference to AGND pin. This voltage is proportional to the RTD resistance.

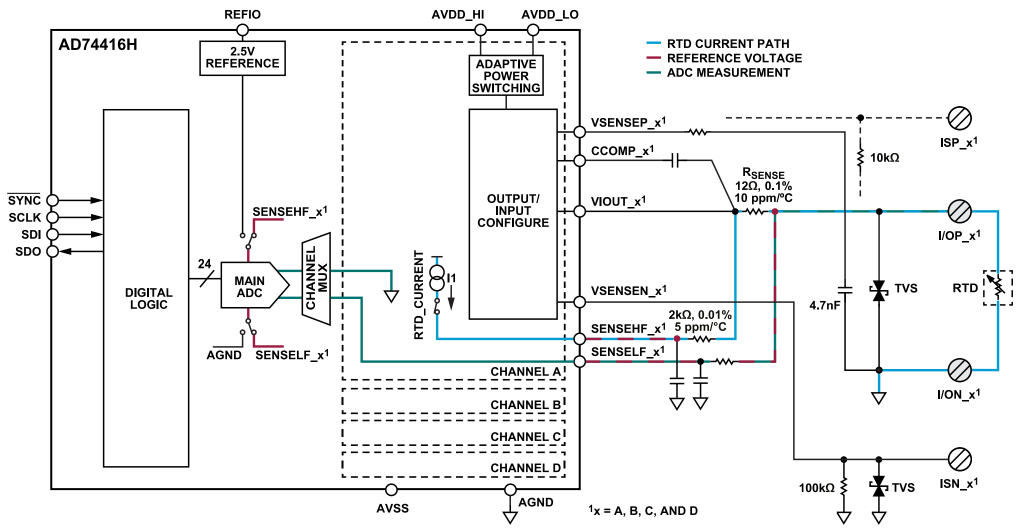


Figure 42. Resistance Measurement Configuration

How to Configure a 2-Wire RTD Measurement for Pt1000 RTD

The following is an example of how to configure a 2-wire RTD measurement for the Pt1000 RTD:

- Select resistance measurement in the CH_FUNC_SETUP[n] register.
- Set the RTD_MODE_SEL bit to high in the RTD_CONFIG[n] register.
- Select b0: I_500UA: 500µA at the RTD_CURRENT bit field in the RTD_CONFIG[n] register.
- Set the RTD_ADC_REF bit field to REF1V: external RTD reference of 1V in the RTD_CONFIG[n] register.
- Set the CONV_RANGE bit field to b000: RNG_0_12V: 0V to 12V in the ADC_CONFIG[n] register.
- Set the CONV_MUX bit field to b000: LF_TO_AGND: SENSELF to AGND in the ADC_CONFIG[n] register.
- Set the CONV_x_EN and CONV_SEQ to start continuous conversions in the ADC_CONV_CTRL register.

It is recommended to perform 2-wire RTD configuration within 200µs, otherwise, the high excitation of the current and load resistance generate a spurious alert.

Interpreting ADC Data

In the resistance measurement mode, the 24-bit, Σ-Δ ADC digitizes the voltage across the RTD.

When a conversion is carried out, the ADC code reflects the ratio between R_{RTD} and R_{REF}:

$$R_{RTD} = \frac{ADC\_CODE}{16,777,216 \times ADC\_GAIN} \times R_{REF}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code read from ADC_RESULT[n] register and CONV_RES[23:16] bit field at ADC_RESULT_UPR[n] registers.
R_{REF} has a value of 2012Ω.
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the 0V to 12V range (Pt1000), the ADC_GAIN is 1/4.8.

THEORY OF OPERATION

3-Wire RTD Measurements

3-wire RTD measurements are supported with the AD74416H. Use the CH_FUNC bits in the CH_FUNC_SETUP[n] register to configure the channel in resistance measurement.

Figure 43 shows a simplified configuration of the 3-wire RTD method. Matched excitation currents, I1 and I2, are sourced to two of the RTD leads. The third lead is connected to ground. One of the excitation currents, I1, generates a voltage across the RTD and lead resistance RL1. The second excitation current, I2, generates a drop across RL3. The resultant voltage across terminals I/OP_x and ISN_x is equivalent to the voltage drop across the RTD. It is assumed that the lead resistances are matched, that is, RL1 = RL2 = RL3.

The voltage between the I/OP_x and ISN_x terminals is measured by the ADC using the SENSELF_x and VSENSEN_x pins. The full-scale range of the ADC is determined by the voltage across the reference resistor, R_{REF}, which guarantees a fully ratiometric measurement.

Program the excitation currents applied to the RTD terminals to 500µA or 1mA in the RTD_CONFIG[n] register.

Take care that the voltage generated on the SENSEHF_x pin (I1 × (R_{REF} + R_{RTD})) is less than V_{AVCC}. The SENSEHF_x pin voltage provides the positive reference to the ADC and must not exceed the value of V_{AVCC}.

The RTD_ADC_REF bit field of the RTD_CONFIG[n] register allows the elimination of ADC offset during ADC measurement. Two reference options are available 2V and 1V. Based upon excitation current and reference resistance (2kΩ + 12Ω resistors). Excitation current flowing through these resistors generates reference voltage, and use the following formula when calculating RTD reference voltage:

RTD_ADC_REF = R_{REF}× I

Three measurement ranges are available in the 3-wire RTD mode. These ranges are listed in Table 7. Configure the measurement range in the ADC_CONFIG register by using the CONV_RANGE bits. Select the best range to suit the RTD in use.

When the 3-wire RTD mode is selected, the AD74416H is automatically configured to measure a 3-wire RTD in a Pt100 range. In this case, an excitation current of 1mA is used, and the ADC measurement range is set to 0V to 0.625V.

If a Pt1000 measurement is required, it is recommended to use a 500µA excitation current with the ADC range set to 0V to 12V.

For a lower resistance RTD, for example Cu10, it is recommended to use 1mA excitation current and the ADC range set to ±104mV.

Change the ADC measurement range by writing to the CONV_RANGE bits in the ADC_CONFIG[n] register. Change the excitation currents by writing to the RTD_CURRENT bits in the RTD_CONFIG[n] register.

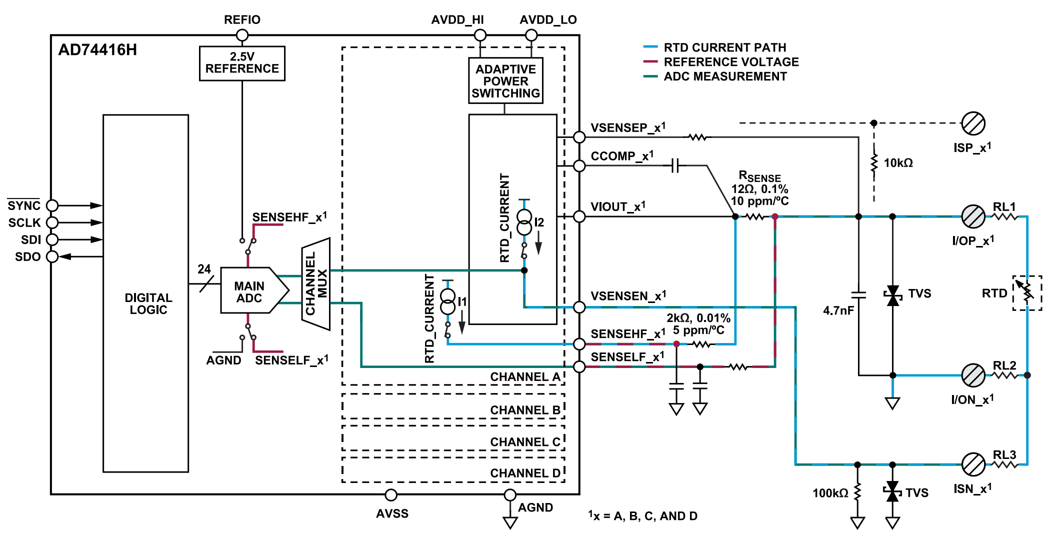


Figure 43. 3-Wire RTD Measurement Configuration

THEORY OF OPERATION

How to Configure a 3-Wire RTD Measurement for Pt1000 RTD

The following is an example of how to configure a 3-wire RTD measurement for the Pt1000 RTD:

- Select resistance measurement in the CH_FUNC_SETUP[n] register.
- Set RTD_ADC_REF bit field REF1V: external RTD reference of 1V in the RTD_CONFIG[n] register.
- Select b0: I_500UA: 500μA at RTD_CURRENT bit field in the RTD_CONFIG[n] register.
- Set CONV_RANGE bit field to b000: RNG_0_12V: 0V to 12V in the ADC_CONFIG[n] register.
- Set CONV_x_EN and CONV_SEQ to start continuous conversions in the ADC_CONV_CTRL register.

Open-Circuit Detection

An open-circuit detect feature is available on the leads of the 3-wire RTD. The combination of excitation current and RTD and lead resistances generates voltages on the SENSEHF_x and VSENSEN_x pins. If the voltage on either of these pins exceeds the open-circuit detect voltage (see Table 7), an open-circuit signal is asserted in the CHANNEL_ALERT_STATUS[n] register.

Interpreting ADC Data

In 3-wire RTD mode, configure the 24-bit, Σ-Δ ADC to measure the voltage from SENSELF_x to VSENSEN_x. When a conversion is carried out, the ADC code reflects the ratio between R_{RTD} and R_{REF}.

When using unipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{ADC\_CODE}{16,777,216 \times ADC\_GAIN} \times R_{REF}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code read from ADC_RESULT[n] register and CONV_RES[23:16] bit field at ADC_RESULT_UPR[n].
R_{REF} has a value of 2012Ω (the combined value of the SENSEHF_x and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the 0V to 0.625V range (Pt100), the *ADC_GAIN* is 4.

When using the 0V to 12V range (Pt1000), the ADC_GAIN is 1/4.8.

When using bipolar ADC ranges, use the ADC code to calculate the RTD resistance with the following equation:

$$R_{RTD} = \frac{ADC\_CODE - 8,388,608}{8,388,608 \times ADC\_GAIN} \times R_{REF}$$

where:
R_{RTD} is the calculated RTD resistance in ohms.
ADC_CODE is the code read from ADC_RESULT[n] register and CONV_RES[23:16] bit field at ADC_RESULT_UPR[n].
R_{REF} has a value of 2012Ω (the combined value of the SENSEHF_x and R_{SENSE} resistors).
ADC_GAIN is the gain of the ADC in the selected ADC range. When using the ±104mV range (Cu10), the ADC_GAIN is 24.

THEORY OF OPERATION

Digital Input Logic

The digital input circuit converts high-voltage digital inputs from the I/OP_x screw terminal to low-voltage digital logic signal. Directly multiplexed a signal to the GPIO_x pin or read by the SPI.

An externally powered sensor provides a high-voltage digital input on the I/OP_x screw terminal. Route the unfiltered screw terminal voltage on the VSENSEP_x pin to the on-chip comparator. Use the DIN_INPUT_SELECT bit in the DIN_CONFIG1 register to choose DIN input pin. Select the VIOUT_x pin without a buffer if high-speed digital input data rates are required. For buffered and unbuffered data rates, see Table 8.

The digital input comparator compares the voltage of the input signal to a programmable threshold (for more details, see the Digital Input Threshold Setting section). To debounce the comparator output, see the Debounce Function section.

The digital input comparator outputs are monitored by reading from the DIN_COMP_OUT register. A user can also monitor the comparator outputs with the GPIO_x pin. Monitoring Digital Input Comparator Output section shows how to configure GPIO_x to monitor comparator output.

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements while the digital input logic mode is enabled.

Figure 44 shows the comparator input, SC/OC current, and output signal paths of the digital input logic mode.

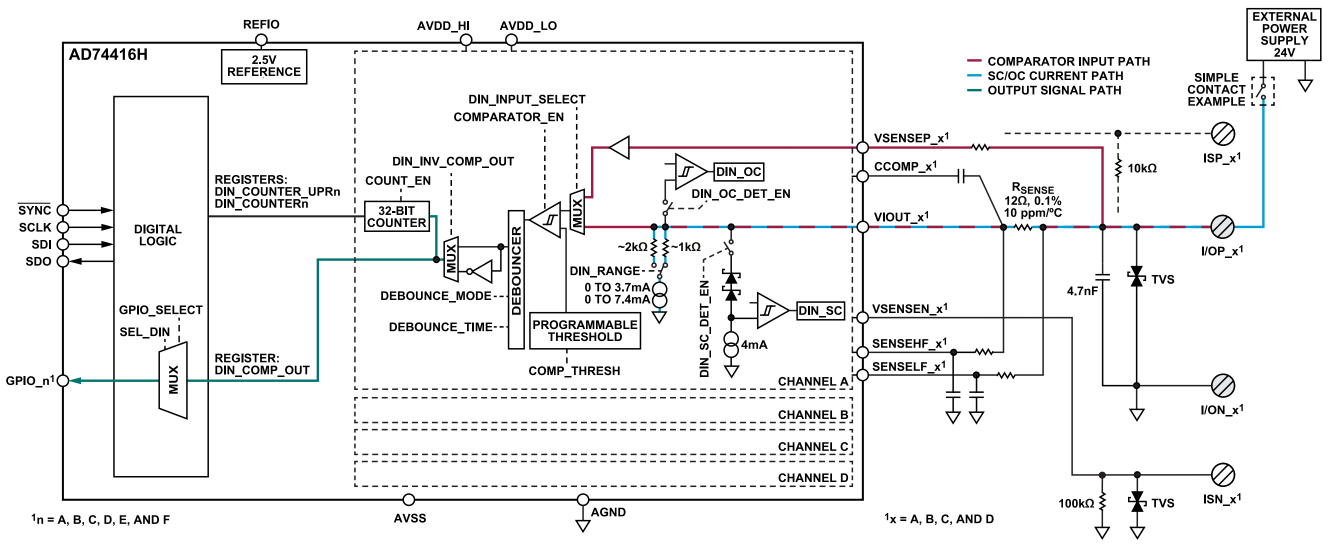


Figure 44. Digital Input Logic Mode Configuration

Digital Input Threshold Setting

The digital input thresholds are set by an internal 7-bit threshold DAC. The reference to this DAC is driven by either the V_{AVDD_HI} or the reference voltage, V_{REFIN}. This reference is configured by writing to the DIN_THRESH_MODE bit within the DIN_CONFIG1 register.

The specific threshold levels are programmed using the COMP_THRESH bits in the DIN_CONFIG1 register. There are 7 bits available to configure the threshold, and the maximum programmable code is Decimal 98.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to AVDD_HI:

$$V_{THRESH\ (AVDD\_HI)} = V_{AVDD\_HI} \times \left(\frac{Code - 48}{50}\right)$$

where:
$V_{THRESH\ (AVDD\_HI)}$ is the comparator threshold expressed in volts.
V_{AVDD_HI} is the AVDD_HI supply value in volts.
Code is the decimal code loaded to the COMP_THRESH bits.

The following equation shows the relationship between the programmed code in the COMP_THRESH bits and the corresponding threshold voltage when the DAC reference is set to V_{REFIO}:

$$V_{THRESH\ (FIXED\ VOLTAGE)} = V_{REFIO} \times (Code - 38)/5$$

where:
$V_{THRESH\ (FIXED\ VOLTAGE)}$ is the comparator threshold expressed in volts.
V_{REFIO} is the reference voltage.
Code is the decimal code loaded to the COMP_THRESH bits.

Digital Input Current Sink

The AD74416H includes a programmable current sink. The current sink is programmed by the DIN_SINK_RANGE bit and the DIN_SINK bit within the DIN_CONFIG0 register. This current sink programmability enables compatibility with Type I, Type II, and Type III of the IEC 61131-2.

THEORY OF OPERATION

Program the current sink and the threshold voltages to enable compatibility with Type I and Type III of the IEC 61131-2.

For Type I and Type III, it is recommended to program the bits in the DIN_CONFIG0 and DIN_CONFIG1 registers as follows:

- DIN_SINK_RANGE bit: 0x0
- DIN_SINK bits: 0x14
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits results in a typical current sink of 2.4mA and a rising voltage trip point of 8.5V, typically.

For Type II, it is recommended to program the DIN_CONFIG0 and DIN_CONFIG1 registers as follows:

- DIN_SINK_RANGE bit: 0x1
- DIN_SINK bits: 0x1D
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits result in a typical current sink of 6.96mA and a rising voltage trip point of 8.5V.

Open-Circuit and Short-Circuit Detection

The AD74416H has open-circuit and short-circuit detection capabilities and can be configured to be compatible with IEC 61131-3D.

To use the open-circuit and short-circuit detection functions, enable the current sink by using the DIN_SINK_RANGE bit. Set the current using the DIN_SINK bits.

To enable the open-circuit diagnostic, use the DIN_OC_DET_EN bit. An open-circuit is detected if the input current is less than 0.35mA.

To enable the short-circuit diagnostic, use the DIN_SC_DET_EN bit. When the DIN_SC_DET_EN bit is set, an additional 4mA of current sink is enabled. A short-circuit fault is triggered if the 4mA sink limit is exceeded.

Once an open-circuit or short-circuit fault is triggered, the appropriate bit is set in the ALERT_STATUS register, and the $\overline{\text{ALERT}}$ pin is asserted.

For Type 3D diagnostics, it is recommended to program the DIN_CONFIG0 and DIN_CONFIG1 registers bits as follows:

- DIN_SINK_RANGE bit: 0x0
- DIN_SINK bits: 0xF
- DIN_OC_DET_EN bit: 0x1
- DIN_SC_DET_EN bit: 0x1
- DIN_THRESH_MODE bit: 0x1
- COMP_THRESH bits: 0x37

Programming these bits results in a typical current sink of 1.6mA and a rising voltage trip point of 8.5V, typically. An open-circuit detection is triggered when sinking currents are less than 220µA. A short-circuit detection is triggered when sinking currents are greater than typically 6.2mA.

Digital Input Inverter

The debounced comparator signal can pass directly to the DIN_COMP_OUT register. Alternatively, invert the signal before being sent to the DIN_COMP_OUT register. To enable this inverter, set the DIN_INV_COMP_OUT bit in the DIN_CONFIG0 register. Bit Inversion of DIN_COMP_OUT is particularly useful when the DIN_COMP_OUT signal is monitored by the GPIO_x pin.

Digital Input Counter

A 32-bit counter is available in the digital input modes, and the counter allows the debounced digital input edges to be counted. Program the counter to count the positive edges or the negative edges, which depends on whether the digital input inverter is used. Enable the digital input counter and configure the inverter in the DIN_CONFIG0 register. First half of count value is accessed in the DIN_COUNTER[n] register and upper half in the DIN_COUNTER_UPR[n] register.

The counter is reset to 0 when the device is reset. When the counter reaches full scale, it rolls over to 0. The counter freezes if the COUNT_EN bit is set to 0.

Digital Input Data Rates

When the AD74416H is configured in digital input mode, the voltage on the VSENSEP_x pin is buffered and monitored by the digital input comparator. Table 8 shows the specified data rate.

To enable higher data rates, a high speed, unbuffered option is available to allow the comparator to monitor high speed signals. For unbuffered operation, the voltage on the VIOUT_x pin is monitored by the digital input comparator. For the specified data rate for high speed mode, see Table 8. Enable the unbuffered mode by setting the DIN_INPUT_SELECT bit in the DIN_CONFIG1 register.

If using unbuffered mode while sourcing or sinking current to the load by the VIOUT pin, consider the voltage drop across R_{SENSE} (12Ω) and the VIOUT_x line protector (15Ω) when setting the threshold voltage.

Debounce Function

The digital input comparator outputs are sampled at regular intervals and passed to a user-programmable debounce operation.

Debounce the comparator outputs for a user-programmable amount of time by the 5-bit DEBOUNCE_TIME bits within the DIN_CONFIG0 register. Set these bits to 0x00 to bypass the debouncer. Table 21 shows the available programmable debounce times.

THEORY OF OPERATION

The debounce circuit has the following two modes of operation: Debounce Mode 0 and Debounce Mode 1. Both modes are programmed by the DEBOUNCE_MODE bit in the DIN_CONFIG0 register.

Table 21. Digital Input Programmable Debounce Times

DEBOUNCE_TIME Code (Hex)	Debounce Time (ms)
00	Bypass
01	0.0130
02	0.0187
03	0.0244
04	0.0325
05	0.0423
06	0.0561
07	0.0756
08	0.1008
09	0.1301
0A	0.1805
0B	0.2406
0C	0.3203
0D	0.4203
0E	0.5602
0F	0.7504
10	1.0008
11	1.3008
12	1.8008
13	2.4008
14	3.2008
15	4.2008
16	5.6008
17	7.5007
18	10.0007
19	13.0007
1A	18.0006
1B	24.0006
1C	32.0005
1D	42.0004
1E	56.0003
1F	75.0000

Debounce Mode 0 (Default)

In this mode, the sampled comparator outputs are counted. A high sample occurrence is counted in one direction (either up or down), whereas a low sample occurrence is counted in the opposite direction. The DIN_COMP_OUT register changes state when the programmed counter target is reached.

Figure 45 shows an example of Debounce Mode 0 in operation. The debounce time is set to 240µs in the DIN_CONFIG0 register. A clock with an approximate period of 800ns sample counts the comparator signal. After the comparator signal changes state from the current debounced signal, the debounce function counter begins to count the duration of the signal at the new state. The count direction changes if the comparator signal reverts back to the original state. After the counter reaches the target count, the DIN_COMP_OUT register is updated with the state of the comparator signal.

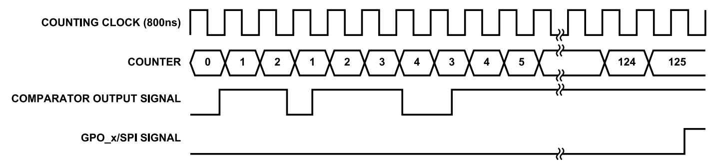


Figure 45. Digital Input Debounce Mode 0 Timing Example

Debounce Mode 1

In this mode, a counter counts the sampled comparator outputs. After a change of state occurs on the sampled comparator output, the counter increments until the programmed debounce time is reached, at which point the DIN_COMP_OUT register changes state, and the counter resets. If the sampled comparator output returns to the current DIN_COMP_OUT register value, the counter resets.

Figure 46 shows an example of Debounce Mode 1 in operation. Similar to Debounce Mode 0, the debounce time is set to 240µs. In Debounce Mode 1, the counter value is reset each time the comparator signal returns to the original state. The comparator output must be at the new state for the full duration of the debounce time to update the DIN_COMP_OUT signal.

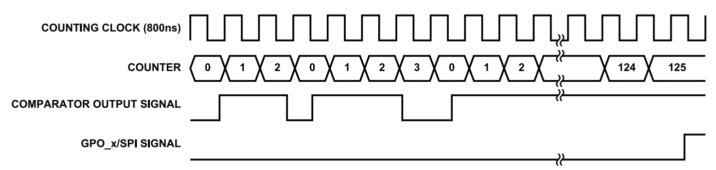


Figure 46. Digital Input Debounce Mode 1 Timing Example

THEORY OF OPERATION

Digital Input, Loop Powered

Similar to current input, loop powered mode (see the Current Input, Loop Powered section), the digital input, loop powered function configures the output stage to provide a high-side current output that can power an external sensor. Program the DAC_CODE[n] register to provide the required wetting current.

Loop powered sensor provides digital input on the I/OP_x screw terminal. Route the unfiltered screw terminal voltage on the VSENSEP_x pin to the on-chip comparator. Use the DIN_INPUT_SELECT bit in the DIN_CONFIG1 register to choose DIN input pin. Select the VIOUT_x pin without a buffer if high speed digital input data rates are required.

This comparator compares the voltage on the selected pin to a programmable threshold that can either be a fixed voltage or a voltage proportional to the V_{AVDD_HI}. For more details on the programmable threshold voltages, see the Digital Input Threshold Setting section.

Debounce the output of the comparators (see the Debounce Function section), pass directly, or invert to the SPI and/or to the GPIO_x pin.

The digital input comparator outputs are monitored by reading from the DIN_COMP_OUT register. Also, monitor the comparator outputs with the GPIO_x pin. Monitoring Digital Input Comparator Output section shows how to configure GPIO_x to monitor comparator output.

Figure 47 shows the comparator input, wetting current, and output signal paths of the digital input, loop powered mode configuration.

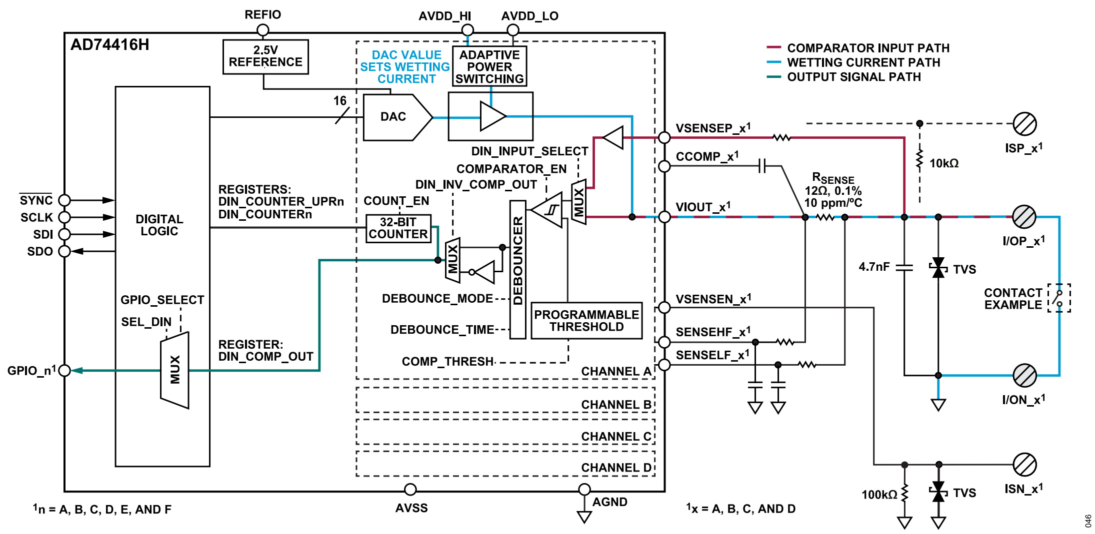


Figure 47. Digital Input, Loop Powered Configuration Mode

Interpreting ADC Data

The ADC is not required for digital input operation. However, the ADC is available for voltage and current measurements when the digital input, loop powered mode is enabled. In digital input, loop powered mode, the ADC, by default, measures the voltage across the I/OP_x to I/ON_x screw terminals in a 0V to 12V range. Use the ADC measurement result to calculate this voltage by using the following equation:

$$V_{ADC} = (ADC\_CODE/16{,}777{,}216) \times Voltage\ Range$$

where:
V_{ADC} is the measured voltage in volts.
ADC_CODE is the value of the ADC_RESULT1 register.
Voltage Range is 12V, the measurement range of the ADC.

THEORY OF OPERATION

Digital Output

The AD74416H supports sourcing digital outputs. When the digital output functionality is enabled, the recommended configuration of the CH_FUNC_SETUP[n] register is to set it to high impedance.

The external sourcing digital output operates with an external, P-channel field effect transistor (PFET). Determine the absolute current value by the R_{SET} and short-circuit voltage values. Short-circuit voltages are shown in Table 10.

Configure the digital output using the DO_EXT_CONFIG[n] register and do the following:

- Wait 300µs, after AD74416H reset or is recovered from any undervoltage scenario flagged at SUPPLY_ALERT_STATUS.
- Select source capability by setting the DO_MODE bit.
- Select the source of the data for the digital output circuit using the DO_SRC_SEL bit. SPI provides the digital output data (by the DO_DATA bit) or by the GPIO_x pin for direct hardware control of the circuits.
- Configure the short-circuit timers using the DO_T1 and DO_T2 bits. For more details on short-circuit functionality, see the Short-Circuit Protection section.

Once the configuration settings are applied, provide stimulus to turn on the external FET. For SPI control, a new write is required to the DO_EXT_CONFIG register, to set the DO_DATA bit. Setting the DO_DATA to 1 turns on the external FET.

For GPIO control, configure the GPIO_x pin to control the digital output circuit by writing to the GPIO_SELECT bit field in the GPIO_CONFIGx register. Drive the GPIO_x pin high to turn on the FET.

If changing from digital output function, first disable the digital output function before changing to the new mode (set DO_MODE to digital output external disable).

Figure 48 shows the current, measurement, and control paths of the sourcing digital output mode with the external FET.

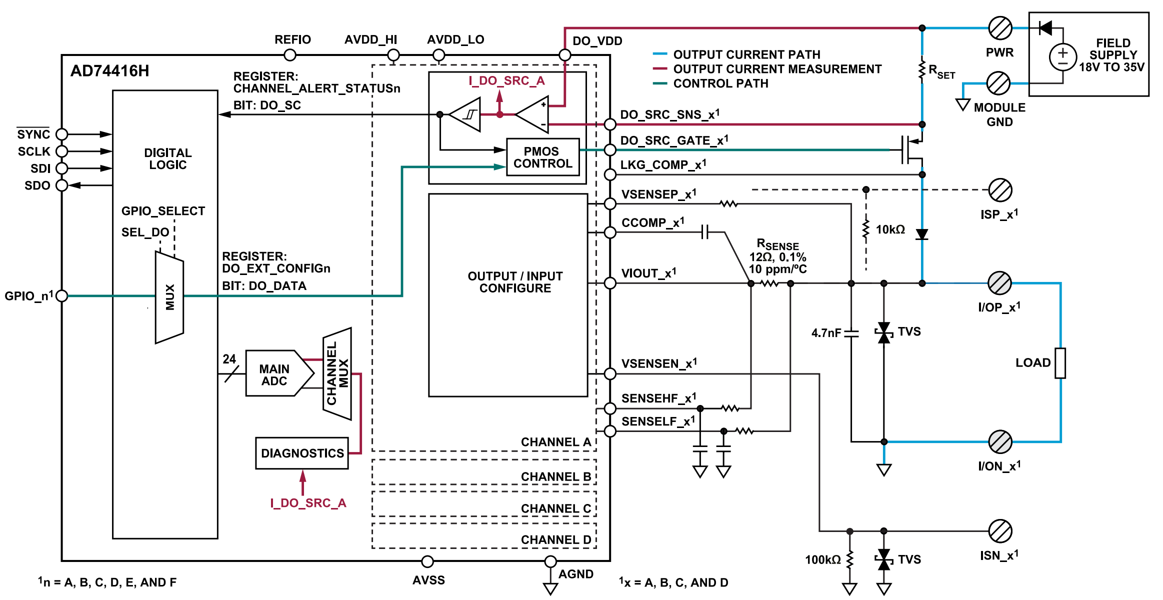


Figure 48. Digital Output Sourcing with External FET

THEORY OF OPERATION

Short-Circuit Protection

When using digital output, short-circuit protection is achieved using a current-limit setting resistor, R_{SET}. A short-circuit event is triggered when the voltage developed across the resistor reaches the short-circuit voltage, as shown in Table 10. In the event of a short-circuit, the DO_SC bit is set in the CHANNEL_ALERT_STATUS[n] register, which in turn asserts the $\overline{\text{ALERT}}$ pin.

There is programmability around how the short-circuit behavior operates. The two configurable short-circuit timeout times are T1 and T2.

To support charging of large current loads on initial power-on of the digital output load, enable a higher short-circuit current limit for a programmable amount of time, T1. The T1 starts counting once the digital output FET is turned on using the DO_DATA bit, even if no short-circuit event is triggered. If a short-circuit event occurs, the digital output FET remains on, clamped at the higher short-circuit current for the remainder of the programmed duration of T1. The short-circuit alert is not triggered during this time.

A second short-circuit limit is deployed once the T1 time elapses, is a lower current limit, and is active for a programmable duration of time, T2. The T2 counter only starts counting if T1 expires and a short-circuit is detected. The FET remains on during a short-circuit event, but the current is limited to the lower short-circuit current for the programmed duration of T2.

The T2 counter is an up and down counter: when in short-circuit, the time increments. If the short-circuit condition goes away, the time count decrements.

Program the T1 and T2 in the DO_EXT_CONFIG[n] register. If the higher short-circuit current limit is not required, disable the T1. For the specified short-circuit values and T1 and T2 durations, see Table 10.

If the short-circuit continues to persist after the T2 time expires, the FET automatically disables. Once disabled, the relevant digital output timeout bit is set in the CHANNEL_ALERT_STATUS[n] register. The digital output is disabled, which is reflected in the DO_EXT_CONFIG[n] register.

Figure 49 shows the operation of the two programmable timeout times along with the short-circuit current limits.

To re-enable the digital output circuit after a timeout event:

- Set the DO_DATA bit to 0.
- Choose a mode in the DO_MODE bits in the relevant configuration register to power on the digital output circuit.
- Set the DO_DATA bit back to 1 to enable the FET.

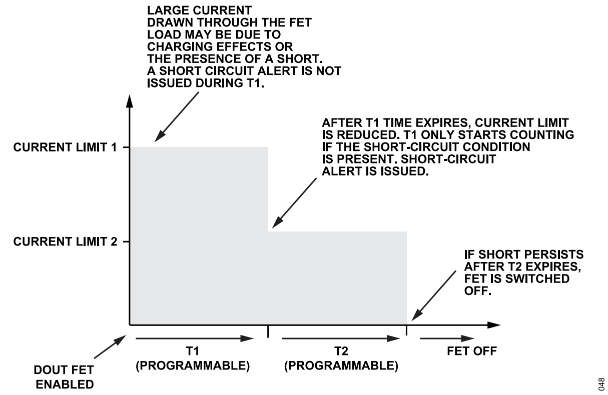


Figure 49. Digital Output Programmable Short-Circuit Control

Current Sensing Diagnostic

A digital output, current sense diagnostic is available to monitor the current in the digital output circuit.

Select the current sense diagnostics by programming the DIAG_ASSIGN register.

Diagnostic 1 measures the voltage dropped across the external R_{SET}. Consider the resistance of the selected R_{SET} when calculating the current being sourced by the digital output circuit.

An additional time is needed to account for the autozero routine performed by the current sensing diagnostic block. Table 27 shows the conversion times.

THEORY OF OPERATION

HART

The AD74416H has four integrated HART modems. Integrated HART modem at each channel can transmit and receive signals to and from the I/OP_x screw terminal. Use the HART modem for HART communications in current output and current input modes of operation.

The HART transmit signal value is added to input value of the DAC. This results in required output signal at VIOUT_x pin.

The HART receive signal is internally coupled to VIOUT_x pin by bandpass filter.

Figure 50 shows the HART functionality.

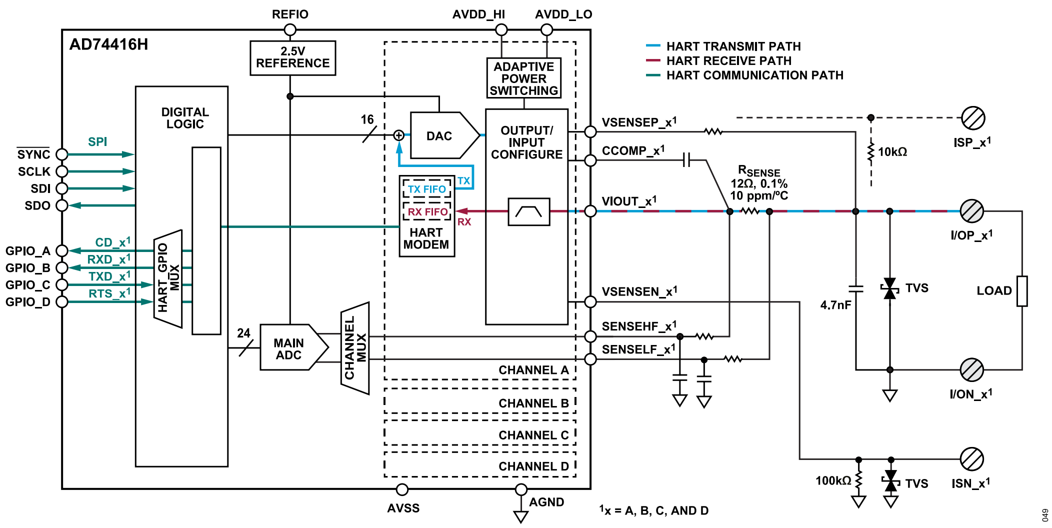


Figure 50. HART Configuration

Configuring the AD74416H for HART Communications

To initiate HART communications with the AD74416H, do the following steps:

- Configure the channel in the appropriate function (current output with HART, current input loop powered with HART, or current input externally powered with HART).
- Wait for channel initialization time (4.2ms for IOUT_HART function or 300µs for others) before proceeding with another step.
- Wait until HART compliant slew is settled (HART_COMPL_SETTLED bit set to high in the OUTPUT_CONFIGn register).
- Enable the HART slew option SLEW_EN to binary 10 (SLEW_HART_COMPL) in the OUTPUT_CONFIGn register if the current output with HART is selected.
- Power up the HART modem (MODEM_PWRUP bit) in the HART_CONFIGn register. Other HART configuration options are available in the HART_CONFIGn register and a user can configure as required. Note that a duplex mode of operation is available to allow for loop back testing of the modem to confirm that a user can transfer and receive the data by the AD74416H.
- Load the HART transmit first in first out (FIFO) with data required for transmission by the HART_TXn register.
- Ensure that the HART alerts are cleared in the HART_ALERT_STATUSn register.
- Set the RTS bit (request to send) in the HART_MCRn register to start HART transmissions.
- Monitor the HART_ALERT_STATUSn register for status alerts on the progress of the HART communication.
- Read the receive FIFO by using the HART_RXn register. Note that the receive bytes of data are stored in the receive FIFO.

Setting the RTS bit once the TX FIFO is empty or before the HART modem power-up (setting the MODEM_PWRUP bit) continuously transmits a 1200Hz sine wave to the modem's output when it is powered up. Clear the RTS bit manually to stop it.

During valid transmission (TX FIFO populated and HART modem powered up), the RTS bit is automatically cleared once the message transmission is completed unless the AUTO_CLR_RTS bit in the HART_CONFIGn register is cleared.

Communicating with the HART Modem

Communication with the modem is by the SPI. The necessary status bits are provided by the SPI to communicate with an existing software stack. The SPI manages the HART transactions and the software configurable input and output transactions.

It is also possible to configure the GPIO_A, GPIO_B, GPIO_C, and GPIO_D pins to either monitor or control the HART modem UART interface.

Control of the HART modem by GPIO is possible by configuring HART_GPIO_IF_CONFIG register. It is possible to control HART modem at one channel at the time.

THEORY OF OPERATION

Monitoring of the HART signals by GPIOs are fully interchangeable and available across all channels. Assign the HART signals to GPIOs by configuring HART_GPIO_MON_CONFIGn registers and its bit fields.

Transmit and Receive FIFOs

The AD74416H is equipped with a HART transmit FIFO and HART receive FIFO. A user can store up to 32 bytes of data in each of the transmit and receive FIFOs.

The transmit FIFO is loaded using the HART_TXn register. Read the data from the receive FIFO by the HART_RXn register. An alert is issued if the number of bytes loaded to the transmit FIFO falls below the programmable threshold value. Similarly, an alert is issued if the number of bytes loaded to the receive FIFO goes above the programmable threshold value. Program these receive and transmit threshold values by the TFTRIG and RFTRIG bits in the HART_FCRn register.

The number of bytes currently stored in the transmit and receive FIFOs is recorded in the HART_TFCn and HART_RFCn registers, respectively. The user must manage the number of FIFO entries, exceeding entries above FIFO size results in data loss.

HART Alerts

The HART_ALERT_STATUSn register contains all the alert bits associated with HART communications. If any bit is asserted in the HART_ALERT_STATUSn register, the HART_ALERT_x bit is asserted in the ALERT_STATUS register, which allows for an interrupt to be generated on the $\overline{\text{ALERT}}$ pin. Mask the HART alert bits by the HART_ALERT_x_MASK register. If an alert bit is masked, it does not generate an interrupt on the $\overline{\text{ALERT}}$ pin when asserted, but the alert is still seen in the HART_ALERT_STATUSn register.

THEORY OF OPERATION

GETTING STARTED

Power up the AD74416H, as shown in the Powering on the AD74416H section. After initial power up, the ALERT pin is pulled low as a result of various bits, such as the RESET_OCCURRED bit being set in the ALERT_STATUS register. It is recommended to clear the ALERT_STATUS register before continuing to use the AD74416H. Clear the Relevant bits in ALERT_STATUS register by writing 1.

Using Channel Functions

The channel function is selected using the CH_FUNC_SETUPn register. Once a channel function is selected, the contents of a number of registers are updated with predefined values that allow the user to configure the device with a minimal set of commands. The updated settings include configuration of the channel conversion on the ADC. Table 22 shows the default settings of the bits for any given channel function. In addition to the default settings shown in Table 22, these bit fields are set to the following values, irrespective of the CH_FUNC_SETUP selection:

- RTD_MODE_SEL in the RTD_CONFIG[n] register is set to 0 (selects 3-wire RTD).
- RTD_CURRENT in the RTD_CONFIG[n] register is set to 1 (selects 1mA).
- RTD_ADC_REF in the RTD_CONFIGn register is set to 0 (selects reference of 2V).
- DIN_SINK in the DIN_CONFIG0 register is set to 0 (turn sinking current off).
- DIN_THRESH_MODE in the DIN_CONFIG1 register is set to 0 (DIN threshold scales with AVDD_HI).

Table 22. Register Defaults Based on Channel Function Selection

CH_FUNC Bits (Programmed by the CH_FUNC_SETUP[n] Register)	Defaults of the ADC_CONFIG[n] Register		Defaults of the DIN_CONFIG0_[n] Register		Defaults of the DIN_CONFIG1_[n] Register	Defaults of the OUTPUT_CONFIG[n] Register
	CONV_MUX Bits	CONV_RANGE Bits	COMPARATOR_EN Bit	DIN_INV_COMP_OUT Bit	COMP_THRESH Bits	AVDD_SELECT Bits
0b0000: HIGH_IMP High Impedance	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	00: Lock to AVDD_HI
0b0001: VOUT Voltage Output	0b001: SENSEHF_x[1] to SENSELF_x[1]	0b010: −0.3125V to +0.3125V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	00: Lock to AVDD_HI
0b0010: IOUT Current Output	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	10: Track Supply
0b0011: VIN Voltage Input	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	00: Lock to AVDD_HI
0b0100: IIN_EXT_PWR Current Input, Externally Powered	0b001: SENSEHF_x[1] to SENSELF_x[1]	0b011: −0.3125V to 0V	1: Enabled	0: Inverted disabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI
0b0101: IIN_LOOP_PWR Current Input, Loop Powered	0b001: SENSEHF_x[1] to SENSELF_x[1]	0b100: 0V to 0.3125V	1: Enabled	1: Inverted enabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI
0b0111: RES_MEAS Resistance Measurement	0b011: SENSELF_x[1] to VSENSEN_x[1]	0b101: 0V to 0.625V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	00: Lock to AVDD_HI
0b1000: DIN_LOGIC Digital Input Logic	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	1: Enabled	0: Inverted disabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI
0b1001: DIN_LOOP Digital Input, Loop Powered	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	1: Enabled	0: Inverted disabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI
0b1010: IOUT_HART Current Output with HART	0b000: SENSELF_x[1] to AGND	0b000: 0V to 12V	0: Disabled	0: Inverted disabled	0: −0.96 × AVDD_HI	10: Track supply
0b1011: IIN_EXT_PWR_HART Current Input, Externally Powered with HART	0b001: SENSEHF_x[1] to SENSELF_x[1]	0b011: −0.3125V to 0V	1: Enabled	0: Inverted disabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI
0b1100: IIN_LOOP_PWR_HART Current Input, Loop Powered with HART	0b001: SENSEHF_x[1] to SENSELF_x[1]	0b100: 0V to 0.3125V	1: Enabled	1: Inverted enabled	0x49: AVDD_HI/2	00: Lock to AVDD_HI

[1] x = A, B, C, and D.

THEORY OF OPERATION

Switching Channel Functions

Set the channel function to high impedance by the CH_FUNC_SETUPn register before transitioning to the new channel function. Use caution when switching from one channel function to another. All functions must be selected for a minimum of channel initialization time (4.2ms for IOUT_HART function or 300µs for others) before changing to another function.

The DAC_CODEn register is not reset by changing channel functions. Before changing channel functions, it is recommended to set the DAC code to the intended value. In the case of outputs, it is recommended to set the DAC code to 0x0000 by the DAC_CODEn register.

For bipolar voltage output range ±12V, update the DAC_CODE to 0x8000 before the voltage output is enabled to ensure that the output stage powers up to 0V. For more details, see the Voltage Output section.

After the new channel function is configured, it is recommended to wait channel initialization time (4.2ms for IOUT_HART function or 300µs for others) before updating the DAC code.

Previous paragraphs are described in the following switching channel functions process:

- Transition to high impedance mode (set CH_FUNC bit field in the CH_FUNC_SETUPn to 0).
- Configure DAC code to the required value (by the DAC_CODEn register).
- Wait 300µs.
- Transition to required mode (set CH_FUNC bit field in the CH_FUNC_SETUPn).
- Channel initialization time (4.2ms for IOUT_HART function or 300µs for others).
- Start operation and update DAC code as needed.

ADC FUNCTIONALITY

The AD74416H provides a single, 24-bit Σ-Δ ADC that is sequenced to measure up to four channel measurements and up to four diagnostics measurements for a single conversion sequence or for continuous conversions. ADC measurements allow for various voltage and current monitoring options on the I/OP_x screw terminal, the VSENSEN_x pin, and the VSENSEP_x pin.

Conversion is targeted at supporting the measurements required for each of the AD74416H use cases. Table 23 shows the measurements available. When any mode of operation is selected in the CH_FUNC_SETUPn register, conversion is configured to a default measurement. These default measurements are shown in the Using Channel Functions section.

Each conversion has an individual conversion rate and voltage range control that is configured in the ADC_CONFIGn register.

The ADC also provides diagnostic information on user-selectable inputs such as supplies, internal die temperature, reference, and regulator. For more details on the diagnostics measurements, see the Diagnostics section.

After the measurements are configured in the ADC_CONFIGn register, enable the relevant ADC measurements by the ADC_CONV_CTRL register.

Select either single conversion or continuous conversion mode by setting the appropriate value to the CONV_SEQ bits in the ADC_CONV_CTRL register.

In single conversion mode, the ADC sequencer starts enabled channel conversions followed by the enabled diagnostics. After each enabled input is converted once, the ADC enters idle mode, and conversions are stopped.

In continuous conversion mode, the ADC channel sequencer continuously converts the enabled channel conversion and each enabled diagnostic until a command is written to stop the conversions. Set the stop command by setting the CONV_SEQ bits in the ADC_CONV_CTRL register to idle mode or power-down mode. The command stops conversion at the end of the current sequence.

If the measurement configuration requires a change, continuous conversions must be stopped before making the changes. Restart the continuous conversions after making the appropriate changes.

After a sequence is complete, all data results are transferred to the relevant ADC_RESULTn, ADC_RESULT_UPRn, and ADC_DIAG_RESULTn registers.

Table 23. Selection Options for ADC Conversion

CONV_MUX Settings in the ADC_CONFIGn Register	Measurement Selection	Description
0b000	SENSELF_x[1] to AGND	Voltage measurement across the I/OP_x[1] and I/ON_x[1] screw terminals.
0b001	SENSEHF_x[1] to SENSELF_x[1]	Voltage measurement across the R_{SENSE}.
0b010	VSENSEN_x[1] to AGND	Voltage measurement across the ISN_x[1] and I/ON_x[1] screw terminals.
0b011	SENSELF_x[1] to VSENSEN_x[1]	Voltage measurement for 3-wire RTD measurement.
0b100	AGND to AGND	Diagnostic.

[1] x = A, B, C, and D.

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ADC Transfer Function

Table 24 shows the ideal input voltage for zero scale, midscale, and full scale codes for each of the available voltage ranges when measuring voltages with the ADC.

Currents through the external R_{SENSE} are determined by measuring the voltage across R_{SENSE}. Set the CONV_MUX bits to measure between SENSEHF_x and SENSELF_x. Table 25 shows the ideal input currents for zero scale, midscale, and full scale codes using each available voltage range (to calculate current, measured voltage is divided by the R_{SENSE} value, 12Ω).

If the voltage measured by the ADC is either more than full scale or less than zero scale, an ADC_ERR bit is set in the ALERT_STATUS registers, asserting the $\overline{\text{ALERT}}$ pin. In this case, the ADC output reads 0xFFFFFF or 0x000000, respectively. Mask the ADC_ERR bit by the ALERT_MASK register (optional) if these alerts are not required.

Table 24. Ideal Output Code to Input Voltage Relationship

	Input Voltage for Selected ADC Codes[1]		
Input Voltage Range	**0x0**	**0x800000**	**0xFFFFFF**
0V to +12V	0V	6V	12V – 1LSB
±12V	−12V	0V	12V – 1LSB
±2.5V	−2.5V	0V	2.5V – 1LSB
0V to +0.625V	0V	0.3125V	0.625V – 1LSB
−0.3125V to 0V	0V	−0.15625V	−0.3125V – 1LSB
0V to +0.3125V	0V	0.15625V	0.3125V – 1LSB
±0.3125V	−0.3125V	0V	0.3125V − 1LSB
±104.16mV	−104.16mV	0V	104.16mV – 1LSB

1 1LSB = (Full Scale – Zero Scale)/16,777,216.

Table 25. Ideal Output Code to Input Current Relationship

	Input Current for Selected ADC Codes[1, 2]			
Input Voltage Range	**0x0**	**0x800000**	**0xFFFFFF**	**Sourcing or Sinking**
±0.3125V	−26.04mA (Sinking)	0mA	26.04mA – 1LSB (Sourcing)	Sink and source
0V to +0.3125V	0mA	13.02mA	26.04mA – 1LSB	Sourcing
−0.3125V to 0V	0mA	13.02mA	26.04mA – 1LSB	Sinking

1 1LSB = (Full Scale – Zero Scale)/16,777,216.

2 The range of the channel function affects the highest achievable ADC code.

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Saving Power When Using the ADC

Each of the high-voltage sense pins available for measurement by the ADC (SENSEHF_x, SENSELF_x, VSENSEP_x, and VSEN-SEN_x) has a high voltage buffer that is in full power mode by default.

If any of the sense pins are not required for measurement by the ADC, put the high voltage buffer associated with that pin in low power mode (standby) to save total power consumption of the AD74416H.

Total power saving is determined by voltage value of the supply rails AVDD_HI, AVSS, or AVCC. Each buffer draws current from AVDD_HI and AVSS pin except SENSE_AGND_OPT, which draws current from AVCC and AVSS pin. The typical current saving of putting buffer from full power into low power mode is shown in Table 13.

Note that all diagnostics measurements are available regardless of the buffers setting.

Configure the AD74416H into the required channel function and put any of the high-voltage sense pin buffers in standby. Buffers are put into standby by setting the appropriate bit in the PWR_OP-TIM_CONFIG register. Wait for the appropriate power-up time, as shown in Table 13, when taking the buffers out of standby mode.

Power up the buffers at least 100μs before starting the conversion sequence.

Note that do not update the PWR_OPTIM_CONFIG settings while an ADC conversion sequence is taking place.

ADC Conversion Rates

The available ADC conversion rates on the AD74416H are 10SPS, 20SPS, 200SPS, 1.2kSPS, 4.8kSPS, and 9.6kSPS. A quick conversion rate of 19.2kSPS is available for diagnostic measurements. In addition, 50Hz and 60Hz rejection is provided on the 10SPS and 20SPS conversion rates. Dedicated conversation rates implement rejection of HART fundamental frequencies at 10SPS, 20SPS, 200SPS and, 1.2kSPS.

Configure each of the channel conversion rates by the ADC_CON-FIG register. The conversion rate of the diagnostics inputs is set by the ADC_CONV_CTRL register. One conversion rate selection applies to all diagnostic inputs.

The time it takes for a sequence of conversions to complete is dependent on several factors, such as the number of selected inputs, the selected conversion rates, and whether single or continuous mode conversions are enabled. Conversions are clocked by an on-chip oscillator. Table 26 shows the various components required to estimate a complete channel conversion time for any given sequence. Table 27 shows the various components for diagnostic measurements.

For single conversion, consider the following time components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers, if previously powered down.
- The initial pipeline delay before the first conversion.
- The conversion time for each ADC conversion.

Figure 51 shows the timing breakdown of a single conversion example. In this example, the ADC and high voltage buffers are in a power-down state before a single conversion on the channel is enabled, and continuous conversions are initiated with a 4.8kSPS conversion rate.

The time to the first complete conversion (the SYNC pin falling edge to the ADC_RDY pin falling edge) is 378.75μs and is calculated by adding the SPI transfer time, the ADC and high voltage buffer power-up time, the pipeline delay time, and the conversion rate on the channel at 4.8kSPS (208.33μs). The time between conversions (the ADC_RDY pin falling edge to the ADC_RDY pin falling edge) is 208.33μs.

For multiple conversions, consider the following components when calculating the overall sequence time:

- The time taken for the SPI transaction to start the conversions.
- The time required to power up the ADC and high voltage buffers if previously powered down.
- An initial pipeline delay before the first conversion.
- The conversion time required for each ADC conversion.
- The channel switch time for each time the selected ADC channel is switched.

Figure 52 shows an example of the timing breakdown for a multi-channel conversion. In this example, Channel Conversion A set to 10SPS_H, Channel Conversion B set to 20SPS, Diagnostic 0, and Diagnostic 2 set to 19.2kSPS all are enabled.

In this example, the I_DO_SCR_C measurement is assigned to enable Diagnostic 2. Besides conventional conversion time, an additional 41μs is required to perform the conversion of this particular diagnostic.

Continuous conversions are initiated with a 10SPS_H conversion rate. In this example, the ADC is in idle mode, and the high-voltage buffers are powered up.

The time it takes for the first complete conversion (SYNC falling edge to ADC_RDY falling edge) is 155.56329ms and is calculated by adding the SPI transfer time, the pipeline delay time, Channel A conversion time, followed by adding the channel switch time and conversion time for the remaining three conversions.

The time between all subsequent conversion sequences (the ADC_RDY pin falling edge to the ADC_RDY pin falling edge) is

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155.29516ms and is calculated by adding the channel switch time with the conversion time for the four selected ADC inputs.

Table 26. Channel Conversion Times Components

ADC_CONFIGn.CONV_RATE Conversion Rate	ADC and/or Buffer Power-Up Time (µs)	SPI Transfer Time (µs), 50ns SCLK	Start-Up Pipeline Delay (µs)	Single ADC Conversion Time	Channel Switch Time, Multiple Enabled Conversions (µs)	HART Rejection (dB)[1]
0b0000: 10SPS_H[1]	100	2.42	5000	100ms	5024	−96
0b0001: 20SPS	100	2.42	67	50ms	100	N/A[2]
0b0011: 20SPS_H[1]	100	2.42	2574	50ms	2519	−96
0b0100: 200SPS_H[1, 3]	100	2.42	1000	5ms	950	−64
0b0110: 200SPS_H[1]	100	2.42	386	4.583ms	331	−90
0b1000: 1.2kSPS	100	2.42	67	833.33µs	13	N/A[2]
0b1001: 1.2kSPS_H[1]	100	2.42	124	833µs	69	−57
0b1100: 4.8kSPS	100	2.42	68	208.33µs	13	N/A[2]
0b1101: 9.6kSPS	100	2.42	40	104.17µs	13	N/A[2]

1 _H indicates HART fundamental frequencies rejection, which is 1.2kHz and 2.2kHz signals.

2 N/A means not applicable.

3 Moderate rejection of HART fundamental frequencies implemented.

Table 27. Diagnostic Conversion Times Components

ADC_CONV_CTRL.CONV_RATE_DIAG Conversion Rate	ADC and/or Buffer Power-Up Time (µs)	SPI Transfer Time (µs), 50ns SCLK	Start-Up Pipeline Delay (µs)	Single ADC Conversion Time[1]	Channel Switch Time, Multiple Enabled Conversions (µs)	HART Rejection (dB)[2]
0b000: 20SPS	100	2.42	67	50ms	100	N/A[3]
0b001: 20SPS_H[2]	100	2.42	1740	48.33ms	1685	−96
0b010: 1.2kSPS_H[2]	100	2.42	124	833µs	69	−57
0b011: 4.8kSPS	100	2.42	68	208.33µs	13	N/A[3]
0b100: 9.6kSPS	100	2.42	40	104.17µs	13	N/A[3]
0b101: 19.2kSPS	100	2.42	40	52.08µs	13	N/A[3]

1 Additional time +41µs (or less) is required to perform I_DO_SRC_x diagnostic conversion.

2 _H indicates HART fundamental frequencies rejection, which is 1.2kHz and 2.2kHz signals.

3 N/A means not applicable.

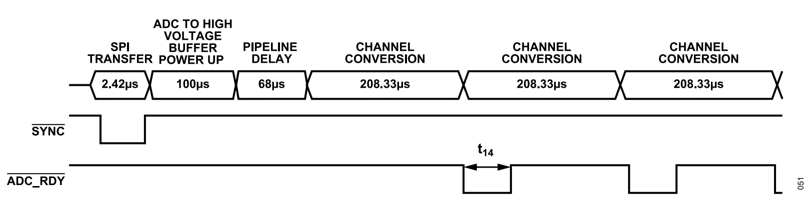

Figure 51. Single Measurement, Continuous Conversions Timing Diagram

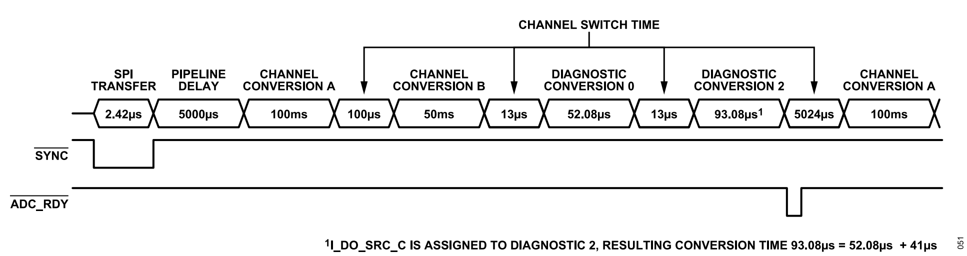

Figure 52. Multiple Measurements, Continuous Conversions Timing Diagram

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ADC_RDY Functionality

The ADC_RDY physical pin asserts are determined by ADC_RDY_CTRL bit in the ADC_CONV_CTRL register. The ADC_RDY pin asserts at end of the each conversions sequence or at the end of each conversion.

If ADC status is monitored only by the SPI, it is recommended to poll the ADC_DATA_RDY bit in LIVE_STATUS register or ADC_RDY bit in the readback SPI frame (see Table 36). Polling any ADC result register must be avoided.

The behavior of ADC_DATA_RDY bit and ADC_RDY physical pin is not identical. In continuous conversion mode, ADC_RDY pin automatically deasserts after 25µs, but ADC_DATA_RDY bit must be cleared manually. Write 0b10 to the CONV_SEQ bit field in ADC_CONV_CTRL register to clear the ADC_DATA_RDY bit. This does not interrupt the currently active continuous conversion. Clearing ADC_DATA_RDY bit also clears ADC_RDY bit in the SPI readback frame.

A user can find the ADC sequence counter in ADC_RESULT_UPR[n] register. Bit field CONV_SEQ_COUNT holds the value of the 2-bit counter, it is used to confirm from which particular sequence ADC results are. Only one counter is shared among all channels. Counter value being increment every single time ADC sequence completes, even when particular channel measurement is disabled.

ADC_RESULT_UPR[n] must be read first, immediately followed by a read of ADC_RESULT[n]. The reason for the same is that reading ADC_RESULT_UPR[n] latches ADC_RESULT[n] register to ensure that data corresponding to the same conversion are read. The same rule applies to LAST_ADC_RESULT_UPR[n] and LAST_ADC_RESULT[n].

Users must use burst read to output 24-bit ADC results in applications where the read sequence and immediate read of the subsequent register cannot be ensured.

To configure ADC_RDY pin asserting at the end of a sequence conversions, set ADC_RDY_CTRL bit to 0. It is expected that the resulting ADC data are read by ADC_RESULT_UPR[n], ADC_RESULT[n], and ADC_DIAG_RESULT[n]. Result registers update at the end of a sequence.

In single conversion mode, the ADC_RDY pin deasserts at the following scenario (see Figure 53):

- The write to the ADC_CONV_CTRL register, which initiates the conversion sequence.

In continuous conversion mode, the ADC_RDY pin deasserts at any of the following scenarios (see Figure 54):

- The write to the ADC_CONV_CTRL register, which initiates the conversion sequence.
- Automatically after 25µs.

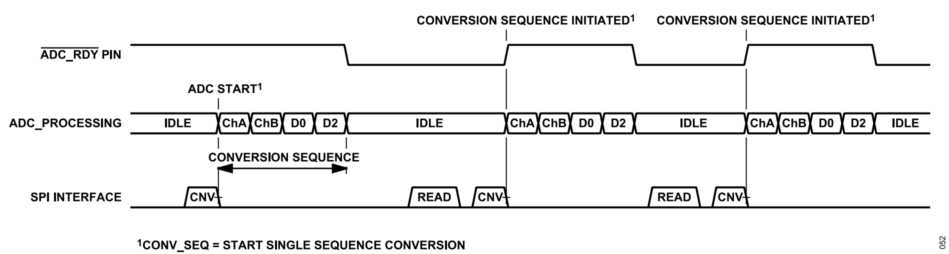

Figure 53. ADC_RDY Functionality in Single Conversion Mode for ADC_RDY_CTRL = 0

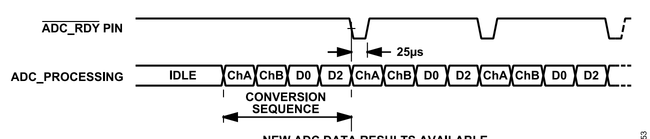

Figure 54. ADC_RDY Functionality in Continuous Conversion Mode for ADC_RDY_CTRL = 0

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To configure the ADC_RDY pin asserting at the end of every conversion, set the ADC_RDY_CTRL bit to 1. Read LAST_ADC_RESULT_UPR[n] and LAST_ADC_RESULT[n] to obtain ADC data. Result registers update immediately at the end of each conversion.

In single conversion mode, the ADC_RDY pin deasserts at any of the following scenarios (see Figure 55):

- The write to the ADC_CONV_CTRL register, which initiates the conversion sequence.
- Automatically after 25µs in the case of more than one conversion is enabled in the sequence.

In continuous conversion mode, the ADC_RDY pin deasserts at any of the following scenarios (see Figure 56):

- The write to the ADC_CONV_CTRL register, which initiates the conversion sequence.
- Automatically after 25µs.

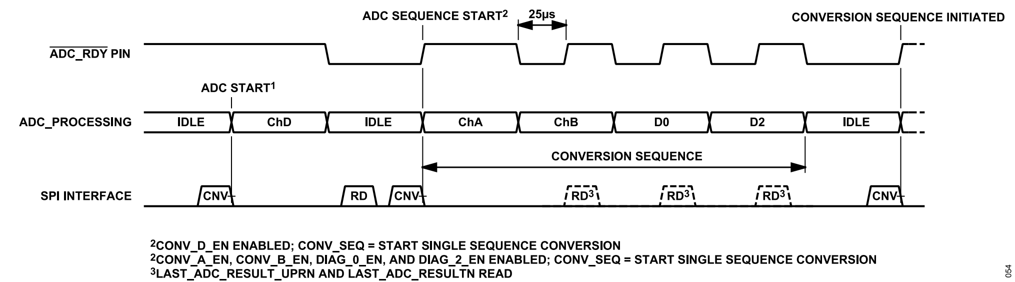

Figure 55. ADC_RDY Functionality in Single Conversion Mode for ADC_RDY_CTRL = 1

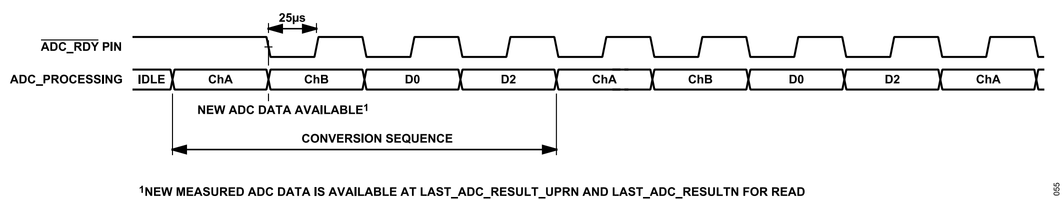

Figure 56. ADC_RDY Functionality in Continuous Conversion Mode for ADC_RDY_CTRL = 1

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ADC Noise

Table 28 shows the peak-to-peak noise of the AD74416H for each of the channel output data rates and voltage ranges. Table 29 shows the peak-to-peak noise of the AD74416H diagnostic. These numbers are typical and are generated with a differential input voltage of 0V when the ADC is continuously converting on a single channel.

Table 28. Peak-to-Peak Noise in LSBs per Voltage Range and Output Data Rate (Inputs Shorted)

ADC_CONFIGn.CONV_RATE Conversion Rate	+12V Range (24-Bit LSBs)	±12V Range (24-Bit LSBs)	±2.5V Range (24-Bit LSBs)	+0.625V Range (24-Bit LSBs)	0.3125 V Range[1] (24-Bit LSBs)	±0.3125V Range (24-Bit LSBs)	±104mV Range (24-Bit LSBs)
0b0000: 10SPS_H[2]	23.4	11.7	13.3	52.2	96.0	48.0	129.0
0b0001: 20SPS	44.8	22.4	25.6	105.4	191.2	95.6	257.7
0b0011: 20SPS_H[2]	31.8	15.9	18.3	73.2	134.6	67.3	183
0b0100: 200SPS_H[2, 3]	85.2	42.6	48.2	186.0	350.2	175.1	480.3
0b0110: 200SPS_H[2]	106.2	53.1	61.9	242.2	452.0	226.0	602.2
0b1000: 1.2kSPS	297.0	148.5	168.8	693.0	1254.0	627.0	1696.0
0b1001: 1.2kSPS_H[2]	234.4	117.2	135.1	587.4	991.0	495.5	1363.2
0b1100: 4.8kSPS	723.2	361.6	430.9	2077.6	3241.4	1620.7	4407.3
0b1101: 9.6kSPS	1417.2	708.6	877.3	4674.4	6340.0	3170.0	8854.8

1 Typical noise values for the +0.3125V to 0V range and the −0.3125V to 0V range are identical.

2 _H indicates HART fundamental frequencies rejection, which is 1.2kHz and 2.2kHz signals.

3 Moderate rejection of HART fundamental frequencies implemented.

Table 29. Diagnostic Peak-to-Peak Noise in LSBs per Output Data Rate (Inputs Shorted)

ADC_CONV_CTRL.CONV_RATE_DIAG Conversion Rate	+2.5V Range (16-bit LSBs[1])
0b000: 20SPS	<1
0b001: 20SPS_H[2]	<1
0b010: 1.2kSPS_H[2]	2
0b011: 4.8kSPS	4
0b100: 9.6kSPS	7
0b101: 19.2kSPS	18

1 Resolution of LVIN Diagnostic is 16-bit.

2 _H indicates HART fundamental frequencies rejection, which is 1.2kHz and 2.2kHz signals.

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Diagnostics

The AD74416H has a diagnostic function that allows the ADC to measure various on-chip voltages. These diagnostic voltages are scaled to be measurable within the ADC range.

The diagnostics inputs are independent of the four available channel measurements of the AD74416H. The DIAG_ASSIGN register assigns the voltage measurements to each diagnostic input. Select a diagnostic input to be measured by the ADC by enabling that input in the ADC_CONV_CTRL register.

A user can also select the conversion rate by the ADC_CONV_CTRL register. The following conversion rates are available for selection within the ADC_CONV_CTRL register: 19.2kSPS, 9.6kSPS, 4.8kSPS, 1.2kSPS, and 20SPS. In addition, 50Hz and 60Hz rejection is provided on the 20SPS conversion rate. HART fundamental frequencies rejection is provided at 1.2kSPS and dedicated 20SPS conversion rate.

Table 30 shows a full list of available diagnostics and the equations required to calculate the diagnostic value. Figure 57 visually emphasizes diagnostics that a user can select.

In the equations, as shown in Table 30, DIAG_CODE is the ADC result code read from the ADC_DIAG_RESULTn registers, and the voltage range is the ADC measurement range and is 2.5V.

Table 30. User-Selectable Diagnostics[1]

DIAGn Settings in the DIAG_ASSIGN Register	Diagnostic	Formula to Interpret ADC Result	Theoretical Measurement Range[2]
0b0000	AGND: V_{AGND}	$V_{AGND} = \frac{DIAG\_CODE}{65,536} \times 2.5$	0V to 2.5V
0b0001	TEMP: Temperature Sensor (Internal Die Temperature Measurement)/°C	$Temperature = \left(\frac{DIAG\_CODE - 2034}{8.95}\right) - 40$	For recommended maximum junction temperature, see Table 15
0b0010	DVCC: Voltage on DVCC Pin (V_{DVCC})	$V_{DVCC} = \frac{DIAG\_CODE}{65,536} \times \frac{25}{3}$	0V to 8.3V
0b0011	AVCC: Voltage on AVCC Pin (V_{AVCC})	$V_{ALDO5V} = \frac{DIAG\_CODE}{65,536} \times 17.5$	0V to 17.5V
0b0100	LDO1V8: Voltage on LDO1V8 Pin (V_{LDO1V8})	$V_{LDO1V8} = \frac{DIAG\_CODE}{65,536} \times 7.5$	0V to 7.5V
0b0101	AVDD_HI: Voltage on AVDD_HI Pin (V_{AVDD_HI})	$V_{AVDD\_HI} = \frac{DIAG\_CODE}{65,536} \times \frac{25}{0.52}$	0V to 48V
0b0110	AVDD_LO: Voltage on AVDD_LO Pin (V_{AVDD_LO})	$V_{AVDD\_LO} = \frac{DIAG\_CODE}{65,536} \times \frac{25}{0.52}$	0V to 48V
0b0111	AVSS: Voltage on AVSS Pin (V_{AVSS})	$V_{AVSS} = \left(\frac{DIAG\_CODE}{65,536} \times 31.017\right) - 20$	−20V to +11V
0b1000	LVIN: Voltage on LVIN Pin (V_{LVIN})[3]	$V_{LVIN} = \frac{DIAG\_CODE}{65,536} \times 2.5$[3]	0V to 2.5V[3]
0b1001	DO_VDD: Voltage on DO_VDD Pin (V_{DO_VDD})	$V_{DO\_VDD} = \frac{DIAG\_CODE}{65,536} \times \frac{25}{0.64}$	0V to 39V
0b1010	VSENSEP_x[4]: Voltage on VSENSEP_x[4] Pin ($V_{VSENSEP\_n}$)		
	DIN_THRESH_MODE Bit = 0	$V_{VSENSEP\_x} = \left(\frac{DIAG\_CODE}{65,536} \times 60\right) - AVDD\_HI$	−AVDD_HI V to +60V − AVDD_HI
	DIN_THRESH_MODE Bit = 1	$V_{VSENSEP\_x} = \left(\frac{DIAG\_CODE}{65,536} \times 50\right) - 20$	−20V to +30V
0b1011	VSENSEN_x[4]: Voltage on VSENSEN_x[4] Pin ($V_{VSENSEN\_x}$)	$V_{VSENSEN\_x} = \left(\frac{DIAG\_CODE}{65,536} \times 50\right) - 20$	−20V to +30V
0b1100	I_DO_SRC_x[4]: Sourcing Current at DO_x[4] Flowing Through R_{SET} (I_{RSET})	$I_{RSET} = \left(\frac{DIAG\_CODE}{65,536} \times 0.5\right) / R_{SET}$	0V to 0.5V/RSET (equivalent to 3.3A when using recommended R_{SET} = 0.15Ω external resistor)
0b1101	AVDD_x[4]: Voltage on AVDD_x[4] Pin (V_{AVDD_x})	$V_{AVDD\_x} = \frac{DIAG\_CODE}{65,536} \times \frac{25}{0.52}$	0V to 48V

1 For the absolute input voltage that is measured by the ADC, see Table 11.

2 Actual measurement range might be limited by the value of the main power supplies (V_{AVDD_HI} and V_{AVSS}).

3 Typically used for auxiliary measurements, for example, cold junction compensation for thermocouple measurement.

4 x = A, B, C, and D.

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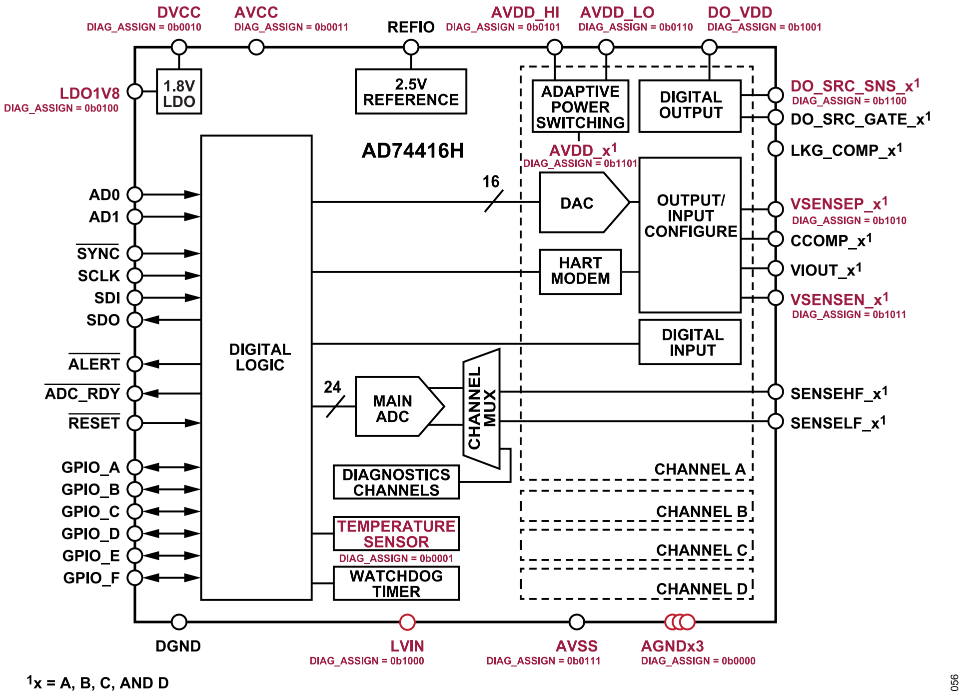

Figure 57. User-Selectable Diagnostics

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DAC FUNCTIONALITY

The AD74416H contains a 16-bit DAC. The DAC core is a 16-bit string DAC. The architecture structure consists of a string of resistors, each with a value of R. The digital input code that is loaded to the DAC_CODE register determines which node on the string the voltage is tapped off from and fed into the output amplifier. This architecture is inherently monotonic and linear.

There are two sources for the code loaded to the DAC. The typical option is to load a code to the DAC from the DAC_CODE register. The second option is to enable slewing to control the rate at which the DAC code is loaded to the DAC.

The code loaded to the DAC from either of the two sources is also loaded to the DAC_ACTIVE register. The DAC_ACTIVE register contains the current code loaded to the DAC, irrespective of the code source.

DAC Transfer Function

Table 31 shows the input code to ideal analog output relationship for each of the available output ranges.

Table 31. Ideal DAC Input Code to Output Relationship

DAC Code				Analog Output		
MSBs		LSBs		±12V	0V to 12V	0mA to 25mA
0000	0000	0000	0000	−12V	0V	0mA
0000	0000	0000	0001	24V × (1/65,536) − 12V	12V × (1/65,536)	25mA × (1/65,536)
1000	0000	0000	0000	0V	6V	12.5mA
1111	1111	1111	1110	24V × (65,534/65,536) − 12V	12V × (65,534/65,536)	25mA × (65,534/65,536)
1111	1111	1111	1111	24V × (65,535/65,536) − 12V	12V × (65,535/65,536)	25mA × (65,535/65,536)

THEORY OF OPERATION

Digital Linear Slew Rate Control

The digital linear slew rate control feature of the AD74416H controls the rate at which the output transitions to the new value. This slew rate control feature is available for both the current and voltage outputs.

When the slew rate control feature is disabled, the output value transitions at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the digital slew rate control feature by the OUTPUT_CONFIG[n] register.

After the digital slew rate control feature is enabled, the output steps digitally at a rate defined by the user in the OUTPUT_CONFIG[n] register. The SLEW_LIN_STEP bits dictate the number of codes per increment, and the SLEW_LIN_RATE bits dictate the rate at which the codes are updated. Table 32 shows the typical programmable slew rates for a zero scale to full scale (or full scale to zero scale) DAC update that is available on the AD74416H.

To give a calculation example, if SLEW_LIN_RATE is configured to 4.8kHz, the DAC active value changes by a single step every 208.33µs. For example, a 16-bit DAC contains 65536 codes to a full scale. With SLEW_LIN_STEP configured to 512, it takes 128 steps to change the DAC value from 0 to full scale, corresponding to 128 × 208.33µs = 26.7ms interval.

The DAC_ACTIVE[n] register can monitor the progress of slewing to a target DAC code. This register contains the code that is currently loaded to the DAC. DAC_CODE[n] must not be changed while actively slewing, only once DAC_ACTIVE[n] is settled.

If the digital slewing is disabled before the end code in the DAC_CODE[n] register is reached, the value remains at the DAC_ACTIVE[n] value and does not ramp to the end code.

HART Compliant Slew

An enhanced slew option allows compatibility with the HART analog rate of change requirements. Do the following steps to enable HART compatible slew rate to prevent glitches at the DAC output:

- Wait until HART compliant slew is settled. HART_COMPL_SETTLED bit is set to high in the OUTPUT_CONFIG[n] register, once HART compliant slew is settled.
- Set the SLEW_EN field to b10: SLEW_HART_COMPL in the OUTPUT_CONFIG[n] register to enable this slew option.

Table 32. Programmable Slew Times for a Zero-Scale to Full-Scale Code Update

	Step Size (% of Full-Scale DAC Voltage), Programmable by SLEW_LIN_STEP Bits[1]			
Update Slew Rate, Programmable by SLEW_LIN_RATE Bits (kHz)	0.8% (512)[2]	1.5% (960)[2]	6.1% (4000)[2]	22.2% (14560)[2]
4.8	26.7ms	14.4ms	3.54ms	1.04ms
76.8	1.7ms	898µs	221µs	65.1µs
153.6	833µs	449µs	111µs	32.6µs
230.4	556µs	299µs	73.78µs	21.7µs

1 These are theoretical values. The final slew rate is limited by the C_{LOAD} value.

2 Number of codes relevant to step size assuming full scale of 16-bit DAC.

THEORY OF OPERATION

Driving Inductive Loads

Use the digital slew rate control when driving inductive loads greater than approximately 4mH. Controlling the output slew rate minimizes ringing when stepping the output current by minimizing the current rate of change (di/dt). See the I_{OUT} typical performance of the settling time with an inductive load with and without the slew rate enabled in Figure 10.

RESET FUNCTION

After the AD74416H is reset, all registers are reset to the default state, and the calibration memory is refreshed. The device is configured in high impedance mode. A user can initiate the reset in several ways.

The hardware reset is initiated by pulsing the $\overline{\text{RESET}}$ pin low. The $\overline{\text{RESET}}$ pulse width must comply with the specifications, as shown in Table 14.

A software reset is initiated by writing the 0x15FA code (Software Reset Key 1) followed by the 0xAF51 code (Software Reset Key 2) to the CMD_KEY register. Software and hardware resets are identical in function and outcome.

Suppose a reset is required for all AD74416H devices connected to the same SPI interface, in such case, the BROADCAST_CMD_KEY register is used. A software reset to all devices is initiated by writing the 0x1A78 code (Software Reset Key 1) followed by the 0xD203 code (Software Reset Key 2) to the BROADCAST_CMD_KEY register.

A user can also initiate the reset by the thermal reset function, as shown in the Thermal Alert and Thermal Reset section.

A watchdog timer can generate the reset. For the description of the watchdog timer, see the Watchdog Timer section.

Low LDO1V8 or DVCC voltage triggers an internal power-on reset function that resets the AD74416H. The device does not come out of reset until the voltage at LDO1V8 and the DVCC is restored.

After a reset cycle completes, the RESET_OCCURRED bit is set in the ALERT_STATUS register. After the reset time elapses, clear relevant bits in the ALERT_STATUS register before continuing to use the device.

If an SPI transfer is attempted before the reset cycle is complete (for the typical reset time, see Table 13), the CAL_MEM_ERR bit in the SUPPLY_ALERT_STATUS register is also set to indicate that the calibration memory is not fully refreshed, and the device must not be configured until the calibration memory load has completed.

It is essential to ensure a proper refresh of the calibration memory. Reset of the AD74416H is required in case of asserted CAL_MEM_ERR bit.

Hardware, software, thermal, and watchdog-initiated resets have identical functionality, resulting in a reset of the AD74416H.

FET LEAKAGE COMPENSATION

A software configurable input and output solution includes a precision analog input and output capability along with a high current, digital output capability on a single screw terminal. In the AD74416H, the external FET used in the digital output function may contribute in off-leakage to the screw terminal when not in use. This leakage can affect the accuracy of the analog functions, especially to RTD measurements.

The AD74416H has a FET leakage compensation feature that provides an alternative path to the FET leakage to prevent it from flowing in the I/OP_x screw terminal (see Figure 33).

To enable this feature, configure the FET_LKG_COMP[n] register by setting the FET_SRC_LKG_COMP_EN bit for digital output.

Connect the LKG_COMP_x pin to the drain of the PMOS FET, as shown in Figure 48.

The FET leakage compensation feature can be used if the specified leakage of the chosen external FET is expected to contribute errors to the precision analog measurements like the current input or 3-wire and 2-wire RTD measurements.

FAULTS AND ALERTS

The AD74416H is equipped with several fault monitors to detect an error condition.

If an alert or fault condition occurs, the $\overline{\text{ALERT}}$ pin asserts. The $\overline{\text{ALERT}}$ pin alerts not only of an fault or error condition, but it also incorporates various informative flags, especially in case of the HART modem.

To determine the source of the alert condition, read the ALERT_STATUS register. This register contains a latched bits of alert conditions and in other cases it points to alert source (HART_ALERT_x, CHANNEL_ALERT_x, SUPPLY_ERR).

If CHANNEL_ALERT_x is asserted, read the CHANNEL_ALERT_STATUS[n] register to determine alert source. When SUPPLY_ERR bit is asserted, the SUPPLY_ALERT_STATUS register gives more insight concerning the alert source. The HART_ALERT_x bit indicates that alerts related to HART modem. Reading the HART_ALERT_STATUS[n] gives more insights.

After the cause for alert condition is removed, clear the activated flag by writing 1 to the location of the corresponding bits in the HART_ALERT_STATUS[n], CHANNEL_ALERT_STATUS[n], SUPPLY_ALERT_STATUS, or ALERT_STATUS. Write 0xFFFF to the ALERT_STATUS register to clear all alert bits. Alerts asserted in SUPPLY_ALERT_STATUS, HART_ALERT_STATUS, or CHANNEL_ALERT_STATUS[n] must be cleared before the ALERT_STATUS register.

The LIVE_STATUS register is a live representation of the error conditions. The bits in this register are not latched and clear automatically when the error condition is no longer present.

THEORY OF OPERATION

Each alert register has a corresponding alert mask register (ALERT_MASK, SUPPLY_ALERT_MASK, CHANNEL_ALERT_MASK[n], HART_ALERT_MASK[n]. A mask register prevents error conditions from activating the ALERT pin.

Channel Faults

The AD74416H is equipped with multiple open-circuit and short-circuit faults in the various functions, as shown in the Device Functions section. Recommendation to respond to open-circuit or short-circuit faults by setting channel to high impedance, if necessary, to avoid overheating of the device.

Power Supply Monitors

The AD74416H includes seven power supply monitors to detect a supply failure. If any of the supplies fall to less than the defined threshold shown in Table 13, the corresponding bit is set in the ALERT_STATUS register.

If AVDD_HI, AVDD_LO, or AVCC fall below the defined threshold, output channels automatically configure to high impedance. The channels revert to the previously selected channel function based on the register map's channel settings.

Channels configured as digital output are disabled once AVCC and DO_VDD fall below the defined thresholds. The channels revert once the power is restored based on the register map's channel settings.

Thermal Alert and Thermal Reset

If the AD74416H die temperature reaches the alert temperature, as shown in Table 13, a high-temperature error bit (TEMP_ALERT) is set in the ALERT_STATUS register to alert the user of the increasing die temperature.

A user can also configure the device to reset at higher die temperatures. To reset the device at higher temperatures, enable the thermal reset function by setting the THERM_RST_EN bit in the THERM_RST register. After this bit is set, the device goes through a full reset after the die temperature reaches the reset temperature, as shown in Table 13.

Burnout Currents

Burnout currents are used to verify the integrity of an attached sensor and to ensure that it has not gone to an open-circuit before taking a measurement from it.

Enable the AD74416H to provide a user-programmable, current source, or current sink that is programmed to a fixed values, as shown in Table 13. Burnout currents are available on the VIOUT pin (to monitor the I/OP screw terminal) and VSENSEN_x pin.

The burnout current sources are disabled on power up. Program the burnout current using the BRN_VIOUT_CURR (or BRN_SEN_VSENSEN_CURR) bit fields in the I_BURNOUT_CONFIG[n] register. Program the current direction to source or sink by BRN_VIOUT_POL (or BRN_SEN_VSENSEN_POL) bit.

Enable the current source at all times or, alternatively, enabled when needed for diagnostic purposes. When a burnout current source is enabled, the selected current is switched onto the selected pin, and it flows into external load connected.

GPIO_X PINS

The AD74416H has six GPIO pins. A user can configure each GPIO_x pin in several ways, which include the following:

- High impedance.
- Logic high or low output.
- Logic input.

The GPIO_x configuration is set by the GPIO_SELECT bits within the GPIO_CONFIG[n] registers. Additionally, configure the GPIO_A, GPIO_B, GPIO_C, and GPIO_D to monitor or control the HART modem. To monitor or control HART modem with GPIOs, configure the HART_GPIO_IF_CONFIG and HART_GPIO_MON_CONFIG[n] registers.Table 33 shows the features of each GPIO.

By default, a weak pull-down is enabled on the GPIO_x pins. Disable the weak pull-down if configuring any of the GPIO_x pins as logic outputs. To enable or disable the pull-down, set the GP_WK_PD_EN bit to 0 in the relevant GPIO_CONFIG[n] register.

Table 33. GPIO Configurability and Settings

Designator	Digital Input Mode	Digital Output Mode	HART Signals	Driving Strength
GPIO_A	Yes	Yes	Yes	Full
GPIO_B	Yes	Yes	Yes	Full
GPIO_C	Yes	Yes	Yes	Full
GPIO_D	Yes	Yes	Yes	Full
GPIO_E	Yes	Yes	No	Reduced[1, 2]
GPIO_F	Yes	Yes	No	Reduced[1, 2]

1 Specified with different loading current. For more details, see Table 13.

2 Decreased latency by 200ns comparing to other GPIO's.

THEORY OF OPERATION

Monitoring Digital Input Comparator Output

Read the output of the comparator in digital input logic or digital input loop powered mode either directly from the DIN_COMP_OUT register or monitored with the GPIO_x pin.

The GPIO_x pin is configured by the GPIO_CONFIGx register to drive out the debounced comparator output signal. Recommended configuration is as follows:

- Configure the GPIO_SELECT bit field to binary value 010 (SEL_GPIO) and GPO_DATA to required initial state in GPIO_CONFIGx register.
- Configure the CH_FUNC bits of CH_FUNC_SETUP register to digital input logic or digital input loop powered mode.
- Configure the comparator in DIN_CONFIG0x register (DIN_INV_COMP_OUT and COMPARATOR_EN bit fields).
- Wait for period of time corresponding to configured DE-BOUNCE_TIME bit field of DIN_CONFIG0.
- Configure the GPIO_SELECT bits to binary value 011 (SEL_DIN) in GPIO_CONFIGx register.

SPI

The AD74416H is controlled over a versatile 4-wire SPI, with a 2-bit address and an 8-bit CRC that operates at clock speeds of up to 20MHz (see the t_1 parameter in Table 14) and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

SPI is addressable for up to four devices. Addressable bits AD0 and AD1 determine address of the SPI subordinate node. Address bits are integrated into the SPI frame to allow identification of each frame on the bus.

Drive the AD0 and AD1 pins with the correct logic levels to give a recognizable address to AD74416H by the connection of the AD0 and AD1 pins to the corresponding voltage level, either DGND or DVCC. Address pins AD0 and AD1 are internally connected to DGND by weak pull-down resistors, which prevents pins from floating once unconnected.

SPI Write

The input shift register is 40 bits wide, and the data is loaded into the device MSB first under the control of SCLK. Data is clocked in on the falling edge of SCLK. Table 34 shows the structure of an SPI write frame.

Table 34. Writing to a Register

MSB						LSB
D39	**D38**	**[D37:D36]**	**[D35:D32]**	**[D31:D24]**	**[D23:D8]**	**[D7:D0]**
0	0	Device address[1]	Reserved	Register address	Data	CRC

[1] The AD0 and AD1 pins set the address for the SPI.

THEORY OF OPERATION

SPI Read

Two SPI frames are required to read a register location. The process is called 2-stage readback. The 2-stage readback is divided into two stages, request stage and read stage.

The first SPI frame, transmitted during request stage, contains the address of the register to be read is written to the READ_SELECT register. Table 35 shows the structure of the first SPI frame.

The second SPI frame, transmitted during read stage, contains of either a no operation (NOP) command or a write to any other register. The data is shifted out, MSB first, on the SDO pin:

- The MSB (Bit 39) is always set to 1 to allow the SPI main to detect if the SDO line is stuck low. This MSB is timed off the falling SYNC edge. All other bits are clocked out on the SCLK rising edge. Bit 38 is always 0. Start frame sequence using 10 (Bit 39, Bit 38) allows the validation of the frame and provides an additional layer of error detection in a harsh environment.
- Bits[D37:D36] provide the information concerning the SPI device address set by the AD0 and AD1 pins.
- Bits[D35:D32] provide the status information on the SDO pin concerning alerts and ADC_RDY pin. For more details, see Table 36.
- Bits[D31:D24] provide the address of the register being read. Content of the READBACK_ADDR bit field is shown in the READ_SELECT register.
- The contents of the selected register are available in Bits[D23:D8].
- An 8-bit CRC is returned in Bits[D7:D0].

Figure 58 shows the timing diagram of the 2-stage readback.

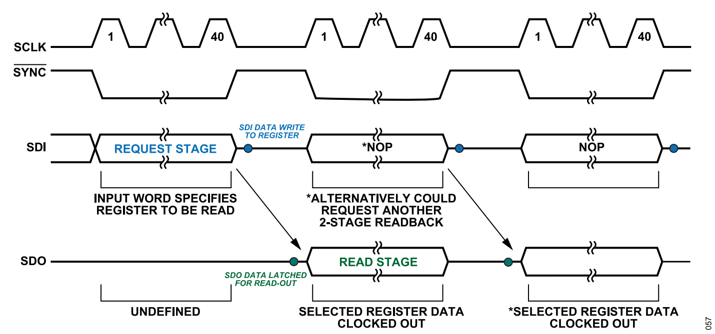

Figure 58. 2-Stage Readback Timing Diagram

Table 35. SDI Contents for a Readback Operation (Request Stage)

MSB									LSB
D39	D38	[D37:D36]	D35	D34	D33	D32	[D31:D24]	[D23:D8]	[D7:D0]
0	0	Device address[1]	0	0	0	0	0x6E	Readback address	CRC

[1] The AD0 and AD1 pins set the address for the SPI.

Table 36. SDO Contents for a Read Operation (Read Stage)

MSB									LSB
D39	D38	[D37:D36]	D35	D34	D33	D32	[D31:D24]	[D23:D8]	[D7:D0]
1	0	Device address[1]	ALERT[2]	HART_ALERT[3]	CHANNEL_ALERT[4]	ADC_RDY[5]	READBACK_ADDR	Read data	CRC

[1] The AD0 and AD1 pins set the address for the SPI.

[2] General alert. Reflects the status of the ALERT pin.

[3] HART alert. Logical OR of the four HART_ALERT_x bits in the ALERT_STATUS register.

[4] Channel alert. Logical OR of the four CHANNEL_ALERT_x bits in the ALERT_STATUS register.

[5] Reflects the ADC_RDY bit in the LIVE_STATUS register. The behavior of ADC_RDY bit and ADC_RDY physical pin is not identical. For more details, see the ADC_RDY Functionality section.

THEORY OF OPERATION

Burst Read Mode

The AD74416H incorporates a burst read mode that allows sequential reading of multiple registers on the SDO pin provided there are sufficient SCLKs.

To readback data from multiple registers, the SYNC line must be kept low after the second frame of a 2-stage readback (see the SPI Read section). The AD74416H increments through the register addresses clocking out the contents until the SYNC pin is returned high. An SPI_ERR error is reported if the transaction does not end with 40 + (n × 24) SCLK rising edges, where n is the number of transactions.

Here is an example of how to complete a burst read of the ADC result registers of Channel A and Channel C:

1. Enable required BURST_READ_SEL bits in the BURST_READ_SEL register. In this case, set only BURST_READ_SEL[2] and BURST_READ_SEL[4] to 1. This allows a read in burst ADC_RESULT_UPR0, ADC_RESULT0, ADC_RESULT_UPR2, and ADC_RESULT2. Note that the register addresses disabled in BURST_READ_SEL register are skipped and not part of burst read output.
2. Set the READBACK_ADDR bits in the READ_SELECT register to 0x41 to read the first of the ADC results registers.
3. Provide a NOP command. The contents of the ADC_RESULT_UPR0 register are clocked out on the SDO pin and the CRC (standard readback frame).
4. Keep the SYNC pin low to provide an additional 24 clocks to allow for the 16 bits of data from the ADC_RESULT0 register to be clocked out along with the 8 bits of the CRC.
5. Repeat step 4 two times. Keep the SYNC pin low to provide an additional 48 (2x24) clocks for another two registers ADC_RESULT_UPR2 and ADC_RESULT2.
6. Return SYNC high.
7. To read again same registers, repeat from step 2.

Figure 59 shows the contents on the SDO line when burst reading the registers. The data appearing on the SDO includes 16-bit of the frame header including device address and status bits, the 16-bit data of the read register, and the 8-bit CRC. For more details concerning the standard readback frame, see Table 36. When the SYNC pin is kept low and the another 24 clocks are applied, the data from the next sequential register address is clocked out.

Remove a register from the burst read sequence by deselecting it in the BURST_READ_SEL register.

If a burst read is started at the HART_RX register, and the SYNC pin is kept low for multiple reads, the HART_RX register is read continuously. The register address is not incremented in this instance.

Writes to the register map are not supported during register streaming in burst mode.

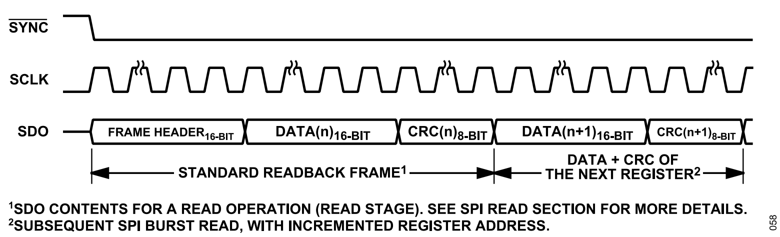

Figure 59. Burst Read Mode SDO Contents

THEORY OF OPERATION

SPI CRC

To ensure that data is received correctly in noisy environments, the AD74416H has a CRC implemented in the SPI. This CRC is based on an 8-bit CRC. The device controlling the AD74416H generates an 8-bit frame check sequence using the following polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

This frame check sequence is added to the end of the data-word, and the 40-bit data-word is sent to the AD74416H before taking the SYNC pin high.

A frame 40 bits wide containing the 32 data bits and 8 CRC bits must be supplied by the user. If the CRC check is valid, the data is written to the selected register. If the CRC check fails, the data is ignored, the SPI_ERR status bit in the ALERT_STATUS register is asserted, and the ALERT pin goes low.

An 8-bit CRC is also provided with the data read during a register readback that is used by the host microcontroller to verify that there are no SPI errors during the read transaction.

Clear the SPI_ERR bit in the ALERT_STATUS register by setting it to 1. Once the alert bit clears, the ALERT pin is deasserted (assuming that there are no other active alerts). Mask the SPI CRC error by writing to the relevant bit in the ALERT_MASK register.

SPI SCLK Count Feature

An SCLK count feature is built into the SPI diagnostics. Only SPI frames with exactly 40 SCLK falling edges are accepted by the SPI as a valid write. In burst read mode, the number of SCLK rising edges must equal 40 + (n × 24), where n is the number of transactions.

SPI frames of lengths other than the valid cases previously listed are ignored, and the SPI_ERR bit asserts in the ALERT_STATUS register. Mask the SPI_ERR bit by the ALERT_MASK register if needed.

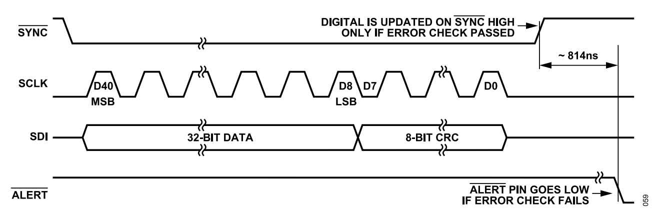

Figure 60. CRC Timing

Watchdog Timer

The watchdog timer (WDT) feature reduces the risk of losing SPI communication by initiating reset that automatically configures all the channels of the AD74416H into known high impedance mode.

Enable the WDT by setting WDT_EN bit field in WDT_CONFIG register. The first SPI transaction after the WDT enable initiates counting of the WDT timer. The WDT is zeroed out every time the valid SPI frame is transferred. Reaching defined timeout without SPI transaction results in reset of the AD74416H and sets RESET_OCCURRED bit in the ALERT_STATUS register, informing the user, that reset has occurred. Figure 61 shows the WDT function.

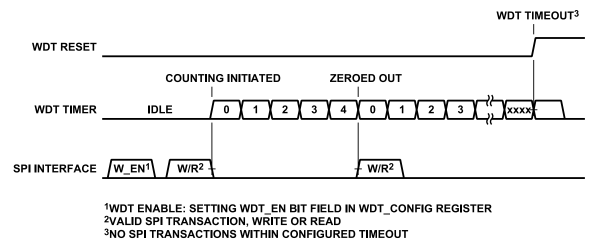

Figure 61. Watchdog Timing Diagram

The WDT allows configuration of a programmable timeout in the range from 1ms to 2s using WDT_TIMEOUT bit field in the WDT_CONFIG register. Table 37 shows the available programmable watchdog timeouts.

Table 37. Programmable Watchdog Timeouts

WDT_TIMEOUT Code[1] (Hex)	Timeout Time (ms)
0	1
1	5
2	10
3	25
4	50
5	100
6	250
7	500
8	750
9	1000
A	2000

1 Configuring WDT_TIMEOUT to other than those listed select 1000ms timeout.

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

Table 38 shows the external components that are recommended to operate the AD74416H.

Table 38. External Components

Component	Value Min	Value Typ	Value Max	Voltage Rating (V)	Suggested Component[1]	Notes/Comments
DECOUPLING						
AVDD_HI Decoupling		10µF		50	Generic	
		0.1µF		50	Generic	
AVDD_LO Decoupling		10µF		50	Generic	
		0.1µF		50	Generic	
AVSS Decoupling		10µF		50	Generic	
		100nF		50	Generic	
AVCC Decoupling		10µF		16	Generic	
		100nF			Generic	
DVCC Decoupling		10µF		16	Generic	
		0.1µF		16	Generic	
DO_VDD		10µF		100	Generic	
LDO1V8 Decoupling	1µF	2.2µF		6.3	C0805C225K9RAC7800	
REFIO Decoupling		22.0nF	50nF	6.3	Generic	
SUPPLY CONFIGURATION						Component placed between AVDD_HI and AVDD_LO pins
Schottky Diode		200mA		50	BAT41KFILM	Dual AVDD supply configuration
AVDD Resistor		2kΩ		Generic	Generic	Single AVDD supply configuration 1% accuracy
ANALOG INPUT AND OUTPUT						
CCOMP_x[2] Pin Compensation		220pF		100	Generic	This part is recommended for a total C_{LOAD} > 14nF, CCOMP capacitor is connected between the CCOMP pin and the I/OP screw terminal
SENSEHF_x[2] Filter Capacitor[3]		4.7nF		100	Generic	
SENSEHF_x[2] Filter Resistor[3]		2kΩ		Generic	Generic	The SENSEH resistor accuracy directly affects RTD specifications Suggested resistor precision 0.05% 2ppm/°C or 0.01% 5ppm/°C RNCF0603TKY2K00 RNCF0805TKY2K00 RU73X1J2K0LTDF RU73X2A2K0LTDF
SENSELF_x[2] Filter Capacitor[3]		4.7nF		100	Generic	
SENSELF_x[2] Filter Resistor[3]		2kΩ		Generic	Generic	1% accuracy
VSENSEP_x[2] Feedback Resistor		10kΩ		Generic	Generic	
VSENSEN_x[2] Pull-Down Resistor		100kΩ		Generic	Generic	
VSENSEP_x[2] Serial Resistor		2kΩ		Generic	Generic	1% accuracy
R_{SENSE}		12Ω		Generic	Generic	R_{SENSE} accuracy directly affects current input and RTD accuracy
SCREW TERMINAL						
Loading Capacitor		4.7nF		100	Generic	
36 V TVS				36	SMBJ36CA	

APPLICATIONS INFORMATION

Table 38. External Components (Continued)

Component	Value Min	Value Typ	Value Max	Voltage Rating (V)	Suggested Component[1]	Notes/Comments
DIGITAL OUTPUT						
External PFET for Sourcing Only				100	Si7113ADN	Suitable for sourcing designs
External Sense Resistor (R_{SET})		0.15Ω		Generic	Generic	Choose R_{SET} resistor value based on the required current resolution and range
Blocking Diode		1A		Generic	MSE1PB	

1 Use recommended components or ones that are similar.

2 x = A, B, C, and D.

3 Antialiasing filter values provide a compromise in performance for all use cases and conditions. Adjust these values to optimize for specific design conditions.

BOARD DESIGN AND LAYOUT CONSIDERATIONS

This section shows the critical board design and layout considerations for the AD74416H.

Track the SENSEHF_x and SENSELF_x filters directly to the pad of the R_{SENSE}.

To guarantee stability for the CCOMP_x pin, limit the capacitance to ground between the CCOMP_x pin and the C_{COMP} (if required) to <10pF.

To guarantee stability for the VSENSEP_x pin, limit the capacitance to ground between the VSENSEP_x pin and the required 2kΩ resistor to <10pF.

To optimize thermal performance, design the AD74416H boards with a minimum of four layers and with multiple thermal vias connecting the paddle to the bottom layer of the board. For more details, refer to the JEDEC JESD-51 specifications. Users are recommended to thermally connect the exposed pad of the AD74416H to the thermal vias.

When grounding the AD74416H pins, connect the AGND pins and DGND pins to a single ground plane. The I/ON_x screw terminal must be connected to the same ground plane.

Track the DO_SRC_SNS_x pin directly to the pad of the external R_{SET}. Considering the currents of the four digital output channels star connection is recommended for DO_VDD and R_{SET}.

Limit SDO ground capacitance to achieve required SPI operation speed.

REGISTER MAP

Table 39 and Table 40 summarizes the register map within formation on how to read and write to and from the registers. R indicates read-only access, R/W indicates read and write access, R/W1C indicates read and write 1 to clear, and W indicates write-only access.

Table 39. Register Map Summary

Address	Name	Description	Reset	Access
0x00	NOP	No Operation Register.	0x0000	R
0x01 to 0x25 by 12	CH_FUNC_SETUPn	Function Setup Register.	0x0000	R/W
0x02 to 0x26 by 12	ADC_CONFIGn	ADC Configuration Register.	0x0100	R/W
0x03 to 0x27 by 12	DIN_CONFIG0n	Digital Input Configuration Register.	0x000B	R/W
0x04 to 0x28 by 12	DIN_CONFIG1n	Digital Input Threshold Register.	0x0049	R/W
0x05 to 0x29 by 12	OUTPUT_CONFIGn	Output Configuration Register.	0x0100	R/W
0x06 to 0x2A by 12	RTD_CONFIGn	Resistance Configuration Register.	0x0001	R/W
0x07 to 0x2B by 12	FET_LKG_COMPn	FET Leakage Compensation Enable Register.	0x0000	R/W
0x08 to 0x2C by 12	DO_EXT_CONFIGn	DO External Control Register.	0x1700	R/W
0x09 to 0x2D by 12	I_BURNOUT_CONFIGn	Burnout Register.	0x0000	R/W
0x0A to 0x2E by 12	DAC_CODEn	DAC Code Register.	0x0000	R/W
0x0C to 0x30 by 12	DAC_ACTIVEn	DAC Active Code Register.	0x0000	R
0x32 to 0x37 by 1	GPIO_CONFIGn	General-Purpose Output Configuration Register.	0x0008	R/W
0x38	PWR_OPTIM_CONFIG	Power Optimization Configuration Register.	0x0000	R/W
0x39	ADC_CONV_CTRL	ADC Conversion Control Register.	0x0000	R/W
0x3A	DIAG_ASSIGN	Diagnostics Select Register.	0x0000	R/W
0x3B	WDT_CONFIG	Configuration Register for the Watchdog.	0x0009	R/W
0x3E	DIN_COMP_OUT	Debounced Digital Input Comparator Output Register.	0x0000	R
0x3F	ALERT_STATUS	Alert Status Register.	0x0001	R/W
0x40	LIVE_STATUS	Live Status Register.	0x0000	R
0x41 to 0x47 by 2	ADC_RESULT_UPRn	ADC Conversion Result Register per Channel (8MSBs).	0x0000	R
0x42 to 0x48 by 2	ADC_RESULTn	ADC Conversion Result Register per Channel (16LSBs).	0x0000	R
0x49 to 0x4C by 1	ADC_DIAG_RESULTn	Main ADC Diagnostic Results Registers.	0x0000	R
0x4D	LAST_ADC_RESULT_UPR	The Upper 8 Bits of the Last ADC Conversion Result Register.	0x0000	R
0x4E	LAST_ADC_RESULT	The Last ADC Conversion Result (16LSBs) Register.	0x0000	R
0x4F to 0x55 by 2	DIN_COUNTER_UPRn	Debounced DIN Count Register per Channel.	0x0000	R
0x50 to 0x56 by 2	DIN_COUNTERn	Debounced DIN Count Register per Channel.	0x0000	R
0x57	SUPPLY_ALERT_STATUS	Channel Error Status Register.	0x0000	R/W
0x58 to 0x5B by 1	CHANNEL_ALERT_STATUSn	Channel Alert Status Register.	0x0000	R/W
0x5C	ALERT_MASK	Alert Mask Register for ALERT_STATUS.	0x0000	R/W
0x5D	SUPPLY_ALERT_MASK	Alert Mask Register for SUPPLY_ALERT_STATUS.	0x0000	R/W
0x5E to 0x61 by 1	CHANNEL_ALERT_MASKn	Alert Mask Registers for the CHANNEL_ALERT_STATUS Registers.	0x0000	R/W
0x6E	READ_SELECT	Readback Select Register.	0x0000	R/W
0x6F	BURST_READ_SEL	Select the Registers Read in Burst Mode.	0xFFFF	R/W
0x73	THERM_RST	Thermal Reset Enable Register.	0x0000	R/W
0x74	CMD_KEY	Command Register.	0x0000	W
0x75	BROADCAST_CMD_KEY	Broadcast Write Register.	0x0000	W
0x76 to 0x79 by 1	SCRATCHn	Scratch or Spare Register.	0x0000	R/W
0x7A	GENERIC_ID	Generic ID Register.	0x0000	R
0x7B	SILICON_REV	Silicon Revision Register.	0x0002	R
0x7D	SILICON_ID0	Silicon ID 0 Register.	0x0000	R
0x7E	SILICON_ID1	Silicon ID 1 Register.	0x0000	R

REGISTER MAP

Table 40. HART Register Summary

Address	Name	Description	Reset	Access
0x80 to 0xB0 by 16	HART_ALERT_STATUSn	HART Communications Alert Register.	0x0020	R/W
0x81 to 0xB1 by 16	HART_RXn	HART Communications Receive Register.	0x0000	R
0x82 to 0xB2 by 16	HART_TXn	HART Communications Transmit Register.	0x0000	W
0x83 to 0xB3 by 16	HART_FCRn	FIFO Control Register.	0x08C1	R/W
0x84 to 0xB4 by 16	HART_MCRn	HART UART Tx Control Register.	0x0000	R/W
0x85 to 0xB5 by 16	HART_RFCn	RX FIFO Byte Count Register.	0x0000	R
0x86 to 0xB6 by 16	HART_TFCn	TX FIFO Byte Count Register.	0x0000	R
0x87 to 0xB7 by 16	HART_ALERT_MASKn	HART Communications Alert Mask Registers.	0x1EFF	R/W
0x88 to 0xB8 by 16	HART_CONFIGn	HART Support Configuration Register.	0x0C30	R/W
0x89 to 0xB9 by 16	HART_TX_PREMn	HART Transmit Preamble Count Register.	0x0005	R/W
0x8A to 0xBA by 16	HART_EVDETn	HART Event Detected Time Register.	0x0000	R
0x8C to 0xBC by 16	HART_CH_RESETn	Per Channel Hart Reset Register.	0x0000	R/W
0xC0	HART_GPIO_IF_CONFIG	Configure the GPIO Pins to Interface to the Modem or UART Register.	0x0000	R/W
0xC1 to 0xC4 by 1	HART_GPIO_MON_CONFIGn	Configure a GPIO Pin to Monitor a HART Signal Register.	0x0000	R/W

SOFTWARE CONFIGURABLE INPUT AND OUTPUT REGISTERS

Use the following registers to configure the input and output functionality and to take measurements from the AD74416H.

No Operation Register

Address: 0x00, Reset: 0x0000, Name: NOP

Write 0x00 to D15:D0 at this address to perform a NOP (No Operation) command.

Table 41. Bit Descriptions for NOP Register

Bits	Bit Name	Description	Reset	Access
[15:0]	NOP	Write 0x0000 to perform a NOP command.	0x0	R

Function Setup Register

Address: 0x01 to 0x25 (Increments of 12), Reset: 0x0000, Name: CH_FUNC_SETUPn

When CH_FUNC_SETUP is written, some fields in the ADC_CONFIG, RTD_CONFIG, DIN_CONFIG0_, DIN_CONFIG1_, and OUTPUT_CONFIG register may change for that channel.

When changing the function, Hi-Z use case must be entered as an intermediate step before entering the new use case.

Table 42. Bit Descriptions for CH_FUNC_SETUPn Register

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	CH_FUNC	Set the Channel Function. The default state on initial power-up/reset is high impedance. Values other than those listed below select the high-impedance function. 0000: High impedance (ADC is functional in this mode). 0001: Voltage output (FVMI). 0010: Current output (FIMV). 0011: Voltage input (measure voltage across the screw terminals I/O). 0100: Current input externally powered. 0101: Current input loop powered.	0x0	R/W

REGISTER MAP

Table 42. Bit Descriptions for CH_FUNC_SETUPn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		0111: Resistance measurement. 1000: Digital input (logic). 1001: Digital input (loop powered). 1010: Current out with HART. 1011: Current input (externally powered) with HART. 1100: Current input (loop powered) with HART.		

ADC Configuration Register

Address: 0x02 to 0x26 (Increments of 12), Reset: 0x0100, Name: ADC_CONFIGn

Table 43. Bit Descriptions for ADC_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:8]	CONV_RATE	Set the ADC Conversion Rate. 0000: Sampling rate of 10SPS. Which provides 50Hz/60Hz noise rejection and HART fundamental frequencies rejection. 0001: Sampling rate of 20SPS. Which provides 50Hz/60Hz noise rejection. 0011: Sampling rate of 20SPS. Which provides 50Hz/60Hz noise rejection and HART fundamental frequencies rejection. 0100: Sampling rate of 200SPS. Which provides moderate HART fundamental frequencies rejection. 0110: Sampling rate of 200SPS. Which provides HART fundamental frequencies rejection. 1000: Sampling rate of 1k2 SPS. 1001: Sampling rate of 1k2 SPS with HART fundamental frequencies rejection. 1100: Sampling rate of 4k8 SPS. 1101: Sampling rate of 9k6 SPS. Others: Reserved.	0x1	R/W
7	RESERVED	Reserved.	0x0	R
[6:4]	CONV_RANGE	Selects the ADC Range for Conversion. Values outside of those listed select the 0V to 12V range. Note that this field may change when the CH_FUNC_SETUP register is written. The value it changes to depends on the channel function. For more details, see CH_FUNC_SETUP. 000: 0V to 12V. 001: −12V to +12V. 010: −312.5mV to +312.5mV. 011: −0.3125V to 0V. 100: 0V to 0.3125V. 101: 0V to 0.625V. 110: −104mV to +104mV. 111: −2.5V to +2.5V.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	CONV_MUX	Selects the ADC Input Node for Conversion. This field may change when the CH_FUNC_SETUP register is written. The value it changes to depends on the channel function. For more details, see CH_FUNC_SETUP. 000: SENSELF to AGND. 001: SENSEHF to SENSELF. 010: VSENSEN to AGND. 011: SENSELF to VSENSEN. 100: AGND to AGND.	0x0	R/W

REGISTER MAP

Digital Input Configuration Register

Address: 0x03 to 0x27 (Increments of 12), Reset: 0x000B, Name: DIN_CONFIG0n

Table 44. Bit Descriptions for DIN_CONFIG0n Register

Bits	Bit Name	Description	Reset	Access
15	COUNT_EN	DIN Count Enable. If DIN_INV_COMP_OUT is 0, then positive edges of debounced DIN are counted. If DIN_INV_COMP_OUT is 1, then negative edges of debounced DIN are counted. The count is reflected in the DIN_COUNTER register.	0x0	R/W
14	DIN_INV_COMP_OUT	Set to 1 to Invert the Output from the DIN Comparator.	0x0	R/W
13	COMPARATOR_EN	Set to 1 to Enable the Comparator. This field may change when the corresponding CH_FUNC_SETUPn register is written. The value it changes to depends on the channel function.	0x0	R/W
12	DIN_SINK_RANGE	Select the DIN_SINK Current Range. 0: Range 0. 0mA to 3.7mA in steps of 120µA ~2k series resistance. 1: Range 1. 0mA to 7.4mA in steps of 240µA ~1k series resistance.	0x0	R/W
[11:7]	DIN_SINK	Sets the Sink Current on the DIN Pins. This bit field allows current to be programmed in steps as defined by DIN_SINK_RANGE. Set DIN_SINK to 0x00 to switch off the current sink. Note that this field goes to 0 when the corresponding CH_FUNC_SETUPn register is written, irrespective of the function.	0x0	R/W
6	DEBOUNCE_MODE	This bit determines the operation of the DIN debounce logic. 0: Debounce Mode 0. Integrator method is used, a counter increments when the signal asserts and decrements when the signal deasserts. 1: Debounce Mode 1. A simple counter increments when the signal asserts and resets when the signal deasserts.	0x0	R/W
5	RESERVED	Reserved.	0x0	R
[4:0]	DEBOUNCE_TIME	This bit field configures the debounce time on the DIN pins. Reset value: 240µs. Set DEBOUNCE_TIME[4:0] to 0x0 to bypass the debounce circuit.	0xB	R/W

Digital Input Threshold Register

Address: 0x04 to 0x28 (Increments of 12), Reset: 0x0049, Name: DIN_CONFIG1n

Configure the comparator threshold when configured to use the DIN function.

Table 45. Bit Descriptions for DIN_CONFIG1n Register

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	DIN_INPUT_SELECT	Digital Input Select. 1: DIN selects VIOUT. 0: DIN selects VSENSEP.	0x0	R/W
9	DIN_SC_DET_EN	Digital Input Short-Circuit Detect Enable.	0x0	R/W
8	DIN_OC_DET_EN	Digital Input Open-Circuit Detect Enable.	0x0	R/W
7	DIN_THRESH_MODE	This bit field sets the reference to the DIN threshold DAC. 0: The threshold scales with AVDD_HI. The threshold range is from −0.96 × AVDD_HI to AVDD_HI. 1: Fixed threshold. Threshold is from −19V to +30V.	0x0	R/W
[6:0]	COMP_THRESH	Comparator Threshold. DIN comparator threshold. Maximum programmable code is decimal 98.	0x49	R/W

Output Configuration Register

Address: 0x05 to 0x29 (Increments of 12), Reset: 0x0100, Name: OUTPUT_CONFIGn

REGISTER MAP

Table 46. Bit Descriptions for OUTPUT_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:14]	AVDD_SELECT	Adaptive Power Switching Setting. 00: Lock to AVDD_HI. 01: Lock to AVDD_LO. 10: Track supply if CH_FUNC = IOUT or if CH_FUNC = IOUT_HART. 11: Reserved.	0x0	R/W
13	RESERVED	Reserved.	0x0	R/W
12	ALARM_DEG_PERIOD	VIOUT Alarm Deglitch Period. Programmable VOUT SC alarm deglitch period. This impacts on the ANALOG_IO_SC and ANALOG_IO_OC interrupts reflected in register CHANNEL_ALERT_STATUS[n]. 0: Deglitch Period Configuration. 4ms digital deglitch is used for the OC or SC alarm in VOUT mode. 1: Deglitch Period Configuration. 20ms digital deglitch is used for the OC or SC alarm in VOUT mode.	0x0	R/W
11	VOUT_4W_EN	Default to 3-Wire VOUT. Set high for 4-wire.	0x0	R/W
10	WAIT_LDAC_CMD	Wait for LDAC Command Key. When 0, a write to the DAC_CODE register is immediately reflected in the DAC output. When 1, the DAC output is updated when a DAC Update Key command is written to the CMD_KEY register.	0x0	R/W
9	VIOUT_DRV_EN_DLY	Delay from VIOUT HV Bias to Drive Enable. Programmable delay only permitted in IOUT_HART CH_FUNC. In IOUT or VOUT default to fixed 200µs delay. Note that in IOUT_HART mode, there is a larger external capacitor to be charged when this mode is enabled. Increasing the delay prior to enabling of the driver ensures lower enable glitch energy when IOUT_HART is enabled. Note that this does come with a penalty of 4ms delay, but this is only at initiation of this mode. 0: 4ms delay. 1: 200µs delay.	0x0	R/W
8	HART_COMPL_SETTLED	HART Compliant Slew Settled. The HART compliant slew block, which is selected when SLEW_EN equals SLEW_HART_COMPL is continuously running and this flag indicates it has settled. If the user has to drive the DAC by SLEW_EN equals SLEW_CTRL_OFF or SLEW_LINEAR, then the HART compliant slew blocks output may lag the DAC_ACTIVE code. If the SLEW_EN is switched to SLEW_HART_COMPL, this results in a discontinuity in the output if the DAC compliant slew block is not settled. If switching from SLEW_CTRL_OFF or SLEW_LINEAR to SLEW_HART_COMPL, it is recommended to ensure that this flag is set prior to configuring SLEW_HART_COMPL. Note that when changing CH_FUNC from HIGH_IMP, this triggers a DAC update with the ADI factory programmed DAC offset. This results in HART_COMP_SETTLED going low, until such time as the HART compliant slew block has settled and HART_COMP_SETTLED returns high.	0x1	R
7	VOUT_RANGE	Voltage Output Range. 0: 0V to 12V. 1: −12V to +12V.	0x0	R/W
[6:5]	SLEW_EN	Set to 1 to Slew to the Requested DAC Code. 00: Slewing disabled. Slewing stops immediately when disabled, there are no further updates to the DAC code. 01: Enable linear slew on the DAC output. 10: Enable HART compliant slewing on the DAC output.	0x0	R/W
[4:3]	SLEW_LIN_STEP	Step Size for Digital Linear Slew. 00: Voltage step size of 0.8% of full-scale DAC voltage. 01: Voltage step size of 1.5% of full-scale DAC voltage. 10: Voltage step size of 6.1% of full-scale DAC voltage. 11: Voltage step size of 22.2% of full-scale DAC voltage.	0x0	R/W
[2:1]	SLEW_LIN_RATE	Update Rate for Digital Linear Slew.	0x0	R/W

REGISTER MAP

Table 46. Bit Descriptions for OUTPUT_CONFIGn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		00: Update at a rate of 4.8kHz. 01: Update at a rate of 76.8kHz. 10: Update at a rate of 153.6kHz. 11: Update at a rate of 230.4kHz.		
0	I_LIMIT	The sink and source current limits in VOUT modes. These are typical current limits. 0: VOUT: 16mA current limit. 1: VOUT: 8mA current limit.	0x0	R/W

Resistance Configuration Register

Address: 0x06 to 0x2A (Increments of 12), Reset: 0x0001, Name: RTD_CONFIGn

Table 47. Bit Descriptions for RTD_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	RTD_ADC_REF	Reference Selected for Scaling. Allows the customer to scale the internal factory offset to the external RTD reference. The internal digital logic automatically scales the factory calibrated ADC offset dependent on the selected reference when a RTD ADC measurement is performed. 0: External RTD reference of 2V. 1: External RTD reference of 1V.	0x0	R/W
2	RTD_MODE_SEL	Select Between 3W and 2W Resistance Measurement. 0: 3-wire RTD. Note that CONV_MUX must be set to LF_TO_VSENSEN when configured for 3-wire RTD. 1: 2-wire RTD. Note that CONV_MUX must be set to LF_TO_AGND when configured for 2-wire RTD .	0x0	R/W
1	RTD_EXC_SWAP	3-Wire RTD Excitation Swap. Setting this bit swaps excitation currents I1 and I2 to the VSENSEN and SENSEH pins, respectively. This feature is only used for 3-wire RTD.	0x0	R/W
0	RTD_CURRENT	RTD Current. 0: 500µA. 1: 1mA.	0x1	R/W

FET Leakage Compensation Enable Register

Address: 0x07 to 0x2B (Increments of 12), Reset: 0x0000, Name: FET_LKG_COMPn

Leakage compensation only operates when DO_MODE = DO_DISABLE.

Table 48. Bit Descriptions for FET_LKG_COMPn Register

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FET_SRC_LKG_COMP_EN	Leakage Compensation Circuit. Enable the source FET leakage compensation circuit. 0: Leakage compensation circuit off. 1: Leakage compensation circuit on.	0x0	R/W

DO External Control Register

Address: 0x08 to 0x2C (Increments of 12), Reset: 0x1700, Name: DO_EXT_CONFIGn

REGISTER MAP

Table 49. Bit Descriptions for DO_EXT_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	DO_T2	Digital Out Time 2. This timer monitors the digital out source FET short-circuit current level. The timer is programmable delay and if a short-circuit event duration exceeds this time then CHANNEL_ALERT_STATUS[n].DO_TIMEOUT is asserted and the DO is switched off. Setting this register to zero results in the min timer count and activation of the T2 timer when a short-circuit is detected. 00: T2 100.812µs. 01: T2 100.812µs. 02: T2 100.812µs. 03: T2 100.812µs. 04: T2 100.812µs. 05: T2 100.812µs. 06: T2 100.812µs. 07: T2 100.812µs. 08: T2 130.08µs. 09: T2 180.486µs. 10: T2 240.648µs. 11: T2 320.322µs. 12: T2 420.321µs. 13: T2 560.157µs. 14: T2 750.399µs. 15: T2 1.000803ms. 16: T2 1.3008ms. 17: T2 1.800795ms. 18: T2 2.400789ms. 19: T2 3.200781ms. 20: T2 4.200771ms. 21: T2 5.600757ms. 22: T2 7.500738ms. 23: T2 10.000713ms. 24: T2 13.000683ms. 25: T2 18.000633ms. 26: T2 24.000573ms. 27: T2 32.000493ms. 28: T2 42.000393ms. 29: T2 56.000253ms. 30: T2 100.000626ms. 31: T2 disabled.	0x17	R/W
7	DO_DATA	FET Drive. 0: Switch off the FET. 1: Switch on the FET.	0x0	R/W
[6:2]	DO_T1	Digital Out Time 1. This timer is used to program from 0ms to 100ms, the duration that an increased short-circuit current limit is enabled, to permit increased current through the FET after it is turned on. Setting this register to zero results in the timer being disabled and immediate activation of the T2 timer when a short-circuit is detected. 00: T1 bypass. 01: T1 100.812µs. 02: T1 100.812µs. 03: T1 100.812µs. 04: T1 100.812µs.	0x0	R/W

REGISTER MAP

Table 49. Bit Descriptions for DO_EXT_CONFIGn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		05: T1 100.812µs. 06: T1 100.812µs. 07: T1 100.812µs. 08: T1 130.08µs. 09: T1 180.486µs. 10: T1 240.648µs. 11: T1 320.322µs. 12: T1 420.321µs. 13: T1 560.157µs. 14: T1 750.399µs. 15: T1 1.000803ms. 16: T1 1.3008ms. 17: T1 1.800795ms. 18: T1 2.400789ms. 19: T1 3.200781ms. 20: T1 4.200771ms. 21: T1 5.600757ms. 22: T1 7.500738ms. 23: T1 10.000713ms. 24: T1 13.000683ms. 25: T1 18.000633ms. 26: T1 24.000573ms. 27: T1 32.000493ms. 28: T1 42.000393ms. 29: T1 56.000253ms. 30: T1 75.000063ms. 31: T1 100.000626ms.		
1	DO_SRC_SEL	Select Driver for FET. 1: The GPIO pin is configured to drive the FET. The user can select any GPIO to drive this channels FET. In addition, program the GPIO to SEL_DO. 0: Direct software control of the FET. When under software control the FET is controlled by DO_DATA.	0x0	R/W
0	DO_MODE	DO Source Enable Bit. If the CHANNEL_ALERT_STATUS[n].DO_TIMEOUT interrupt asserts, then the DO sourcing function disables. To reflect this, the DO_MODE BF automatically switches from DO_DRC selection mode to DO_DISABLE. 0: DO source disable. 1: DO source enable. If DO_SRC mode is selected, then leakage compensation mode is disabled, regardless of the value configured in FET_LKG_COMP[n].FET_SRC_LKG_COMP_EN.	0x0	R/W

Burnout Register

Address: 0x09 to 0x2D (Increments of 12), Reset: 0x0000, Name: I_BURNOUT_CONFIGn

Table 50. Bit Descriptions for I_BURNOUT_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:5]	BRN_SEN_VSENSEN_CURR	Sense VSENSEN Burnout Current. 00: No current. 01: 100nA. 10: 1µA.	0x0	R/W

REGISTER MAP

Table 50. Bit Descriptions for I_BURNOUT_CONFIGn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		11: 10µA.		
4	BRN_SEN_VSENSEN_POL	Sense VSENSEN Burnout Polarity. 0: Sinking current. 1: Sourcing current.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:1]	BRN_VIOUT_CURR	VIOUT Burnout Current. 00: No current. 01: 100nA. 10: 1µA. 11: 10µA.	0x0	R/W
0	BRN_VIOUT_POL	VIOUT Burnout Polarity. 0: Sinking current. 1: Sourcing current.	0x0	R/W

DAC Code Register

Address: 0x0A to 0x2E (Increments of 12), Reset: 0x0000, Name: DAC_CODEn

The DAC_CODE register is not reset by changing channel functions. Prior to changing channel functions, it is recommended to set the DAC code to 0x0000 by the DAC_CODE register. Set the channel function to high impedance by the CH_FUNC_ SETUP registers before transitioning to the new channel function.

After the new channel function is configured, it is recommended to wait channel characterization time (4.2ms for IOUT_HART function or 300µs for others) before updating the DAC code.

Table 51. Bit Descriptions for DAC_CODEn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_CODE	DAC Code Data for the Channel. If this register is written while OUTPUT_CONFIG.WAIT_LDAC_CMD is 0, then the new DAC code is immediately passed to the DAC. If this register is written while OUTPUT_CONFIG.WAIT_LDAC_CMD is 1, then the new DAC code is not passed to the DAC until a software LDAC update is triggered by the CMD register.	0x0	R/W

DAC Active Code Register

Address: 0x0C to 0x30 (Increments of 12), Reset: 0x0000, Name: DAC_ACTIVEn

Current value of the code loaded to the DAC.

Table 52. Bit Descriptions for DAC_ACTIVEn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	DAC_ACTIVE_CODE	The active DAC code passed to the analog domain. If slewing, use this field to determine the current slew position.	0x0	R

General-Purpose Output Configuration Register

Address: 0x32 to 0x37 (Increments of 1), Reset: 0x0008, Name: GPIO_CONFIGn

Table 53. Bit Descriptions for GPIO_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:6]	DIN_DO_CH	Select Channel If SEL_DO or SEL_DIN is Configured.	0x0	R/W

REGISTER MAP

Table 53. Bit Descriptions for GPIO_CONFIGn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		00: Channel A selected for SEL_DO or SEL_DIN. 01: Channel B selected for SEL_DO or SEL_DIN. 10: Channel C selected for SEL_DO or SEL_DIN. 11: Channel D selected for SEL_DO or SEL_DIN.		
5	GPI_DATA	General-Purpose Input Data Bit. This bit reflects the current state of the corresponding general-purpose input pin. Deglitch: A digital glitch filter is present on GPI to remove glitches of less than 4 periods of the system clock (typically 9.8304MHz). Latency: The synchronization and deglitching introduce a latency from pin to GPI_DATA of between 8 to 10 clock periods.	0x0	R
4	GPO_DATA	This bit sets the GPIO logic level when GPIO_SELECT = 01. 0: Drive a logic low on GPIO_n pin. 1: Drive a logic high on GPIO_n pin.	0x0	R/W
3	GP_WK_PD_EN	Pad Weak Pull-Down Enable. 0: Disable weak pull-down. 1: Enable weak pull-down.	0x1	R/W
[2:0]	GPIO_SELECT	Select the General-Purpose Output Mode. The GPI input pad is disabled for the high-impedance option. Values other than those listed below select high impedance. 000: High impedance. The GPIO output driver is off. The GPIO pad input buffer is disabled. 001: The GPIO pin logic output level is set by the GPO_DATA field. The GPIO pad input buffer is also enabled, so the pad functions in bidirectional mode. 010: The GPIO pin is configured as an input. GPIO output driver is configured in high-impedance state. 011: Select DIN as GPIO output. The debounced DIN comparator value, from the selected channel is output on this GPIO pin. The channel source is determined by BF DIN_DO_CH. 100: Select GPIO input as source of DO external. This mode allows the driver source for the DO external FET to be this GPIO pin. Note that BF DO_EXT_CONFIG[n].DO_SRC_SEL.GPIO_PIN must also be set. If two or more channels are programmed to select DO source for a particular channel, then the highest channel index configured to DO source have the priority.	0x0	R/W

Power Optimization Configuration Register

Address: 0x38, Reset: 0x0000, Name: PWR_OPTIM_CONFIG

If any of the SENSE_*OPT_* are taken out of standby mode, the ADC_CONV_CTRL.CONV_SEQ bit field must not be written for 100µs to allow time for the buffers to settle.

Table 54. Bit Descriptions for PWR_OPTIM_CONFIG Register

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	REF_EN	Power Enable for Internal Precision Reference Buffer.	0x0	R/W
12	SENSE_AGND_OPT	Sense AGND Buffer Optimization Enable. 0 =>, the sense AGND buffer is in full power mode. 1 =>, the sense AGND buffer is in low power mode.	0x0	R/W
11	SENSE_HF_OPT_D	Sense HF Buffer Optimization Enable. 0 =>, the sense HF buffer is in full power mode. 1 =>, the sense HF buffer is in low power mode.	0x0	R/W
10	SENSE_HF_OPT_C	Sense HF Buffer Optimization Enable. 0 =>, the sense HF buffer is in full power mode. 1 =>, the sense HF buffer is in low power mode.	0x0	R/W
9	SENSE_HF_OPT_B	Sense HF Buffer Optimization Enable. 0 =>, the sense HF buffer is in full power mode. 1 =>, the sense HF buffer is in low power mode.	0x0	R/W
8	SENSE_HF_OPT_A	Sense HF Buffer Optimization Enable. 0 =>, the sense HF buffer is in full power mode. 1 =>, the sense HF buffer is in low power mode.	0x0	R/W
7	SENSE_LF_OPT_D	Sense LF Buffer Optimization Enable. 0 =>, the sense LF buffer is in full power mode. 1 =>, the sense LF buffer is in low power mode.	0x0	R/W

REGISTER MAP

Table 54. Bit Descriptions for PWR_OPTIM_CONFIG Register (Continued)

Bits	Bit Name	Description	Reset	Access
6	SENSE_LF_OPT_C	Sense LF Buffer Optimization Enable. 0 =>, the sense LF buffer is in full power mode. 1 =>, the sense LF buffer is in low power mode.	0x0	R/W
5	SENSE_LF_OPT_B	Sense LF Buffer Optimization Enable. 0 =>, the sense LF buffer is in full power mode. 1 =>, the sense LF buffer is in low power mode.	0x0	R/W
4	SENSE_LF_OPT_A	Sense LF Buffer Optimization Enable. 0 =>, the sense LF buffer is in full power mode. 1 =>, the sense LF buffer is in low power mode.	0x0	R/W
3	VSENSEN_OPT_D	Sense VSENSEN Buffer Optimization Enable. 0 =>, the sense external buffer is in full power mode. 1 =>, the sense external buffer is in low power mode.	0x0	R/W
2	VSENSEN_OPT_C	Sense VSENSEN Buffer Optimization Enable. 0 =>, the sense external buffer is in full power mode. 1 =>, the sense external buffer is in low power mode.	0x0	R/W
1	VSENSEN_OPT_B	Sense VSENSEN Buffer Optimization Enable. 0 =>, the sense external buffer is in full power mode. 1 =>, the sense external buffer is in low power mode.	0x0	R/W
0	VSENSEN_OPT_A	Sense VSENSEN Buffer Optimization Enable. 0 =>, the sense external buffer is in full power mode. 1 =>, the sense external buffer is in low power mode.	0x0	R/W

ADC Conversion Control Register

Address: 0x39, Reset: 0x0000, Name: ADC_CONV_CTRL

This register controls the ADC conversions performed.

Writing 1 to an EN field and setting CONV_SEQ to Single in this register triggers a single conversion. Fields in the register do not clear when a conversion completes. To enable a subsequent conversion, do not clear a field, simply write again.

When CONV_SEQ is set to Continuous, the device continuously loops through the enabled channels. The channels/diagnostics enabled cannot be modified while a continuous sequence is in progress. To modify the enabled channels stop the sequence, modify the enabled channels/diagnostics and start the sequence again.

When enabling a sequence, first ensure that any previous sequence has completed, that is wait until LIVE_STATUS.ADC_BUSY bit is 0.

Table 55. Bit Descriptions for ADC_CONV_CTRL Register

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	ADC_RDY_CTRL	ADC_RDY Pin Control. 0: End of a sequence of conversions. The ADC_RDY pin asserts at the end of every sequence of conversions. When using this mode, its expected that a user reads data by the ADC_RESULTS* and DIAG_RESULTS* registers, which update at the end a sequence. If CONV_SEQ == CONTINUOUS, then the ADC_RDY pin deasserts after 25µs. If CONV_SEQ == SINGLE, then the ADC_RDY pin deasserts when the ADC_CONV_CTRL register is written. 1: End of every conversion. The ADC_RDY pin asserts at the end of every conversion. When using this mode, its expected that a user reads the latest results by the LAST_ADC_RESULT* registers. However, a user can still read the ADC data read by the ADC_RESULTS* and DIAG_RESULTS* registers, which update immediately at the end each conversion (rather than at the end of the sequence). If CONV_SEQ == CONTINUOUS, then the ADC_RDY pin deasserts 25µs after it asserts. If CONV_SEQ == SINGLE, then the ADC_RDY pin deasserts when ADC_CONV_CTRL register is written if there is only one conversion enabled in the sequence. If there is more than one conversion in the sequence, then ADC_RDY pin deasserts 25µs after it asserts.	0x0	R/W
[12:10]	CONV_RATE_DIAG	Conversion Rate for Diagnostics. A value outside of those listed below will select a rate of 20SPS. 000: Sampling rate of 20SPS. Which provides 50Hz/60 Hz noise rejection. 001: Sampling rate of 20SPS. Which provides 50Hz/60 Hz noise rejection and HART 1.2kHz and 2.2kHz rejection. 010: Sampling rate of 1k2 SPS. Which provides HART 1.2kHz and 2.2kHz rejection. 011: Sampling rate of 4k8 SPS.	0x0	R/W

REGISTER MAP

Table 55. Bit Descriptions for ADC_CONV_CTRL Register (Continued)

Bits	Bit Name	Description	Reset	Access
		100: Sampling rate of 9k6 SPS. 101: Sampling rate of 19k2 SPS.		
[9:8]	CONV_SEQ	Selects Single or Continuous Mode. 00: Stop continuous conversions or power up the ADC. If converting continuously, stop conversions at the end of the current sequence and leave the ADC powered up. Or, if the ADC is powered down then power up the ADC. If exiting ADC IDLE, then it may take up to 100µs to power up the HV Buffers, if HV Buffers need to be powered up. ADC_BUSY is 1 while the HV Buffers are powering up. If using this command to exit ADC IDLE, then wait for the HV Buffers to power up before writing to this field again. 01: Start single sequence conversion. Perform a single conversion on each enabled channel and diagnostic. If the ADC is currently powered down, then it automatically powers up the ADC and wait 100µs before starting conversions when this value is written. On exiting from single sequence conversion mode, the sequencer moves to the IDLE state. 10: Start continuous conversions. Sequence continuously through the enabled channels and diagnostics. If the ADC is currently powered down, then it automatically powers up the ADC and wait 100µs before starting conversions when this value is written. If exiting continuous conversion mode, the sequencer waits until the end of the current sequence before moving to IDLE or ADC_PWRDWN. 11: Stop continuous conversions or power down the ADC. If converting continuously, then stop conversions at the end of the current sequence and power down the ADC. If not currently converting, then simply power down the ADC. If exiting ADC is powered down, then it takes 100µs to power up the ADC. ADC_BUSY is 1 while the ADC is powering up. If using this command to exit ADC power down, then wait for the ADC to power up before writing to this field again.	0x0	R/W
7	DIAG_3_EN	Enable Conversions on Diagnostic 3. The diagnostic ADC result associated with this BF is located in register ADC_DIAG_RESULT[3].	0x0	R/W
6	DIAG_2_EN	Enable Conversions on Diagnostic 2. The diagnostic ADC result associated with this BF is located in register ADC_DIAG_RESULT[2].	0x0	R/W
5	DIAG_1_EN	Enable Conversions on Diagnostic 1. The diagnostic ADC result associated with this BF is located in register ADC_DIAG_RESULT[1].	0x0	R/W
4	DIAG_0_EN	Enable Conversions on Diagnostic 0. The diagnostic ADC result associated with this BF is located in register ADC_DIAG_RESULT[0].	0x0	R/W
3	CONV_D_EN	Enable Conversions on Channel D. The ADC result associated with this BF is located in register ADC_RESULT[3].	0x0	R/W
2	CONV_C_EN	Enable Conversions on Channel C. The ADC result associated with this BF is located in register ADC_RESULT[2].	0x0	R/W
1	CONV_B_EN	Enable Conversions on Channel B. The ADC result associated with this BF is located in register ADC_RESULT[1].	0x0	R/W
0	CONV_A_EN	Enable Conversions on Channel A. The ADC result associated with this BF is located in register ADC_RESULT[0].	0x0	R/W

Diagnostics Select Register

Address: 0x3A, Reset: 0x0000, Name: DIAG_ASSIGN

Values outside of those listed in Table 56 are connected to AGND.

Table 56. Bit Descriptions for DIAG_ASSIGN Register

Bits	Bit Name	Description	Reset	Access
[15:12]	DIAG3	Selects the Diagnostic Assigned to DIAG_RESULT[3]. 0000: Assign AGND to Diagnostic 3. 0001: Assign the temperature sensor to Diagnostic 3. 0010: Assign DVCC to Diagnostic 3. 0011: Assign AVCC to Diagnostic 3.	0x0	R/W

REGISTER MAP

Table 56. Bit Descriptions for DIAG_ASSIGN Register (Continued)

Bits	Bit Name	Description	Reset	Access
		0100: Assign LDO1V8 to Diagnostic 3. 0101: Assign AVDD_HI to Diagnostic 3. 0110: Assign AVDD_LO to Diagnostic 3. 0111: Assign AVSS to Diagnostic 3. 1000: Assign LVIN to Diagnostic 3. 1001: Assign DO_VDD to Diagnostic 3. 1010: Assign VSENSEP_D to Diagnostic 3. 1011: Assign VSENSEN_D to Diagnostic 3. 1100: Measure sourcing current from DO_D. 1101: Assign AVDD_D to Diagnostic 3.		
[11:8]	DIAG2	Selects the Diagnostic Assigned to DIAG_RESULT[2]. 0000: Assign AGND to Diagnostic 2. 0001: Assign the temperature sensor to Diagnostic 2. 0010: Assign DVCC to Diagnostic 2. 0011: Assign AVCC to Diagnostic 2. 0100: Assign LDO1V8 to Diagnostic 2. 0101: Assign AVDD_HI to Diagnostic 2. 0110: Assign AVDD_LO to Diagnostic 2. 0111: Assign AVSS to Diagnostic 2. 1000: Assign LVIN to Diagnostic 2. 1001: Assign DO_VDD to Diagnostic 2. 1010: Assign VSENSEP_C to Diagnostic 2. 1011: Assign VSENSEN_C to Diagnostic 2. 1100: Measure sourcing current from DO_C. 1101: Assign AVDD_C to Diagnostic 2.	0x0	R/W
[7:4]	DIAG1	Selects the Diagnostic Assigned to DIAG_RESULT[1]. 0000: Assign AGND to Diagnostic 1. 0001: Assign the temperature sensor to Diagnostic 1. 0010: Assign DVCC to Diagnostic 1. 0011: Assign AVCC to Diagnostic 1. 0100: Assign LDO1V8 to Diagnostic 1. 0101: Assign AVDD_HI to Diagnostic 1. 0110: Assign AVDD_LO to Diagnostic 1. 0111: Assign AVSS to Diagnostic 1. 1000: Assign LVIN to Diagnostic 1. 1001: Assign DO_VDD to Diagnostic 1. 1010: Assign VSENSEP_B to Diagnostic 1. 1011: Assign VSENSEN_B to Diagnostic 1. 1100: Measure sourcing current from DO_B. 1101: Assign AVDD_B to Diagnostic 1.	0x0	R/W
[3:0]	DIAG0	Selects the Diagnostic Assigned to DIAG_RESULT[0]. 0000: Assign AGND to Diagnostic 0. 0001: Assign the temperature sensor to Diagnostic 0. 0010: Assign DVCC to Diagnostic 0. 0011: Assign AVCC to Diagnostic 0. 0100: Assign LDO1V8 to Diagnostic 0. 0101: Assign AVDD_HI to Diagnostic 0. 0110: Assign AVDD_LO to Diagnostic 0.	0x0	R/W

REGISTER MAP

Table 56. Bit Descriptions for DIAG_ASSIGN Register (Continued)

Bits	Bit Name	Description	Reset	Access
		0111: Assign AVSS to Diagnostic 0. 1000: Assign LVIN to Diagnostic 0. 1001: Assign DO_VDD to Diagnostic 0. 1010: Assign VSENSEP_A to Diagnostic 0. 1011: Assign VSENSEN_A to Diagnostic 0. 1100: Measure sourcing current from DO_A. 1101: Assign AVDD_A to Diagnostic 0.		

Configuration Register for Watchdog

Address: 0x3B, Reset: 0x0009, Name: WDT_CONFIG

If the event that a successfully decoded SPI read or write command is not received during the WDT internal, the digital logic resets and the WDT_ERR interrupt asserts. Note that clear the WDT_ERR interrupt by using a W1C by the host software.

Table 57. Bit Descriptions for WDT_CONFIG Register

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
4	WDT_EN	Enable the Watchdog. The next SPI transaction starts the watchdog. 0: Disable (default). 1: Enable.	0x0	R/W
[3:0]	WDT_TIMEOUT	Set the Timeout Value. Values other than those listed below selects 1second. 0x0: Timeout set to 1ms. 0x1: Timeout set to 5ms. 0x2: Timeout set to 10ms. 0x3: Timeout set to 25ms. 0x4: Timeout set to 50ms. 0x5: Timeout set to 100ms. 0x6: Timeout set to 250ms. 0x7: Timeout set to 500ms. 0x8: Timeout set to 750mS. 0x9: Timeout set to 1s (default). Writing unused bits defaults to this threshold value. 0xA: Timeout set to 2s.	0x9	R/W

Debounced Digital Input Comparator Output Register

Address: 0x3E, Reset: 0x0000, Name: DIN_COMP_OUT

The DIN pin value is compared to a threshold voltage. The output of this comparison is fed into a programmable debounce circuit. The DIN_COMP_OUT register represents the output of the debounce circuit for each channel.

Table 58. Bit Descriptions for DIN_COMP_OUT Register

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	DIN_COMP_OUT_D	Debounced Digital Input State of Channel D.	0x0	R
2	DIN_COMP_OUT_C	Debounced Digital Input State of Channel C.	0x0	R
1	DIN_COMP_OUT_B	Debounced Digital Input State of Channel B.	0x0	R
0	DIN_COMP_OUT_A	Debounced Digital Input State of Channel A.	0x0	R

REGISTER MAP

Alert Status Register

Address: 0x3F, Reset: 0x0001, Name: ALERT_STATUS

This register contains a combination of channel alerts and system alerts. User action must be taken if any of these alerts asserts.

If a bit field access is W1C, then write 1 to the relevant bit to clear an alert condition. If a bit field access is R, then read the appropriate register to gain further insights (HART_ALERT_STATUS, CHANNEL_ALERT_STATUS, or SUPPLY_ALERT_STATUS).

An alert bit remains set if the condition causing the alert does not clear.

Table 59. Bit Descriptions for ALERT_STATUS Register

Bits	Bit Name	Description	Reset	Access
15	HART_ALERT_D	HART Communications Alert for Channel D. Read the HART_ALERT_STATUS[3] register to determine the source of this error. This bit is set if any of the fields in the HART_ALERT_STATUS[3] register are set (excluding CD and FRM_MON_STATE) and the corresponding field in HART_ALERT_MASK[3] is 0. This bit clears when all of fields (excluding CD and FRM_MON_STATE) in HART_ALERT_STATUS[3] are 0 or masked.	0x0	R
14	HART_ALERT_C	HART Communications Alert for Channel C. Read the HART_ALERT_STATUS[2] register to determine the source of this error. This bit is set if any of the fields in the HART_ALERT_STATUS[2] register are set (excluding CD and FRM_MON_STATE) and the corresponding field in HART_ALERT_MASK[2] is 0. This bit clears when all of fields (excluding CD and FRM_MON_STATE) in HART_ALERT_STATUS[2] are 0 or masked.	0x0	R
13	HART_ALERT_B	HART Communications Alert for Channel B. Read the HART_ALERT_STATUS[1] register to determine the source of this error. This bit is set if any of the fields in the HART_ALERT_STATUS[1] register are set (excluding CD and FRM_MON_STATE) and the corresponding field in HART_ALERT_MASK[1] is 0. This bit clears when all of fields (excluding CD and FRM_MON_STATE) in HART_ALERT_STATUS[1] are 0 or masked.	0x0	R
12	HART_ALERT_A	HART Communications Alert for Channel A. Read the HART_ALERT_STATUS[0] register to determine the source of this error. This bit is set if any of the fields in the HART_ALERT_STATUS[0] register are set (excluding CD and FRM_MON_STATE) and the corresponding field in HART_ALERT_MASK[0] is 0. This bit clears when all of fields (excluding CD and FRM_MON_STATE) in HART_ALERT_STATUS[0] are 0 or masked.	0x0	R
11	CHANNEL_ALERT_D	Alert for Channel D. Read the CHANNEL_ALERT_STATUS[3] register to determine the source. This bit is set if any of the fields in the CHANNEL_ALERT_STATUS[3] register are set and the corresponding field in CHANNEL_ALERT_MASK[3] is 0. This bit clears when all of fields in CHANNEL_ALERT_STATUS[3] are 0 or masked.	0x0	R
10	CHANNEL_ALERT_C	Alert for Channel C. Read the CHANNEL_ALERT_STATUS[2] register to determine the source. This bit is set if any of the fields in the CHANNEL_ALERT_STATUS[2] register are set and the corresponding field in CHANNEL_ALERT_MASK[2] is 0. This bit clears when all of fields in CHANNEL_ALERT_STATUS[2] are 0 or masked.	0x0	R
9	CHANNEL_ALERT_B	Alert for Channel B. Read the CHANNEL_ALERT_STATUS[1] register to determine the source. This bit is set if any of the fields in the CHANNEL_ALERT_STATUS[1] register are set and the corresponding field in CHANNEL_ALERT_MASK[1] is 0. This bit clears when all of fields in CHANNEL_ALERT_STATUS[1] are 0 or masked.	0x0	R
8	CHANNEL_ALERT_A	Alert for Channel A. Read the CHANNEL_ALERT_STATUS[0] register to determine the source. This bit is set if any of the fields in the CHANNEL_ALERT_STATUS[0] register are set and the corresponding field in CHANNEL_ALERT_MASK[0] is 0. This bit clears when all of fields in CHANNEL_ALERT_STATUS[0] are 0 or masked.	0x0	R
[7:6]	RESERVED	Reserved.	0x0	R
5	ADC_ERR	ADC Conversion or Saturation Error.	0x0	R/W1C
4	TEMP_ALERT	High Temperature Detected. If the die temperature reaches 115°C, this bit asserts.	0x0	R/W1C
3	SPI_ERR	SPI Error Detected. This bit is asserted if an SPI command is applied but 40 SCLK's are not provided or a CRC error is detected.	0x0	R/W1C
2	SUPPLY_ERR	Supply Error. Read the SUPPLY_ALERT_STATUS register to determine the source of this error. This bit is set if any of the fields in the SUPPLY_ALERT_STATUS register are set and the	0x0	R

REGISTER MAP

Table 59. Bit Descriptions for ALERT_STATUS Register (Continued)

Bits	Bit Name	Description	Reset	Access
		corresponding fields in SUPPLY_ALERT_MASK are 0. This bit clears when all the bit fields in SUPPLY_ALERT_STATUS are 0 or masked.		
1	RESERVED	Reserved.	0x0	R/W1C
0	RESET_OCCURRED	Reset Occurred. This bit is asserted after a reset event and, therefore, the $\overline{\text{ALERT}}$ pin is asserted after a reset. Write a 1 to this bit to clear the flag. Note that a mask bit is not provided for this bit.	0x1	R/W1C

Live Status Register

Address: 0x40, Reset: 0x0000, Name: LIVE_STATUS

This register contains the live status of some of the status bits (these bits are not latched and directly reflect the status bits).

Table 60. Bit Descriptions for LIVE_STATUS Register

Bits	Bit Name	Description	Reset	Access
15	ANALOG_IO_STATUS_D	Live Status of Analog IO for Channel D. Logical OR of the live status of ANALOG_IO_SC and ANALOG_IO_OC for Channel D.	0x0	R
14	ANALOG_IO_STATUS_C	Live Status of Analog IO for Channel C. Logical OR of the live status of ANALOG_IO_SC and ANALOG_IO_OC for Channel C.	0x0	R
13	ANALOG_IO_STATUS_B	Live Status of Analog IO for Channel B. Logical OR of the live status of ANALOG_IO_SC and ANALOG_IO_OC for Channel B.	0x0	R
12	ANALOG_IO_STATUS_A	Live Status of Analog IO for Channel A. Logical OR of the live status of ANALOG_IO_SC and ANALOG_IO_OC for Channel A.	0x0	R
11	DO_STATUS_D	Current Live Status of Ch D DO_SC Detect. Note that this field does not assert while the DO FET is in the T1 period of operation.	0x0	R
10	DO_STATUS_C	Current Live Status of Ch C DO_SC Detect. Note that this field does not assert while the DO FET is in the T1 period of operation.	0x0	R
9	DO_STATUS_B	Current Live Status of Ch B DO_SC Detect. Note that this field does not assert while the DO FET is in the T1 period of operation.	0x0	R
8	DO_STATUS_A	Current Live Status of Ch A DO_SC Detect. Note that this field does not assert while the DO FET is in the T1 period of operation.	0x0	R
7	DIN_STATUS_D	Live Status of DIN Circuit on Channel D. Logic OR of the live version of DIN_SC and DIN_OC for Channel D.	0x0	R
6	DIN_STATUS_C	Live Status of DIN Circuit on Channel C. Logic OR of the live version of DIN_SC and DIN_OC for Channel C.	0x0	R
5	DIN_STATUS_B	Live Status of DIN Circuit on Channel B. Logic OR of the live version of DIN_SC and DIN_OC for Channel B.	0x0	R
4	DIN_STATUS_A	Live Status of DIN Circuit on Channel A. Logic OR of the live version of DIN_SC and DIN_OC for Channel A.	0x0	R
3	TEMP_ALERT_STATUS	Temperature Alert Live Status. This bit field reflects the live status of the die temperature monitor. If the die temperature is at or above typically 115°C, this bit is asserted.	0x0	R
2	ADC_DATA_RDY	ADC Data Ready. If ADC_RDY_CTRL is 0, then this field asserts at the end of a sequence of conversions. This field self clears when the last results register in the sequence is read. If ADC_RDY_CTRL is 1, then this field asserts at the end of every conversion and self clears to 0 when any of one the registers LAST_ADC_RESULT*, ADC_RESULT*, or ADC_DIAG_RESULT* are read. Setting the CONV_SEQ bit field in the ADC_CONV_CTRL register to SINGLE or CONTINUOUS clears this bit.	0x0	R
1	ADC_BUSY	ADC Busy Status Bit. This bit resets to 1 as the ADC is initially in a power up state.	0x0	R
0	SUPPLY_STATUS	Supply Live Status. Logical OR of the inputs to the SUPPLY_ALERT_STATUS register.	0x0	R

ADC Conversion Result Register Per Channel (8MSBs)

Address: 0x41 to 0x47 (Increments of 2), Reset: 0x0000, Name: ADC_RESULT_UPRn

REGISTER MAP

To guarantee the accuracy of a 24-bit ADC result, ADC_RESULT_UPR must be read first followed immediately by a read of ADC_RESULT. Internally, the device holds on to the lower 16 bits corresponding to the read of the ADC_RESULT_UPR register, until the next read.

Table 61. Bit Descriptions for ADC_RESULT_UPRn Register

Bits	Bit Name	Description	Reset	Access
[15:13]	CONV_RES_MUX	ADC MUX. This field reflects the configuration of ADC_CONFIG.CONV_MUX for this result.	0x0	R
[12:10]	CONV_RES_RANGE	ADC Range. This field reflects the configuration of ADC_CONFIG.CONV_RANGE for this result.	0x0	R
[9:8]	CONV_SEQ_COUNT	ADC Sequence Count. This 2-bit counter increments every time an ADC sequence completes. When using continuous conversions, use it to confirm which sequence the ADC results are from. For example, use it to confirm that the same set of results are not read twice in the scenario where the host reads results registers faster than the time required for a sequence to complete. Note that for the first set of results after starting conversions, CONV_SEQ_COUNT is 1. It increments to 2, 3, 0, 1, 2, 3, and 0, thereafter. If the ADC is operating in single conversion mode, this BF is of limited use as the CONV_SEQ_COUNT resets at the start of the single conversion sequence.	0x0	R
[7:0]	CONV_RES[23:16]	ADC Conversion Result on Channel N.	0x0	R

ADC Conversion Result Register Per Channel (16LSBs)

Address: 0x42 to 0x48 (Increments of 2), Reset: 0x0000, Name: ADC_RESULTn

This register contains the lower 16 bits of the 24-bit ADC conversion result for each channel.

Table 62. Bit Descriptions for ADC_RESULTn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	CONV_RES[15:0]	ADC Conversion Result on Channel N.	0x0	R

Main ADC Diagnostic Results Registers

Address: 0x49 to 0x4C (Increments of 1), Reset: 0x0000, Name: ADC_DIAG_RESULTn

These four registers contain the 16-bit diagnostic ADC conversion results.

Table 63. Bit Descriptions for ADC_DIAG_RESULTn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	DIAGNOSTIC_RESULT	Contains the 16-bit Diagnostic Result on Diagnostic Channel.	0x0	R

The Upper 8 Bits of the Last ADC Conversion Result Register

Address: 0x4D, Reset: 0x0000, Name: LAST_ADC_RESULT_UPR

To guarantee the accuracy of a 24-bit ADC result, LAST_ADC_RESULT_UPR must be read first followed immediately by a read of LAST_ADC_RESULT. Internally, the device holds on to the lower 16 bits corresponding to the read of the LAST_ADC_RESULT_UPR register, until the next read. Even if only reading a 16-bit diagnostic result, LAST_ADC_RESULT_UPR must be read first followed immediately by a read of LAST_ADC_RESULT to ensure that the LAST_CONV_CH corresponds to the result read by LAST_ADC_RESULT.

If the last ADC conversion is for a diagnostic, then the upper 8 bits of LAST_CONV_RES returns 0, as diagnostics results are a maximum of 16 bits.

Table 64. Bit Descriptions for LAST_ADC_RESULT_UPR Register

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
[10:8]	LAST_CONV_CH	The Source of the Last Conversion Result. This field indicates that the source of the last conversion result. 000: Channel A.	0x0	R

REGISTER MAP

Table 64. Bit Descriptions for LAST_ADC_RESULT_UPR Register (Continued)

Bits	Bit Name	Description	Reset	Access
		001: Channel B. 010: Channel C. 011: Channel D. 100: Diagnostic 0. 101: Diagnostic 1. 110: Diagnostic 2. 111: Diagnostic 3.		
[7:0]	LAST_CONV_RES[23:16]	The Last ADC Conversion Result.	0x0	R

The Last ADC Conversion Result (16LSBs) Register

Address: 0x4E, Reset: 0x0000, Name: LAST_ADC_RESULT

This register contains the lower 16 bits of an ADC conversion result for the last conversion, which is for any channel or any diagnostic.

Use this register to get the latest conversion result. It is expected that this register is used in conjunction with ADC_CONV_CTRL.ADC_RDY_CTRL = 1 ($\overline{\text{ADC\_RDY}}$ asserts at the end of every conversion).

Table 65. Bit Descriptions for LAST_ADC_RESULT Register

Bits	Bit Name	Description	Reset	Access
[15:0]	LAST_CONV_RES[15:0]	The Last ADC Conversion Result.	0x0	R

Debounced DIN Count Register Per Channel

Address: 0x4F to 0x55 (Increments of 2), Reset: 0x0000, Name: DIN_COUNTER_UPRn

This counter is enabled when the COUNT_EN bit in DIN_CONFIGn register is set. This count is allowed to roll over from full-scale back to 0 so this register must be read often enough to avoid unexpected roll over.

When the enable signal is low the count is frozen.

The DIN_INV_COMP_OUT register inverts the deglitched output, thereby, allowing the counter increment edge to be modified.

Table 66. Bit Descriptions for DIN_COUNTER_UPRn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	DIN_CNT[31:16]	Contains the Count from the DIN Counter. This counter is enabled when the COUNT_EN bit within DIN_CONFIGn is set. When the enable signal is low, the count is frozen. This count is allowed to roll over by design as in normal operation its update rate must be slow. The customer software needs to manage the reading of this counter to ensure that its read often enough to avoid unexpected roll over. The DIN_INV_COMP_OUT register inverts the deglitched output, thereby, allowing the counter increment edge to be modified.	0x0	R

Debounced DIN Count Register Per Channel

Address: 0x50 to 0x56 (Increments of 2), Reset: 0x0000, Name: DIN_COUNTERn

This counter is enabled when the COUNT_EN bit in DIN_CONFIGn register is set. This count is allowed to roll over from full-scale back to 0 so this register must be read often enough to avoid unexpected roll over.

When the enable signal is low the count is frozen.

The DIN_INV_COMP_OUT register inverts the deglitched output, thereby, allowing the counter increment edge to be modified.

REGISTER MAP

Table 67. Bit Descriptions for DIN_COUNTERn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	DIN_CNT[15:0]	Contains the Count from the DIN Counter. This counter is enabled when the COUNT_EN bit within DIN_CONFIGn is set. When the enable signal is low, the count is frozen. This count is allowed to roll over by design as in normal operation its update rate must be slow. The customer software needs to manage the reading of this counter to ensure that its read often enough to avoid unexpected roll over. The DIN_INV_COMP_OUT register inverts the deglitched output, thereby, allowing the counter increment edge to be modified.	0x0	R

Channel Error Status Register

Address: 0x57, Reset: 0x0000, Name: SUPPLY_ALERT_STATUS

Table 68. Bit Descriptions for SUPPLY_ALERT_STATUS Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AVDD_HI_ERR	AVDD Hi Power Supply Monitor Error. This bit is asserted when AVDD falls below 5.5V.	0x0	R/W1C
5	AVDD_LO_ERR	AVDD Lo Power Supply Monitor Error. This bit is asserted when AVDD falls below 5.5V.	0x0	R/W1C
4	DO_VDD_ERR	DO VDD Power Supply Monitor Error. This bit is asserted when DO VDD falls below 9.3V.	0x0	R/W1C
3	AVCC_ERR	AVCC Power Supply Monitor Error. This bit is asserted when AVCC falls below 4.1V.	0x0	R/W1C
2	DVCC_ERR	DVCC Power Supply Monitor Error. This bit is asserted when DVCC falls below 2.2V. While a user can clear this alert with a W1C, it is recommended to reset the device to ensure correct operation.	0x0	R/W1C
1	AVSS_ERR	AVSS Power Supply Monitor Error. This bit is asserted when AVSS reaches above −1.6V.	0x0	R/W1C
0	CAL_MEM_ERR	Calibration Memory Error. This flag asserts under the following two conditions: 1. When a calibration memory CRC error or an uncorrectable ECC error is detected on calibration memory upload. 2. When there is an attempted SPI access to a register before the calibration memory refresh has completed. The part must not be addressed until calibration memory has been uploaded. Note that the calibration memory has not refreshed until after Device Power-Up Time or Device Reset Time. It is possible to determine which condition above caused CAL_MEM_ERR to assert. Once the user has waited until after Device Power-Up Time or Device Reset Time, write 1 to clear CAL_MEM_ERR. If CAL_MEM_ERR clears, then the bit is set to 1 due to an SPI access prior to calibration memory refresh being completed. If CAL_MEM_ERR stays asserted and cannot be cleared then a calibration memory error is detected. In this case, it is recommended to check the supplies and reset the device.	0x0	R/W1C

Channel Alert Status Register

Address: 0x58 to 0x5B (Increments of 1), Reset: 0x0000, Name: CHANNEL_ALERT_STATUSn

Table 69. Bit Descriptions for CHANNEL_ALERT_STATUSn Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	VIOUT_SHUTDOWN	The VOUT or IOUT has been shut down. The VOUT or IOUT channel has been shut down due to incorrect configuration or due to either of the following: 1. Switching between VOUT or IOUT modes without the prescribed wait period in HIGH_IMP state. 2. Changing VOUT_RANGE or VIOUT_DRV_EN_DLY while CH_FUNC[n] not equal to HIGH_IMP.	0x0	R/W1C
5	ANALOG_IO_OC	Analog IO Open-Circuit Detected. If CH_FUNC = IOUT or IOUT_HART, then ANALOG_IO_OC indicates that an open-circuit has been detected. This alarm has a configurable digital deglitch period as set by the bit field ALARM_DEG_PERIOD. If CH_FUNC = RES_MEAS, then	0x0	R/W1C

REGISTER MAP

Table 69. Bit Descriptions for CHANNEL_ALERT_STATUSn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		ANALOG_IO_OC indicates that resistance is out of range. This alarm has a fixed digital deglitch of 200μS.		
4	ANALOG_IO_SC	Analog IO Short-Circuit Detected. If CH_FUNC = VOUT, ANALOG_IO_SC indicates that a short-circuit has been detected. This alarm has a configurable digital deglitch period as set by the bit field ALARM_DEG_PERIOD. If CH_FUNC = IIN_EXT_PWR, IIN_LOOP_PWR, IIN_EXT_PWR_HART, or IIN_LOOP_PWR_HART, then ANALOG_IO_SC reflects the DIN comparator output. The comparator output has configurable digital deglitch period set by BF DEBOUNCE_TIME.	0x0	R/W1C
3	DO_TIMEOUT	DO Timeout.	0x0	R/W1C
2	DO_SC	DO Short-Circuit Detected. Note that this interrupt does not assert while the DO FET is in the T1 period of operation.	0x0	R/W1C
1	DIN_OC	DIN Open-Circuit Error.	0x0	R/W1C
0	DIN_SC	DIN Short-Circuit Error.	0x0	R/W1C

Alert Mask Register for ALERT_STATUS

Address: 0x5C, Reset: 0x0000, Name: ALERT_MASK

This register is used to mask particular status bits from activating the $\overline{\text{ALERT}}$ pin. The position of mask bits in this register line up the corresponding status bits in the ALERT_STATUS register.

To mask a particular alert, set the corresponding mask bit to 1.

Note that masking a bit does not prevent it from setting the equivalent alert bit in the ALERT_STATUS register.

Table 70. Bit Descriptions for ALERT_MASK Register

Bits	Bit Name	Description	Reset	Access
15	HART_ALERT_D_MASK	Mask Bit for HART_ALERT_D.	0x0	R/W
14	HART_ALERT_C_MASK	Mask Bit for HART_ALERT_C.	0x0	R/W
13	HART_ALERT_B_MASK	Mask Bit for HART_ALERT_B.	0x0	R/W
12	HART_ALERT_A_MASK	Mask Bit for HART_ALERT_A.	0x0	R/W
11	CHANNEL_ALERT_D_MASK	Mask Bit for CHANNEL_ALERT_D.	0x0	R/W
10	CHANNEL_ALERT_C_MASK	Mask Bit for CHANNEL_ALERT_C.	0x0	R/W
9	CHANNEL_ALERT_B_MASK	Mask Bit for CHANNEL_ALERT_B.	0x0	R/W
8	CHANNEL_ALERT_A_MASK	Mask Bit for CHANNEL_ALERT_A.	0x0	R/W
[7:6]	RESERVED	Reserved.	0x0	R
5	ADC_ERR_MASK	Mask Bit for ADC_SAT_ERR.	0x0	R/W
4	TEMP_ALERT_MASK	Mask Bit for TEMP_ALERT.	0x0	R/W
3	SPI_ERR_MASK	Mask Bit for SPI_ERR.	0x0	R/W
2	SUPPLY_ERR_MASK	Mask Bit for SUPPLY_ERR.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Alert Mask Register for SUPPLY_ALERT_STATUS

Address: 0x5D, Reset: 0x0000, Name: SUPPLY_ALERT_MASK

This register is used to mask particular status bits from activating the SUPPLY_ERR status bit in ALERT_STATUS register. The position of mask bits in this register line up the corresponding status bits in the SUPPLY_ALERT_STATUS register.

To mask a particular alert, set the corresponding mask bit to 1.

REGISTER MAP

Table 71. Bit Descriptions for SUPPLY_ALERT_MASK Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	AVDD_HI_ERR_MASK	Mask Bit for AVDD_HI_ERR.	0x0	R/W
5	AVDD_LO_ERR_MASK	Mask Bit for AVDD_LO_ERR.	0x0	R/W
4	DO_VDD_ERR_MASK	Mask Bit for DOVDD_ERR.	0x0	R/W
3	AVCC_ERR_MASK	Mask Bit for AVCC_ERR.	0x0	R/W
2	DVCC_ERR_MASK	Mask Bit for the DVCC_ERR.	0x0	R/W
1	AVSS_ERR_MASK	Mask Bit for the AVSS_ERR.	0x0	R/W
0	CAL_MEM_ERR_MASK	Mask Bit for CAL_MEM_ERR.	0x0	R/W

Alert Mask Registers for the CHANNEL_ALERT_STATUS Registers

Address: 0x5E to 0x61 (Increments of 1), Reset: 0x0000, Name: CHANNEL_ALERT_MASKn

These registers are used to mask particular status bits from activating the CHANNEL_ALERT_A/B/C/D status bits in ALERT_STATUS register.

The position of mask bits in this register line up the corresponding status bits in the CHANNEL_ALERT_STATUS register.

To mask a particular alert, set the corresponding mask bit to 1.

Table 72. Bit Descriptions for CHANNEL_ALERT_MASKn Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	VIOUT_SHUTDOWN_MASK	Mask Bit for VIOUT_SHUTDOWN.	0x0	R/W
5	ANALOG_IO_OC_MASK	Mask Bit for ANALOG_IO_OC.	0x0	R/W
4	ANALOG_IO_SC_MASK	Mask Bit for ANALOG_IO_SC.	0x0	R/W
3	DO_TIMEOUT_MASK	Mask Bit for DO_TIMEOUT.	0x0	R/W
2	DO_SC_MASK	Mask Bit for DO_SC.	0x0	R/W
1	DIN_OC_MASK	Mask Bit for DIN_OC.	0x0	R/W
0	DIN_SC_MASK	Mask Bit for DIN_SC.	0x0	R/W

Readback Select Register

Address: 0x6E, Reset: 0x0000, Name: READ_SELECT

This register selects the address of the register required to be readback and also determines the contents of the SPI readback frame.

Table 73. Bit Descriptions for READ_SELECT Register

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x0	R
[8:0]	READBACK_ADDR	D7 to D0 contains the register address to be read.	0x0	R/W

Select the Registers Read in Burst Mode

Address: 0x6F, Reset: 0xFFFF, Name: BURST_READ_SEL

Use this register to select which register are returned on a burst read that includes any of the registers ALERT_STATUS, LIVE_STATUS, ADC_RESULT*, DIAGNOSTIC_RESULT*, and DIN_COUNTER*.

REGISTER MAP

Table 74. Bit Descriptions for BURST_READ_SEL Register

Bits	Bit Name	Description	Reset	Access
[15:0]	BURST_READ_SEL	Select the Registers Returned on a Burst Read. If a bit corresponding to a register is 1, then that register is returned when a burst read reaches the register. If a bit corresponding to a register is 0, then that register is skipped when the burst read reaches the register. Bit 0: Enable ALERT_STATUS burst read. Bit 1: Enable LIVE_STATUS burst read. Bit 2: Enable ADC_RESULT_UPR[0] and ADC_RESULT[0] burst read. Bit 3: Enable ADC_RESULT_UPR[1] and ADC_RESULT[1] burst read. Bit 4: Enable ADC_RESULT_UPR[2] and ADC_RESULT[2] burst read. Bit 5: Enable ADC_RESULT_UPR[3] and ADC_RESULT[3] burst read. Bit 6: Enable ADC_DIAG[0] burst read. Bit 7: Enable ADC_DIAG[1] burst read. Bit 8: Enable ADC_DIAG[2] burst read. Bit 9: Enable ADC_DIAG[3] burst read. Bit 10: Enable LAST_ADC_RESULT_UPR and LAST_ADC_RESULT burst read. Bit 11: Enable DIN_COUNTER[0] burst read. Bit 12: Enable DIN_COUNTER[1] burst read. Bit 13: Enable DIN_COUNTER[2] burst read. Bit 14: Enable DIN_COUNTER[3] burst read. Bit 15: Enable SUPPLY_ALERT_STATUS burst read. Read data for all registers outside of those listed above are always returned on a burst read if the burst read includes the register. Note that the starting address location of a burst read is always returned even if its corresponding BURST_READ_SEL bit is 0. For example, if BURST_READ_SEL[2] is 0 and a burst read is started at the address for ADC_RESULT_UPR[0], then the first two words returned in a burst are ADC_RESULT_UPR[0] followed by ADC_RESULT[0]. Note that burst reads can start at DIN_COMP_OUT to include this as the first register in a burst read, DIN_COMP_OUT does not need a corresponding BURST_READ_SEL bit.	0xFFFF	R/W

Thermal Reset Enable Register

Address: 0x73, Reset: 0x0000, Name: THERM_RST

Table 75. Bit Descriptions for THERM_RST Register

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	THERM_RST_EN	Set to 1 to Enable Thermal Reset Functionality. If the die temperature reaches typically 140°C, a thermal reset event triggers a digital reset. This is detected by a change in the $\overline{\text{ALERT}}$ pin and the RESET_OCCURRED flag.	0x0	R/W

Command Register

Address: 0x74, Reset: 0x0000, Name: CMD_KEY

This register is used to issue commands to the part, that is, software reset, fuse upload, and configuration lock.

Table 76. Bit Descriptions for CMD_KEY Register

Bits	Bit Name	Description	Reset	Access
[15:0]	CMD_KEY	Enter a Key to Execute a Command. 0x15FA: Software Reset Key1. To trigger a Software Reset, write this key followed by Software Reset Key2. The SPI writes must be back-to-back. 0xAF51: Software Reset Key2. To trigger a Software Reset, write Software Reset Key1 followed by this key. The SPI writes must be back-to-back.	0x0	W

REGISTER MAP

Table 76. Bit Descriptions for CMD_KEY Register (Continued)

Bits	Bit Name	Description	Reset	Access
		0x1C7D: DAC Update Key. A DAC update is triggered on all channels when this key is entered.		

Broadcast Write Register

Address: 0x75, Reset: 0x0000, Name: BROADCAST_CMD_KEY

Table 77. Bit Descriptions for BROADCAST_CMD_KEY Register

Bits	Bit Name	Description	Reset	Access
[15:0]	BROADCAST_CMD_KEY	Broadcast Write. 0x1a78: Broadcast Software Reset Key1. 0xd203: Broadcast Software Reset Key2. Note that to issue a Software Reset, the Key1 and Key2 commands must be back-to-back SPI broadcast writes. 0x964e: Broadcast DAC Update Key. The contents of the DAC.	0x0	W

Scratch or Spare Register

Address: 0x76 to 0x79 (Increments of 1), Reset: 0x0000, Name: SCRATCHn

Table 78. Bit Descriptions for SCRATCHn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	SCRATCH_BITS	Scratch or Spare Register Field.	0x0	R/W

Generic ID Register

Address: 0x7A, Reset: 0x0000, Name: GENERIC_ID

Table 79. Bit Descriptions for GENERIC_ID Register

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GENERIC_ID	Generic Identification. AD74416H ID: 0b110 = 6	0x0	R

Silicon Revision Register

Address: 0x7B, Reset: 0x0002, Name: SILICON_REV

Table 80. Bit Descriptions for SILICON_REV Register

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	SILICON_REV_ID	Silicon Revision Identification.	0x2	R

Silicon ID 0 Register

Address: 0x7D, Reset: 0x0000, Name: SILICON_ID0

Table 81. Bit Descriptions for SILICON_ID0 Register

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
[6:0]	UID0	Unique Identifier 0.	0x0	R

REGISTER MAP

Silicon ID 1 Register

Address: 0x7E, Reset: 0x0000, Name: SILICON_ID1

Table 82. Bit Descriptions for SILICON_ID1 Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
[11:6]	UID2	Unique Identifier 2.	0x0	R
[5:0]	UID1	Unique Identifier 1.	0x0	R

REGISTER MAP

HART MODEM REGISTERS

The following registers (Address 0x80 to Address 0xC4) are HART modem configuration registers.

HART Communications Alert Register

Address: 0x80 to 0xB0 (Increments of 16), Reset: 0x0020, Name: HART_ALERT_STATUSn

Table 83. Bit Descriptions for HART_ALERT_STATUSn Register

Bits	Bit Name	Description	Reset	Access
[15:13]	FRM_MON_STATE	HART Frame Monitor State. This field indicates the current state of the frame monitor. 000: Receiving preamble bytes. 001: Receiving address bytes. 010: Receiving expansion bytes. 011: Receiving command byte. 100: Receiving frame size byte. 101: Receiving payload data. 110: Receiving the check byte.	0x0	R
12	EOM	End of Message/Frame Detected. This bit asserts when all of a frame is received up to and including the check byte. If there is a gap error in the received frame, then the EOM bit does not assert. A parity error or frame error in one of the received bytes does not prevent this bit from asserting, except if the error is in the byte count byte. Write 1 to clear this bit.	0x0	R/W1C
11	RX_BCNT	Received the HART Frame Header up to the Byte Count. The RX FIFO contains the header of a frame. This bit asserts when the frame header up to the byte count is received. A gap error in the received bytes prevents this bit from asserting. A parity error or frame error in the byte count byte also prevents this bit from asserting. A parity error or frame error in any other received byte does not prevent this bit from asserting. Write 1 to clear this bit.	0x0	R/W1C
10	RX_CMD	Received the HART Frame Header up to the Command Byte. The RX FIFO contains the header of a frame. This bit asserts when the frame header up to the command byte is received. A gap error in the received bytes prevents this bit from asserting. A parity error or frame error in one of the received bytes does not prevent this bit from asserting. Write 1 to clear this bit.	0x0	R/W1C
9	SOM	Start of Message/Frame Detected. The RX FIFO contains the header of a frame. This bit asserts when at least 2 preamble bytes and a delimiter are received and there are no errors in the received bytes. Write 1 to clear this bit.	0x0	R/W1C
8	CD	Carrier Detect. This bit directly reflects the CD signal. It does not drive $\overline{\text{ALERT}}$ and, therefore, does not have a corresponding ALERT_HART_MASK bit.	0x0	R
7	CD_EDGE_DET	Carrier Detect Status. Use this bit to detect edges on the CD bit. CD_EDGE_SEL[1:0] is used to determine if a falling, rising, or any edge on CD asserts this bit. After changing CD_EDGE_SEL, the next selected edge (rising or falling) causes this bit to assert.	0x0	R/W1C
6	TX_COMPLETE	Transmission completes. This bit asserts when the Tx Engine has finished transmitting the last bit of a byte and there are no more bytes in the Tx FIFO.	0x0	R/W1C
5	TX_FIFO_ALERT	The configured transmit FIFO threshold is reached. This bit asserts when the number of bytes in the TX FIFO is less than or equal to the value configured in COMFCR.TFTRIG. If COMFCR.TFTRIG = 0, then this bit indicates when the FIFO is empty. As the FIFO is empty on power up and COMFCR.TFTRIG powers up to 8, this bit is 1 on power up. It deasserts when greater than TFTRIG bytes are written to the Tx FIFO.	0x1	R
4	RX_FIFO_ALERT	The configured receive FIFO threshold is reached.	0x0	R
3	RX_OVERFLOW_ERR	Rx FIFO Overflow. A received byte was not written to the receive FIFO as it is full.	0x0	R/W1C
2	FRAME_ERR	Received a Frame Error. This bit asserts when a frame error is detected in a received character. Write 1 to clear this bit.	0x0	R/W1C
1	PARITY_ERR	Received a Parity Error. This bit asserts when a parity error is detected in a received byte. Write 1 to clear this bit.	0x0	R/W1C

REGISTER MAP

Table 83. Bit Descriptions for HART_ALERT_STATUSn Register (Continued)

Bits	Bit Name	Description	Reset	Access
0	GAP_ERR	Gap Error. This bit asserts when there is a gap between characters of 1 character time (9ms) or more. This may assert at the end of frame but is not guaranteed to assert at the end of a frame. That is, there may not be a gap of 1 character between frames. Write 1 to clear this bit.	0x0	R/W1C

HART Communications Receive Register

Address: 0x81 to 0xB1 (Increments of 16), Reset: 0x0000, Name: HART_RXn

The receive FIFO is read by this register.

It is possible to burst read the contents of the Rx FIFO over SPI. If the burst read is started at this register, then internally, the logic does not increment to the next address. Instead, it stays at the address of the HART_RX register and repeatedly returns characters from the Rx FIFO.

When the address of this register is written to the READ_SELECT register, then the clock to the HART UART logic is automatically enabled. Therefore, when finished using the UART, write any address other than HART_RX to the READ_SELECT register to disable the clock to the UART and save power.

Table 84. Bit Descriptions for HART_RXn Register

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	RFGI	GAP Indicator. RXD is detected high for at least a character time (11 bits) since the last character is received. This indicates that there is a gap before this character. RFGI does not set in the 1st word of the 1st frame received after exiting reset. It is asserted at the start of all subsequent frames received if the frames are preceded by a gap.	0x0	R
10	RFFE	Frame Error Associated to Current Byte at Top of Rx FIFO.	0x0	R
9	RFPE	Parity Error Associated to Current Byte at Top of Rx FIFO.	0x0	R
8	RFBI	Break Indicator. RXD is detected low for a character time (11 bits). This indicates that a break associated with the byte at top of Rx FIFO.	0x0	R
[7:0]	RBR	Receive Buffer Register. Reading this register returns the character at the top of the receive FIFO and pops the entry from the FIFO.	0x0	R

HART Communications Transmit Register

Address: 0x82 to 0xB2 (Increments of 16), Reset: 0x0000, Name: HART_TXn

The transmit FIFO is written by this register.

Table 85. Bit Descriptions for HART_TXn Register

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	TDR	Transmit Data Register. Writing to this register adds a byte to the TX FIFO.	0x0	W

FIFO Control Register

Address: 0x83 to 0xB3 (Increments of 16), Reset: 0x08C1, Name: HART_FCRn

Table 86. Bit Descriptions for HART_FCRn Register

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
[12:8]	TFTRIG	Tx FIFO Trigger Level. Sets the Tx FIFO level to trigger an interrupt. When the Tx FIFO fill level is less than or equal to the configured level, the ALERT_HART_STATUS.TX_FIFO_ALERT goes to 1.1 ≥ 1 byte, and 2 ≥ 2 bytes.	0x8	R/W

REGISTER MAP

Table 86. Bit Descriptions for HART_FCRn Register (Continued)

Bits	Bit Name	Description	Reset	Access
[7:3]	RFTRIG	Rx FIFO Trigger Level. Sets the Rx FIFO level to trigger an interrupt. When the Rx FIFO fill level is greater than or equal to the configured level, the ALERT_HART_STATUS.RX_FIFO_ALERT goes to 1.1 => 1 byte, and 2 => 2 bytes.	0x18	R/W
2	TFCLR	Clear the Transmit FIFO. If the UART TxFIFO is cleared while frame transmission is in progress, then the host software must wait until HART_ALERT_STATUS.TX_COMPLETE asserts before attempting to transmit another frame. That is, the host software must not write to the Tx FIFO (HART_TX.TDR) until TX_COMPLETE asserts. Otherwise, the next frame is transmitted without a preamble if HART_CONFIG.TX_PREM_CNT is non zero. Alternatively, write 0x0 to HART_CONFIG.TX_PREM_CNT and proceed to write the preamble bytes and the next frame to the Tx FIFO. In this case after writing to the FIFO, check if TX_COMPLETE has asserted. If it has, then RTS must be set again to start frame transmission. If TX_COMPLETE has not asserted, then frame transmission continues as normal.	0x0	W
1	RFCLR	Clear the Receive FIFO.	0x0	W
0	FIFOEN	FIFO Enable.	0x1	R/W

HART UART Tx Control Register

Address: 0x84 to 0xB4 (Increments of 16), Reset: 0x0000, Name: HART_MCRn

Table 87. Bit Descriptions for HART_MCRn Register

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	RTS	Request to Send.	0x0	R/W

RX FIFO Byte Count Register

Address: 0x85 to 0xB5 (Increments of 16), Reset: 0x0000, Name: HART_RFCn

Table 88. Bit Descriptions for HART_RFCn Register

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	RFC	The Number of Characters in the Receive FIFO. The Rx FIFO is has a depth of 32 characters.	0x0	R

TX FIFO Byte Count Register

Address: 0x86 to 0xB6 (Increments of 16), Reset: 0x0000, Name: HART_TFCn

Table 89. Bit Descriptions for HART_TFCn Register

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	TFC	The Number of Bytes in the Transmit FIFO. The Tx FIFO has a depth of 32 bytes.	0x0	R

HART Communications Alert Mask Registers

Address: 0x87 to 0xB7 (Increments of 16), Reset: 0x1EFF, Name: HART_ALERT_MASKn

These registers are used to mask particular status bits from activating the HART_ALERT_A/B/C/D status bits in ALERT_STATUS register.

The position of mask bits in this register line up the corresponding status bits in the HART_ALERT_STATUS register.

To mask a particular field, set the corresponding mask bit to 1.

REGISTER MAP

Table 90. Bit Descriptions for HART_ALERT_MASKn Register

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	EOM_MASK	Mask Bit for EOM.	0x1	R/W
11	RX_BCNT_MASK	Mask Bit for RX_BCNT.	0x1	R/W
10	RX_CMD_MASK	Mask Bit for RX_CMD.	0x1	R/W
9	SOM_MASK	Mask Bit for SOM.	0x1	R/W
8	RESERVED	Reserved.	0x0	R
7	CD_EDGE_DET_MASK	Mask Bit for CD_EDGE.	0x1	R/W
6	TX_COMPLETE_MASK	Mask Bit for TX_COMPLETE.	0x1	R/W
5	TX_FIFO_ALERT_MASK	Mask Bit for TX_FIFO_ALERT.	0x1	R/W
4	RX_FIFO_ALERT_MASK	Mask Bit for RX_FIFO_ALERT.	0x1	R/W
3	RX_OVERFLOW_ERR_MASK	Mask Bit for RX_OVERFLOW_ERR.	0x1	R/W
2	FRAME_ERR_MASK	Mask Bit for FRAME_ERR.	0x1	R/W
1	PARITY_ERR_MASK	Mask Bit for PARITY_ERR.	0x1	R/W
0	GAP_ERR_MASK	Mask Bit for GAP_ERR.	0x1	R/W

HART Support Configuration Register

Address: 0x88 to 0xB8 (Increments of 16), Reset: 0x0C30, Name: HART_CONFIGn

Table 91. Bit Descriptions for HART_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	CD_EXTD_QUAL	Enable an Extended Qualification of the CD Signal. By default, CD asserts when the carrier reaches an energy level. Setting this field to 1 enables an additional qualification of the carrier signal. In addition, four zero-crossing points must be detected before CD asserts. This adds an additional 2-bit times of latency to the assertion of the CD bit.	0x0	R/W
12	FRM_MON_RX_PREMX2	Require the Frame Monitor to Receive two Preamble Bytes. By default, the protocol monitor looks to receive only 1 byte of preamble to identify the start of a frame. Set this field to 1 to require the protocol monitor receive two preamble bytes. At the physical layer, if the modem receives 2 bytes of preamble (possibly preceded by corrupted bytes), then the 1st byte of preamble is dropped/corrupted as at least two preamble bytes are needed to synchronize the received bit stream to a valid start bit. So the protocol monitor may only see one good preamble byte, hence this field is defaulted to 0. 0: Frame monitor looks for only one Preamble Byte. 1: Frame monitor requires two Preamble Bytes.	0x0	R/W
11	FRM_MON_RST_GAP	Enable Reset of the Frame Monitor If a GAP is Detected. 0: Frame monitor is not reset on detecting a GAP. The frame monitor state machine is not reset if a GAP is detected. 1: Frame monitor is reset on detecting a GAP. The frame monitor state machine is reset to the PREAMBLE state if a gap is detected.	0x1	R/W
10	FRM_MON_RST_CD	Enable Reset of the Frame Monitor If CD is Low. 0: Frame monitor is not reset on CD low. The frame monitor state machine is not reset when CD goes low. 1: Frame monitor is reset on CD low. The frame monitor state machine is reset to the PREAMBLE state when CD goes low.	0x1	R/W
9	RX_ALL_CHARS	Write All Characters Received into the Rx FIFO. If 0 and FRM_MON_EN is also set, then only valid characters from a frame (as determined by the frame monitor) are written to the Rx FIFO. If 1 all characters received are written to the Rx FIFO.	0x0	R/W
8	FRM_MON_EN	Enable the HART Frame Monitor State Machine. If FRM_MON_EN is set, then only valid characters from a frame (as determined by the frame monitor) are written to the Rx FIFO.	0x0	R/W

REGISTER MAP

Table 91. Bit Descriptions for HART_CONFIGn Register (Continued)

Bits	Bit Name	Description	Reset	Access
		Characters are not written into the receive FIFO until two or more good preamble bytes are received first. That is the delimiter field is the first byte of a frame written to the receive FIFO.		
[7:6]	EVENT_DET_SEL	Select an EOM or SOM to Start the EVENT_DET_TIME Counter. 00: Start the event counter on detecting an EOM on receive. 01: Start the event counter on detecting an SOM on receive. 10: Start the event counter on detecting Tx complete. 11: Start the event counter on detecting an edge on CD. As configured by CD_EDGE_SEL.	0x0	R/W
5	TX_1B_AFTER_RTS	Start Transmission 1-Bit Time After RTS is Set. If 1, then frame transmission starts 1-bit time (at 1200baud) after RTS is asserted and there is data in the Tx FIFO. This gives the receiving modem 1-bit time to enable the carrier. If 0, then frame transmission starts immediately when data is written to the TX FIFO, irrespective of the value on RTS.	0x1	R/W
4	AUTO_CLR_RTS	Auto Clear RTS. If 1, then when frame transmission completes (that is, the last word in the Tx FIFO is transmitted) the RTS signal is automatically deasserted and HART_MCR.RTS goes to 0. If 0, then the HART_MCR.RTS does not go to 0 at the end of frame transmission and the RTS signal stays asserted. In this case, software must deasserts the RTS signal by writing 0 to HART_MCR.RTS.	0x1	R/W
[3:2]	CD_EDGE_SEL	Carrier Detect Edge Detect Select. 00: Detect a falling edge. 01: Detect a rising edge. 10: Detect any edge. 11: Edges detect disable.	0x0	R/W
1	MODEM_DUPLEX	Enables the HART Modem in Duplex Mode. This allows to loopback testing of the modem.	0x0	R/W
0	MODEM_PWRUP	Powers up the HART Modem.	0x0	R/W

HART Transmit Preamble Count Register

Address: 0x89 to 0xB9 (Increments of 16), Reset: 0x0005, Name: HART_TX_PREMn

Table 92. Bit Descriptions for HART_TX_PREMn Register

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
[4:0]	TX_PREM_CNT	Tx Preamble Count. Indicates that the number of preamble bytes to transmit at the start of a frame. If 0, then preamble bytes must be written directly to the Tx FIFO.	0x5	R/W

HART Event Detected Time Register

Address: 0x8A to 0xBA (Increments of 16), Reset: 0x0000, Name: HART_EVDETn

Table 93. Bit Descriptions for HART_EVDETn Register

Bits	Bit Name	Description	Reset	Access
[15:0]	EVENT_DET_TIME	Elapsed time since an event is detected. Indicates that the time since an Rx EOM, Rx SOM, CD edge, or TX_COMPLETE are detected. The counter increments in steps of 3.255μS (307.2kHz). The counter starts incrementing on detecting an EOM, SOM, CD edge (see EVENT_DET_SEL), or TX_COMPLETE. It increments until it reaches 0xFFFF. It stays at 0xFFFF until another event is detected. The maximum duration that the counter can measure is 213ms.The counter is cleared if FRM_MON_EN is 0.This counter allows the software more accurately determine when HART frames started or ended.	0x0	R

REGISTER MAP

Per Channel HART Reset Register

Address: 0x8C to 0xBC (Increments of 16), Reset: 0x0000, Name: HART_CH_RESETn

Table 94. Bit Descriptions for HART_CH_RESETn Register

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	HRST	HART Channel Reset. Setting this field to 1 resets the HART Tx and Rx paths in the modem, the UART, and the HART registers for a channel. After writing this field to 1, it must then be written to 0 to release reset to the HART logic for a channel.	0x0	R/W

Configure the GPIO Pins to Interface to the Modem or UART Register

Address: 0xC0, Reset: 0x0000, Name: HART_GPIO_IF_CONFIG

Use four GPIO pins to interface to either the modem or the UART. Configure the GPIO pins to interface to only one channel at a time.

Table 95. Bit Descriptions for HART_GPIO_IF_CONFIG Register

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:2]	HART_GPIO_IF_CH	Select the HART Channel to Interface to by the GPIO Pins. 00: Select Channel A. 01: Select Channel B. 10: Select Channel C. 11: Select Channel D.	0x0	R/W
[1:0]	HART_GPIO_IF_SEL	Configure Four GPIO Pins to Interface to the Modem or UART. This register takes priority over the GPIO_CONFIG and HART_GPIO_MON_CONFIG registers. If set to SEL_IF_MODEM or SEL_IF_UART, then settings in the GPIO_CONFIG and HART_GPIO_MON_CONFIG are overridden. If this field is programmed to 0x3, then the GPIO pins are not connected to the HART Modem or UART. 00: GPIO pins are not connected to the HART modem or UART. 01: Interface to the HART modem by four GPIO pins. HART_GPIO_CH determines which channel's modem is connected to the GPIO pins. In this mode, the internal SPI to UART interface is disabled and the GPIO pins are used to interface to the HART Modem. GPIO A: CD Output, GPIO B: RXD Output, GPIO C: TXD Input, GPIO D: RTS Input, this option is used for conformance testing of the modem. 10: Interface to the UART by four GPIO pins. HART_GPIO_IF_CH determines which channel's UART is connected to the GPIO pins. GPIO A: CD Input, GPIO B: RXD Input, GPIO C: TXD Output, GPIO D: RTS Output, this option is used to test the software interface to the UART by the GPIO pins. When this option is selected, note that the RTS and TXD signals to the modem are held at 0.	0x0	R/W

Configure a GPIO Pin to Monitor a HART Signal Register

Address: 0xC1 to 0xC4 (Increments of 1), Reset: 0x0000, Name: HART_GPIO_MON_CONFIGn

A register per GPIO pin for four GPIO pins is provided to separately configure each GPIO pin to monitor one of four UART interface signals or monitor one of three HART status bits.

HART_GPIO_MON_CONFIG[0] : Use to configure GPIO_A.

HART_GPIO_MON_CONFIG[1] : Use to configure GPIO_B.

HART_GPIO_MON_CONFIG[2] : Use to configure GPIO_C.

HART_GPIO_MON_CONFIG[3] : Use to configure GPIO_D.

REGISTER MAP

Table 96. Bit Descriptions for HART_GPIO_MON_CONFIGn Register

Bits	Bit Name	Description	Reset	Access
[15:5]	RESERVED	Reserved.	0x0	R
[4:3]	HART_GPIO_MON_CH	Configure the Channel for a GPIO Pin to Monitor. Use in conjunction with HART_GPIO_MON_SEL. 00: Select Channel A. 01: Select Channel B. 10: Select Channel C. 11: Select Channel D.	0x0	R/W
[2:0]	HART_GPIO_MON_SEL	Configure a GPIO Pin to Monitor a Signal in the HART Logic. Use in conjunction with HART_GPIO_MON_CH. This register takes priority over a GPIO_CONFIG[n] register for a pin. If set to anything other than MON_NONE then settings in the corresponding GPIO_CONFIGn] register are overridden. 0: No monitoring on this GPIO pin. 1: Monitor the CD signal. 2: Monitor the RXD signal. 3: Monitor the TXD signal. 4: Monitor the RTS signal. 5: Monitor HART_ALERT_STATUS[n].EOM. 6: Monitor HART_ALERT_STATUS[n].SOM. 7: Monitor HART_ALERT_STATUS[n].TX_COMPLETE.	0x0	R/W

OUTLINE DIMENSIONS

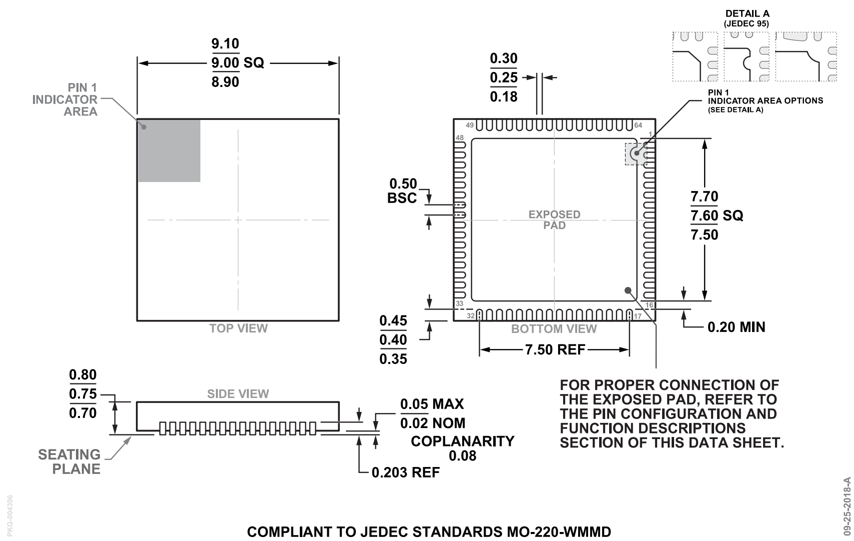

Figure 62. 64-Lead Lead Frame Chip-Scale Package [LFCSP]
9mm × 9mm Body and 0.75mm Package Height
(CP-64-15)
Dimensions Shown in millimeters

Updated: March 31, 2025

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD74416HBCPZ	−40°C to +105°C	64-Lead Lead Frame Chip-Scale Package [LFCSP]	Tray, 260	CP-64-15
AD74416HBCPZ-RL7	−40°C to +105°C	64-Lead Lead Frame Chip-Scale Package [LFCSP]	Reel7, 750	CP-64-15

[1] Z = RoHS-Compliant Part.

EVALUATION BOARDS

Evaluation Board[1]	Description
EV-AD74416H-ARDZ	Evaluation Board

[1] Z = RoHS-Compliant Part.