

FEATURES

Supports defense and aerospace applications (AQEC standard)

Military temperature range (-55°C to $+125^{\circ}\text{C}$)

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available on request

Enhanced replacement for LF412 and TL082

AC performance

Settles to $\pm 0.01\%$ in $1.0\ \mu\text{s}$

$16\ \text{V}/\mu\text{s}$ minimum slew rate

$3\ \text{MHz}$ minimum unity-gain bandwidth

DC performance

$150\ \text{V}/\text{mV}$ minimum open-loop gain

Available in a SOIC_N package

GENERAL DESCRIPTION

The AD712-EP is a high speed, precision, monolithic operational amplifier offering high performance over the military temperature range of -55°C to $+125^{\circ}\text{C}$. Its low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFET or bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of $16\ \text{V}/\mu\text{s}$ and a settling time of $1\ \mu\text{s}$ to $\pm 0.01\%$, the AD712-EP is ideal as a buffer for 12-bit digital-to-analog converters (DACs) and 12-bit analog-to-digital converters (ADCs) and as a high speed integrator.

CONNECTION DIAGRAM

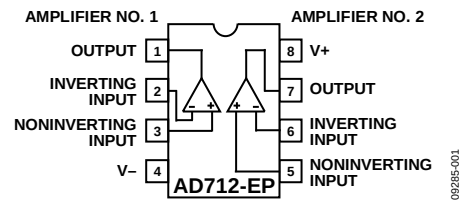


Figure 1. 8-Lead SOIC_N (R-Suffix)

The combination of excellent noise performance and low input current also make the AD712-EP useful for photodiode preamps. Common-mode rejection of 88 dB and open-loop gain of $400\ \text{V}/\text{mV}$ ensure 12-bit performance even in high speed unity-gain buffer circuits.

The AD712-EP is available in an 8-lead SOIC_N package.

Additional applications information is available in the [AD712](#) data sheet.

Rev. 0

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REVISION HISTORY

8/10—Revision 0: Initial Version

SPECIFICATIONS

$V_S = \pm 15\text{ V}$ @ $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
INPUT OFFSET VOLTAGE¹				
Initial Offset		0.3	3	mV
T_{MIN} to T_{MAX}			4	mV
vs. Temperature		7	20	$\mu\text{V}/^\circ\text{C}$
vs. Supply	76	95		dB
T_{MIN} to T_{MAX}	76			dB
Long-Term Offset Stability		15		$\mu\text{V}/\text{month}$
INPUT BIAS CURRENT²				
$V_{\text{CM}} = 0\text{ V}$		25	75	pA
$V_{\text{CM}} = 0\text{ V}$ @ T_{MAX}		26	77	nA
$V_{\text{CM}} = \pm 10\text{ V}$			100	pA
INPUT OFFSET CURRENT				
$V_{\text{CM}} = 0\text{ V}$		10	25	pA
$V_{\text{CM}} = 0\text{ V}$ @ T_{MAX}		11	26	nA
MATCHING CHARACTERISTICS				
Input Offset Voltage			3	mV
T_{MIN} to T_{MAX}			4	mV
Input Offset Voltage Drift			20	$\mu\text{V}/^\circ\text{C}$
Input Bias Current			25	pA
Crosstalk				
At $f = 1\text{ kHz}$		120		dB
At $f = 100\text{ kHz}$		90		dB
FREQUENCY RESPONSE				
Small Signal Bandwidth	3.0	4.0		MHz
Full Power Response		200		kHz
Slew Rate	16	20		V/ μs
Settling Time to 0.01%		1.0	1.2	μs
Total Harmonic Distortion		0.0003		%
INPUT IMPEDANCE				
Differential		$3 \times 10^{12} 5.5$		ΩpF
Common Mode		$3 \times 10^{12} 5.5$		ΩpF
INPUT VOLTAGE RANGE				
Differential ³		± 20		V
Common-Mode Voltage ⁴		$+14.5, -11.5$		V
T_{MIN} to T_{MAX}	$-V_S + 4$		$+V_S - 2$	V
Common-Mode Rejection Ratio				
$V_{\text{CM}} = \pm 10\text{ V}$	76	88		dB
T_{MIN} to T_{MAX}	76	84		dB
$V_{\text{CM}} = \pm 11\text{ V}$	70	84		dB
T_{MIN} to T_{MAX}	70	80		dB
INPUT VOLTAGE NOISE				
0.1 Hz to 10 Hz		2		$\mu\text{V p-p}$
$f = 10\text{ Hz}$		45		nV/ $\sqrt{\text{Hz}}$
$f = 100\text{ Hz}$		22		nV/ $\sqrt{\text{Hz}}$
$f = 1\text{ kHz}$		18		nV/ $\sqrt{\text{Hz}}$
$f = 10\text{ kHz}$		16		nV/ $\sqrt{\text{Hz}}$
INPUT CURRENT NOISE				
$f = 1\text{ kHz}$		0.01		pA/ $\sqrt{\text{Hz}}$

AD712-EP

Parameter	Min	Typ	Max	Unit
OPEN-LOOP GAIN	150			V/mV
T_{MIN} to T_{MAX}	100			V/mV
OUTPUT CHARACTERISTICS				
Output Voltage Swing High		13.9	13.0	V
T_{MIN} to T_{MAX}			12.0	V
Output Voltage Swing Low	-12.5	-13.1		V
T_{MIN} to T_{MAX}	-12.0			V
Current		25		mA
POWER SUPPLY				
Rated Performance		±15		V
Operating Range	±4.5		±18	V
Quiescent Current		5.0	6.8	mA

¹ Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = 25^\circ\text{C}$.

² Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = 25^\circ\text{C}$. For higher temperatures, the current doubles every 10°C .

³ Defined as voltage between inputs, such that neither exceeds ± 10 V from ground.

⁴ Typically exceeding -14.1 V negative common-mode voltage on either input results in an output phase reversal.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Internal Power Dissipation ¹	
Input Voltage ²	$\pm 18\text{ V}$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range	-65°C to $+125^{\circ}\text{C}$
Operating Temperature Range	-55°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering 60 sec)	300°C

¹ Thermal characteristics: 8-lead SOIC_N, $\theta_{JA} = 100^{\circ}\text{C}$.

² For supply voltages less than $\pm 18\text{ V}$, the absolute maximum voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

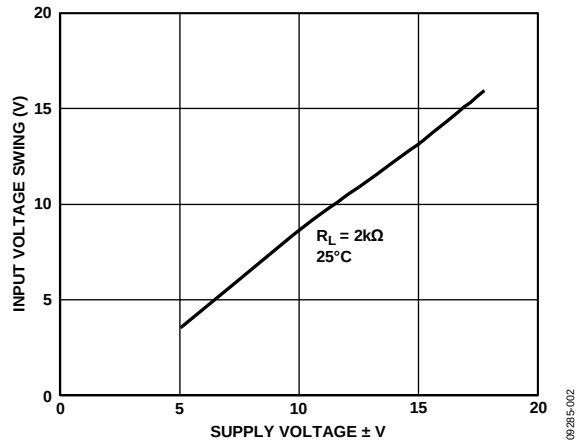


Figure 2. Input Voltage Swing vs. Supply Voltage

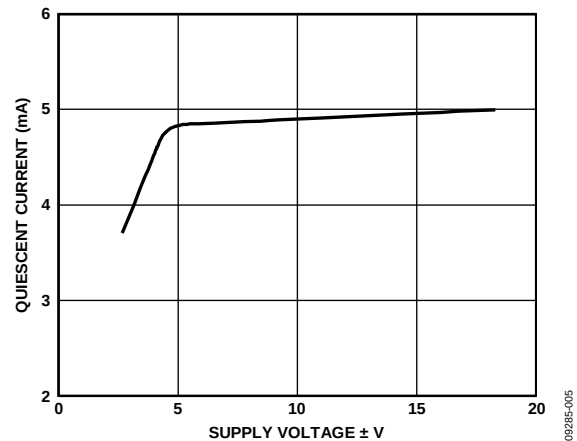


Figure 5. Quiescent Current vs. Supply Voltage

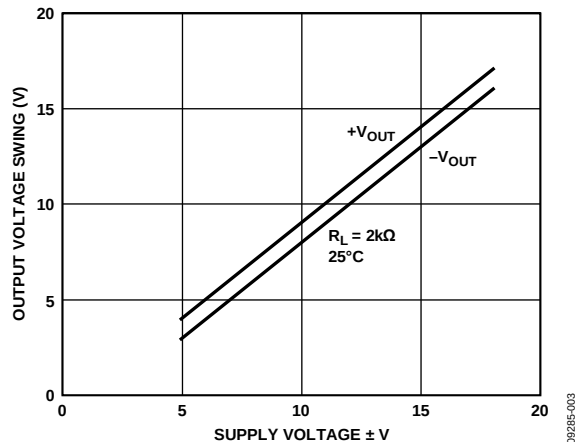


Figure 3. Output Voltage Swing vs. Supply Voltage

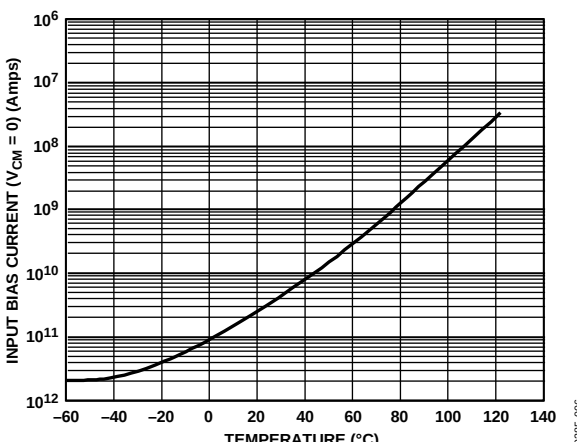


Figure 6. Input Bias Current vs. Temperature

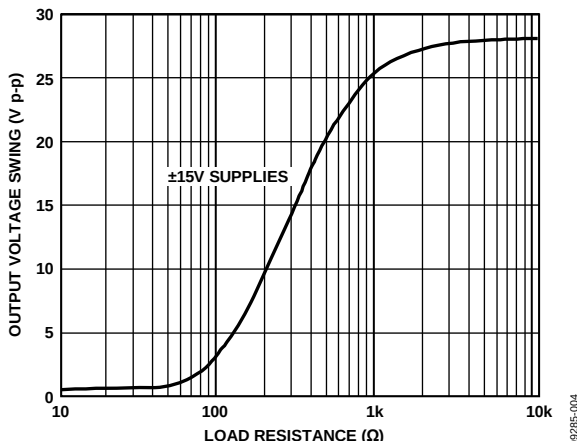


Figure 4. Output Voltage Swing vs. Load Resistance

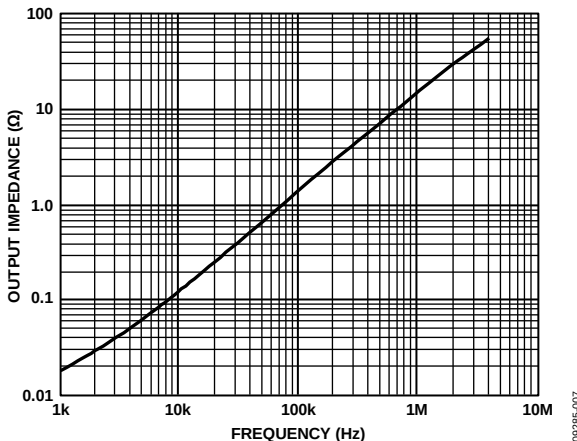


Figure 7. Output Impedance vs. Frequency

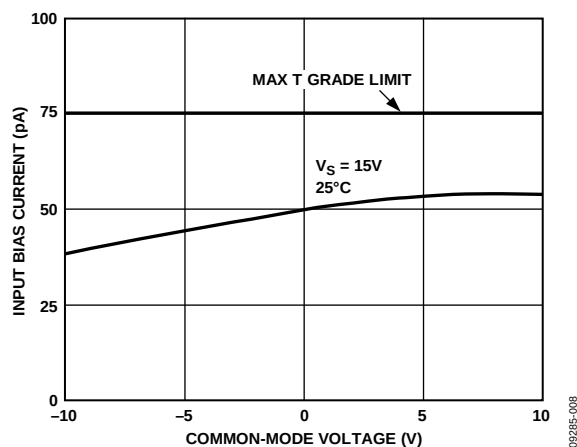


Figure 8. Input Bias Current vs. Common-Mode Voltage

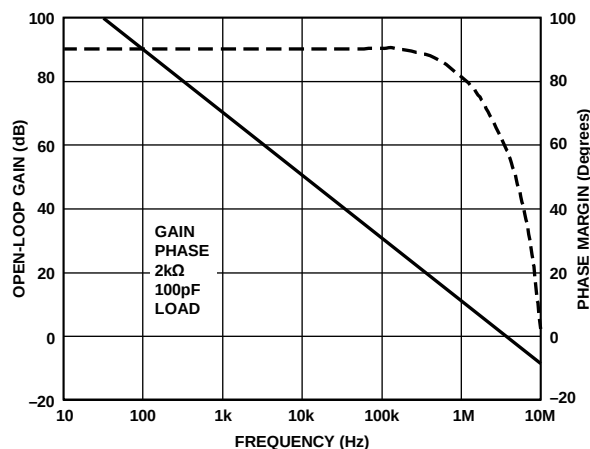


Figure 11. Open-Loop Gain and Phase Margin vs. Frequency

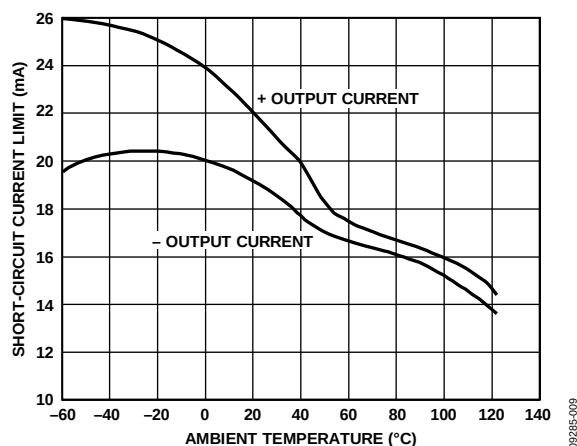


Figure 9. Short-Circuit Current Limit vs. Temperature

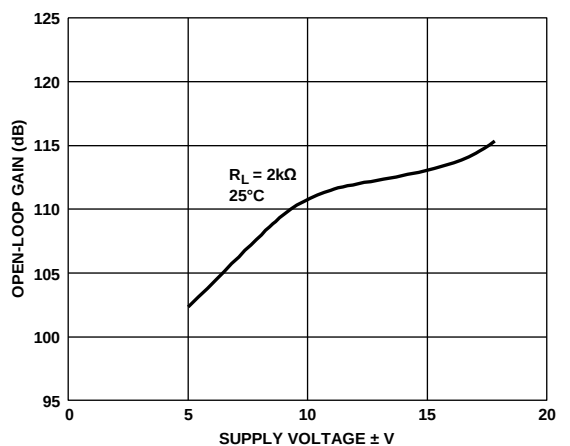


Figure 12. Open-Loop Gain vs. Supply Voltage

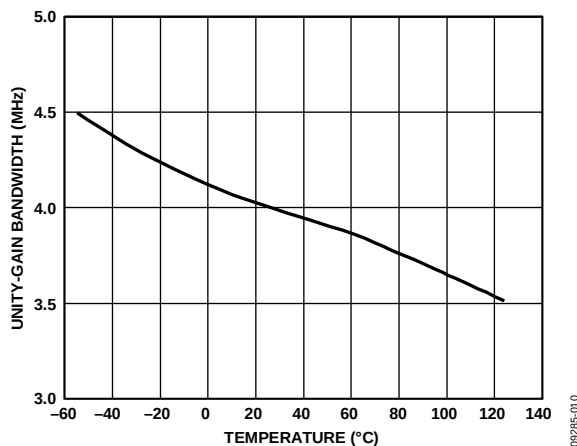


Figure 10. Unity-Gain Bandwidth vs. Temperature

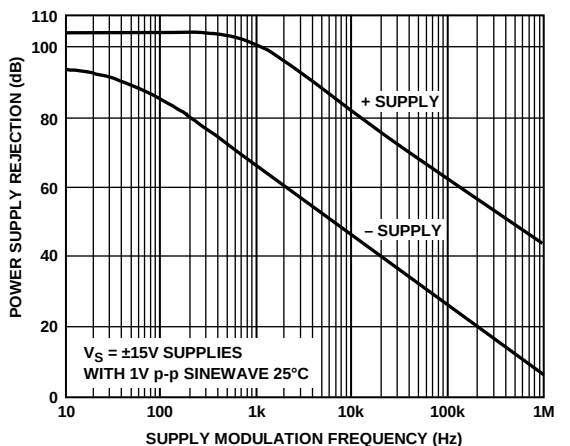


Figure 13. Power Supply Rejection vs. Frequency

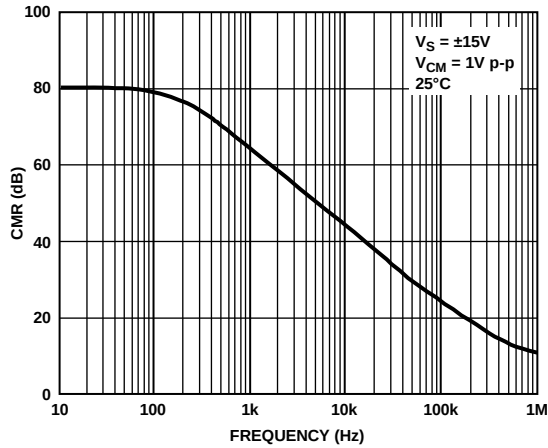


Figure 14. Common-Mode Rejection (CMR) vs. Frequency

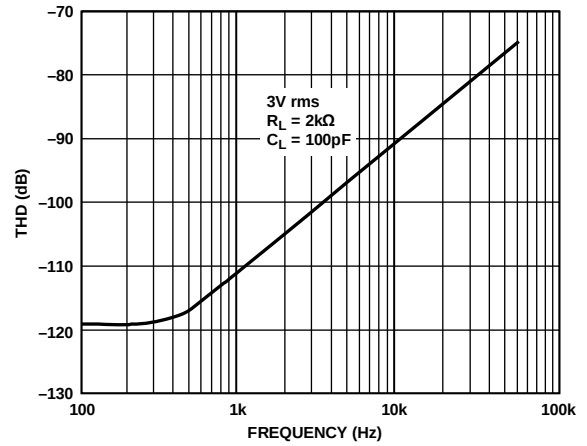


Figure 17. Total Harmonic Distortion (THD) vs. Frequency

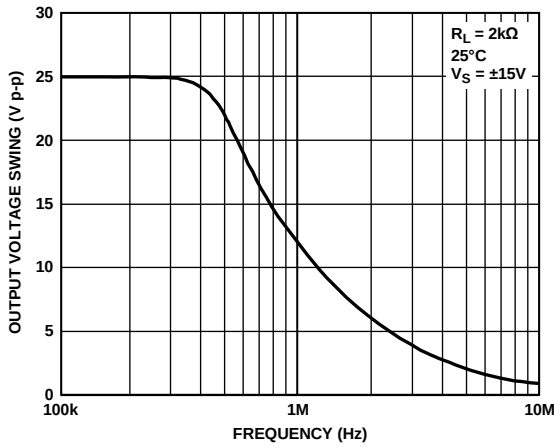


Figure 15. Large Signal Frequency Response

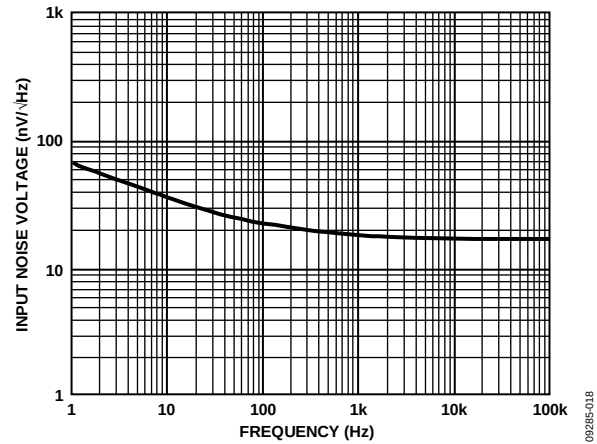


Figure 18. Input Noise Voltage Spectral Density

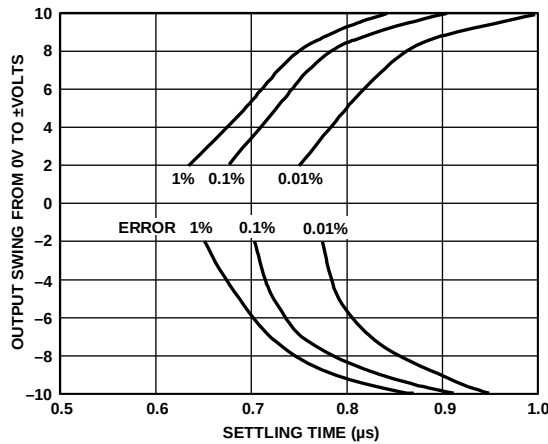


Figure 16. Output Swing and Error vs. Settling Time

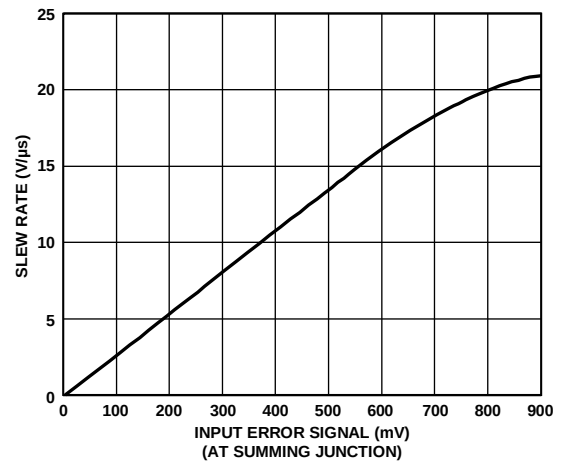


Figure 19. Slew Rate vs. Input Error Signal

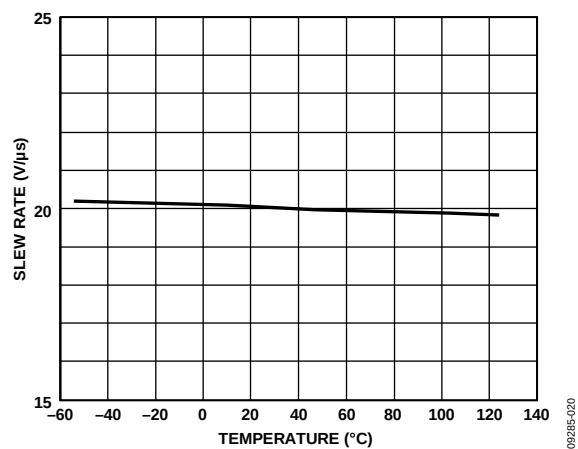
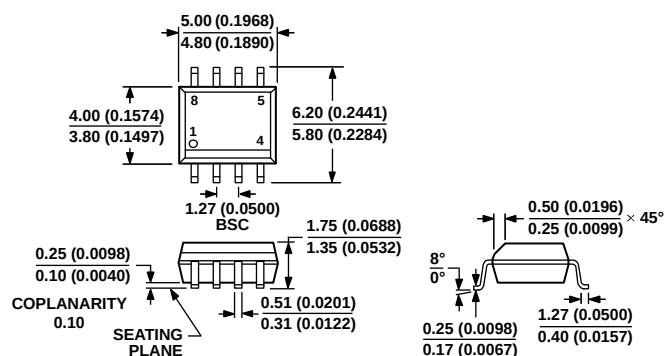


Figure 20. Slew Rate vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 21. 8-Lead Standard Small Outline Package [SOIC_N]

Narrow Body

(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD712TRZ-EP	−55°C to +125°C	8-Lead SOIC_N	R-8
AD712TRZ-EP-R7	−55°C to +125°C	8-Lead SOIC_N	R-8

¹ Z = RoHS Compliant Part.

NOTES

NOTES