

## FEATURES

High relative accuracy (INL):  $\pm 4$  LSB maximum at 16 bits  
 Low drift 2.5 V reference: 4 ppm/°C typical  
 Tiny package: 3 mm  $\times$  3 mm, 16-lead LFCSP  
 Total unadjusted error (TUE):  $\pm 0.1\%$  of FSR maximum  
 Offset error:  $\pm 1.5$  mV maximum  
 Gain error:  $\pm 0.1\%$  of FSR maximum  
 High drive capability: 15 mA, 0.5 V from supply rails  
 User-selectable gain of 1 or 2 (GAIN pin)  
 Reset to zero scale or midscale (RSTSEL pin)  
 1.8 V logic compatibility  
 50 MHz SPI with readback or daisy chain  
 Low glitch: 0.5 nV-sec  
 Low power: 3.3 mW at 3 V  
 2.7 V to 5.5 V power supply

## ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)  
 Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
 Controlled manufacturing baseline  
 1 assembly/test site  
 1 fabrication site  
 Enhanced product change notification  
 Qualification data available on request

## APPLICATIONS

Optical transceivers  
 Base station power amplifiers  
 Process control (PLC input/output cards)  
 Industrial automation  
 Data acquisition systems

## GENERAL DESCRIPTION

The [AD5689R-EP](#), a member of the *nanoDAC+*™ family, is a low power, dual, 16-bit buffered voltage output digital-to-analog converter (DAC). The device includes a 2.5 V, 4 ppm/°C internal reference (enabled by default) and a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). The device operates from a single 2.7 V to 5.5 V supply, is guaranteed monotonic by design, and exhibits less than 0.1% FSR gain error and 1.5 mV offset error performance.

The [AD5689R-EP](#) also incorporates a power-on reset circuit and a RSTSEL pin that ensures that the DAC outputs power up to zero scale or midscale and remains there until a valid write occurs. The device contains a per channel power-down feature that reduces the current consumption of the device to 4  $\mu\text{A}$  at 3 V while in power-down mode.

## FUNCTIONAL BLOCK DIAGRAM

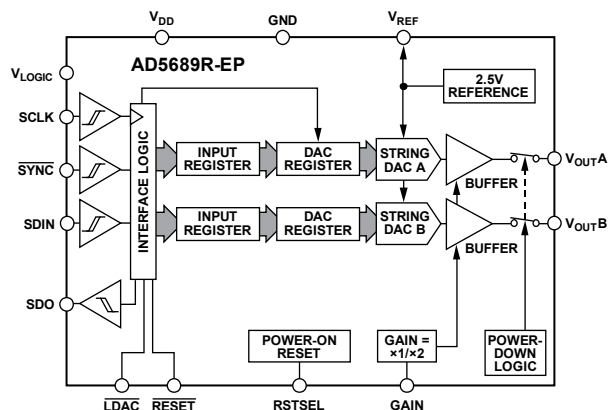


Figure 1.

The [AD5689R-EP](#) uses a versatile serial peripheral interface (SPI) that operates at clock rates up to 50 MHz, and contains a  $V_{\text{LOGIC}}$  pin that is intended for 1.8 V/3 V/5 V logic.

Additional application and technical information can be found in the [AD5689R/AD5687R](#) data sheet.

## PRODUCT HIGHLIGHTS

1. High Relative Accuracy (INL).  
 $\pm 4$  LSB maximum
2. Low Drift 2.5 V On-Chip Reference.  
4 ppm/°C typical temperature coefficient  
13 ppm/°C maximum temperature coefficient

Rev. A

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## REVISION HISTORY

### 11/2016—Rev. 0 to Rev. A

Changed $1.8\text{ V} \leq V_{\text{LOGIC}} \leq 5.5\text{ V}$ to $1.62\text{ V} \leq V_{\text{LOGIC}} \leq 5.5\text{ V}$ .....	Throughout
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### 8/2015—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $1.62\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ ,  $C_L = 200\text{ pF}$ , and all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>STATIC PERFORMANCE<sup>1</sup></b>					
Resolution	16			Bits	
Relative Accuracy		$\pm 1$	$\pm 4$	LSB	Gain = 2
		$\pm 1$	$\pm 5$	LSB	Gain = 1
Differential Nonlinearity (DNL)			$\pm 1$	LSB	Guaranteed monotonic by design
Zero-Code Error		0.4	1.5	mV	All zeros loaded to DAC register
Offset Error		+0.1	$\pm 1.5$	mV	
Full-Scale Error		+0.01	$\pm 0.1$	% of FSR	All ones loaded to DAC register
Gain Error		$\pm 0.02$	$\pm 0.1$	% of FSR	Gain = 2
		$\pm 0.02$	$\pm 0.15$	% of FSR	Gain = 1
Total Unadjusted Error		$\pm 0.01$	$\pm 0.1$	% of FSR	External reference; gain = 2
			$\pm 0.2$	% of FSR	Internal reference; gain = 1
Offset Error Drift <sup>2</sup>		$\pm 1$		$\mu\text{V}/^\circ\text{C}$	
Gain Temperature Coefficient (TC) <sup>2</sup>		$\pm 1$		ppm	Of FSR/ $^\circ\text{C}$
DC Power Supply Rejection Ratio <sup>2</sup>		0.15		mV/V	DAC code = midscale, $V_{DD} = 5\text{ V} \pm 10\%$
DC Crosstalk <sup>2</sup>					
		$\pm 2$		$\mu\text{V}$	Due to single channel, full-scale output change
		$\pm 3$		$\mu\text{V}/\text{mA}$	Due to load current change
		$\pm 2$		$\mu\text{V}$	Due to powering down (per channel)
<b>OUTPUT CHARACTERISTICS<sup>2</sup></b>					
Output Voltage Range	0		$V_{REF}$	V	Gain = 1
	0		$2 \times V_{REF}$	V	Gain = 2, see Figure 28
Capacitive Load Stability		2		nF	$R_L = \infty$
		10		nF	$R_L = 1\text{ k}\Omega$
Resistive Load <sup>3</sup>	1			k $\Omega$	
Load Regulation		80		$\mu\text{V}/\text{mA}$	$5\text{ V} \pm 10\%$ , DAC code = midscale; $-30\text{ mA} \leq I_{OUT} \leq +30\text{ mA}$
		80		$\mu\text{V}/\text{mA}$	$3\text{ V} \pm 10\%$ , DAC code = midscale; $-20\text{ mA} \leq I_{OUT} \leq +20\text{ mA}$
Short-Circuit Current <sup>4</sup>		40		mA	
Load Impedance at Rails <sup>5</sup>		25		$\Omega$	See Figure 28
Power-Up Time		2.5		$\mu\text{s}$	Coming out of power-down mode; $V_{DD} = 5\text{ V}$
<b>REFERENCE OUTPUT</b>					
Output Voltage <sup>6</sup>	2.4975		2.5025	V	At ambient
Reference TC <sup>7,8</sup>		4	13	ppm/ $^\circ\text{C}$	
Output Impedance <sup>2</sup>		0.04		$\Omega$	
Output Voltage Noise <sup>2</sup>		12		$\mu\text{V p-p}$	0.1 Hz to 10 Hz
Output Voltage Noise Density <sup>2</sup>		240		nV/ $\sqrt{\text{Hz}}$	At ambient; $f = 10\text{ kHz}$ , $C_L = 10\text{ nF}$
Load Regulation Sourcing <sup>2</sup>		20		$\mu\text{V}/\text{mA}$	At ambient
Load Regulation Sinking <sup>2</sup>		40		$\mu\text{V}/\text{mA}$	At ambient
Output Current Load Capability <sup>2</sup>		$\pm 5$		mA	$V_{DD} \geq 3\text{ V}$
Line Regulation <sup>2</sup>		100		$\mu\text{V}/\text{V}$	At ambient
Thermal Hysteresis <sup>2</sup>		125		ppm	First cycle
		25		ppm	Additional cycles
<b>LOGIC INPUTS<sup>2</sup></b>					
Input Current			$\pm 2$	$\mu\text{A}$	Per pin
Input Voltage					
Low ( $V_{INL}$ )			$0.3 \times V_{LOGIC}$	V	
High ( $V_{INH}$ )	$0.7 \times V_{LOGIC}$			V	
Pin Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
<b>LOGIC OUTPUTS (SDO)<sup>2</sup></b>					
Output Voltage					
Low ( $V_{OL}$ )			0.4	V	$I_{SINK} = 200 \mu A$
High ( $V_{OH}$ )	$V_{LOGIC} - 0.4$			V	$I_{SOURCE} = 200 \mu A$
Floating State Output Capacitance		4		pF	
<b>POWER REQUIREMENTS</b>					
$V_{LOGIC}$	1.62		5.5	V	
$I_{LOGIC}$			3	$\mu A$	
$V_{DD}$	2.7		5.5	V	Gain = 1
$V_{DD}$	$V_{REF} + 1.5$		5.5	V	Gain = 2
$I_{DD}$					$V_{IH} = V_{DD}$ , $V_{IL} = GND$ , $V_{DD} = 2.7 V$ to $5.5 V$
Normal Mode <sup>9</sup>		0.59	0.7	mA	Internal reference off
		1.1	1.3	mA	Internal reference on at full scale
All Power-Down Modes <sup>10</sup>		1	4	$\mu A$	$-40^{\circ}C$ to $+85^{\circ}C$
			6	$\mu A$	$-55^{\circ}C$ to $+125^{\circ}C$

<sup>1</sup> DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when  $V_{REF} = V_{DD}$  with gain = 1 or when  $V_{REF}/2 = V_{DD}$  with gain = 2. Linearity is calculated using a reduced code range of 256 to 65,280.

<sup>2</sup> Guaranteed by design and characterization; not production tested.

<sup>3</sup> Channel A can have an output current of up to 15 mA. Similarly, Channel B can have an output current of up to 15 mA, up to a junction temperature of 135°C.

<sup>4</sup>  $V_{DD} = 5 V$ . The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature may be exceeded during current limit, but operation above the specified maximum operation junction temperature can impair device reliability.

<sup>5</sup> When drawing a load current at either rail, the output voltage headroom, with respect to that rail, is limited by the 25  $\Omega$  typical channel resistance of the output device. For example, when sinking 1 mA, the minimum output voltage =  $25 \Omega \times 1 mA = 25 mV$  (see Figure 28).

<sup>6</sup> Initial accuracy presolder reflow is  $\pm 750 \mu V$ ; output voltage includes the effects of preconditioning drift. See the [AD5689R/AD5687R](#) data sheet for more information.

<sup>7</sup> Reference is trimmed and tested at two temperatures and is characterized from  $-55^{\circ}C$  to  $+125^{\circ}C$ .

<sup>8</sup> Reference temperature coefficient is calculated as per the box method. See the [AD5689R/AD5687R](#) data sheet for more information.

<sup>9</sup> Interface inactive. Both DACs active. DAC outputs unloaded.

<sup>10</sup> Both DACs powered down.

**AC CHARACTERISTICS**

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ ,  $R_L = 2\text{ k}\Omega$  to GND,  $C_L = 200\text{ pF}$  to GND,  $1.62\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$ , and all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Guaranteed by design and characterization; not production tested.

**Table 2.**

Parameter <sup>1</sup>	Min	Typ	Max	Unit	Test Conditions/Comments <sup>2</sup>
Output Voltage Settling Time		5	8	$\mu\text{s}$	$\frac{1}{4}$ to $\frac{3}{4}$ scale settling to $\pm 2$ LSB
Slew Rate		0.8		$\text{V}/\mu\text{s}$	
Digital-to-Analog Glitch Impulse		0.5		$\text{nV-sec}$	1 LSB change around major carry
Digital Feedthrough		0.13		$\text{nV-sec}$	
Digital Crosstalk		0.1		$\text{nV-sec}$	
Analog Crosstalk		0.2		$\text{nV-sec}$	
DAC-to-DAC Crosstalk		0.3		$\text{nV-sec}$	
Total Harmonic Distortion (THD) <sup>3</sup>		−80		$\text{dB}$	At ambient, $\text{BW} = 20\text{ kHz}$ , $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$
Output Noise Spectral Density (NSD)		300		$\text{nV}/\sqrt{\text{Hz}}$	DAC code = midscale, $10\text{ kHz}$ ; gain = 2
Output Noise		6		$\mu\text{V p-p}$	0.1 Hz to 10 Hz
Signal-to-Noise Ratio (SNR)		90		$\text{dB}$	At ambient, $\text{BW} = 20\text{ kHz}$ , $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$
Spurious Free Dynamic Range (SFDR)		83		$\text{dB}$	At ambient, $\text{BW} = 20\text{ kHz}$ , $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$
Signal-to-Noise-and-Distortion Ratio (SINAD)		80		$\text{dB}$	At ambient, $\text{BW} = 20\text{ kHz}$ , $V_{DD} = 5\text{ V}$ , $f_{OUT} = 1\text{ kHz}$

<sup>1</sup> See the [AD5689R/AD5687R](#) data sheet.

<sup>2</sup> Temperature range is  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , typical at  $25^{\circ}\text{C}$ .

<sup>3</sup> Digitally generated sine wave at  $1\text{ kHz}$ .

## TIMING CHARACTERISTICS

All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ . See Figure 2.  $V_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ ,  $1.62 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$ , and  $V_{REF} = 2.5 \text{ V}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 3.

Parameter <sup>1</sup>	Symbol	1.62 V $\leq V_{LOGIC} < 2.7 \text{ V}$		2.7 V $\leq V_{LOGIC} \leq 5.5 \text{ V}$		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	$t_1$	20		20		ns
SCLK High Time	$t_2$	10		10		ns
SCLK Low Time	$t_3$	10		10		ns
$\overline{\text{SYNC}}$ to SCLK Falling Edge Setup Time	$t_4$	15		10		ns
Data Setup Time	$t_5$	5		5		ns
Data Hold Time	$t_6$	5		5		ns
SCLK Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	$t_7$	10		10		ns
Minimum $\overline{\text{SYNC}}$ High Time	$t_8$	20		20		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{SYNC}}$ Rising Edge (DAC Register Update/s)	$t_9$	870		830		ns
$\overline{\text{SYNC}}$ Falling Edge to SCLK Fall Ignore	$t_{10}$	16		10		ns
$\overline{\text{LDAC}}$ Pulse Width Low	$t_{11}$	15		15		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Rising Edge	$t_{12}$	20		20		ns
$\overline{\text{SYNC}}$ Rising Edge to $\overline{\text{LDAC}}$ Falling Edge	$t_{13}$	30		30		ns
$\overline{\text{LDAC}}$ Falling Edge to $\overline{\text{SYNC}}$ Rising Edge	$t_{14}$	840		800		ns
Minimum Pulse Width Low	$t_{15}$	30		30		ns
Pulse Activation Time	$t_{16}$	30		30		ns
Power-Up Time <sup>2</sup>		4.5		4.5		$\mu\text{s}$

<sup>1</sup> Guaranteed by design and characterization; not production tested.

<sup>2</sup> Time to exit power-down to normal mode of AD5689R-EP operation, 32<sup>nd</sup> clock edge to 90% of DAC midscale value, with output unloaded.

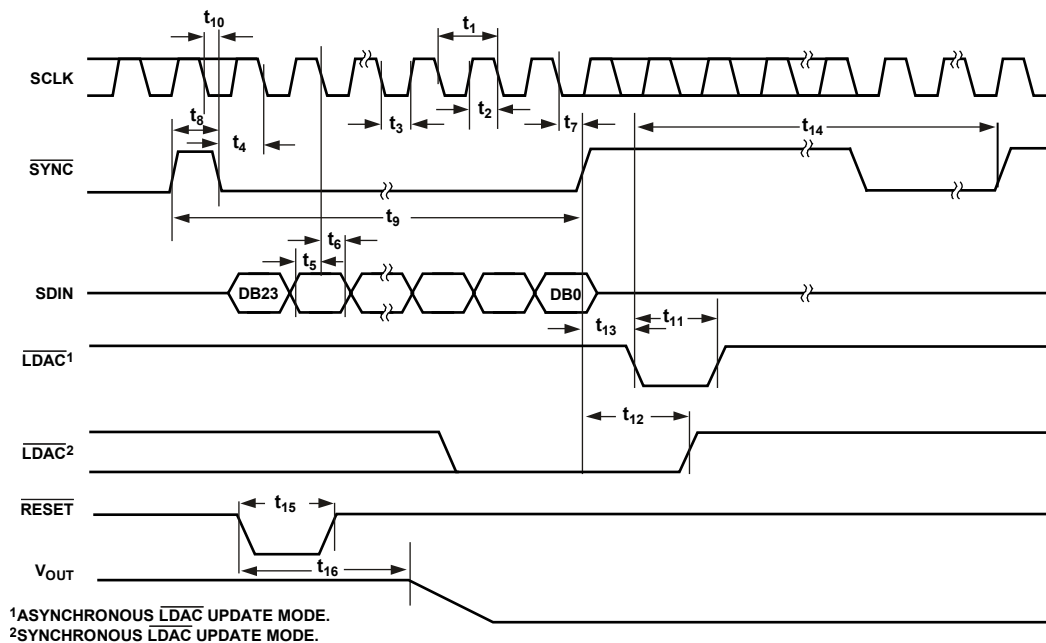


Figure 2. Serial Write Operation

1340E-003

### DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with  $t_R = t_F = 1 \text{ ns/V}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ . See Figure 4 and Figure 5.  $V_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ ,  $1.62 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$ , and  $V_{REF} = 2.5 \text{ V}$ . All specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.  $V_{DD} = 2.7 \text{ V}$  to  $5.5 \text{ V}$ .

Table 4.

Parameter <sup>1</sup>	Symbol	1.62 V $\leq V_{LOGIC} < 2.7 \text{ V}$		2.7 V $\leq V_{LOGIC} \leq 5.5 \text{ V}$		Unit
		Min	Max	Min	Max	
SCLK Cycle Time	$t_1$	66		40		ns
SCLK High Time	$t_2$	33		20		ns
SCLK Low Time	$t_3$	33		20		ns
SYNC to SCLK Falling Edge	$t_4$	33		20		ns
Data Setup Time	$t_5$	5		5		ns
Data Hold Time	$t_6$	5		5		ns
SCLK Falling Edge to SYNC Rising Edge	$t_7$	15		10		ns
Minimum SYNC High Time	$t_8$	60		30		ns
SDO Data Valid from SCLK Rising Edge	$t_9$		45		30	ns
SYNC Rising Edge to SCLK Rising Edge	$t_{10}$	15		10		ns
SYNC Rising Edge to SDO Disable	$t_{11}$	60		60		ns

<sup>1</sup> Guaranteed by design and characterization; not production tested.

### Circuit and Timing Diagrams

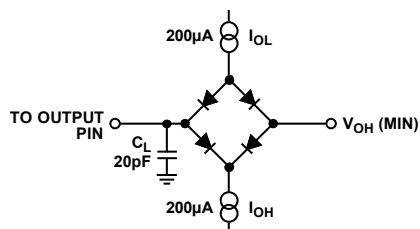


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

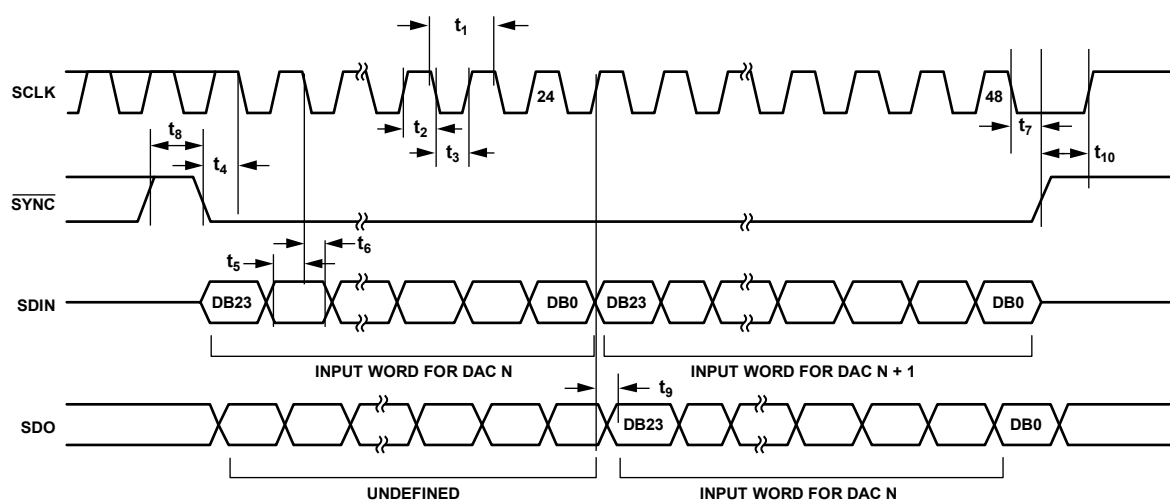


Figure 4. Daisy-Chain Timing Diagram

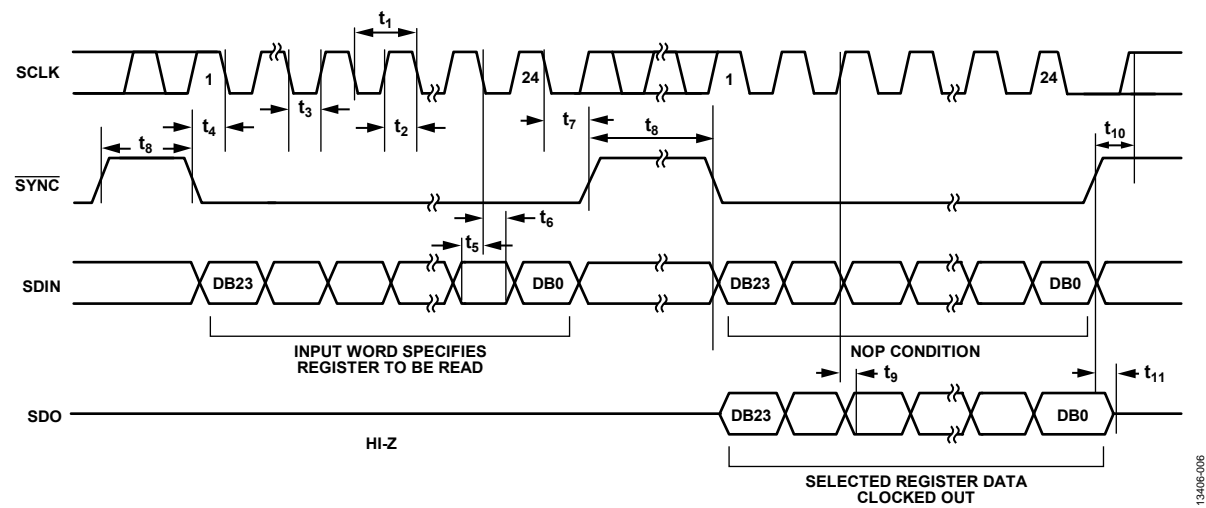


Figure 5. Readback Timing Diagram

13406-008



## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 5.**

Parameter	Rating
$V_{DD}$ to GND	$-0.3\text{ V to }+7\text{ V}$
$V_{\text{LOGIC}}$ to GND	$-0.3\text{ V to }+7\text{ V}$
$V_{\text{OUT}}$ to GND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
$V_{\text{REF}}$ to GND	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Digital Input Voltage to GND	$-0.3\text{ V to }V_{\text{LOGIC}} + 0.3\text{ V}$
Operating Temperature Range	$-55^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	$135^\circ\text{C}$
16-Lead LFCSP, $\theta_{JA}$ Thermal Impedance, 0 <sub>JA</sub> Airflow (4-Layer Board)	$70^\circ\text{C/W}$
Reflow Soldering Peak Temperature, Pb Free (J-STD-020)	$260^\circ\text{C}$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

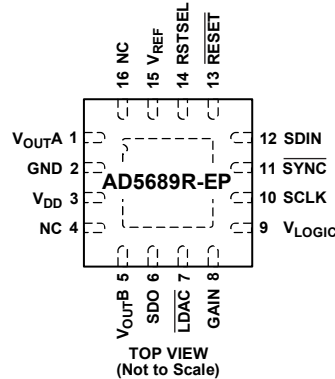
### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. THE EXPOSED PAD MUST BE TIED TO GND.
2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

13406-007

Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No	Mnemonic	Description
1	V <sub>OUTA</sub>	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
2	GND	Ground Reference Point for All Circuitry on the <a href="#">AD5689R-EP</a> .
3	V <sub>DD</sub>	Power Supply Input. The <a href="#">AD5689R-EP</a> can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 $\mu$ F capacitor in parallel with a 0.1 $\mu$ F capacitor to GND.
4	NC	No Connect. Do not connect to this pin.
5	V <sub>OUTB</sub>	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
6	SDO	Serial Data Output. SDO can be used to daisy-chain a number of <a href="#">AD5689R-EP</a> devices together, or it can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
7	LDAC	LDAC can be operated in two modes: asynchronously and synchronously. Pulsing this pin low allows either or both DAC registers to be updated if the input registers have new data; both DAC outputs can be updated simultaneously. This pin can also be tied permanently low.
8	GAIN	Gain Select. When this pin is tied to GND, both DACs output a span from 0 V to V <sub>REF</sub> . If this pin is tied to V <sub>LOGIC</sub> , both DACs output a span of 0 V to 2 $\times$ V <sub>REF</sub> .
9	V <sub>LOGIC</sub>	Digital Power Supply. Voltage ranges from 1.62 V $\leq$ V <sub>LOGIC</sub> $\leq$ 5.5 V.
10	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
11	SYNC	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 24 clocks.
12	SDIN	Serial Data Input. This device has a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input.
13	RESET	Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all LDAC pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. If this pin is forced low at power-up, the power-on reset (POR) circuit does not initialize the device correctly until this pin is released.
14	RSTSEL	Power-On Reset Select. Tying this pin to GND powers up both DACs to zero scale. Tying this pin to V <sub>LOGIC</sub> powers up both DACs to midscale.
15	V <sub>REF</sub>	Reference Voltage. The <a href="#">AD5689R-EP</a> has a common reference pin. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference output.
16	NC	No Connect. Do not connect to this pin.
17	EPAD	Exposed Pad. The exposed pad must be tied to GND.

## TYPICAL PERFORMANCE CHARACTERISTICS

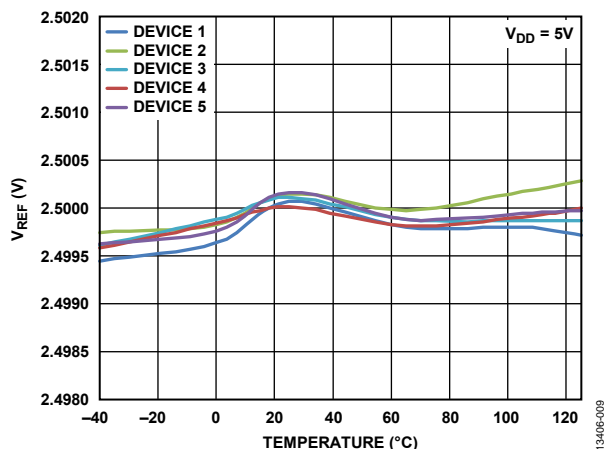
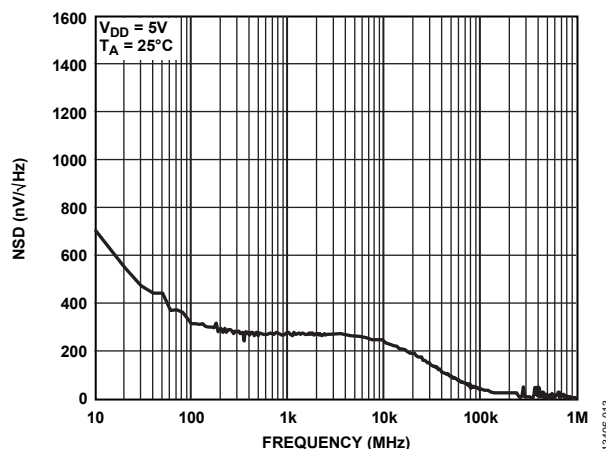
Figure 7. Internal Reference Voltage ( $V_{REF}$ ) vs. Temperature

Figure 10. Internal Reference Noise Spectral Density (NSD) vs. Frequency

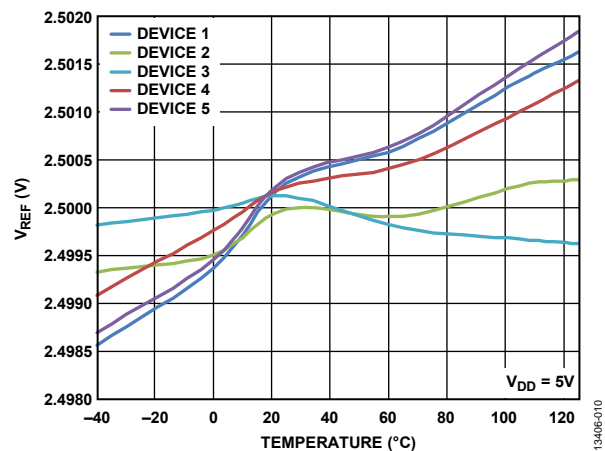
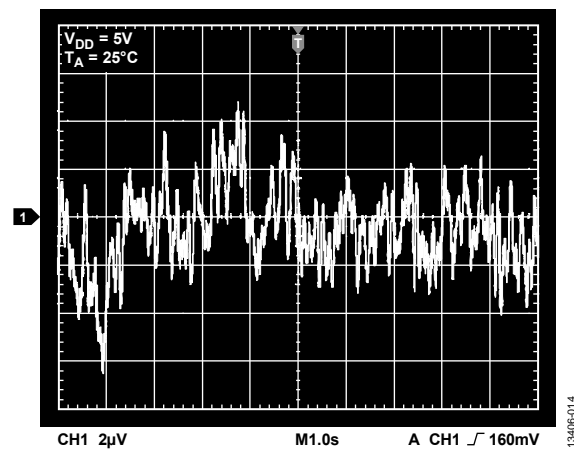
Figure 8.  $V_{REF}$  vs. Temperature

Figure 11. Internal Reference Noise, 0.1 Hz to 10 Hz

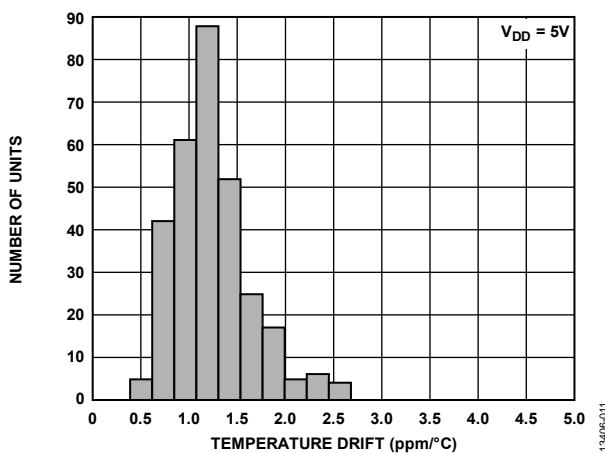
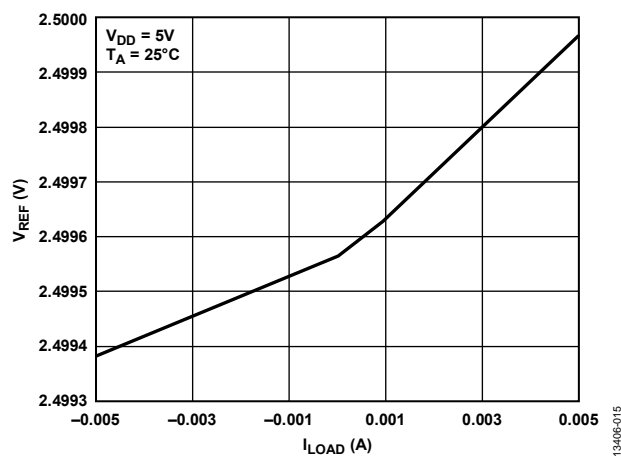


Figure 9. Reference Output Temperature Drift Histogram

Figure 12.  $V_{REF}$  vs. Load Current ( $I_{LOAD}$ )

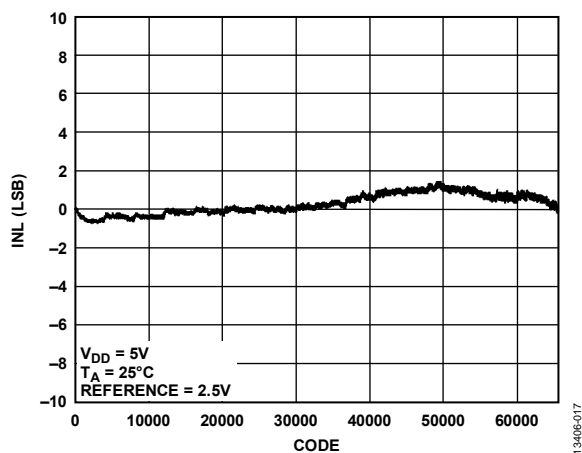


Figure 13. Integral Nonlinearity (INL) vs. Code

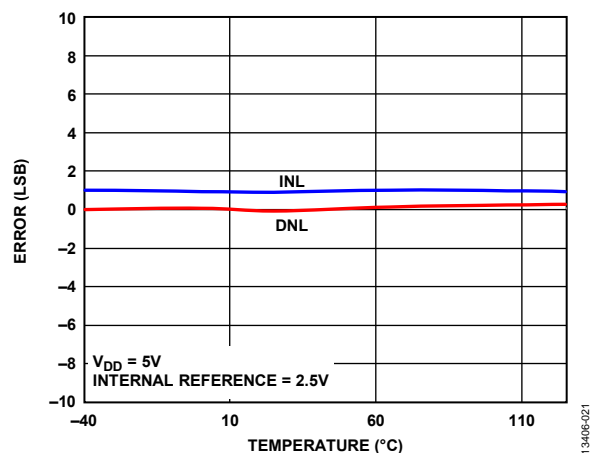


Figure 16. INL Error and DNL Error vs. Temperature

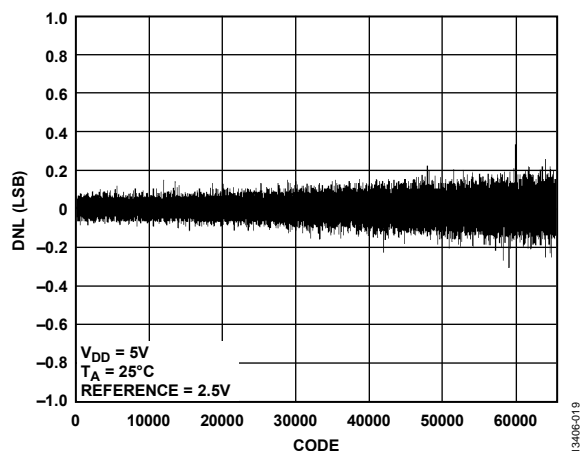


Figure 14. Differential Nonlinearity (DNL) vs. Code

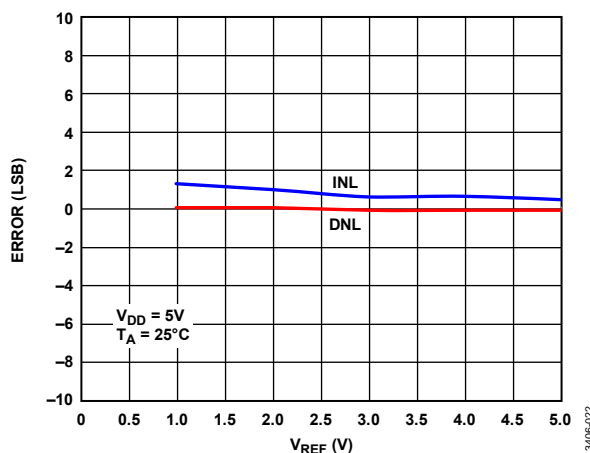
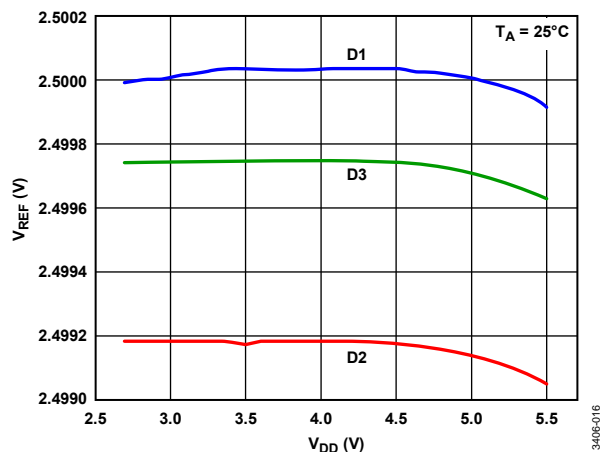
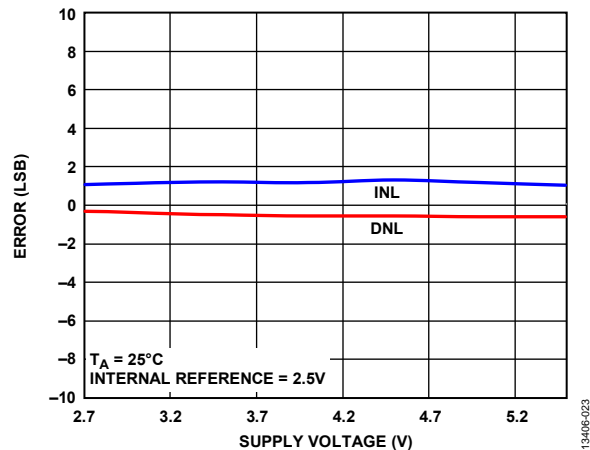
Figure 17. INL Error and DNL Error vs.  $V_{REF}$ Figure 15.  $V_{REF}$  vs. Supply Voltage ( $V_{DD}$ )

Figure 18. INL Error and DNL Error vs. Supply Voltage

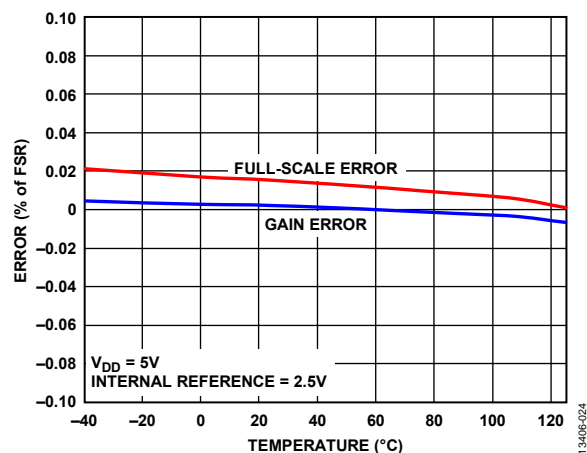


Figure 19. Gain Error and Full-Scale Error vs. Temperature

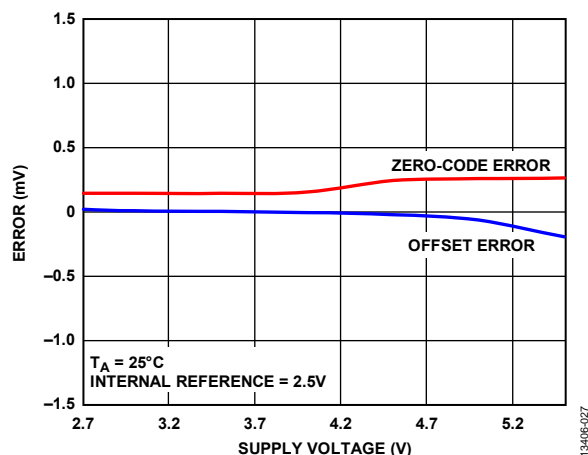


Figure 22. Zero-Code Error and Offset Error vs. Supply Voltage

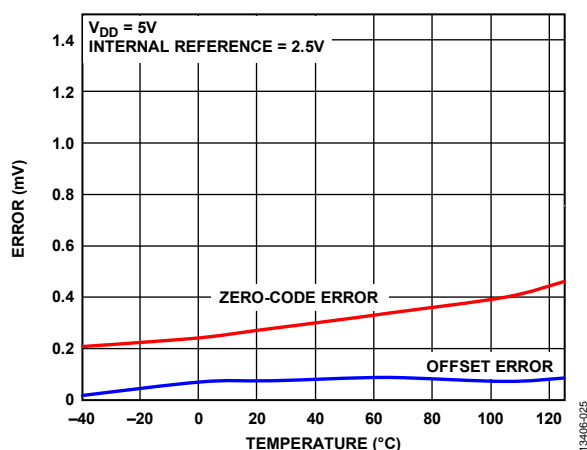


Figure 20. Zero-Code Error and Offset Error vs. Temperature

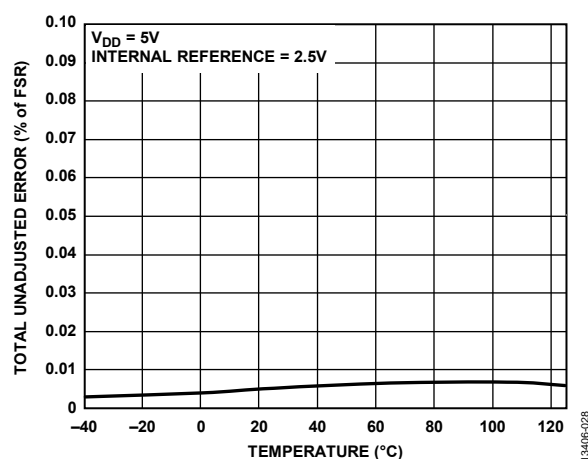


Figure 23. Total Unadjusted Error (TUE) vs. Temperature

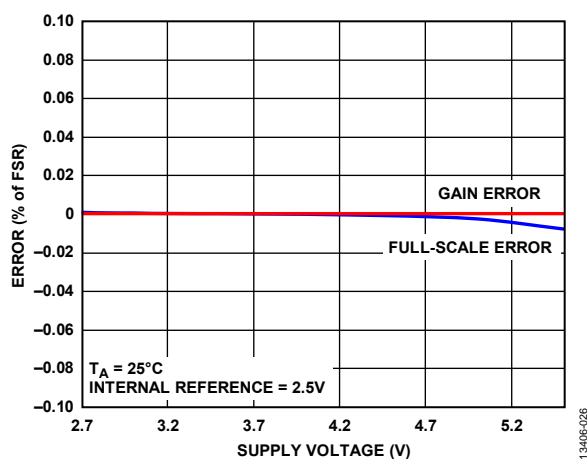


Figure 21. Gain Error and Full-Scale Error vs. Supply Voltage

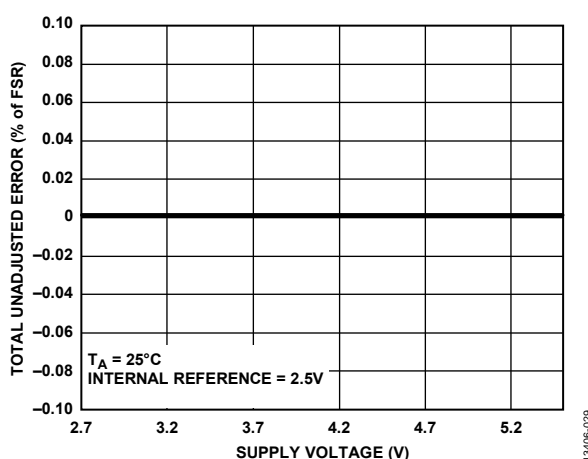


Figure 24. Total Unadjusted Error (TUE) vs. Supply Voltage, Gain = 1

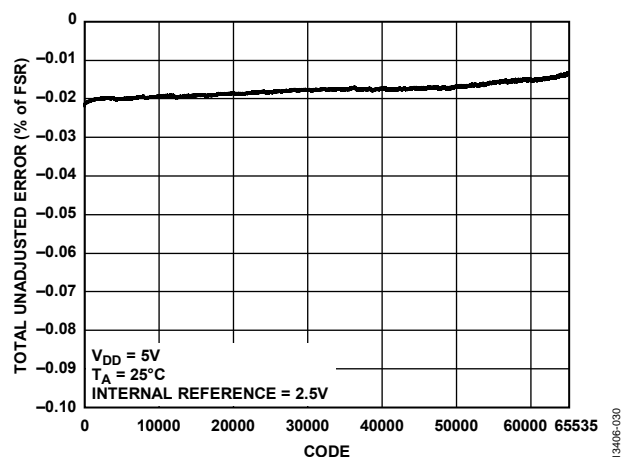


Figure 25. Total Unadjusted Error (TUE) vs. Code

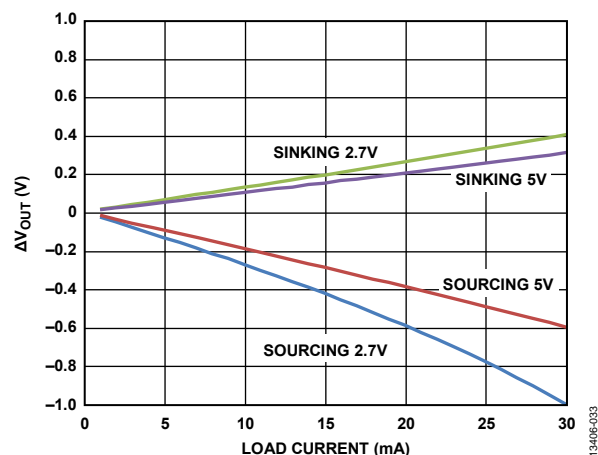


Figure 28. Headroom/Footroom vs. Load Current

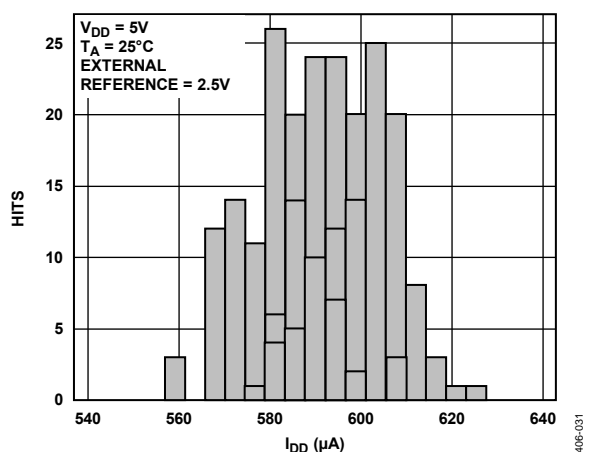
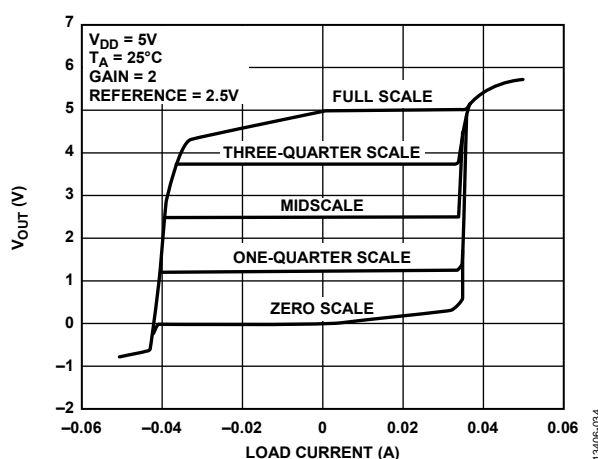
Figure 26.  $I_{DD}$  Histogram with External Reference,  $V_{DD} = 5V$ 

Figure 29. Source and Sink Capability at 5 V, Gain = 2

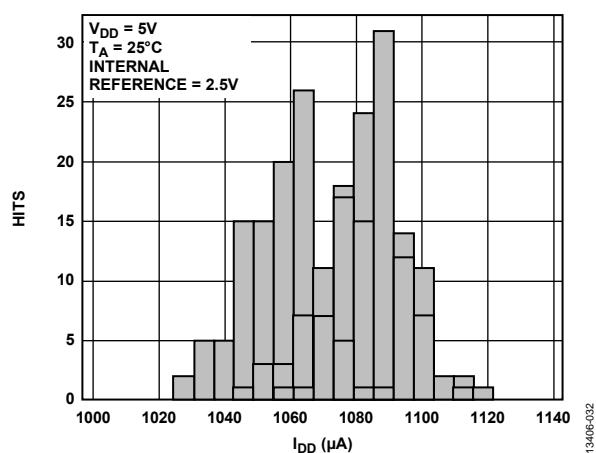
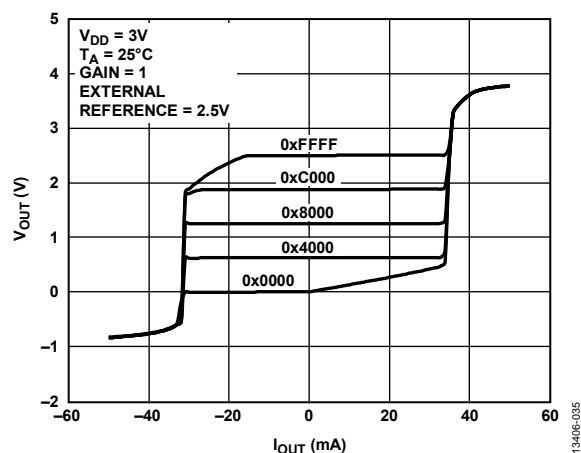
Figure 27.  $I_{DD}$  Histogram with Internal Reference,  $V_{REF} = 2.5V$ , Gain = 2

Figure 30. Source and Sink Capability at 3 V, Gain = 1

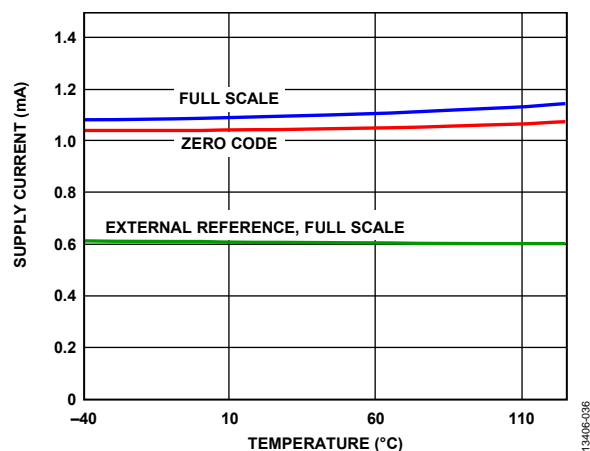


Figure 31. Supply Current vs. Temperature

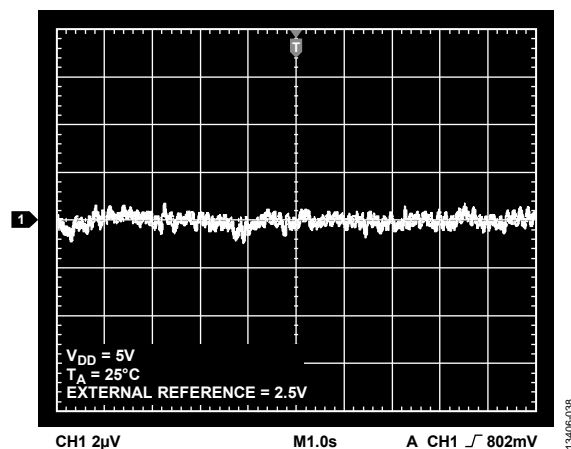


Figure 33. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V External Reference

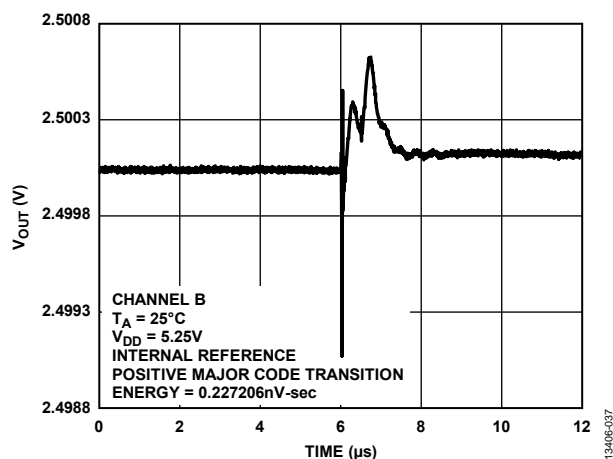


Figure 32. Digital-to-Analog Glitch Impulse

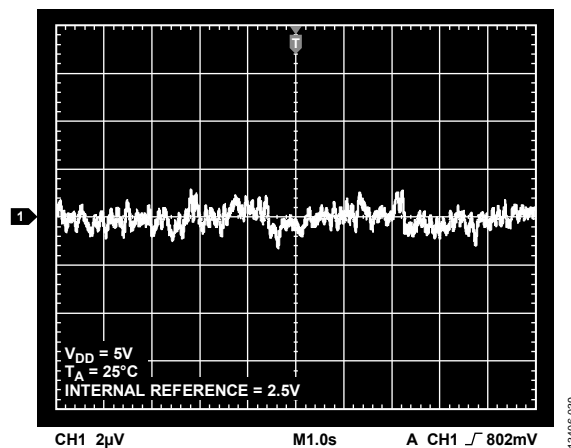


Figure 34. 0.1 Hz to 10 Hz Output Noise Plot, 2.5 V Internal Reference

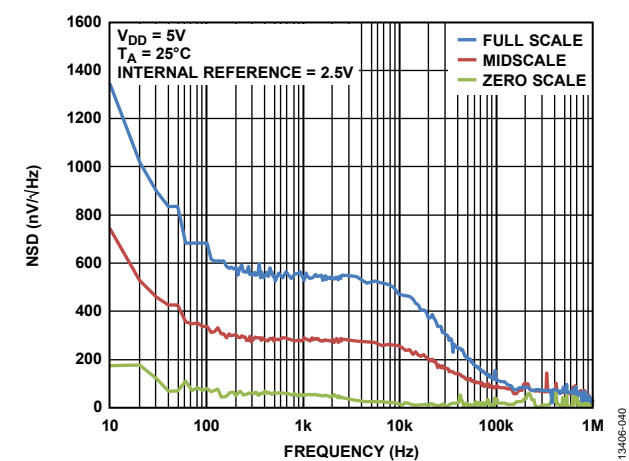


Figure 35. Noise Spectral Density (NSD) vs. Frequency

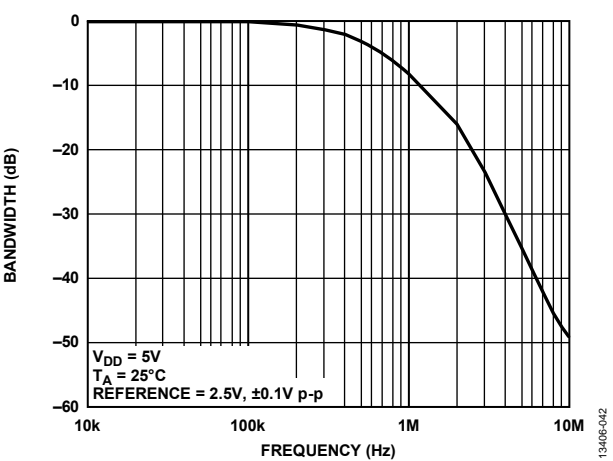


Figure 37. Multiplying Bandwidth, External Reference = 2.5 V, ±0.1 V p-p, 10 kHz to 10 MHz

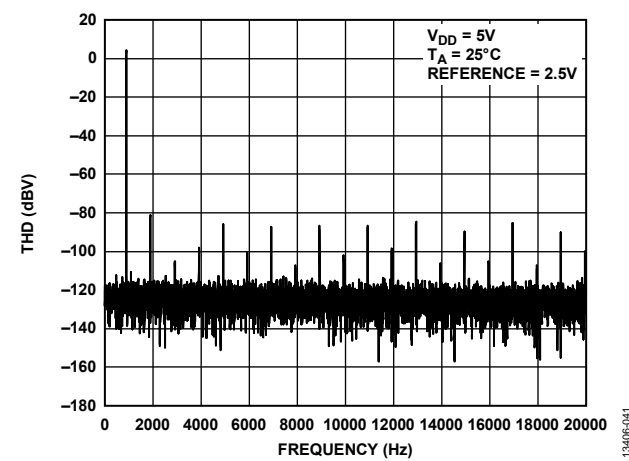
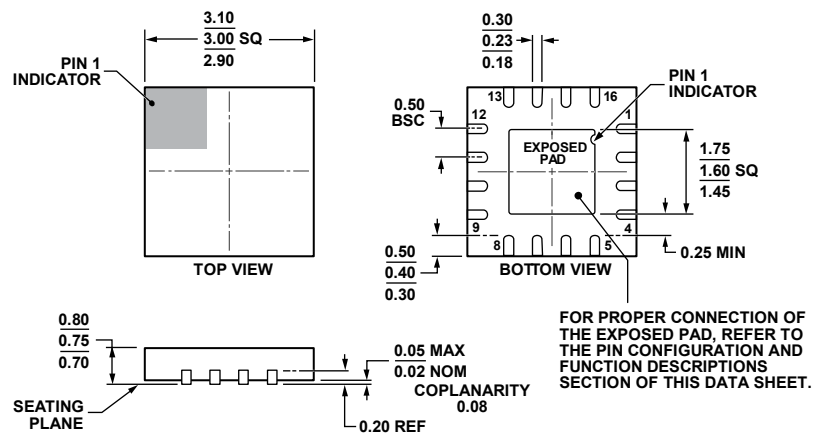


Figure 36. Total Harmonic Distortion at 1 kHz vs. Frequency



## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 3 mm × 3 mm Body, Very Very Thin Quad  
 (CP-16-22)  
 Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Resolution	Temperature Range	Package Description	Package Option
AD5689RTCPZ-EP-RL7	16 Bits	−55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-22

<sup>1</sup> Z = RoHS Compliant Part.