Variable Resolution, 10-Bit to 16-Bit R/D Converter with Reference Oscillator

Data Sheet

AD2S1210-EP

FEATURES

Complete monolithic resolver-to-digital converter
3125 rps maximum tracking rate (10-bit resolution)
±2.5 arc minutes of accuracy
10-/12-/14-/16-bit resolution, set by user
Parallel and serial 10-bit to 16-bit data ports
Absolute position and velocity outputs
System fault detection
Programmable fault detection thresholds
Differential inputs
Incremental encoder emulation
Programmable sinusoidal oscillator on board
Compatible with DSP and SPI interface standards
5 V supply with 2.3 V to 5 V logic interface

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range: −55°C to +125°C
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Product change notification
Qualification data available on request

APPLICATIONS

DC and ac servo motor control
Encoder emulation
Electric power steering
Electric vehicles
Integrated starter generators/alternators
Automotive motion sensing and control

GENERAL DESCRIPTION

The AD2S1210-EP is a complete 10-bit to 16-bit resolution tracking resolver-to-digital converter, integrating an on-board programmable sinusoidal oscillator that provides sine wave excitation for resolvers.

The converter accepts 3.15 V p-p ± 27% input signals, in the range of 2 kHz to 20 kHz on the sine and cosine inputs. A Type II servo loop is employed to track the inputs and convert the input sine and cosine information into a digital representation of the input angle and velocity. The maximum tracking rate is 3125 rps.

Full details about this enhanced product, including theory of operation, registers details, and applications information, are available in the AD2S1210 data sheet, which should be concluded in conjunction with this data sheet.

FUNCTIONAL BLOCK DIAGRAM

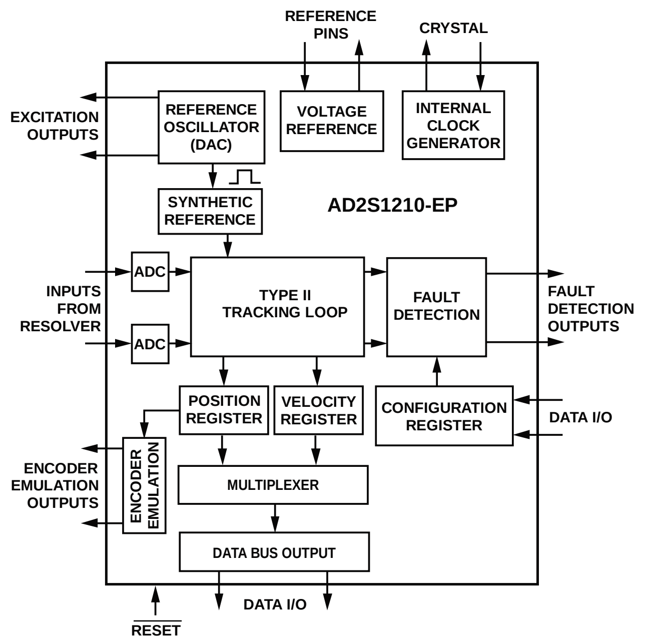

Figure 1.

PRODUCT HIGHLIGHTS

1. Ratiometric tracking conversion. The Type II tracking loop provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.
2. System fault detection. A fault detection circuit can sense loss of resolver signals, out-of-range input signals, input signal mismatch, or loss of position tracking. The fault detection threshold levels can be individually programmed by the user for optimization within a particular application.
3. signal range. The sine and cosine inputs can accept differential input voltages of 3.15 V p-p ± 27%.
4. Programmable excitation frequency. Excitation frequency is easily programmable to a number of standard frequencies between 2 kHz and 20 kHz.
5. Triple format position data. Absolute 10-bit to 16-bit angular position data is accessed via either a 16-bit parallel port or a 4-wire serial interface. Incremental encoder emulation is in standard A-quad-B format with direction output available.
6. Digital velocity output. 10-bit to 16-bit signed digital velocity accessed via either a 16-bit parallel port or a 4-wire serial interface.

Rev. A Document Feedback
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6/2010—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = 5.0$ V ± 5%, CLKIN = 8.192 MHz ± 25%, EXC, $\overline{EXC}$ frequency = 10 kHz to 20 kHz (10-bit); 6 kHz to 20 kHz (12-bit); 3 kHz to 12 kHz (14-bit); 2 kHz to 10 kHz (16-bit); $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.[1]

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
SINE, COSINE INPUTS[2]					
Voltage Amplitude	2.3	3.15	4.0	V p-p	Sinusoidal waveforms, differential SIN to SINLO, COS to COSLO
Input Bias Current			8.25	µA	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Input Impedance	485			kΩ	V_{IN} = 4.0 V p-p, CLKIN = 8.192 MHz
Phase Lock Range	−44		+44	Degrees	Sine/cosine vs. EXC output, Control Register D3 = 0
Common-Mode Rejection		±20		arc sec/V	10 Hz to 1 MHz, Control Register D4 = 0
ANGULAR ACCURACY[3]					
Angular Accuracy		±2.5 + 1 LSB	±7 + 1 LSB	arc min	
Resolution		10, 12, 14, 16		Bits	No missing codes
Linearity INL					
10-Bit			±1	LSB	
12-Bit			±2	LSB	
14-Bit			±4	LSB	
16-Bit			±16	LSB	
Linearity DNL			±0.9	LSB	
Repeatability		±1		LSB	
VELOCITY OUTPUT					
Velocity Accuracy[4]					
10-Bit			±2	LSB	Zero acceleration
12-Bit			±2	LSB	Zero acceleration
14-Bit			±4	LSB	Zero acceleration
16-Bit			±16	LSB	Zero acceleration
Resolution[5]		9, 11, 13, 15		Bits	
DYNAMNIC PERFORMANCE					
Bandwidth					
10-Bit	2000		6600	Hz	
	2900		5400	Hz	CLKIN = 8.192 MHz
12-Bit	900		2800	Hz	
	1200		2200	Hz	CLKIN = 8.192 MHz
14-Bit	400		1500	Hz	
	600		1200	Hz	CLKIN = 8.192 MHz
16-Bit	100		350	Hz	
	125		275	Hz	CLKIN = 8.192 MHz
Tracking Rate					
10-Bit			3125	rps	CLKIN = 10.24 MHz
			2500		CLKIN = 8.192 MHz
12-Bit			1250	rps	CLKIN = 10.24 MHz
			1000		CLKIN = 8.192 MHz
14-Bit			625	rps	CLKIN = 10.24 MHz
			500		CLKIN = 8.192 MHz
16-Bit			156.25	rps	CLKIN = 10.24 MHz
			125		CLKIN = 8.192 MHz
Acceleration Error					
10-Bit		30		arc min	At 50,000 rps^2, CLKIN = 8.192 MHz
12-Bit		30		arc min	At 10,000 rps^2, CLKIN = 8.192 MHz
14-Bit		30		arc min	At 2500 rps^2, CLKIN = 8.192 MHz
16-Bit		30		arc min	At 125 rps^2, CLKIN = 8.192 MHz

Parameter	Min	Typ	Max	Unit	Conditions/Comments
Settling Time 10° Step Input					
10-Bit		0.6	0.9	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
12-Bit		2.2	3.3	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-Bit		6.5	9.8	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
16-Bit		27.5	48	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
Settling Time 179° Step Input					
10-Bit		1.5	2.4	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
12-Bit		4.75	6.1	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
14-Bit		10.5	15.2	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
16-Bit		45	68	ms	To settle to within ±2 LSB, CLKIN = 8.192 MHz
EXC, $\overline{\text{EXC}}$ OUTPUTS					
Voltage	3.2	3.6	4.0	V p-p	Load ±100 μA, typical differential output (EXC to $\overline{\text{EXC}}$) = 7.2 V p-p
Center Voltage	2.40	2.47	2.53	V	
Frequency	2		20	kHz	
EXC/$\overline{\text{EXC}}$ DC Mismatch			30	mV	
EXC/$\overline{\text{EXC}}$ AC Mismatch			132	mV	
THD		−58		dB	First five harmonics
VOLTAGE REFERENCE					
REFOUT	2.40	2.47	2.53	V	$\pm I_{OUT}$ = 100 μA
Drift		100		ppm/°C	
PSRR		−60		dB	
CLKIN, XTALOUT[6]					
V_{IL} Voltage Input Low			0.8	V	
V_{IH} Voltage Input High	2.0			V	
LOGIC INPUTS					
V_{IL} Voltage Input Low			0.8	V	V_{DRIVE} = 2.7 V to 5.25 V
			0.7	V	V_{DRIVE} = 2.3 V to 2.7 V
V_{IH} Voltage Input High	2.0			V	V_{DRIVE} = 2.7 V to 5.25 V
	1.7			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{IL} Low Level Input Current (Non-Pull-Up)			10	μA	
I_{IL} Low Level Input Current (Pull-Up)			80	μA	RES0, RES1, $\overline{\text{RD}}$, $\overline{\text{WR}}/\overline{\text{FSYNC}}$, A0, A1, and $\overline{\text{RESET}}$ pins
I_{IH} High Level Input Current	−10			μA	
LOGIC OUTPUTS					
V_{OL} Voltage Output Low			0.4	V	V_{DRIVE} = 2.3 V to 5.25 V
V_{OH} Voltage Output High	2.4			V	V_{DRIVE} = 2.7 V to 5.25 V
	2.0			V	V_{DRIVE} = 2.3 V to 2.7 V
I_{OZH} High Level Three-State Leakage	−10			μA	
I_{OZL} Low Level Three-State Leakage			10	μA	
POWER REQUIREMENTS					
AV_{DD}	4.75		5.25	V	
DV_{DD}	4.75		5.25	V	
V_{DRIVE}	2.3		5.25	V	
POWER SUPPLY					
I_{AVDD}			12	mA	
I_{DVDD}			35	mA	
I_{OVDD}			2	mA	

[1] Temperature range is as follows: −55°C to +125°C.
[2] The voltages SIN, SINLO, COS, and COSLO, relative to AGND, must always be between 0.15 V and AV_{DD} − 0.2 V.
[3] All specifications within the angular accuracy parameter are tested at constant velocity, that is, zero acceleration.
[4] The velocity accuracy specification includes velocity offset and dynamic ripple.
[5] For example, when RES0 = 0 and RES1 = 1, the position output has a resolution of 12 bits. The velocity output has a resolution of 11 bits with the MSB indicating the direction of rotation. In this example, with a CLKIN frequency of 8.192 MHz, the velocity LSB is 0.488 rps, that is, 1000 rps/(2^{11}).
[6] The clock frequency of the AD2S1210-EP can be supplied with a crystal, an oscillator, or directly from a DSP/microprocessor digital output. When using a single-ended clock signal directly from the DSP/microprocessor, the XTALOUT pin should remain open circuit and the logic levels outlined under the logic inputs parameter in Table 1 apply.

TIMING SPECIFICATIONS

$AV_{DD} = DV_{DD} = 5.0\ V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.[1]

Table 2.

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
f_{CLKIN}	Frequency of clock input	6.144	MHz min
		10.24	MHz max
t_{CK}	Clock period ($t_{CK} = 1/f_{CLKIN}$)	98	ns min
		163	ns max
t_1	A0 and A1 setup time before $\overline{RD}/\overline{CS}$ low	2	ns min
t_2	Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ rising edge	22	ns min
t_3	Address/data setup time during a write cycle	3	ns min
t_4	Address/data hold time during a write cycle	2	ns min
t_5	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_6	Delay $\overline{CS}$ rising edge to $\overline{CS}$ falling edge	10	ns min
t_7	Delay between writing address and writing data	$2 \times t_{CK} + 20$	ns min
t_8	A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ rising edge	2	ns min
t_9	Delay between successive write cycles	$6 \times t_{CK} + 20$	ns min
t_{10}	Delay between rising edge of $\overline{WR}/\overline{FSYNC}$ and falling edge of $\overline{RD}$	2	ns min
t_{11}	Delay $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	2	ns min
t_{12}	Enable delay $\overline{RD}$ low to data valid in configuration mode		
	V_{DRIVE} = 4.5 V to 5.25 V	37	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	25	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	30	ns min
t_{13}	$\overline{RD}$ rising edge to $\overline{CS}$ rising edge	2	ns min
t_{14A}	Disable delay $\overline{RD}$ high to data high-Z	16	ns min
t_{14B}	Disable delay $\overline{CS}$ high to data high-Z	16	ns min
t_{15}	Delay between rising edge of $\overline{RD}$ and falling edge of $\overline{WR}/\overline{FSYNC}$	2	ns min
t_{16}	$\overline{SAMPLE}$ pulse width	$2 \times t_{CK} + 20$	ns min
t_{17}	Delay from $\overline{SAMPLE}$ before $\overline{RD}/\overline{CS}$ low	$6 \times t_{CK} + 20$	ns min
t_{18}	Hold time $\overline{RD}$ before $\overline{RD}$ low	2	ns min
t_{19}	Enable delay $\overline{RD}/\overline{CS}$ low to data valid		
	V_{DRIVE} = 4.5 V to 5.25 V	17	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	21	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	33	ns min
t_{20}	$\overline{RD}$ pulse width	6	ns min
t_{21}	A0 and A1 set time to data valid when $\overline{RD}/\overline{CS}$ low		
	V_{DRIVE} = 4.5 V to 5.25 V	36	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	37	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min
t_{22}	Delay $\overline{WR}/\overline{FSYNC}$ falling edge to SCLK rising edge	3	ns min
t_{23}	Delay $\overline{WR}/\overline{FSYNC}$ falling edge to SDO release from high-Z		
	V_{DRIVE} = 4.5 V to 5.25 V	16	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	26	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	29	ns min
t_{24}	Delay SCLK rising edge to DBx valid		
	V_{DRIVE} = 4.5 V to 5.25 V	24	ns min
	V_{DRIVE} = 2.7 V to 3.6 V	18	ns min
	V_{DRIVE} = 2.3 V to 2.7 V	32	ns min
t_{25}	SCLK high time	$0.4 \times t_{SCLK}$	ns min
t_{26}	SCLK low time	$0.4 \times t_{SCLK}$	ns min
t_{27}	SDI setup time prior to SCLK falling edge	3	ns min
t_{28}	SDI hold time after SCLK falling edge	2	ns min

Parameter	Description	Limit at T_{MIN}, T_{MAX}	Unit
t_{29}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to SDO high-Z	15	ns min
t_{30}	Delay from $\overline{SAMPLE}$ before $\overline{WR}/\overline{FSYNC}$ falling edge	$6 \times t_{CK} + 20$ ns	ns min
t_{31}	Delay $\overline{CS}$ falling edge to $\overline{WR}/\overline{FSYNC}$ falling edge in normal mode	2	ns min
t_{32}	A0 and A1 setup time before $\overline{WR}/\overline{FSYNC}$ falling edge	2	ns min
t_{33}	A0 and A1 hold time after $\overline{WR}/\overline{FSYNC}$ falling edge[2]		
	In normal mode, A0 = 0, A1 = 0/1	$24 \times t_{CK} + 5$ ns	ns min
	In configuration mode, A0 = 1, A1 = 1	$8 \times t_{CK} + 5$ ns	ns min
t_{34}	Delay $\overline{WR}/\overline{FSYNC}$ rising edge to $\overline{WR}/\overline{FSYNC}$ falling edge	10	ns min
f_{SCLK}	Frequency of SCLK input		
	V_{DRIVE} = 4.5 V to 5.25 V	20	MHz
	V_{DRIVE} = 2.7 V to 3.6 V	25	MHz
	V_{DRIVE} = 2.3 V to 2.7 V	15	MHz

[1] Temperature range is as follows: −55°C to +125°C.
[2] A0 and A1 should remain constant for the duration of the serial readback. This may require 24 clock periods to read back the 8-bit fault information in addition to the 16 bits of position/velocity data. If the fault information is not required, A0/A1 may be released after 16 clock cycles.

ABSOLUTE MAXIMUM RATINGS

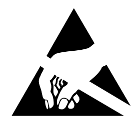
Table 3.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3 V to +7.0 V
DV_{DD} to AGND, DGND	−0.3 V to +7.0 V
V_{DRIVE} to AGND, DGND	−0.3 V to AV_{DD}
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Analog Output Voltage Swing	−0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range (Ambient)	
EP Grade	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance[2]	54°C/W
θ_{JC} Thermal Impedance[2]	15°C/W
RoHS-Compliant Temperature, Soldering Reflow	260(−5/+0)°C
ESD	2 kV HBM

[1] Transient currents of up to 100 mA do not cause latch-up.
[2] JEDEC 2S2P standard board.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

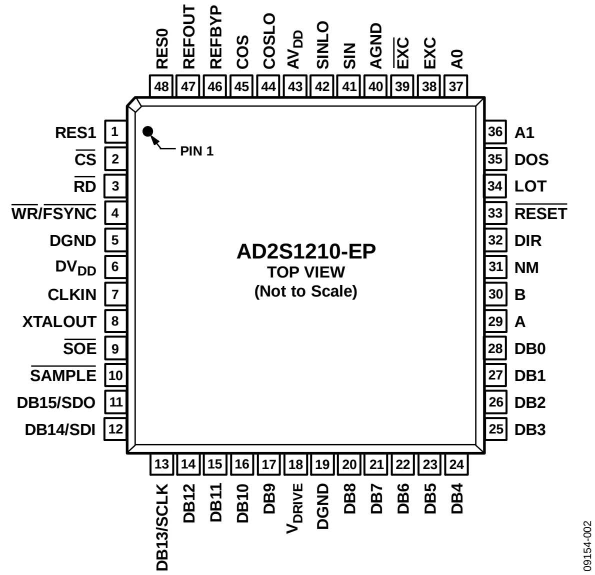


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RES1	Resolution Select 1. Logic input. RES1 in conjunction with RES0 allows the resolution of the AD2S1210-EP to be programmed.
2	$\overline{\text{CS}}$	Chip Select. Active low logic input. The device is enabled when $\overline{\text{CS}}$ is held low.
3	$\overline{\text{RD}}$	Edge-Triggered Logic Input. When the $\overline{\text{SOE}}$ pin is high, this pin acts as a frame synchronization signal and output enable for the parallel data outputs, DB15 to DB0. The output buffer is enabled when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are held low. When the $\overline{\text{SOE}}$ pin is low, the $\overline{\text{RD}}$ pin should be held high.
4	$\overline{\text{WR}}/\overline{\text{FSYNC}}$	Edge-Triggered Logic Input. When the $\overline{\text{SOE}}$ pin is high, this pin acts as a frame synchronization signal and input enable for the parallel data inputs, DB7 to DB0. The input buffer is enabled when $\overline{\text{CS}}$ and $\overline{\text{WR}}/\overline{\text{FSYNC}}$ are held low. When the $\overline{\text{SOE}}$ pin is low, the $\overline{\text{WR}}/\overline{\text{FSYNC}}$ pin acts as a frame synchronization signal and enable for the serial data bus.
5, 19	DGND	Digital Ground. These pins are ground reference points for digital circuitry on the AD2S1210-EP. Refer all digital input signals to this DGND voltage. Both of these pins can be connected to the AGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
6	DV_{DD}	Digital Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD2S1210-EP. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
7	CLKIN	Clock Input. A crystal or oscillator can be used at the CLKIN and XTALOUT pins to supply the required clock frequency of the AD2S1210-EP. Alternatively, a single-ended clock can be applied to the CLKIN pin. The input frequency of the AD2S1210-EP is specified from 6.144 MHz to 10.24 MHz.
8	XTALOUT	Crystal Output. When using a crystal or oscillator to supply the clock frequency to the AD2S1210-EP, apply the crystal across the CLKIN and XTALOUT pins. When using a single-ended clock source, the XTALOUT pin should be considered a no connect pin.
9	$\overline{\text{SOE}}$	Serial Output Enable. Logic input. This pin enables either the parallel or serial interface. The serial interface is selected by holding the $\overline{\text{SOE}}$ pin low, and the parallel interface is selected by holding the $\overline{\text{SOE}}$ pin high.
10	$\overline{\text{SAMPLE}}$	Sample Result. Logic input. Data is transferred from the position and velocity integrators to the position and velocity registers after a high-to-low transition on the $\overline{\text{SAMPLE}}$ signal. The fault register is also updated after a high-to-low transition on the $\overline{\text{SAMPLE}}$ signal.
11	DB15/SDO	Data Bit 15/Serial Data Output Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB15, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDO, the serial data output bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR}}/\overline{\text{FSYNC}}$. The bits are clocked out on the rising edge of SCLK.
12	DB14/SDI	Data Bit 14/Serial Data Input Bus. When the $\overline{\text{SOE}}$ pin is high, this pin acts as DB14, a three-state data output pin controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. When the $\overline{\text{SOE}}$ pin is low, this pin acts as SDI, the serial data input bus controlled by $\overline{\text{CS}}$ and $\overline{\text{WR}}/\overline{\text{FSYNC}}$. The bits are clocked in on the falling edge of SCLK.

Pin No.	Mnemonic	Description
13	DB13/SCLK	Data Bit 13/Serial Clock. In parallel mode, this pin acts as DB13, a three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$. In serial mode, this pin acts as the serial clock input.
14 to 17	DB12 to DB9	Data Bit 12 to Data Bit 9. Three-state data output pins controlled by $\overline{CS}$ and $\overline{RD}$.
18	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. Decouple this pin to DGND. The voltage range on this pin is 2.3 V to 5.25 V and may be different from the voltage range at AV_{DD} and DV_{DD} but should never exceed either by more than 0.3 V.
20	DB8	Data Bit 8. Three-state data output pin controlled by $\overline{CS}$ and $\overline{RD}$.
21 to 28	DB7 to DB0	Data Bit 7 to Data Bit 0. Three-state data input/output pins controlled by $\overline{CS}$, $\overline{RD}$, and $\overline{WR}/\overline{FSYNC}$.
29	A	Incremental Encoder Emulation Output A. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
30	B	Incremental Encoder Emulation Output B. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
31	NM	North Marker Incremental Encoder Emulation Output. Logic output. This output is free running and is valid if the resolver format input signals applied to the converter are valid.
32	DIR	Direction. Logic output. This output is used in conjunction with the incremental encoder emulation outputs. The DIR output indicates the direction of the input rotation and is high for increasing angular rotation.
33	$\overline{RESET}$	Reset. Logic input. The AD2S1210-EP requires an external reset signal to hold the $\overline{RESET}$ input low until V_{DD} is within the specified operating range of 4.75 V to 5.25 V.
34	LOT	Loss of Tracking. Logic output. Loss of tracking (LOT) is indicated by a logic low on the LOT pin and is not latched.
35	DOS	Degradation of Signal. Logic output. Degradation of signal (DOS) is detected when either resolver input (sine or cosine) exceeds the specified DOS sine/cosine threshold or when an amplitude mismatch occurs between the sine and cosine input voltages. DOS is indicated by a logic low on the DOS pin.
36	A1	Mode Select 1. Logic input. A1 in conjunction with A0 allows the mode of the AD2S1210-EP to be selected.
37	A0	Mode Select 0. Logic input. A0 in conjunction with A1 allows the mode of the AD2S1210-EP to be selected.
38	EXC	Excitation Frequency. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
39	$\overline{EXC}$	Excitation Frequency Complement. Analog output. An on-board oscillator provides the sinusoidal excitation signal (EXC) and its complement signal ($\overline{EXC}$) to the resolver. The frequency of this reference signal is programmable via the excitation frequency register.
40	AGND	Analog Ground. This pin is the ground reference points for analog circuitry on the AD2S1210-EP. Refer all analog input signals and any external reference signal to this AGND voltage. Connect the AGND pin to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
41	SIN	Positive Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
42	SINLO	Negative Analog Input of Differential SIN/SINLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
43	AV_{DD}	Analog Supply Voltage, 4.75 V to 5.25 V. This pin is the supply voltage for all analog circuitry on the AD2S1210-EP. The AV_{DD} and DV_{DD} voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
44	COSLO	Negative Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
45	COS	Positive Analog Input of Differential COS/COSLO Pair. The input range is 2.3 V p-p to 4.0 V p-p.
46	REFBYP	Reference Bypass. Connect reference decoupling capacitors at this pin. Typical recommended values are 10 μF and 0.01 μF.
47	REFOUT	Voltage Reference Output.
48	RES0	Resolution Select 0. Logic input. RES0 in conjunction with RES1 allows the resolution of the AD2S1210-EP to be programmed.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, AV_{DD} = DV_{DD} = V_{DRIVE} = 5 V, SIN/SINLO = 3.15 V p-p, COS/COSLO = 3.15 V p-p, CLKIN = 8.192 MHz, unless otherwise noted.

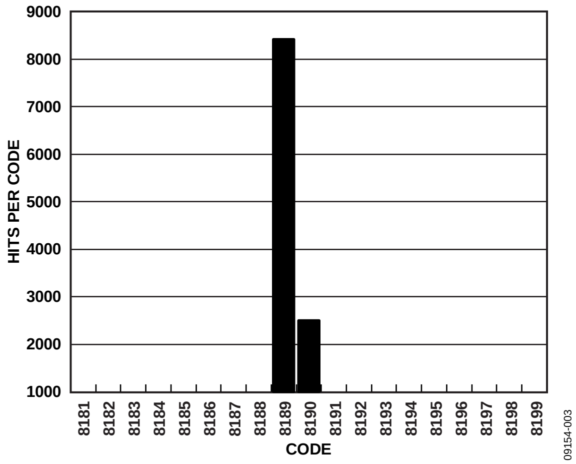


Figure 3. Typical 16-Bit Angular Accuracy Histogram Of Codes, 10,000 Samples

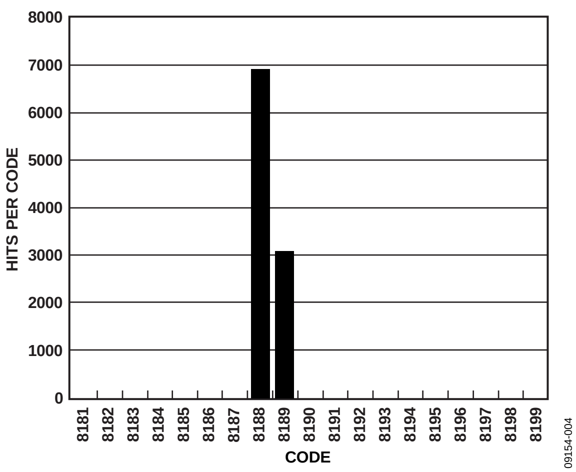


Figure 4. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

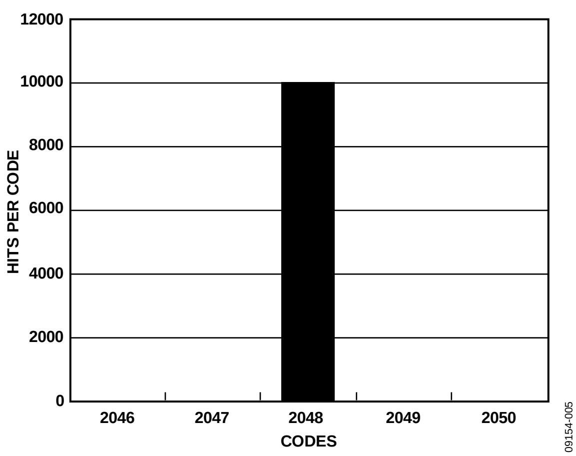


Figure 5. Typical 14-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

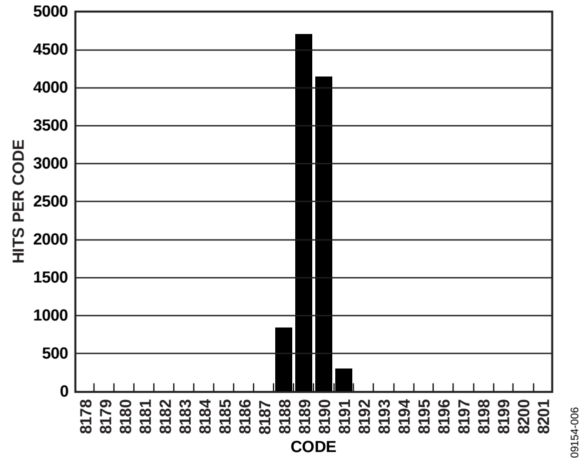


Figure 6. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

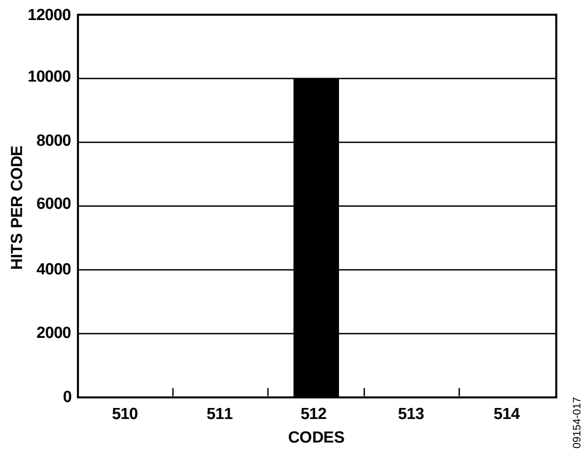


Figure 7. Typical 12-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

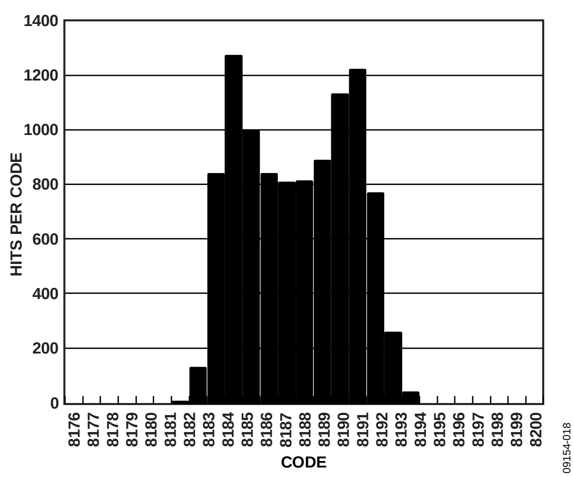


Figure 8. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Disabled

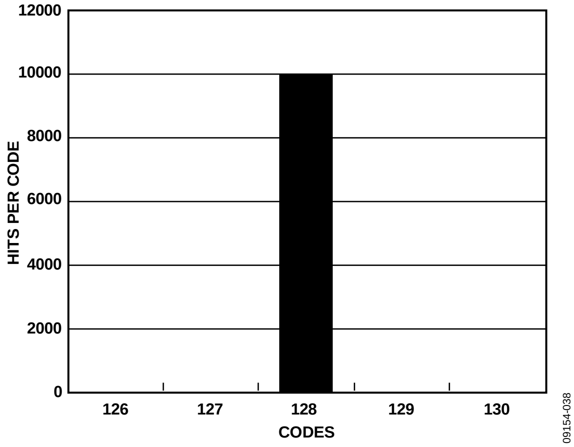


Figure 9. Typical 10-Bit Angular Accuracy Histogram of Codes, 10,000 Samples, Hysteresis Enabled

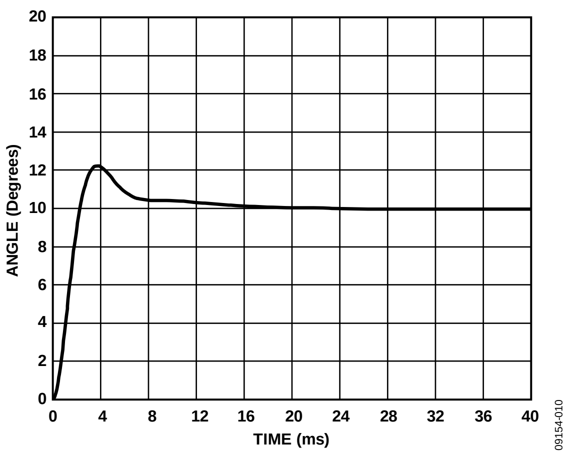


Figure 10. Typical 16-Bit 10° Step Response

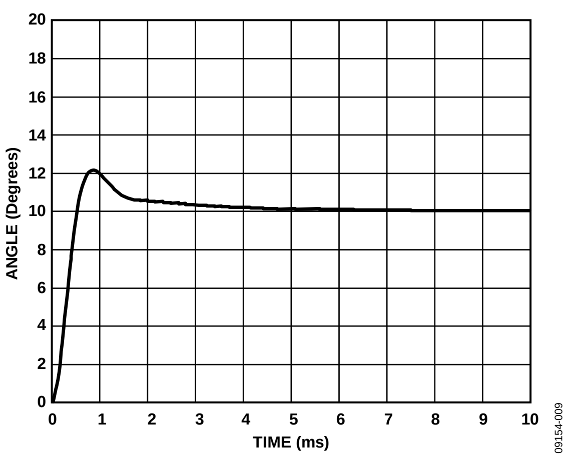


Figure 11. Typical 14-Bit 10° Step Response

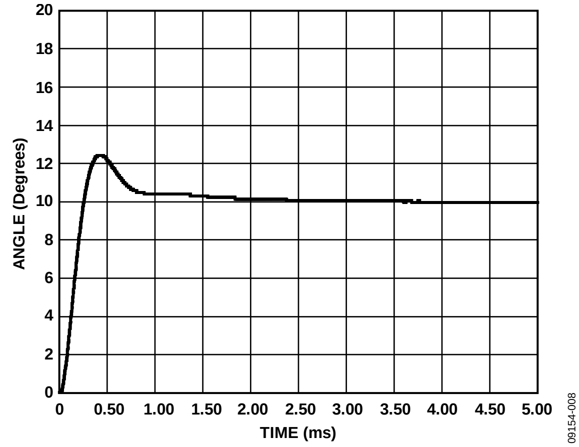


Figure 12. Typical 12-Bit 10° Step Response

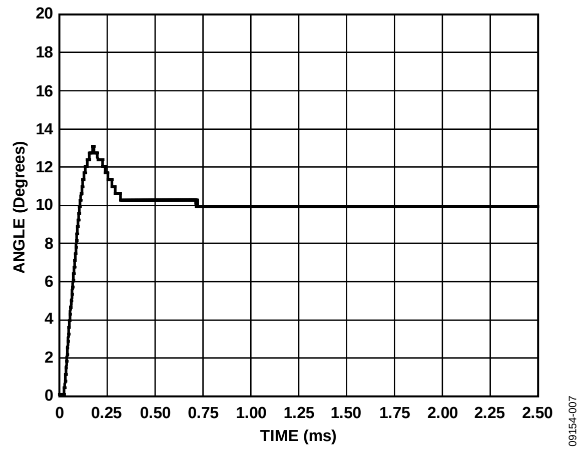


Figure 13. Typical 10-Bit 10° Step Response

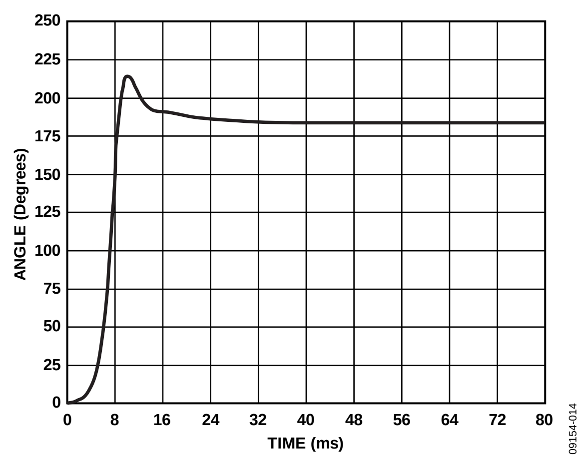


Figure 14. Typical 16-Bit 179° Step Response

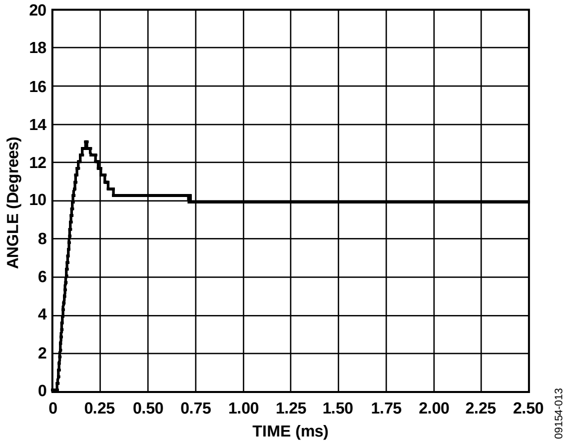


Figure 15. Typical 14-Bit 179° Step Response

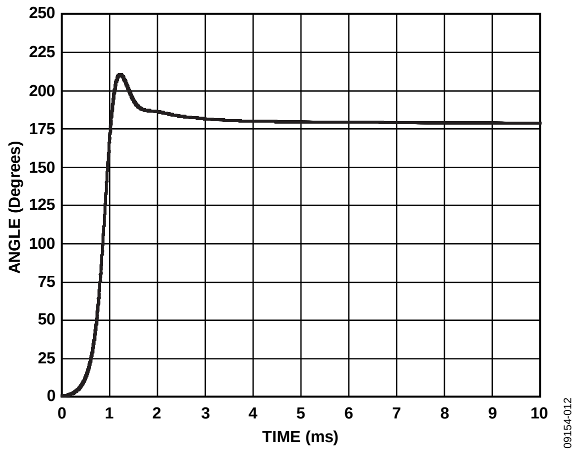


Figure 16. Typical 12-Bit 179° Step Response

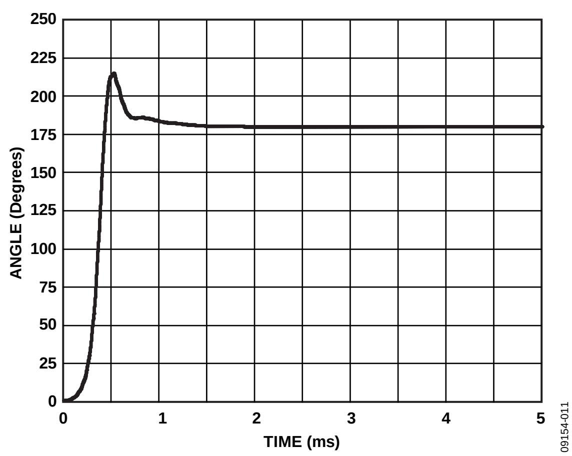


Figure 17. Typical 10-Bit 179° Step Response

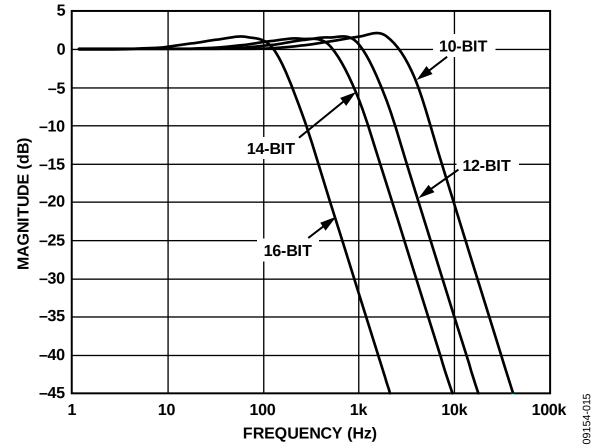


Figure 18. Typical System Magnitude Response

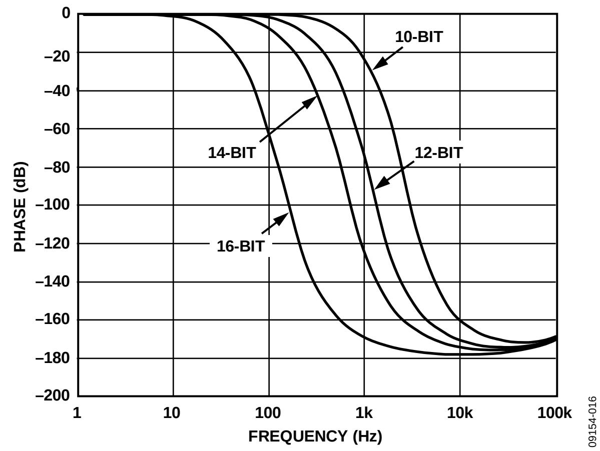


Figure 19. Typical System Phase Response

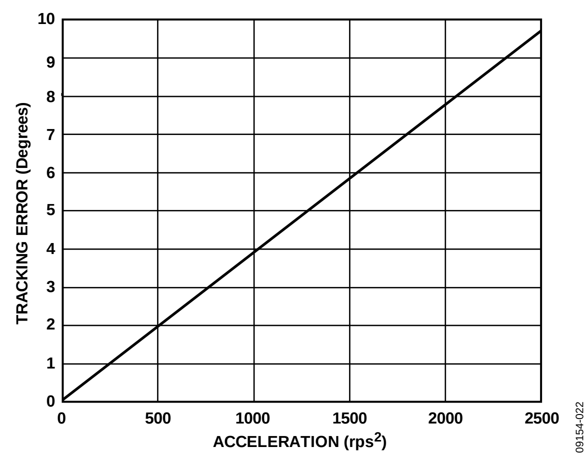


Figure 20. Typical 16-Bit Tracking Error vs. Acceleration

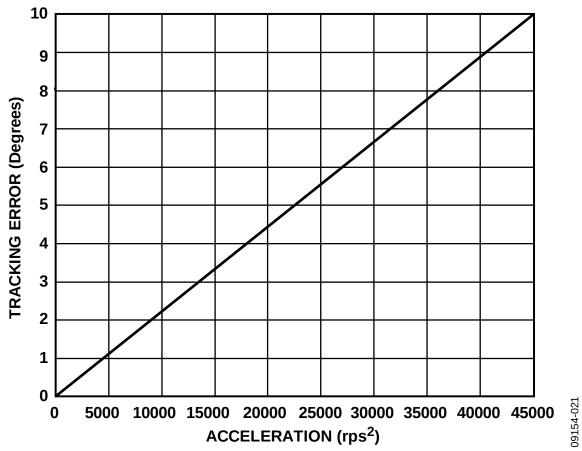


Figure 21. Typical 14-Bit Tracking Error vs. Acceleration

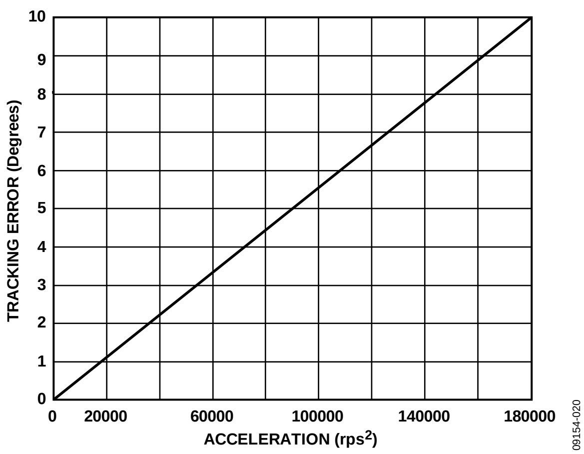


Figure 22. Typical 12-Bit Tracking Error vs. Acceleration

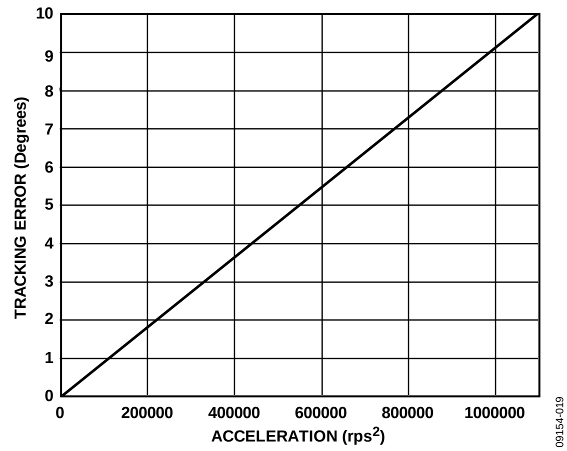


Figure 23. Typical 10-Bit Tracking Error vs. Acceleration

OUTLINE DIMENSIONS

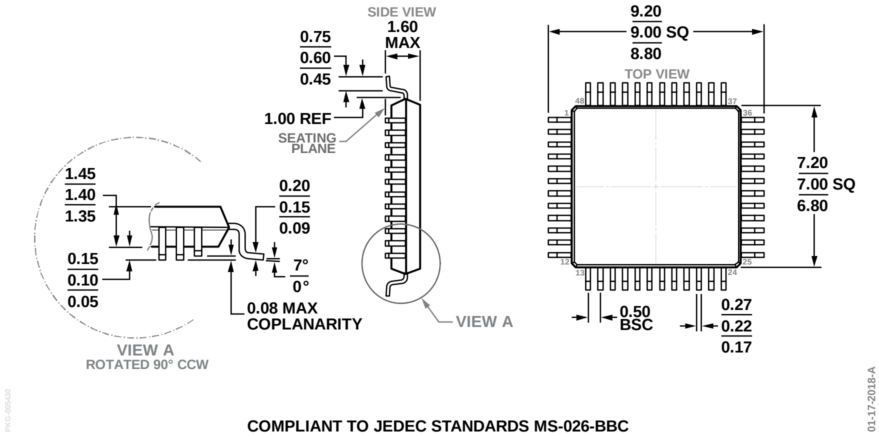


Figure 24. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD2S1210SST-EP-RL7	−55°C to +125°C	48-Lead LQFP	ST-48
AD2S1210SSTZ-EPRL7	−55°C to +125°C	48-Lead LQFP	ST-48

[1] Z = RoHS Compliant Part

NOTES

NOTES

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